
INSTALLATION
UPDATE INFO

TSV05 TAPE TRANSPORT SUBSYSTEM
Installation Update Information

Order Number EK-TSV05-UP.A01

Digital Equipment Corporation

1st Edition, April 1991

The postpaid Reader's Comment Card included in this document requests the user's critical evaluation to assist in preparing future documentation.

FCC NOTICE: The equipment described in this manual generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such radio frequency interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his own expense may be required to take measures to correct the interference.

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About This Manual

The information in this manual is directed toward the DIGITAL Customer Services Engineer and is intended to address the installers need for information on the TSV05 Tape Drive. The unpacking instructions in this manual supersede previous unpacking instructions after the implimentation of Engineering Change Orders H9542-F-MK111 and TS05-B-MK108.)

Structure Of The Manual

Chapter 1 provides information on the unpacking and inspection procedures for the TSV05-S cabinet models (-SE). The unpacking procedures for the TSV05-Sx rack-mount kit and cable kit applies equally to the TSV05 rack models (-SA).

Chapter 2 provides information on the unpacking and inspection procedures for the TSV05-A, TSV05-B, and the TSV05-Z variations.

Notes, Cautions, And Warnings

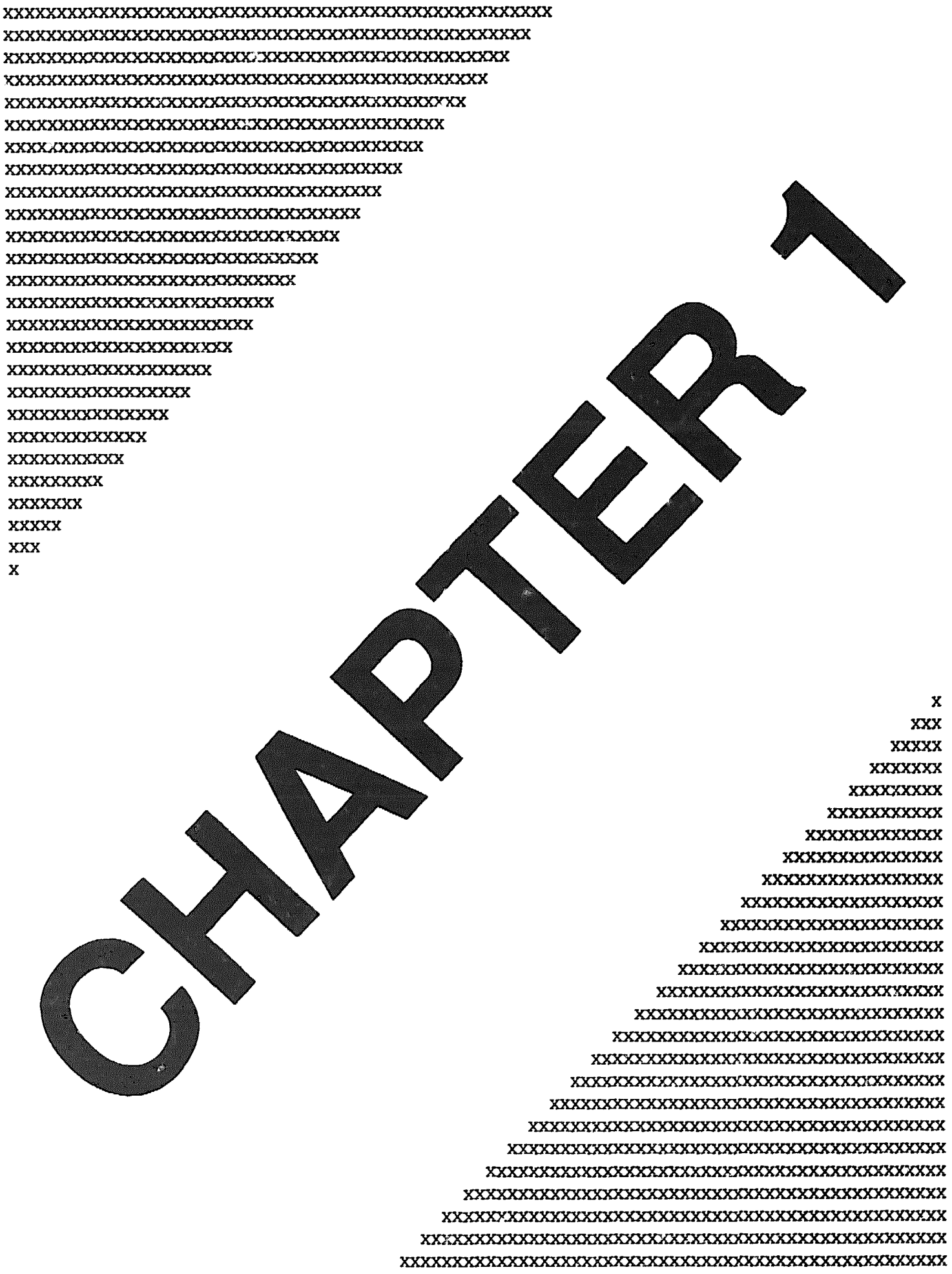
The following conventions are observed in this manual:

Table 1 Notes, Cautions, & Warnings

NOTE	Highlights important information or explanations.
CAUTION	Highlights areas that could cause damage to the equipment or corrupt the data on the system.
WARNING	Calls attention to areas that could injure personnel.

Related Documentation

1. TSV05 Tape Transport Installation Manual (EK-TSV05-IN).
2. TSV05 Tape Subsystem Installation/Owner's Manual (EK-TSV05-IO).
3. TSV05 Tape Transport Subsystem User's Guide (EK-TSV05-UG).
4. TSV05 Pocket Service Guide (EK-TSV05-PS).
5. TSV05 Tape Transport Subsystem Technical Manual (EK-TSV05-TM).


CHAPTER 1

1
INSTALLING THE TSV05-S

1.1 Overview

This document has been written to define the new packaging which will be implemented after the following Engineering Change Orders (ECO's) have been processed:

- H9542-F-MK111
- TS05-B-MK108

The unpacking instructions in this manual supersede the unpacking instructions defined in Chapters 2 and 3 of the TSV05 Tape Transport Subsystem Technical Manual (EK-TSV05-TM) and Chapter 2 of the TSV05 Tape Subsystem Installation/Owner's Manual (EK-TSV05-IO).

1.2 Unpacking And Inspection (TSV05-S Models)

The unpacking instructions defined in this section supersede the unpacking instructions defined in Section 2.2 of TSV05 Tape Transport Subsystem Technical Manual (EK-TSV05-TM) and Chapter 2 of the TSV05 Tape Subsystem Installation/Owner's Manual (EK-TSV05-IO).

The following paragraphs describe the unpacking and inspection procedures for the TSV05-S cabinet models (-SE). The unpacking procedures for the TSV05-Sx rack-mount kit and cable kit applies equally to the TSV05 rack models (-SA).

CAUTION
The TSV05-Sx installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment prior to unpacking the installation kit. Failure to do so can result in equipment damage.

Only qualified service personnel should remove or install modules.

The TSV05-SE cabinet models are shipped as one skid-mounted carton and one or more smaller cartons. The carton on the skid contains the TS05 tape transport cabinet. The smaller carton(s) contains the TSV05-Sx installation kit (M7530-PA), one of two cable kits [CK-TS05-15 (eight foot cables) or CK-TS05-16 (16 foot cables)], and a soft box kit containing documentation, a cleaning kit and a reel of magnetic tape. These smaller items may be shipped in one carton or two, depending on shipping requirements.

Check the shipping documents to ensure that the correct model has been shipped. If anything is missing, damaged, or incorrect, contact the dealer from whom the equipment was ordered.

1.3 Tools And Working Space

The following tools are required:

1. Scissors
2. 3/8 inch wrench
3. 11/16 inch wrench
4. 3/4 inch wrench
5. 5/32 inch hex key
6. Anti-static kit (p/n 29-26246-00)

Also, a space of approximately 3 meters (10 feet) square is required for moving the cabinet off of the shipping skid.

1.4 Removing The TS05 Tape Transport From The Carton

Use the following procedure to remove the TS05 Tape Transport from its carton.

WARNING
Once the leveling feet are raised, the cabinet is free to roll on its casters. The cabinet is top-heavy and must be handled with care.

1. Use scissors to cut the nylon straps and remove the cardboard box (Figure 1–1). Remove the plastic bag.
2. Using a 3/8 inch wrench, remove the four shipping bolts that hold the cabinet to the skid. Figure 1–2 shows the sequence in which to unpack the unit.
3. Remove the metal hold-down brackets.
4. Using a 11/16 inch wrench, loosen the leveling feet locking nuts (Figure 1–3).
5. Using a 3/8 inch wrench, screw the leveling feet up into the cabinet base all the way.

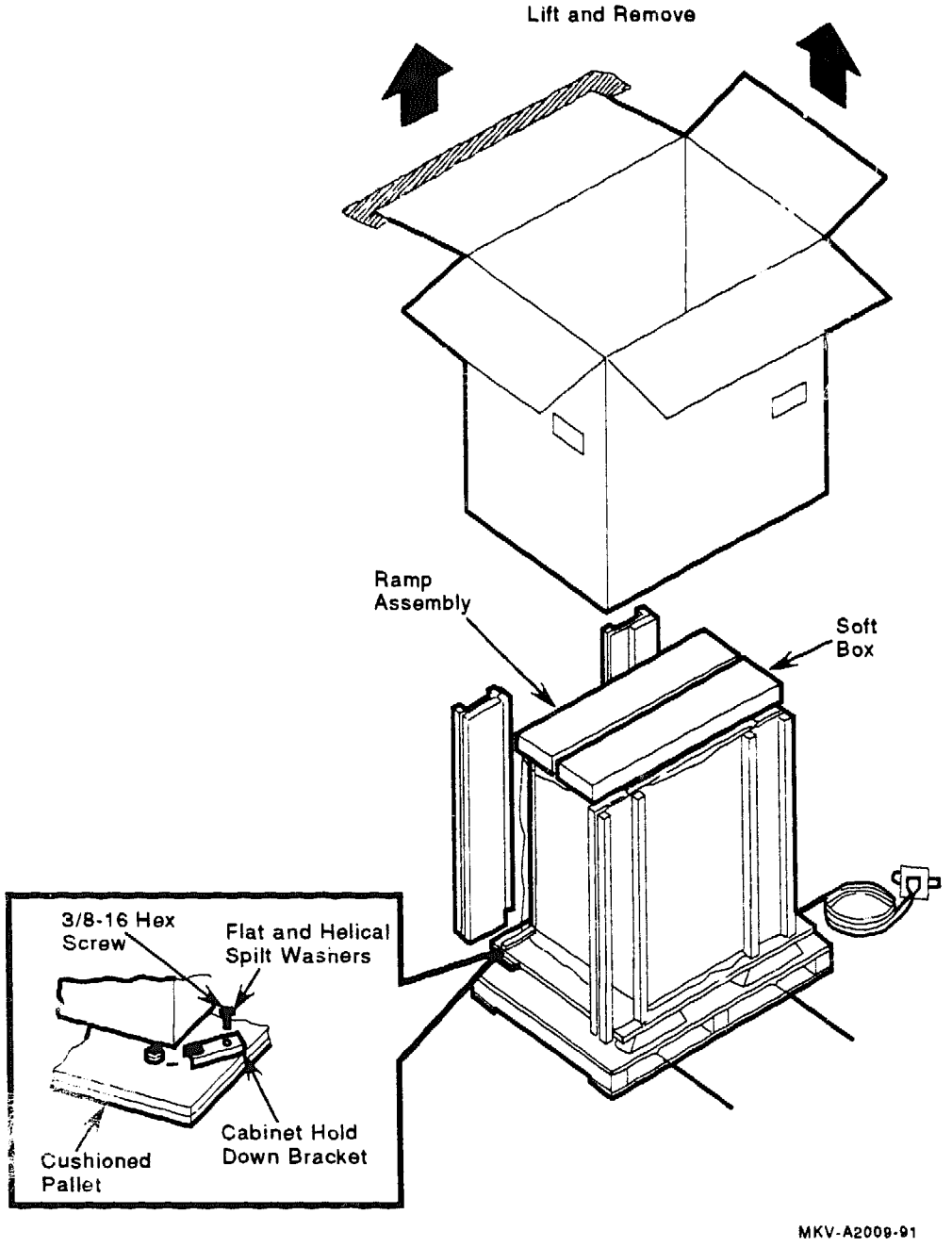


Figure 1–1 Cabinet Carton Removal

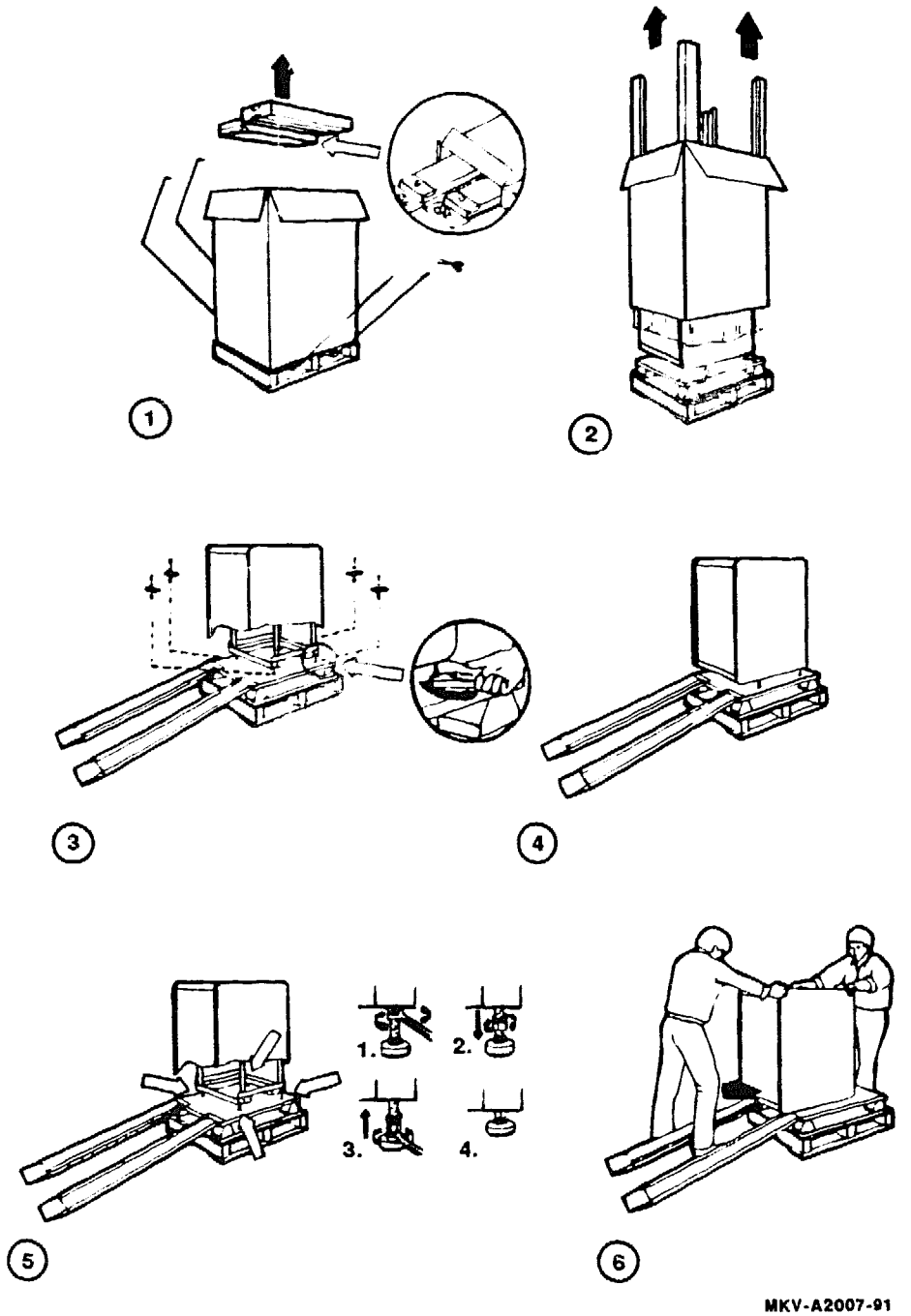
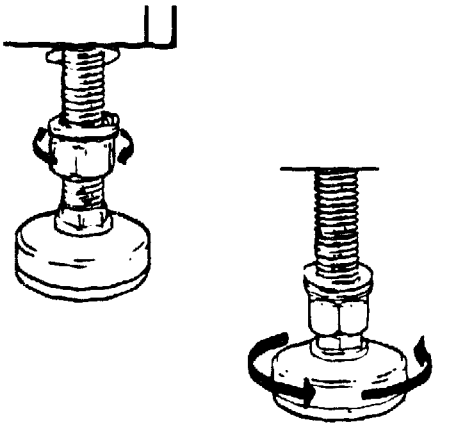


Figure 1–2 Unpacking Sequence



1. Turn Nut Down to Bottom.
2. Screw Foot into Cabinet Far Enough to Permit Cabinet to be Rolled on its Casters.

MKV-A2000-91

Figure 1–3 Raising Leveling Feet

1.5 Removing The Cabinet From The Skid

Use the following procedure to remove the cabinet from the skid.

WARNING
Use sufficient manpower to move the cabinet off of the skid.

1. Grasp cabinet by the right top and the left top (Figure 1–4).
2. Install both ramps onto the pallet deck.
3. Roll the cabinet off of the skid and down ramps, taking care to prevent it from toppling over.
4. Open the rear door using a 5/32 inch hex key (Figure 1–5) and verify that the envelope taped to the bottom of the cabinet contains:
   a. Remote Cable (p/n 70-08288-8F)
   b. Intercabinet Hardware (p/n 74-22224/74-22225)
   c. Four 1/4-20 x 2.75 inch bolts
   d. Twelve 1/4-20 self-retaining nuts

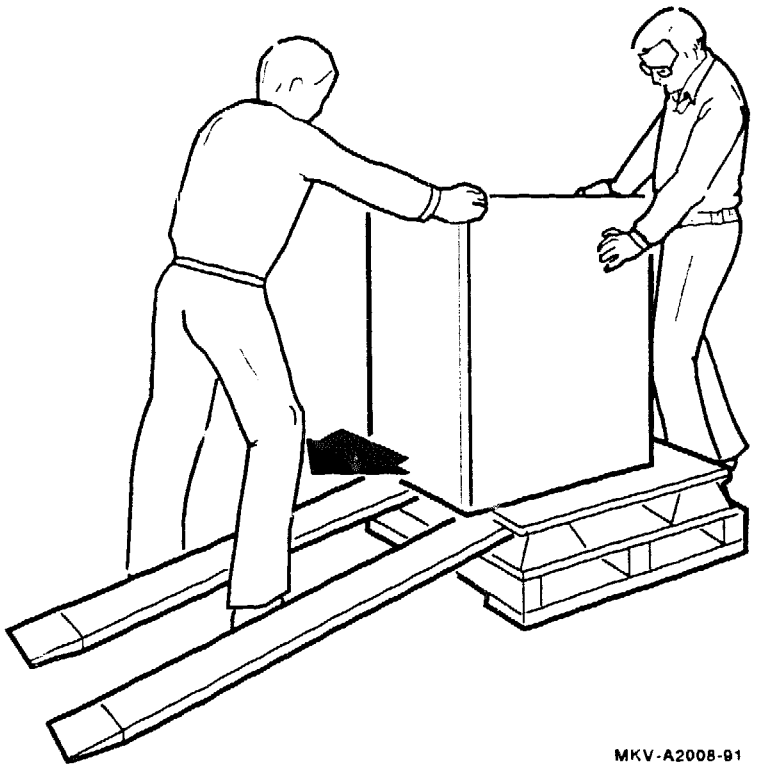


Figure 1–4 Deskidding The Cabinet

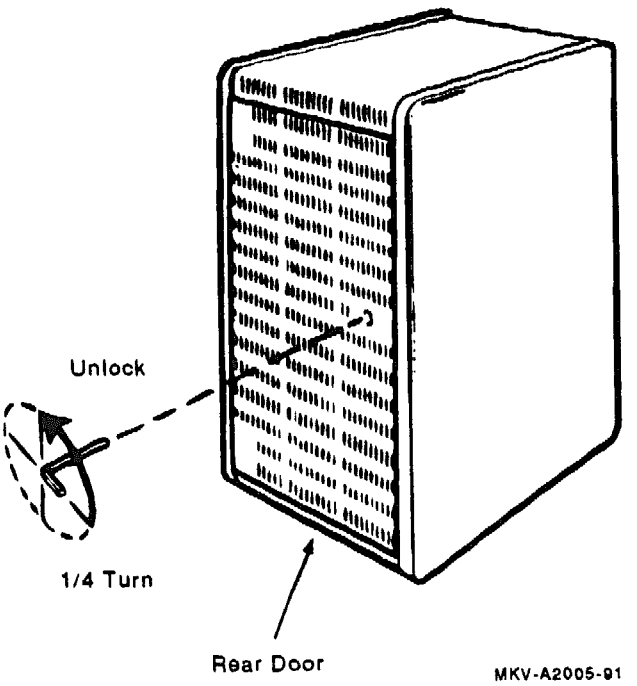


Figure 1–5 Opening Cabinet Door

1.6 Unpacking The TSV05-Sx Installation Kit

CAUTION
The TSV05-Sx installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment (see note 1) prior to unpacking the installation kit. Failure to do so can result in equipment damage.

NOTE
Do not dispose of the packing material until the module has been successfully installed and is operational.

1. Before opening the shipping container, look for external damage to the shipping container such as dents, holes, or crushed corners.
2. Put on your anti-static wrist strap.
3. Ground the wrist strap and the anti-static mat to a local ground. Use the anti-static mat for placement of the module.
4. Open the shipping container.
5. Remove the M7530 module from the anti-static bag.

6. Inspect the module for shipping damage. Check carefully for cracks, breaks, and loose components. Ensure that all PROMs are fully seated in their sockets.
7. Report any damage to the shipper and notify the DIGITAL representative.
8. Ensure that there is no residue or corrosion on the handle EOS and FCC clips (Figure 1–6). If so, remove it with alcohol or other approved mild cleaners.
9. Ensure that there is no residue or corrosion on the gap filler assemblies. If so, remove it with alcohol or other approved mild cleaners.
10. Ensure that the EOS and FCC clips on the handle are in an arch shape. When pressing slightly, they should return to their original shape.
11. If any clip is missing, broken, distorted, or corroded, replace it with EOS clip p/n 12-26922-01, or FCC clip p/n 12-23640-01.
12. Either install the controller at this time or return it to the anti-static bag it was originally packaged in (until it is ready to be installed).

Note that the Anti-static Kit (29-26246-00) is not included, but is part of the Field Service Tool Kit.

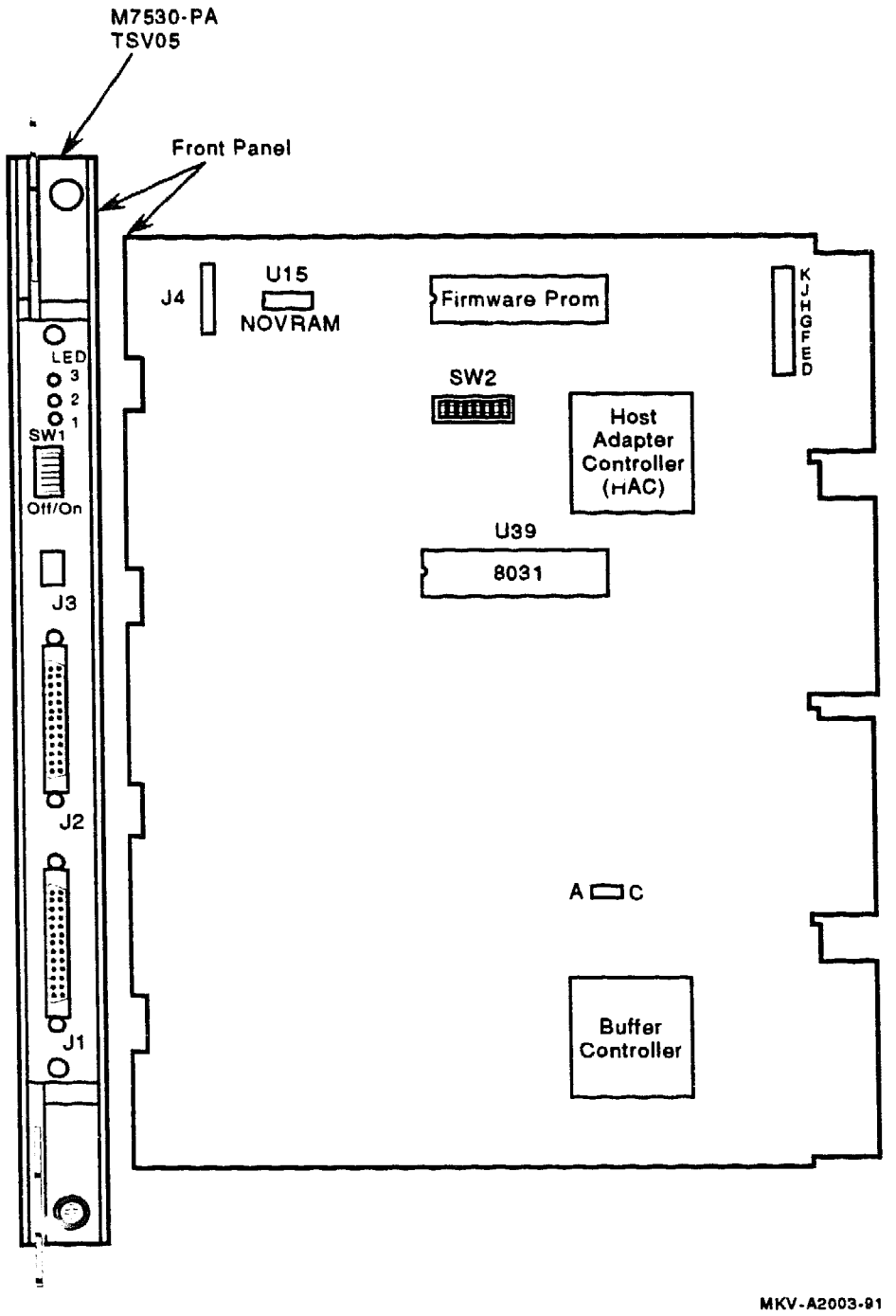


Figure 1–6 M7530-PA Module

1.7 Unpacking The Cable Kit (CK-TS05-15 or CK-TS05-16)

Open the shipping container and check its contents. Reference Table 1–1 and locate the configuration that was ordered. Locate the parts described for that configuration in the Parts List Breakdown (Table 1–2). Table 1–2 contains a list of the contents of the cable kits.

Table 1–1 CK Kits

Configuration	Configuration Description
CK-TS05-15	TS05-Sx Cable Kit (8 foot cables)
CK-TS05-16	TS05-Sx Cable Kit (16 foot cables)

Table 1–2 Parts List Breakdown

Item	Part Number	Description	15	16
1	17-02487-01	50-Pin Cable, 8 ft.	2	-
2	17-02487-02	50-Pin Cable, 16 ft.	-	2
3	70-24505-01	Bulkhead Panel	1	1
4	90-00063-39	Screw, #10	1	1
5	90-07032-00	Cable Tie	2	2
6	90-07867-00	Mount, Cable Tie	2	2

1.8 Unpacking The Other Small Cartons

Open the other soft box kit (p/n 70-27321-00) and check its contents. The kit should contain the following:

1. TSV05 Installation/Owner's Manual (EK-TSV05-IO)
2. TSV05 Installation Addendum (EK-TSV05-UP)
3. TSV05 Pocket Service Guide (EK-TSV05-PG)
4. Tape Cleaning Kit
5. Magnetic Tape (2400 feet, blank)

If any item is damaged, missing, or incorrect, contact dealer from whom the system was purchased.

Note that the filler panel kit should include two gap filler assemblies and four 1/4 inch flat-head machine screws.

CHAPTER 2

2
INSTALLING THE TSV05-A/B/Z

2.1 Unpacking And Inspection (TSV05-A/B/Z Models)

The unpacking instructions defined in this section supersede the unpacking instructions defined in Section 3.2 of TSV05 Tape Transport Subsystem Technical Manual (EK-TSV05-TM).

The TSV05-A and the TSV05-Z variations are shipped in one large carton and one (or more) small carton(s). The TSV05-B is shipped as one skid-mounted carton and one (or more) smaller carton(s). The carton on the skid contains the TS05 tape transport cabinet. The smaller carton(s) contains the M7196 interface/controller module, the documentation and accessories, and two individually packaged cables. These smaller items may be shipped in one carton or two, depending on shipping requirements. Check the shipping documents to ensure that the correct model has been shipped. If anything is missing, damaged, or incorrect, contact the dealer from whom the equipment was ordered.

2.2 Tools And Working Space

The following tools are required for unpacking the TSV05-B subsystem:

1. Scissors
2. 3/8 inch wrench
3. 11/16 inch wrench
4. 3/4 inch wrench
5. 5/32 inch hex key
6. Anti-static kit (p/n 29-26246-00)

Also, a space of approximately 3 meters (10 feet) square is required for moving the cabinet off of the shipping skid.

2.3 Unpacking The Cabinet

WARNING
Once the leveling feet are raised, the cabinet is free to roll on its casters. The cabinet is top-heavy and must be handled with care.

1. Use scissors to cut the nylon straps and remove the cardboard box (Figure 2–1). Remove the plastic bag.

2. Using a 3/8 inch wrench, remove the four shipping bolts that hold the cabinet to the skid. Figure 2–2 shows the sequence in which to unpack the unit.
3. Remove the metal hold-down brackets.
4. Using a 11/16 inch wrench, loosen the leveling feet locking nuts (Figure 2–3).
5. Using a 3/8 inch wrench, screw the leveling feet up into the cabinet base all the way.

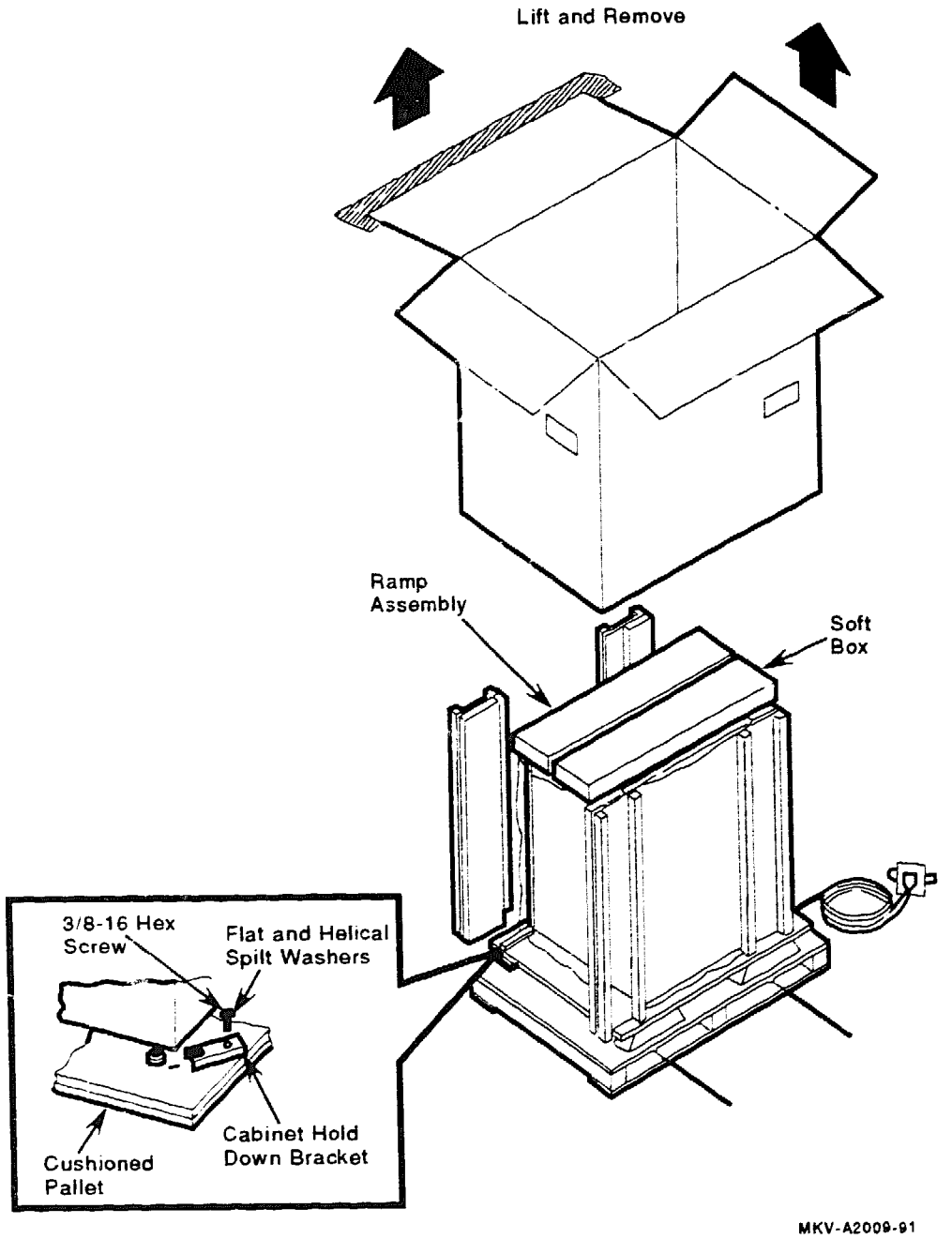


Figure 2–1 Cabinet Carton Removal

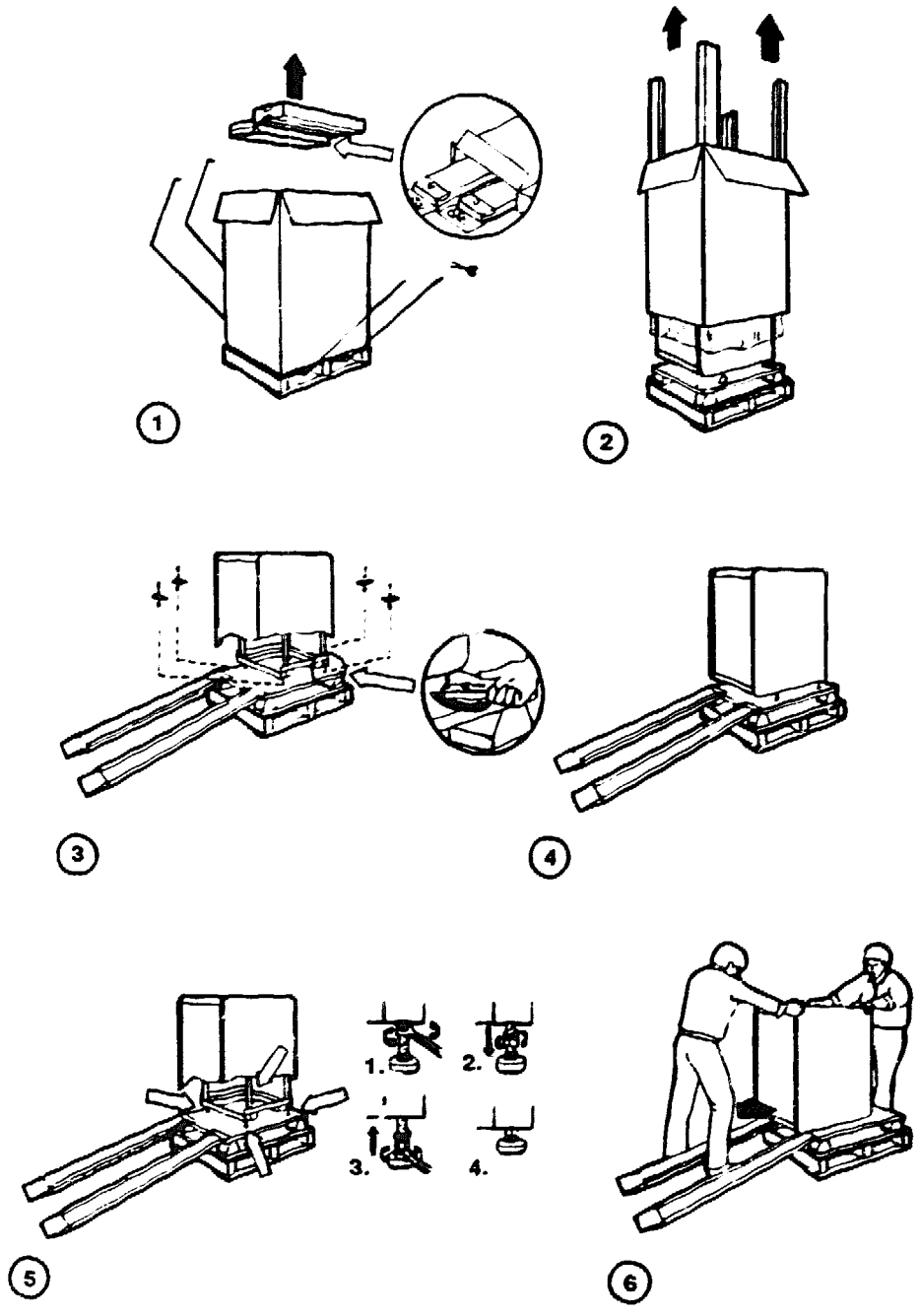


Figure 2–2 Unpacking Sequence

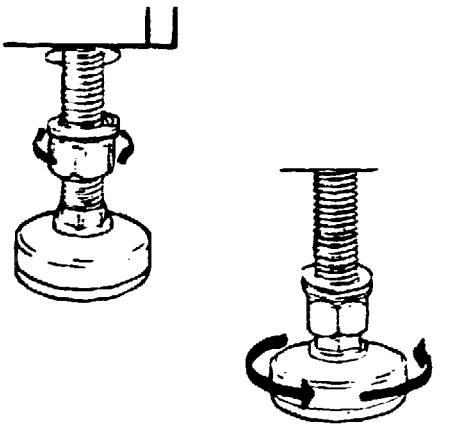


Figure 2–3 Raising Leveling Feet

2.4 Deskidding The Cabinet

Use the following procedure to remove the cabinet from the skid.

WARNING
Use sufficient manpower to move the cabinet off of the skid.

1. Grasp cabinet by the right top and the left top (Figure 2–4).
2. Install both ramps onto the pallet deck.
3. Roll the cabinet off of the skid and down ramps, taking care to prevent it from toppling over.
4. Open the rear door using a 5/32 inch hex key (Figure 2–5) and verify that the envelope taped to the bottom of the cabinet contains:
   a. Remote Cable (p/n 70-08288-8F)
   b. Intercabinet Hardware (p/n 74-22224/74-22225)
   c. Four 1/4-20 x 2.75 inch bolts
   d. Twelve 1/4-20 self-retaining nuts

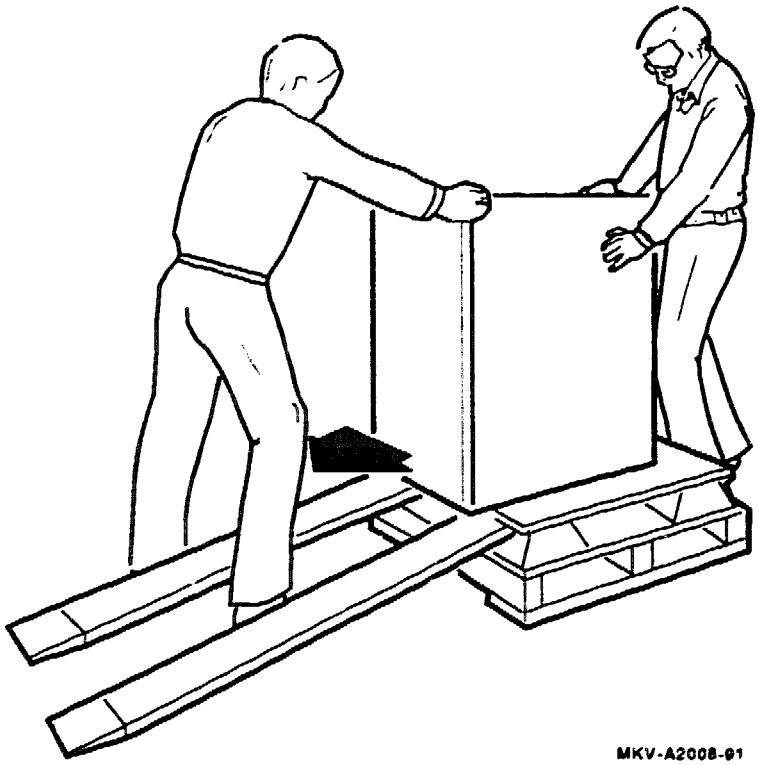


Figure 2–4 Deskidding The Cabinet

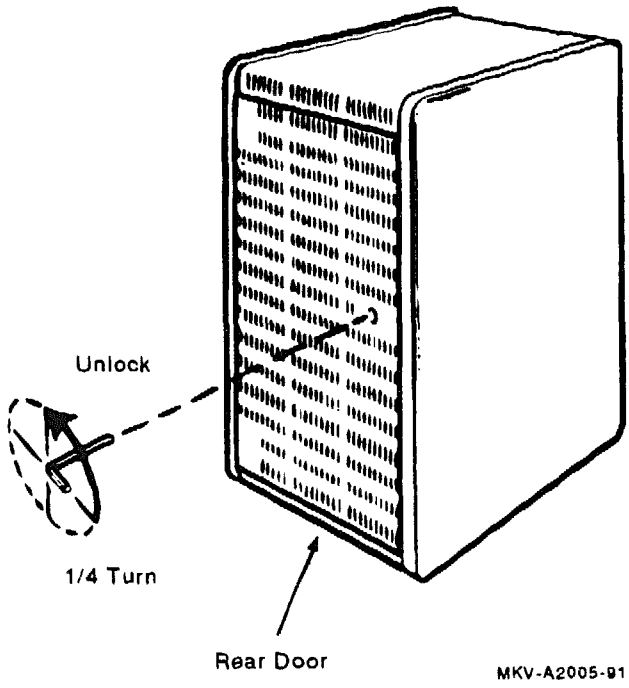


Figure 2–5 Opening Cabinet Door

2.5 Unpacking TSV05-A, TSV05-B or TSV05-Z Installation Kit

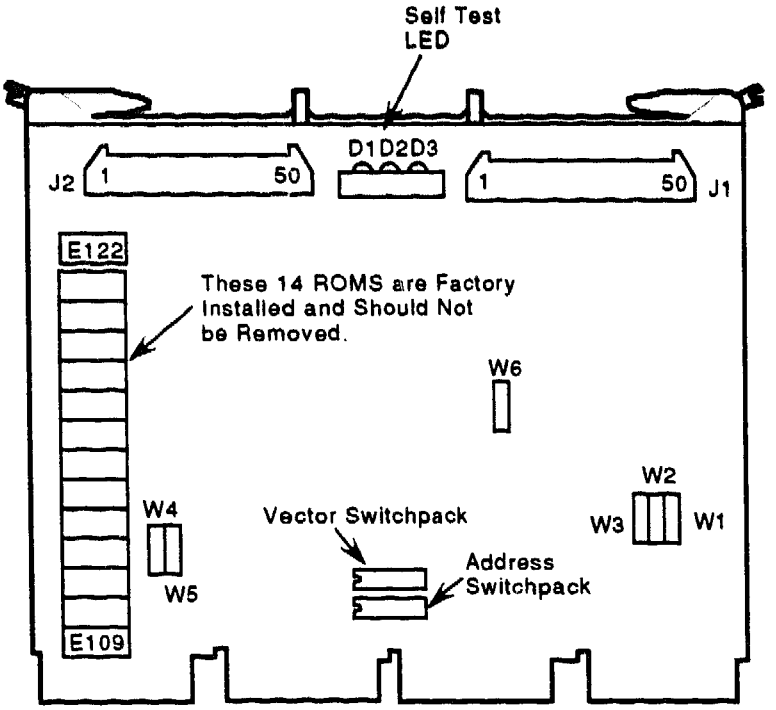
CAUTION
The TSV05 installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment (see note 1) prior to unpacking the installation kit. Failure to do so can result in equipment damage.

NOTE
Do not dispose of the packing material until the module has been successfully installed and is operational.

1. Before opening the shipping container, look for external damage to the shipping container such as dents, holes, or crushed corners.
2. Put on your anti-static wrist strap.
3. Ground the wrist strap and the anti-static mat to a local ground. Use the anti-static mat for placement of the module.
4. Open the shipping container.
5. Remove the M7196 module from the anti-static bag.

6. Inspect the module for shipping damage. Check carefully for cracks, breaks, and loose components. Ensure that all PROMs are fully seated in their sockets.
7. Report any damage to the shipper and notify the DIGITAL representative.
8. Return the M7196 to its protective anti-static bag or proceed to install the controller in the host system.

Note that the anti-static kit (29-26246-00) is not included, but is part of the Field Service Tool Kit.



Vector Switchpack

	1	2	3	4	5	6	7	8	9	10	
On / Off	V8	V7	V6	V5	V4	V3	V2	S1	S0	A12	E58

Vector Switchpack

	1	2	3	4	5	6	7	8	9	10	
On / Off	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	E57

V = Vector Bit
A = Address Bit
S1 = Buffering ("ON" Increases Throughput but Data May be Lost if Power Fails.)
S0 = Extended Features ("ON" for 22 Bit Addressing.)

Jumpers		Default Settings
W1	BIRQ5	Out
W2	BIRQ7	Out
W3	BIRQ6	Out
W4	Bus Grant Continuity	In
W5	Bus Grant Continuity	In
W6	SCLOCK Enable (Used During Factory Repair Only)	In

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Figure 2–6 M7196 Switch And Jumper Identification

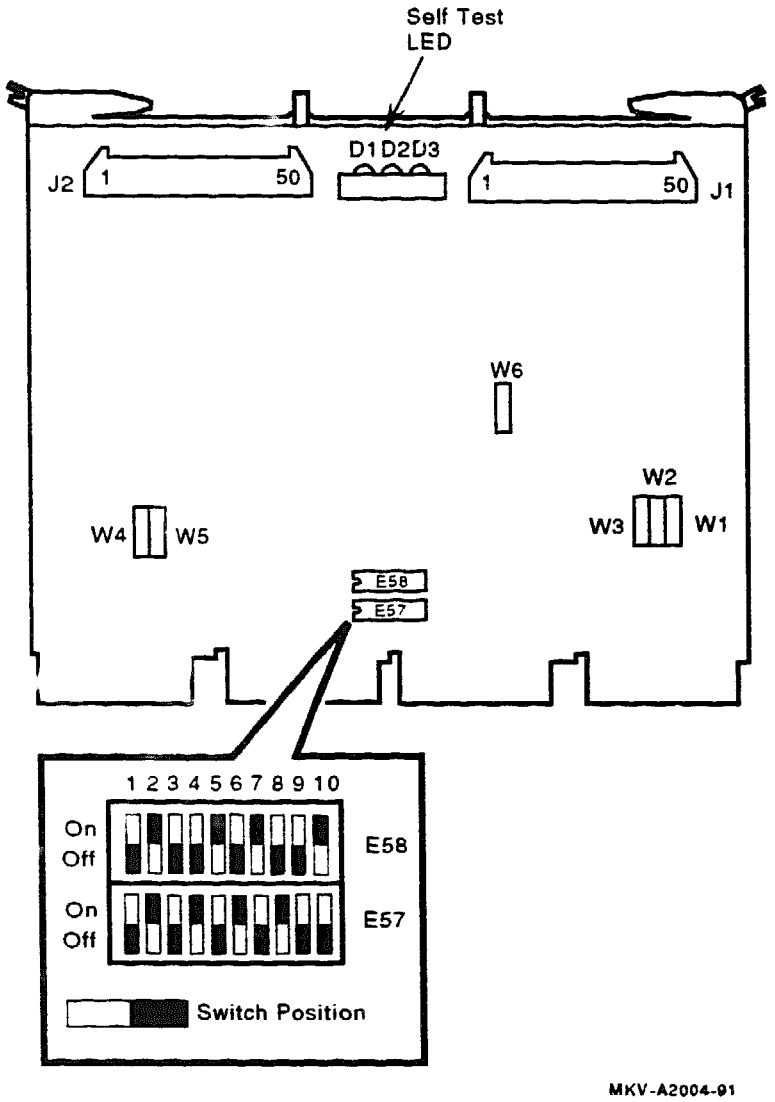


Figure 2–7 M7196 Module

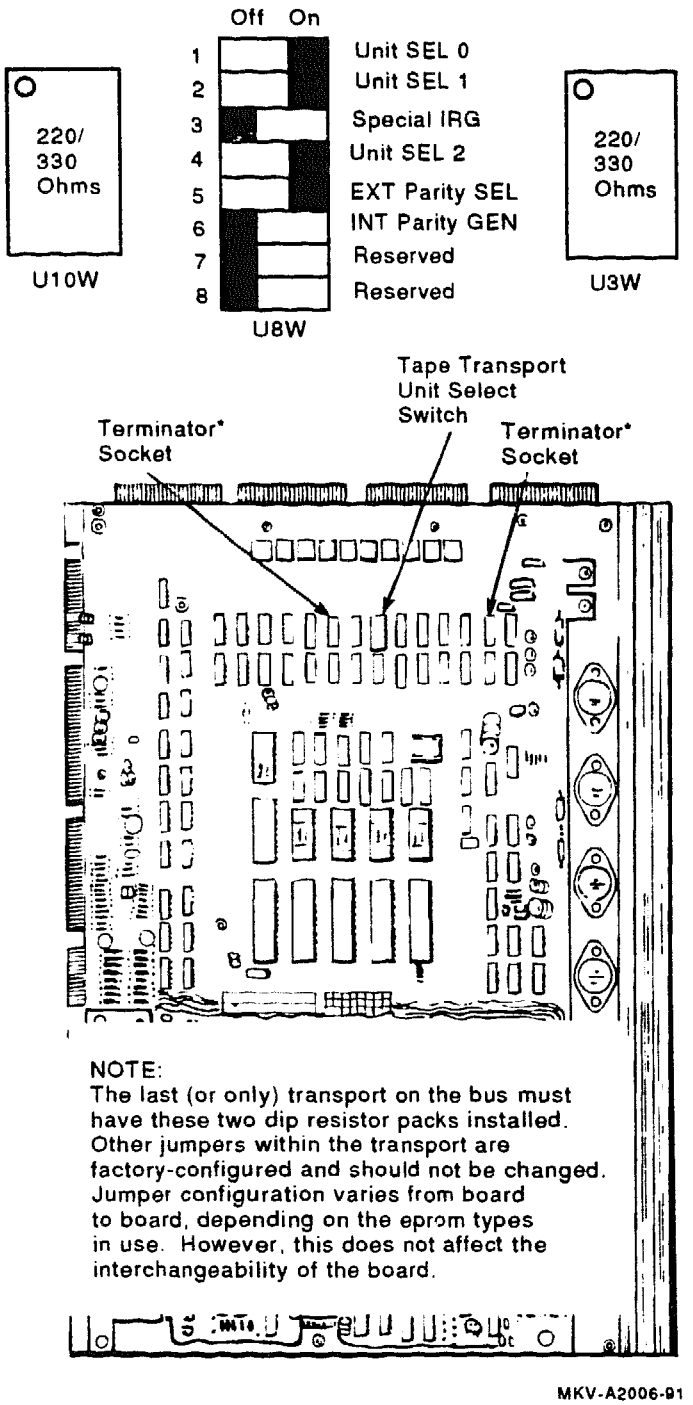


Figure 2–8 Transport Switch And Terminator Identification

2.6 Unpacking The Cable Kits

Open the shipping container and check its contents. Reference Table 2–1 and locate the configuration that was ordered. Locate the parts described for that configuration in the Parts List Breakdown (Table 2–2). Table 2–2 contains a list of the contents of the cable kits.

Table 2–1 CK Kits

Configuration	Configuration Description
CK-TS05-11	TS05-A/B Cable Kit for BA123A (World Box Enclosure)
CK-TS05-12	TS05-A/B Cable Kit for OEM
CK-TS05-13	TS05-A/B Cable Kit for H9642 Deep Cabinet (H3490 I/O)
CK-TS05-14	TS05-A/B Cable Kit for BA23A (Pedestal Enclosure and TSV05 Cabinet)

Table 2–2 Parts List Breakdown

Item	Part Number	Description	11	12	13	14
1	12-14614-02	Filter Con. 50 Pin	2	-	2	2
2	BC06L-1C	Cable, 1 ft. 3 in.	-	-	-	2
3	BC06L-03	Cable, 36 in.	2	-	2	-
4	70-16855-12	Cable, 12 ft.	2	-	-	2
5	70-16855-06	Cable, 6 ft.	-	-	2	-
6	36-25190-01	Label, I.D.	1	-	1	1
7	74-27575-01	Plate, Cover	-	-	-	1
8	70-16855-16	Cable, 16 in.	-	2	-	2

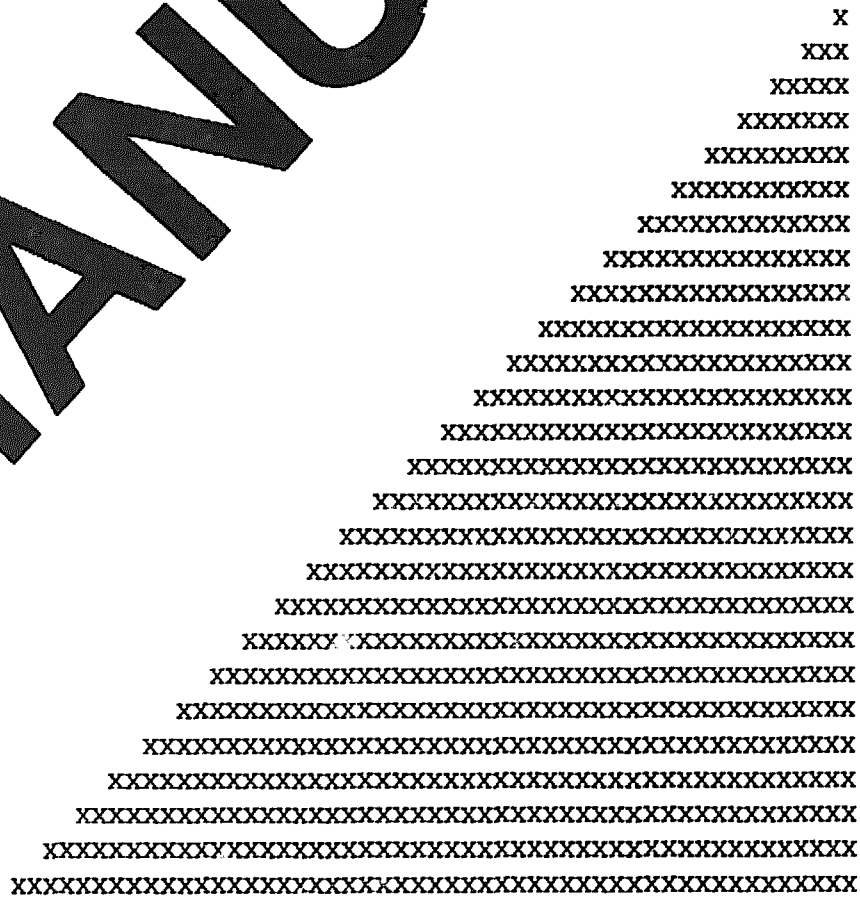
2.7 Unpacking The Smaller Cartons

Open the other soft box kit (p/n 70-22428-01) and check its contents. It should contain the following:

1. TSV05 Installation Manual (EK-TSV05-IN).
2. TSV05 User's Guide (EK-TSV05-UG).
3. TSV05 Pocket Service Guide (EK-TSV05-PS).
4. Magnetic Tape (2400 feet, blank)
5. Tape Cleaning Kit
6. TSV05 Installation Update Information (EK-TSV05-UP)

Inspect each item. If any item is damaged, missing, or incorrect, contact dealer from whom the system was purchased.

TECHNICAL MANUAL



EK-TSV05-TM-004

TSV05 Tape Transport Subsystem

Technical Manual

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PREFACE

PREFACE

ABOUT THIS MANUAL

This manual describes how to install, check out, operate, and perform operator maintenance on TSV05 magnetic tape subsystems. It also contain a technical description of the TSV05 magnetic tape subsystems and the TSV05 programming protocol.

ORGANIZATION

The TSV05 magnetic tape subsystem can include a TS05 tape transport and one of two interface/controller modules. The TSV05 magnetic tape subsystem can be used with either a MicroVAX II or PDP-11 processor, and can be either be rack-mounted or cabinet-mounted. This manual covers all of these variations.

Some of the chapters apply to all TSV05 variations, while other chapters only apply to some of the TSV05 variations. The following lists each variation and which chapters apply to that variation.

TSV05-S - Rack-mounted (MicroVAX II processor)	Chapters 1, 2, 5, 6, 7, 8, 10, and Appendices A, B, C, E
TSV05-S - Cabinet-installed (MicroVAX II processor)	Chapters 1, 2, 5, 6, 7, 8, 10, and Appendices A, B, D, E
TSV05-S - Rack-mounted (PDP-11 processor)	Chapters 1, 2, 4, 6, 7, 8, 10, and Appendices A, B, C, E
TSV05-S - Cabinet-installed (PDP-11 processor)	Chapters 1, 2, 4, 6, 7, 8, 10, and Appendices A, B, D, E
TSV05-A - Rack-mounted (MicroVAX II processor)	Chapters 1, 3, 5, 6, 7, 9, 10, and Appendices A, B, C, E
TSV05-A - Rack-mounted (PDP-11 processor)	Chapters 1, 3, 4, 6, 7, 9, 10, and Appendices A, B, C, E
TSV05-B - Cabinet-installed (MicroVAX II processor)	Chapters 1, 3, 5, 6, 7, 9, 10, and Appendices A, B, D, E
TSV05-B - Cabinet-installed (PDP-11 processor)	Chapters 1, 3, 4, 6, 7, 9, 10, and Appendices A, B, D, E

RELATED DOCUMENTS

Title	Document No.
TSV05 Tape Transport Subsystem Technical Manual	EK-TSV05-TM
TSV05 Tape Transport Subsystem Installation Manual	EK-TSV05-IN
TSV05 Tape Transport Subsystem Installation Manual	EK-TSV5K-IN
TSV05 Tape Transport Subsystem User's Guide	EK-TSV05-UG
TSV05 Pocket Service Guide	EK-TSV05-PS
TS05 Tape Transport Operation and Acceptance, Preventive Maintenance and Remove/Replace Procedures	EY-D3142-PS
TSV05 Field Maintenance Print Set	MP-01157
TSV05-S Field Maintenance Print Set	MP-02347
Operation and Maintenance Instructions for Model F880 Tape Transport	799816-000[1]
CVTSAA TSV05 Magtape Diagnostic User's Document	BA-T965I-MC
DEC/X11 User Document	AC-8240Z-MC

NOTES, CAUTIONS, AND WARNINGS

Where notes, cautions, and warnings are used in this document, they highlight specific types of information as follows:

NOTE — Calls attention to information in text that may be of special importance.

CAUTION — Calls attention to information in text essential to avoiding system or equipment damage.

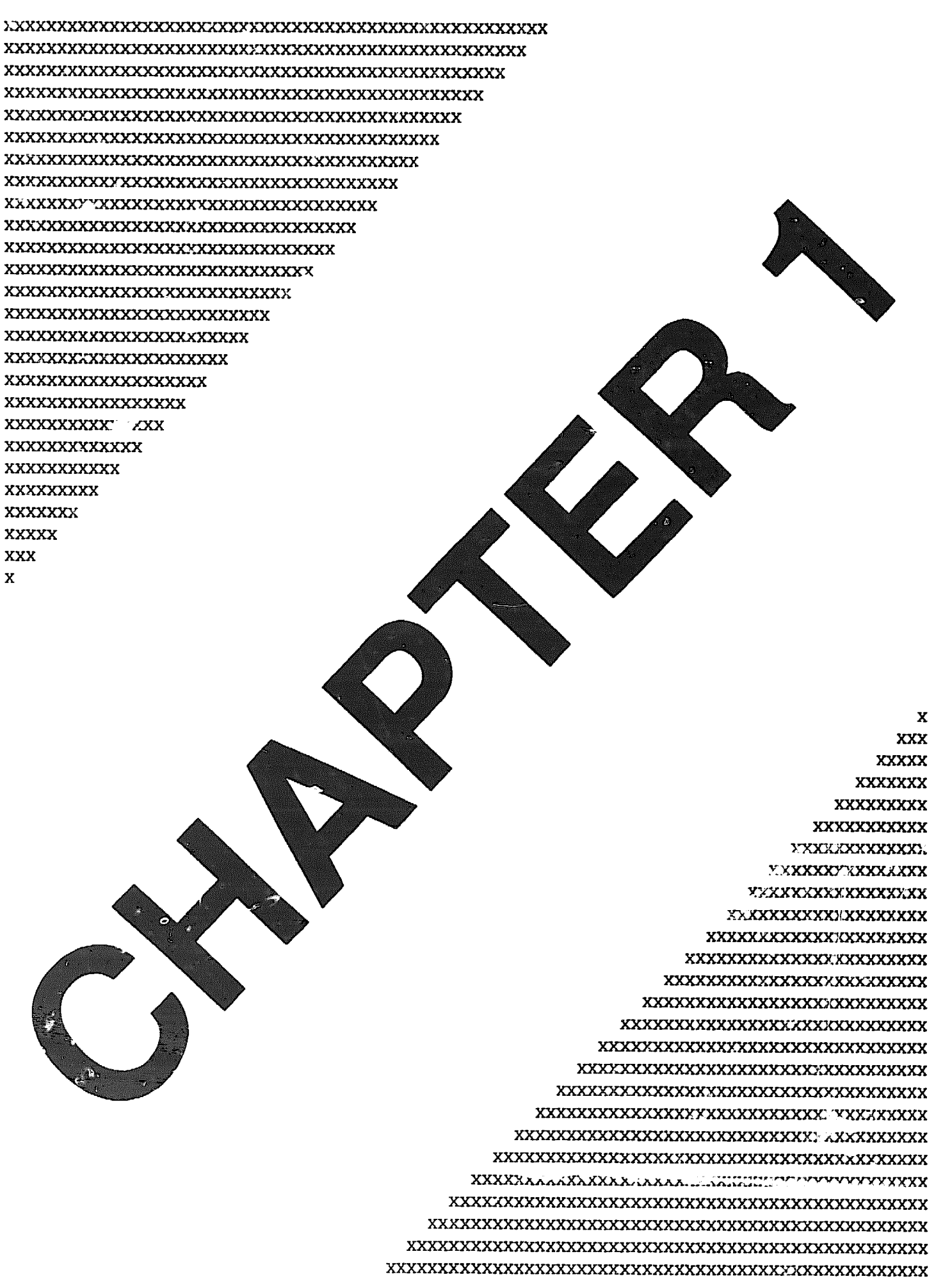
WARNING — Calls attention to information in text essential to the safety of personnel.

FCC USER STATEMENT

NOTICE:

This equipment generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such radio frequency interference. Operation of this equipment in a residential area may cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

[1] Available from Cipher Data Products, 10225 Willow Creek Road, San Diego, California 92131. This document contains detailed drawing of the TS05 formatter and power supply.


CHAPTER 1

CHAPTER 1
INTRODUCTION

1.1 DESCRIPTION

The TSV05 tape transport subsystem provides magnetic tape storage capabilities to computer systems using quad-sized Q-bus backplanes. The subsystem reads or writes up to 160,000 bytes per second in ANSI standard format. Data is recorded by phase encoding 1600 bits per inch on nine-track tape. Reading and writing are performed at either 25 or 100 inches per second.[1] The TSV05 subsystem is hardware compatible with 18- and 22-bit addressing versions of the Q-bus quad backplane. It is software compatible with system and application programs written for the TS11 tape transport subsystem (as long as such programs use a DIGITAL™ supplied device handler). Tape formatting, error detection and correction, and self-test diagnostics are included as integral components of the TSV05 subsystem.

1.1.1 TSV05 Models

NOTE

This manual describes the 120V, 50/60 Hz rack (-AA, -SA) and cabinet models (-BA, -SE, and SK), but this description applies to all the other models.

Model	Applicability
-AA	-AA, -AB, -AC, and AD
-SA	-SA, -SB, -SC, and SD
-BA	-BA, -BB, -BC, and BD
-SE	-SE, -SF, -SH, and SJ
-SK	-SK, -SL, -SM, and SN

[1] (TSV05-S only) the 100 inches per second mode speed requires enabling special features, the appropriate software, and a data rate from the host sufficient to maintain the streaming mode of operation. (Other models) 100 inches per second operating speed requires enabling special features, and the appropriate software.

The TSV05 tape transport systems are available in both rack and cabinet models. The rack models include:

Model	Description
-AA, -SA	Tape Transport 120V, 50/60 Hz
-AB, -SB	Tape Transport 240V, 50/60 Hz
-AC, -SC	Tape Transport 100V, 50/60 Hz
-AD, -SD	Tape Transport 220V, 50/60 Hz

The cabinet models include:

Model	Description
-BA, -SE, -SK	Tape Transport 120V, 50/60 Hz
-BB, -SF, -SL	Tape Transport 240V, 50/60 Hz
-BC, -SH, -SM	Tape Transport 100V, 50/60 Hz
-BD, -SJ, -SN	Tape Transport 220V, 50/60 Hz

The -A_ and the -B_ models use the controller module (M7196) and two flat cables to interface with a standard PDP-11 or MicroVAX II computer system. The -S_ models use the controller module (M7206) and two round cables to interface with a industrial PDP-11 or MicroVAX II computer system. Appendix A contains more detailed information for each model.

1.1.2 Features and Capabilities

A TSV05 subsystem, consisting of a TS05 tape transport and one of two controllers, is available in both rack-mount and cabinet models. All TSV05 magnetic tape subsystem models include a 50/60 Hz TS05 tape transport that operates on one of the following voltages: 100 Vac, 120 Vac, 220 Vac, or 240 Vac. The controller module (M7196) is used with the standard Q-bus systems and the controller module (M7206) is used with the industrial Q-bus systems. Table 1-1 contains a listing of the various models and their contents.

Table 1-1 Model Variations

TSV05-A tape transport subsystem (no cabinet)	
TSV05-AA	TS05-AA Tape Transport (120V, 50/60 Hz) + controller (M7196) + cables
TSV05-AB	TS05-AB Tape Transport (240V, 50/60 Hz) + controller (M7196) + cables
TSV05-AC	TS05-AC Tape Transport (100V, 50/60 Hz) + controller (M7196) + cables
TSV05-AD	TS05-AD Tape Transport (220V, 50/60 Hz) + controller (M7196) + cables
TSV05-B tape transport subsystem (Q-bus VAX or Q-bus PDP interface in H9642 cabinet)	
TSV05-BA	TS05-AA Tape Transport (120V, 50/60 Hz) + controller (M7196) + cables. Housed with 874D power controller in H9642 cabinet.
TSV05-BB	TS05-AB Tape Transport (240V, 50/60 Hz) + controller (M7196) + cables. Housed with 874B power controller in H9642 cabinet.
TSV05-BC	TS05-AC Tape Transport (100V, 50/60 Hz) + controller (M7196) + cables. Housed with 874D power controller in H9642 cabinet.
TSV05-BD	TS05-AD Tape Transport (220V, 50/60 Hz) + controller (M7196) + cables. Housed with 874B power controller in H9642 cabinet.
TSV05-S tape transport subsystem (IVAX or IPDP interface withc cabinet)	
TSV05-SA	TS05-AA Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit
TSV05-SB	TS05-AB Tape Transport (240V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit
TSV05-SC	TS05-AC Tape Transport (100V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit
TSV05-SD	TS05-AD Tape Transport (220V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit

Table 1-1 Model Variations (Cont)

TSV05-S tape transport subsystem (IVAX or IPDP interface in H9642 cabinet)	
TSV05-SE	TS05-AA Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit. Housed with 874D power controller in H9642 cabinet.
TSV05-SF	TS05-AB Tape Transport (240V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit. Housed with 874B power controller in H9642 cabinet.
TSV05-SH	TS05-AC Tape Transport (100V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit. Housed with 874D power controller in H9642 cabinet.
TSV05-SJ	TS05-AD Tape Transport (220V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit. Housed with 874B power controller in H9642 cabinet.
TSV05-S tape transport subsystem (IVAX or IPDP interface with cabinet top cover)	
TSV05-SK	TS05-AA Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit + 70-16864 cover assembly
TSV05-SL	TS05-AB Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit + 70-16864 cover assembly
TSV05-SM	TS05-AC Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit + 70-16864 cover assembly
TSV05-SN	TS05-AD Tape Transport (120V, 50/60 Hz) + controller (M7206) + CK-TS05-16 cable kit + 70-16864 cover assembly
TSV05-Z tape transport subsystem (no cabinet)	
TSV05-ZA	TS05-AA Tape Transport (120V, 50/60 Hz) + TSV05 controller (M7196) + cables + top access cover for PDP-11/83 or MicroVAX II DH-630Q5 deep cabinet systems
TSV05-ZB	TS05-AB Tape Transport (240V, 50/60 Hz) + TSV05 controller (M7196) + cables + top access cover for PDP-11/83 or MicroVAX II DH-630Q5 deep cabinet systems
TSV05-ZC	TS05-AC Tape Transport (100V, 50/60 Hz) + TSV05 controller (M7196) + cables + top access cover for PDP-11/83 or MicroVAX II DH-630Q5 deep cabinet systems
TSV05-ZD	TS05-AD Tape Transport (220V, 50/60 Hz) + TSV05 controller (M7196) + cables + top access cover for PDP-11/83 or MicroVAX II DH-630Q5 deep cabinet systems

All models include one 70-22428-00 soft box containing manuals, a tape cleaning kit, and a 2400-foot reel of magnetic tape.

There are two TSV05 variations: Sandcast unit and Diecast unit. Each variation can be recognized in the following way. The Sandcast unit has a sandcasted top plate which is painted black, while the Diecast top plate has the appearance of a plain aluminum surface.

The interface/controller modules plug into the Q-bus. See Figure 1-1 for model -A, Figure 1-2 for model -B, and Figure 1-3 for model -S. Two cables connect a interface/controller module with the TS05 tape transport. The cables for models -A and -B are flat, and the cables for model -S are round.

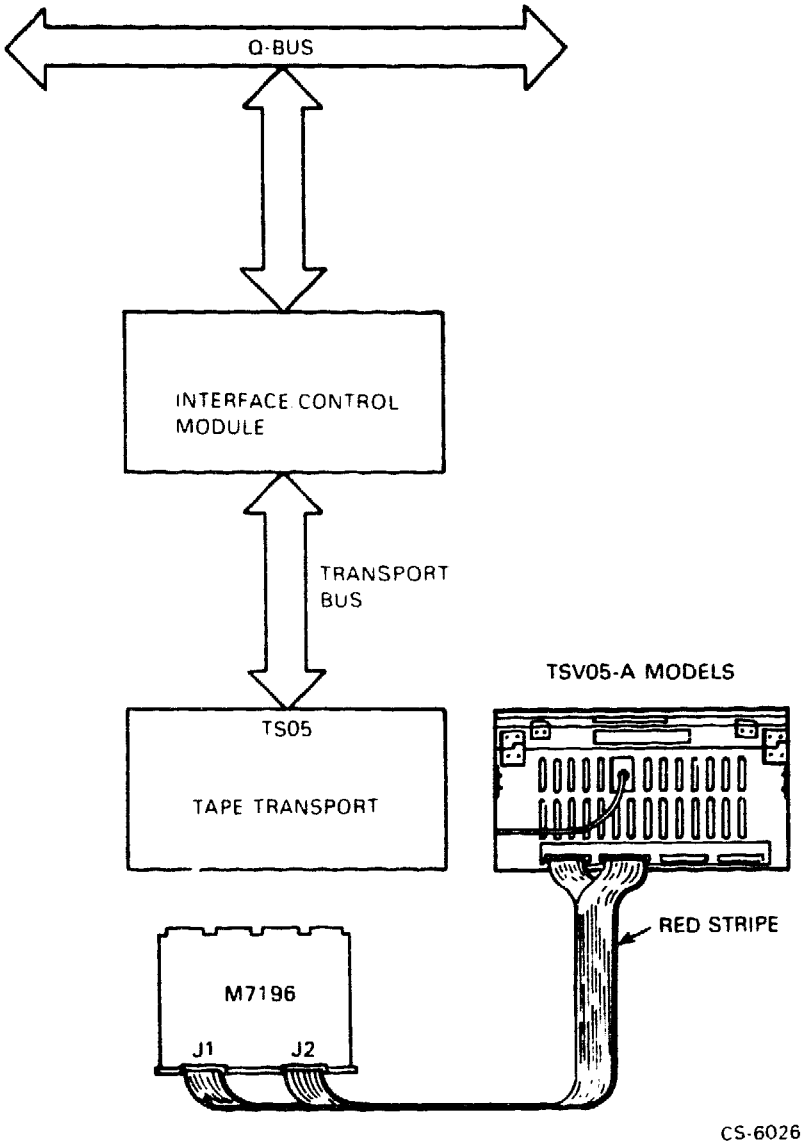


Figure 1-1 TSV05-A Subsystem Components

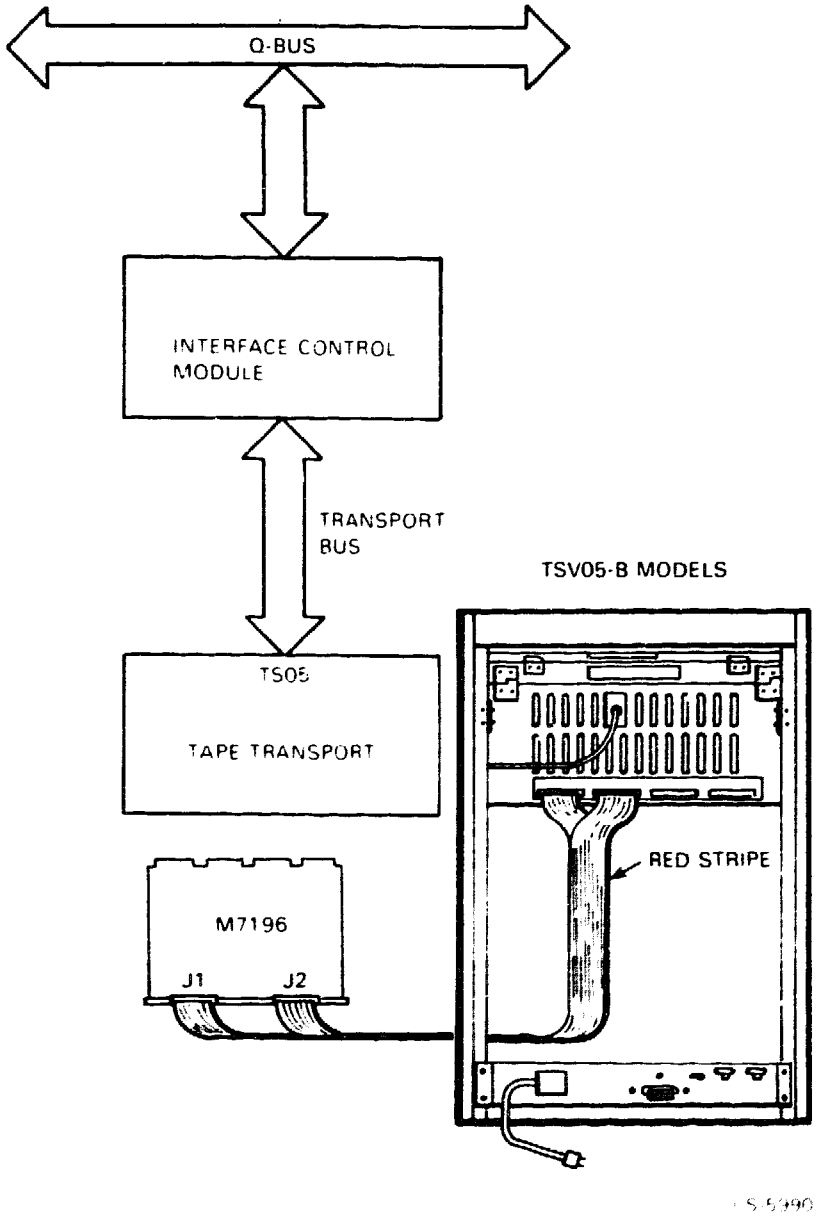


Figure 1-2 TSV05-B Subsystem Components

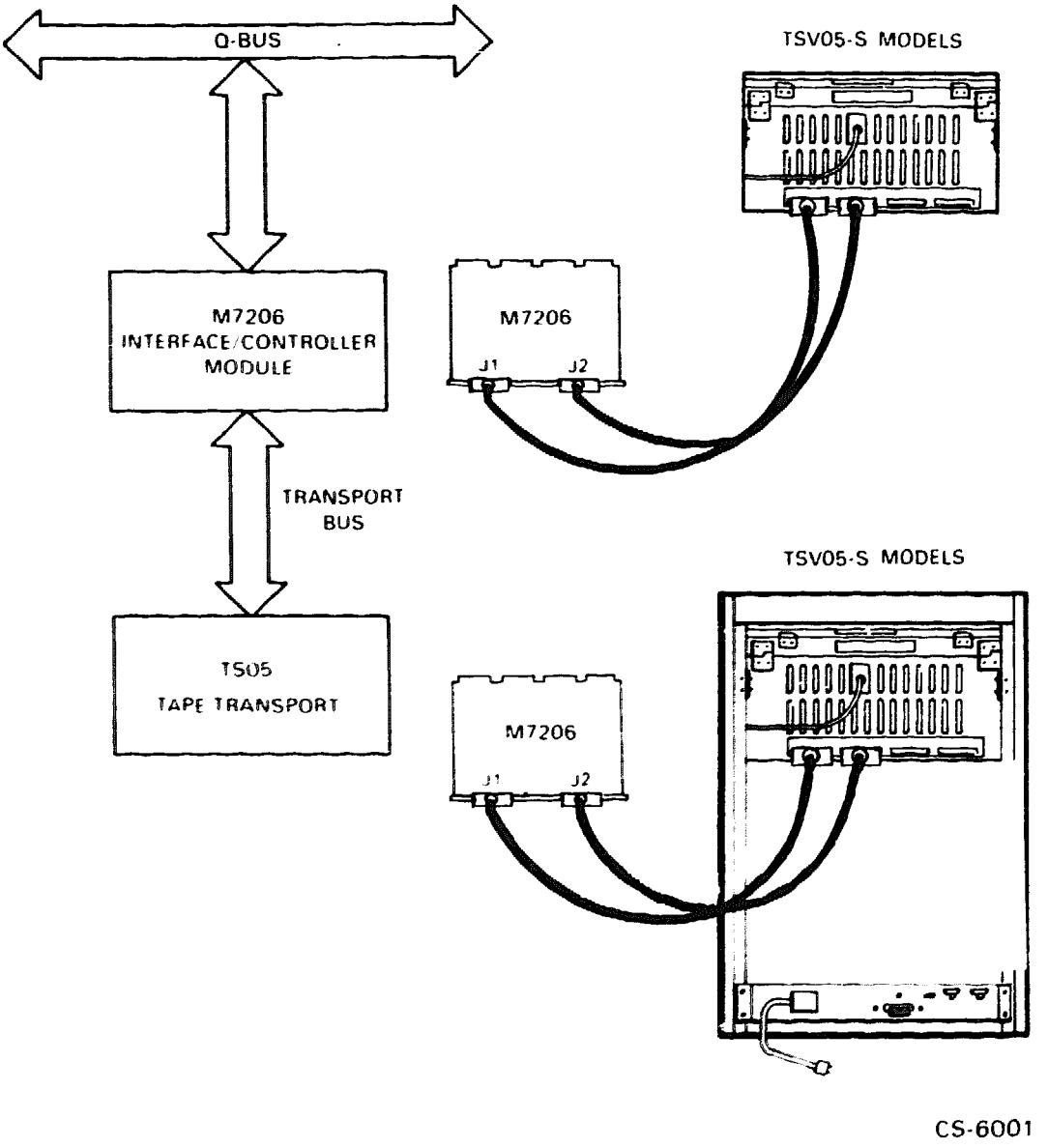


Figure 1-3 TSV05-S Subsystem Components

See the following for TSV05 features and capabilities (see Appendix A for the TSV05 specifications):

- Bidirectional reading capability.
- 3.5K bytes of Random Access Memory (RAM) in controller for buffering tape data[2].
- Streaming or reel-to-reel technology (that is, the tape is not required to stop in the interrecord gap).
- Automatic tape loading (threading).
- Microprocessor control in both the controller and the tape transport.
- Microcoded diagnostic and maintenance features.
- Tape formatting and error detection conforming to ANSI X 3.39-1973 standard.
- Both ANSI and IBM tape mark detection.
- Industry standard bus between controller and tape transport.
- On-line diagnostics that verify data path integrity during idle periods.
- Automatic read after write verification.
- Small form factor with low power consumptions.

[2] Applies to all models except TSV05-S models.

1.2 FUNCTIONAL OVERVIEW

Tape loading is automatic. There are no vacuum columns, retaining clips, or multiple tension arms. When the tape transport is powered up, sets of internal diagnostics are run by the microprocessors in the tape transport electronics package and the interface/controller module. The subsystem is then ready for loading. Once the tape has been inserted and the door closed, the tape transport automatically seats and locks the tape reel on the spindle and threads the tape through the correct path to the takeup reel. The threading operation is accomplished by precisely directed air flows that blow the tape along the path to the takeup reel. When this power-up and load sequence is complete, control of the tape transport switches to the interface/controller module.

The TSV05 subsystem operates under the control of a microprocessor on the interface/controller module. The module is a Direct Memory Access (DMA) device in that it transfers data directly into or out of the memory without requiring the control of the CPU. To per- form a data transaction with the TSV05 subsystem, the CPU first builds a packet of command words in main memory. Next, it passes the starting address of the command packet to the interface/controller module. Using this address, the module performs a DMA transfer to bring the command packet out to the controller memory. The command packet tells the controller what type of operation is to be performed, and where the data is to come from or go to. The module then controls the movement of data from memory to the tape, or from tape to memory. It buffers this data so that DMA transfers can be handled independently of the mechanical movements of the tape. Additionally, it generates interrupts when necessary to provide the CPU with status information.

The tape transport has an internal formatter that controls tape motion, formatting and writing of data on tape, reading of data from tape, and tape transport status monitoring. Commands from the interface/controller module are latched into registers and then processed by a microprocessor in the formatter electronics. The formatter creates the identification (ID) burst, preamble, postamble, and file mark during a write operation, and it interprets these during a read operation. The formatter also oversees the handling of error conditions.

1.3 CONTROLS AND INDICATORS

The interface/controller module has jumpers, switchpacks, and Light-Emitting Diode (LED) indicators. The jumpers and switch packs are preset to the normal configuration, and do not need to be changed unless there is an address conflict with an existing device. The LED indicators are provided as maintainability features, and are not exposed to view during normal operation.

The tape transport has an ON/OFF (1/0) POWER switch and five tactile switches, each with an LED indicator (refer to Figure 1-4). The functions of these controls and indicators are described in Table 1-2. The tape transport also has internal switches for selecting tape units and enabling certain features, but these are preset and normally not changed. It also has an LED fault indicator. This LED is not exposed to view during normal operation.

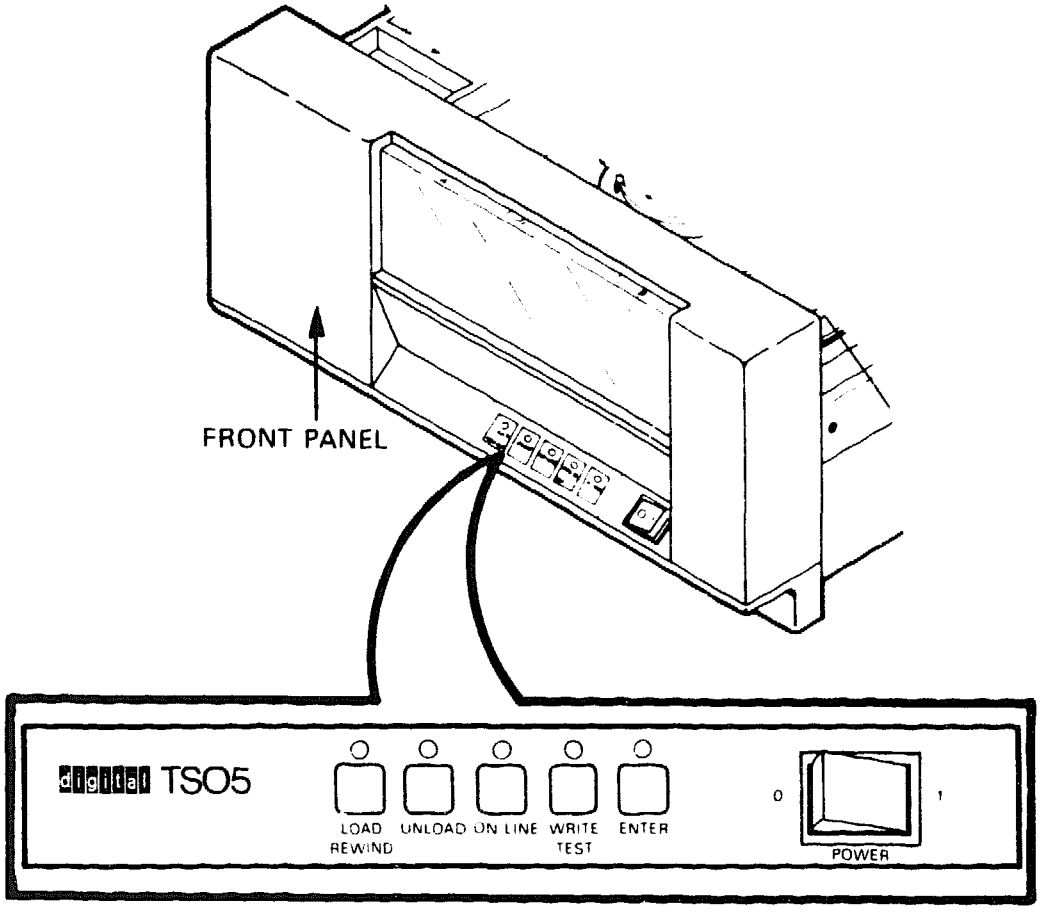


Figure 1-4 Operator Front Panel

Table 1-2 Controls and Indicators

Control/ Indicator	Type	Function
POWER	ON/OFF rocker switch and indicator	Switches line power ON and OFF.
LOAD/REWIND	Tactile switch and indicator	Blinks when the tape drive is executing a load or rewind sequence. Lit continuously when the BOT marker is sensed. Pressing the switch: 1. Initiates load sequence and advances tape to load point. 2. Rewinds the tape to load point.
UNLOAD	Tactile switch and indicator	Pressing the switch unloads the tape regardless of tape position. Blinks when the tape drive is executing an unload sequence. Lit continuously when the tape drive has completed its unload sequence and the front access door is unlocked. At this time, the tape may be removed and another tape inserted into the drive. Lit continuously after a successful power up, indicating a tape may be loaded.
		NOTE **Pressing the on-line switch during a load sequence puts the tape drive on-line when the BOT marker is sensed.**
ON-LINE	Tactile switch and indicator	Lit when drive is ready and on-line. Pressing the switch: 1. Takes the tape drive off-line and extinguishes the indicator. 2. Puts the tape drive on-line and lights the indicator.

Table 1-2 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
WRITE TEST	Tactile switch	Operational only in the test mode. Selects alternative operational mode for other switches.
WRITE TEST	Indicator	Lit when the write ring is installed and data may be written on tape. When indicator is off, write ring is not installed and tape is file protected.
ENTER	Tactile switch	This control is used for manual loading, and controlling the test mode.

1.4 RELATED DOCUMENTS

Additional information regarding the purpose, use, configuration, operation, and maintenance of the TSV05 tape transport subsystem is available in the documents listed in the Preface of this manual. Other related information can be found in the following documents.

Title	Document No.
TSV05 Tape Transport Subsystem Installation Manual	EK-TSV05-IN
TSV05 Tape Transport Subsystem User's Guide	EK-TSV05-UG
XXDP User Guide	AC-90931-MC
DEC/X11 User Document	AC-8240Z-MC
Microcomputers and Memories Handbook	EB-18451-20
Microcomputer Interfaces Handbook	EB-17723-20
TSV05 Pocket Service Guide	EK-TSV05-PG

1.4.1 Customer Ordering

Publications, accessories, and supplies may be ordered from the following distribution centers.

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Digital Equipment Corporation
Accessories and Supplies Group
1050 East Remington Road
Schaumberg, Illinois 60195

Digital Equipment Corporation
Accessories and Supplies Group
Moffett Park Warehouse
632 East Caribbean Drive
Sunnyvale, California 94086

Telephone Orders

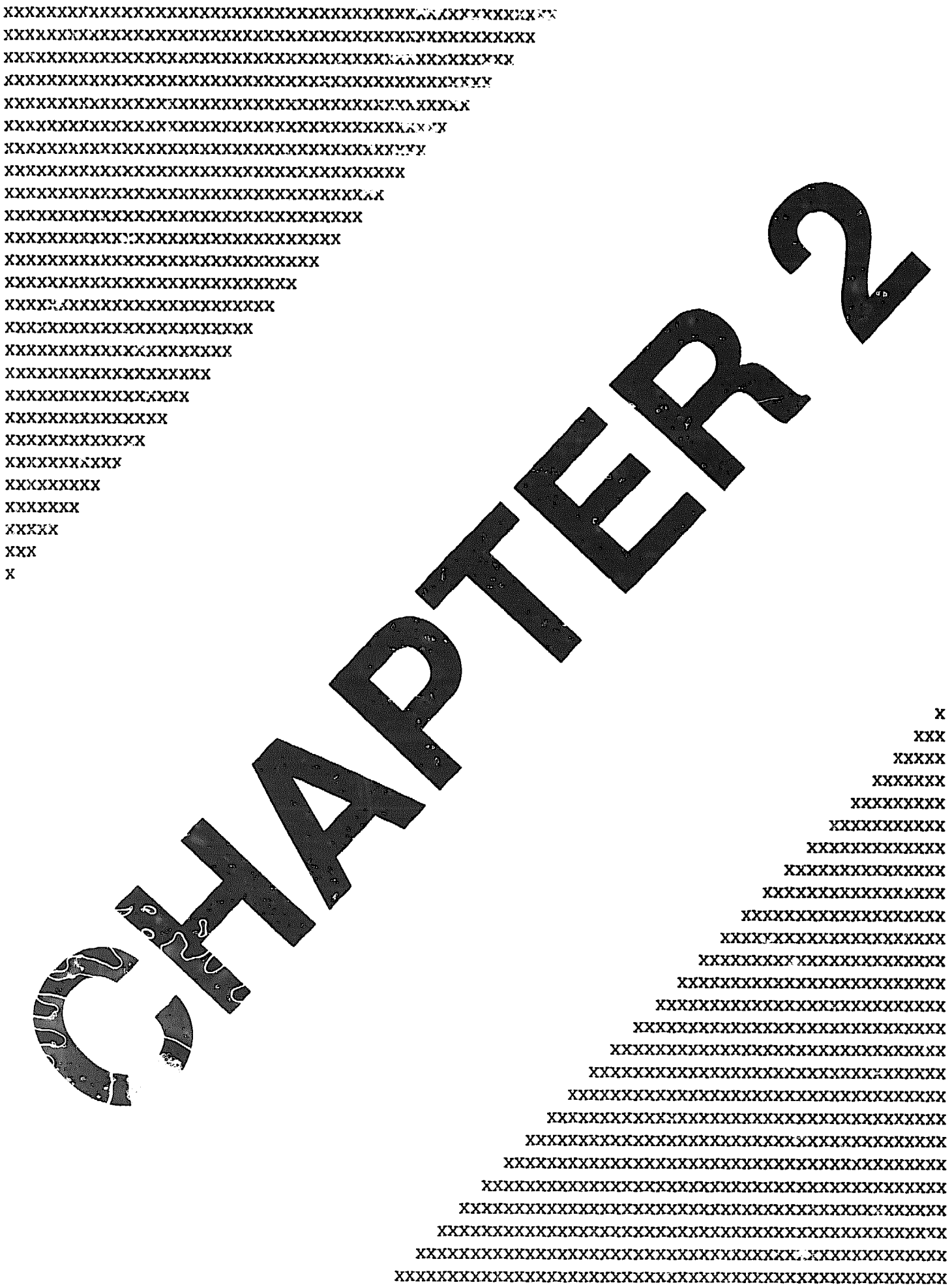
Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-344-4825 from 8:30 a.m. to 5:00 p.m. Eastern Standard Time (U.S. customers only). New Hampshire, Alaska, and Hawaii customers should dial 603-884-6660.

1.4.2 DIGITAL Field Service Ordering

Additional copies of this document and the documents listed above and in the Preface can be obtained from the following address.

Digital Equipment Corporation
444 Whitney Street
Northboro, Massachusetts 01532

ATTN: Printing and Circulation Service (NR2/M15) Customer Services Section


CHAPTER 2

CHAPTER 2
TSV05-S INSTALLATION

NOTE

This chapter describes the 120V, 50/60 Hz rack (-SA) and cabinet models (-SE, and SK), but this description applies to all the other models.

Model	Applicability
-SA	-SA, -SB, -SC, and SD
-SE	-SE, -SF, -SH, and SJ
-SK	-SK, -SL, -SM, and SN

This chapter explains how to install a TSV05 tape transport subsystem into a BA200 series enclosure. Chapter 3 explains how to install a TSV05 tape transport subsystem into other Micro system enclosures. A section is devoted to each of the following:

1. Site preparation.
2. Unpacking and inspection.
3. TS05 tape transport installation.
4. Tape transport checkout.
5. Bus interface/controller preparation.
6. Bus interface/controller installation.
7. Interconnecting cables installation.
8. TSV05 subsystem checkout.

NOTE

Before you unpack the cartons, inspect for signs of shipping damage. If the shipment has been damaged, call the dealer from whom the equipment was purchased. If the equipment is covered under "DIGITAL Transit Insurance", the DIGITAL representative will estimate the damage and put in a claim. If the equipment is not insured by "DIGITAL Transit Insurance", contact the carrier who handled the equipment and your own insurance company. DIGITAL Field Service is available on a per-call basis to make estimates of damage for any resulting insurance claims.

Save all packaging materials for return.

2.1 SITE PREPARATION

2.1.1 Space

All TSV05-S subsystems models require room for access to the cabinet, the correct power receptacle, and an adequate flow of cooling air.

In addition, a TSV05-S subsystem cabinet model (-SE) requires a 597 mm (23.5 in) wide by 838 mm (33 in) deep by 1111 mm (43.75 in) high area of floor space that is capable of supporting a minimum of 121 kg (265 lbs). The cabinet is capable of supporting up to 205 kg (450 lbs).

2.1.2 Accessibility

A TSV05-S subsystem cabinet model (-SE) requires sufficient space behind it for opening the rear door. If any expansion is anticipated, room in front of the cabinet will be required to allow future equipment to be pulled out of the cabinet for maintenance. Refer to Figure 2-1 for required dimensions.

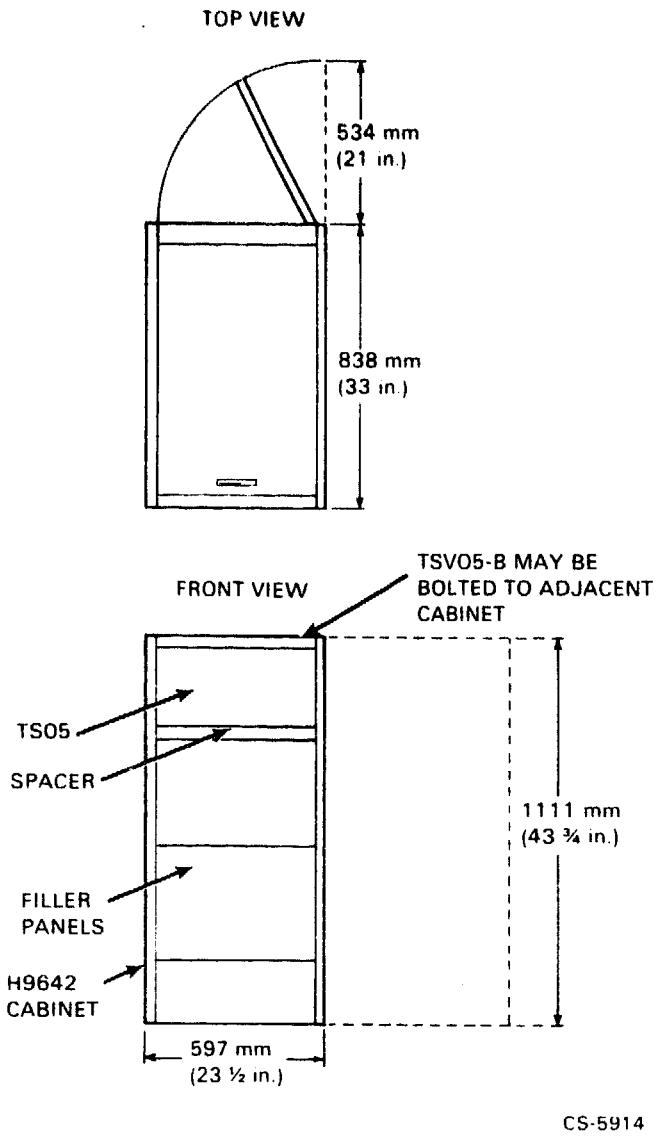


Figure 2-1 Cabinet Access Requirements

2.1.3 Power Receptacles

Ensure that the correct power receptacle is available (Figure 2-2). It should be capable of handling at least the 270 watts required by the tape transport.

2.1.4 Cooling

The TSV05-S subsystems require 1100 Btu per hour of cooling to be provided by the movement of room air through the cabinet.

2.1.5 Air Purity

The tape transport is equipped with internal filters to prevent dust from accumulating on the tape and tape heads. Nevertheless, it is good practice to avoid placing the cabinet in the path of a dust-laden current of air (such as beside a door).

Power Cord Color Code		**Pin Connection**	
Color	Function	L5-30P	6-15P
Brown	Hot	Brass	Brass 1
Blue	Neutral	Silver	Brass 2
Green/yellow	Ground	Ground	Ground

MODEL	PLUG	RECEPTACLE	CIRCUIT RATING
TSV05-SA TSV05-SE TSV05-SC	 NEMA #15-30P DEC # 12-11193	 L5-30R 12-11194	120 V 24 A
TSV05-SB TSV05-SD TSV05-SF TSV05-SJ	 NEMA #6-15P DEC#90-08853	 6-15R 12-11204	220/240 V 12 A

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Figure 2-2 Power Line Connections

2.2 UNPACKING AND INSPECTION

The following paragraphs describe the unpacking and inspection procedures for the TSV05-S cabinet models (-SE). The unpacking procedures for the TSV05-Sx rack-mount kit and cable kit applies equally to the TSV05 rack models (-SA).

CAUTION

The TSV05-Sx installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment prior to unpacking the installation kit. Failure to do so can result in equipment damage.

Only qualified service personnel should remove or install modules.

The TSV05-SE cabinet models are shipped as one skid-mounted carton and one or more smaller cartons. The carton on the skid contains the TS05 tape transport cabinet. The smaller carton(s) contains the TSV05-Sx installation kit (M7206-PA), one of two cable kits [CK-TS05-15 (eight foot cables) or CK-TS05-16 (16 foot cables)], and a soft box kit containing documentation, a cleaning kit and a reel of magnetic tape. These smaller items may be shipped in one carton or two, depending on shipping requirements.

Check the shipping documents to ensure that the correct model has been shipped. If anything is missing, damaged, or incorrect, contact the dealer from whom the equipment was ordered.

2.2.1 Tools and Working Space

The following tools are required:

1. Scissors
2. 9/16 inch wrench
3. 11/16 inch wrench
4. 3/4 inch wrench
5. 5/32 inch hex key
6. Anti-static kit (P/N 29-26246-00)

Also, a space of approximately 3 meters (10 feet) square is required for moving the cabinet off the shipping skid.

2.2.2 Removing the TS05 Tape Transport from the Carton

Use the following procedure to remove the TS05 Tape Transport from its carton.

WARNING

Once the leveling feet are raised, the cabinet is free to roll on its casters. The cabinet is top-heavy and must be handled with care.

1. Cut the nylon straps and remove the cardboard tube (Figure 2-3). Remove the plastic bag.
2. Using a 9/16-inch wrench, remove the four shipping bolts that hold the cabinet to the skid (Figure 2-4).
3. Remove the metal hold-down brackets.
4. Using an 11/16-inch wrench, loosen the leveling feet locking nuts (Figure 2-5).
5. Using a 9/16-inch wrench, screw the leveling feet up into the cabinet base all the way.

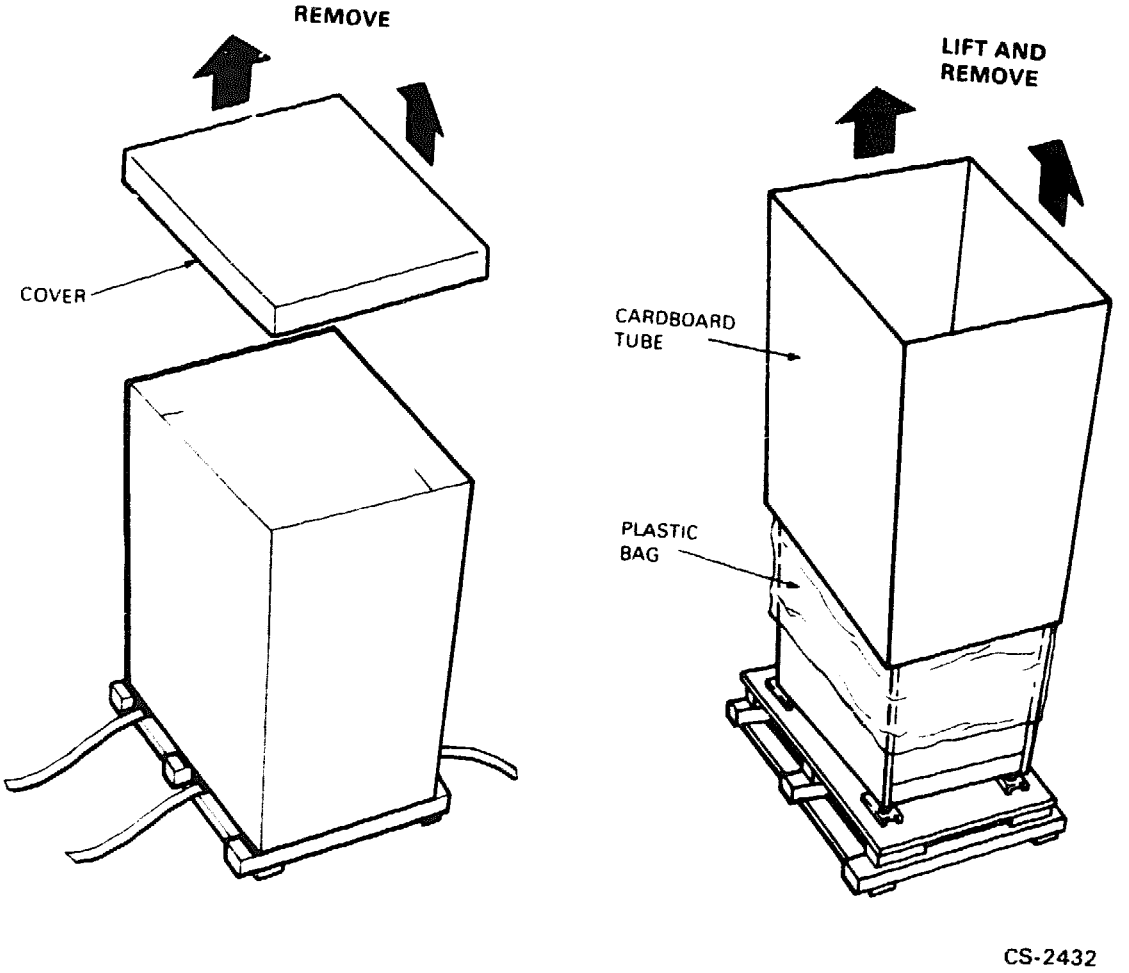

Figure 2-3 Cabinet Carton Removal

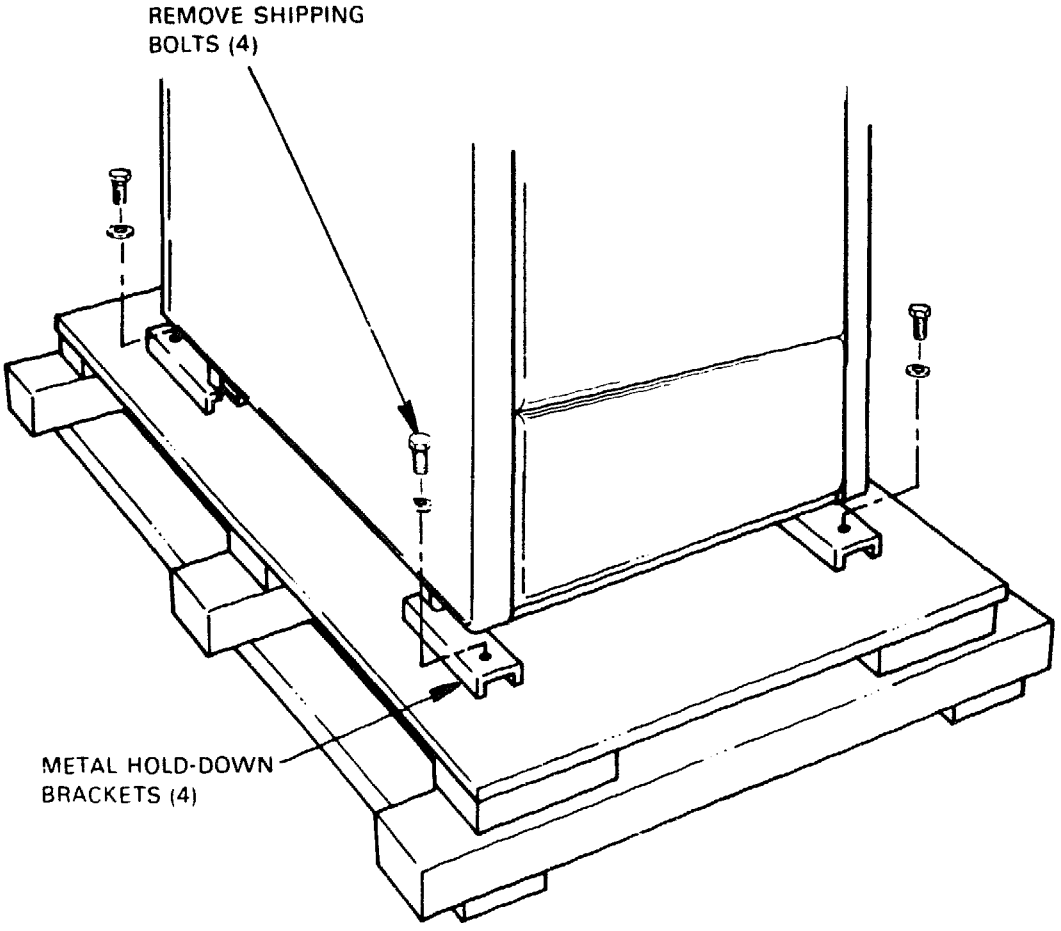

Figure 2-4 Cabinet Shipping Brackets

1. TURN NUT DOWN TO BOTTOM.

2. SCREW FOOT INTO CABINET FAR ENOUGH TO PERMIT CABINET TO BE ROLLED ON ITS CASTERS.

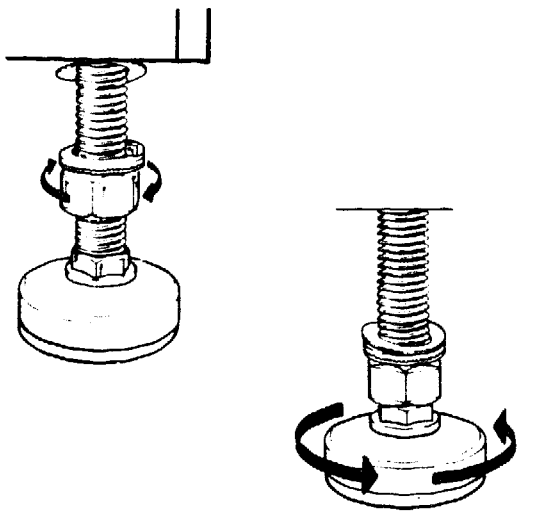

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Figure 2-5 Raising Leveling Feet

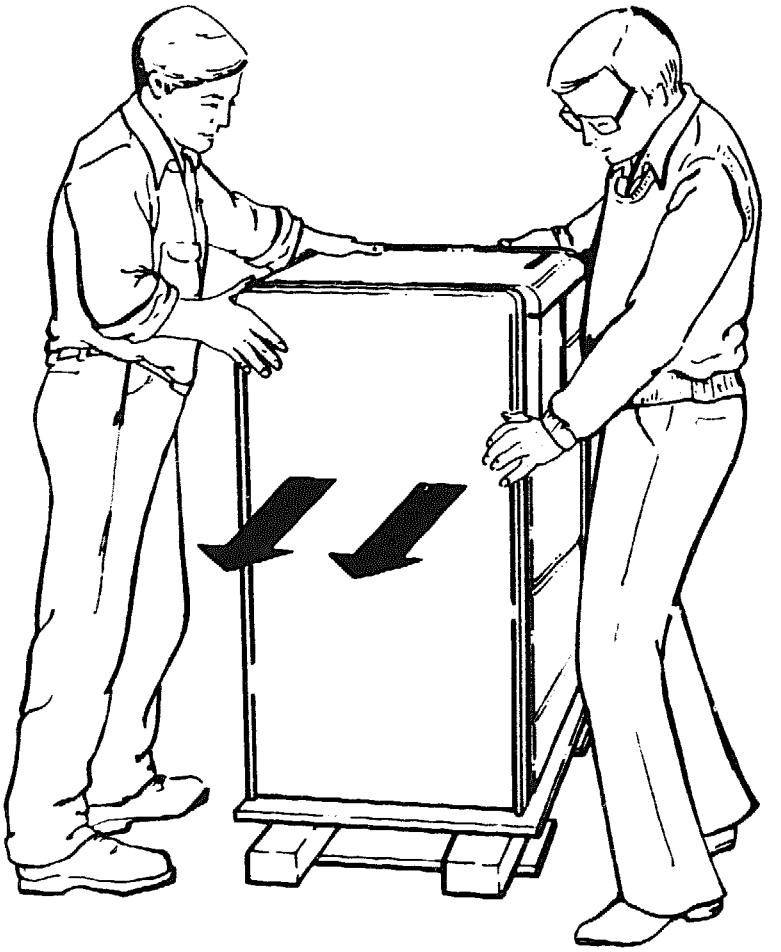
2.2.3 Removing the Cabinet from the Skid

Use the following procedure to remove the cabinet from the skid.

WARNING

Use sufficient manpower to move the cabinet off the skid.

1. Grasp the cabinet by right top and by the left center (Figure 2-6).
2. Roll the cabinet off the side of the skid, taking care to prevent it from toppling over.
3. When the casters on the left side of the cabinet are on the floor, push the skid out from under the right side of the cabinet. Take care to prevent the cabinet from hitting the floor hard or toppling.
4. Open the rear door using a 5/32-inch hex key (Figure 2-7) and verify that the envelope taped to the bottom of the cabinet contains:
   a. Remote cable (P/N 70-08288-8F)
   b. Intercabinet hardware (P/N 74-22224/74-22225)
   c. Four 1/4-20 x 2.75 inch bolts
   d. Twelve 1/4-20 self-retaining nuts



CS-2435

Figure 2-6 Deskidding the Cabinet

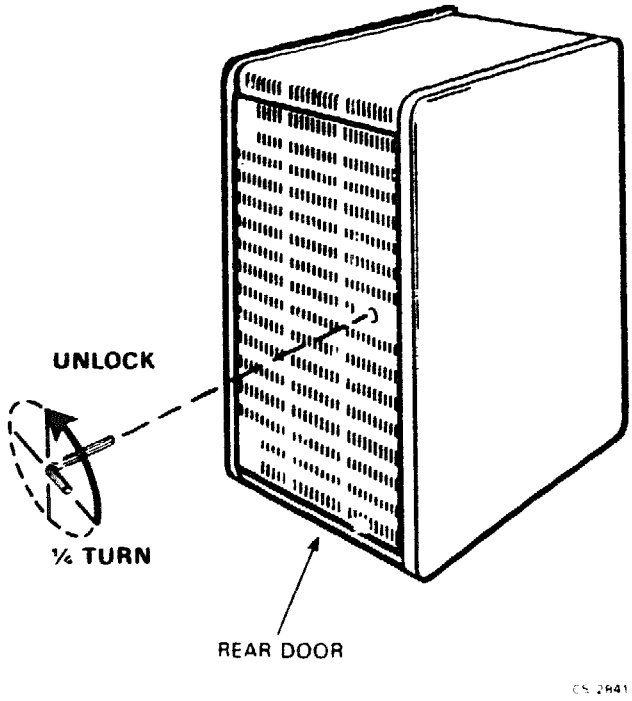


Figure 2-7 Opening Cabinet Door

2.2.4 Unpacking the TSV05-Sx Installation Kit

CAUTION

The TSV05-Sx installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment[1] prior to unpacking the installation kit. Failure to do so can result in equipment damage.

NOTE

Do not dispose of the packing material until the module has been successfully installed and is operational.

1. Before you open the shipping container, look for external damage on the shipping container such as dents, holes, or crushed corners.
2. Put on your anti-static wrist strap.
3. Ground the wrist strap and anti-static mat to a local ground. Use the anti-static mat for placement of the module.
4. Open the shipping container.
5. Remove the M7206 module from the anti-static bag.
6. Inspect the module for shipping damage. Check carefully for cracks, breaks, and loose components. Ensure that the seven PROMs are fully seated in their sockets.
7. Report any damage to the shipper and notify the DIGITAL representative.
8. Ensure that there is no residue or corrosion on the handle's EOS and FCC clips (Figure 2-8). If so, remove it with alcohol or other approved mild cleaners.
9. Ensure that there is no residue or corrosion on the gap filler assemblies. If so, remove it with alcohol or other approved mild cleaners.
10. Ensure that the EOS and FCC clips on the handle are in an arch shape. When pressed slightly, they should return to their original shape.
11. If any clip is missing, broken, distorted, or corroded, replace it with EOS clip P/N 12-26922-01, or FCC clip P/N 12-23640-01.

[1] Anti-Static Kit (29-26246-00) is not included, but is part of Field Service Tool Kit.

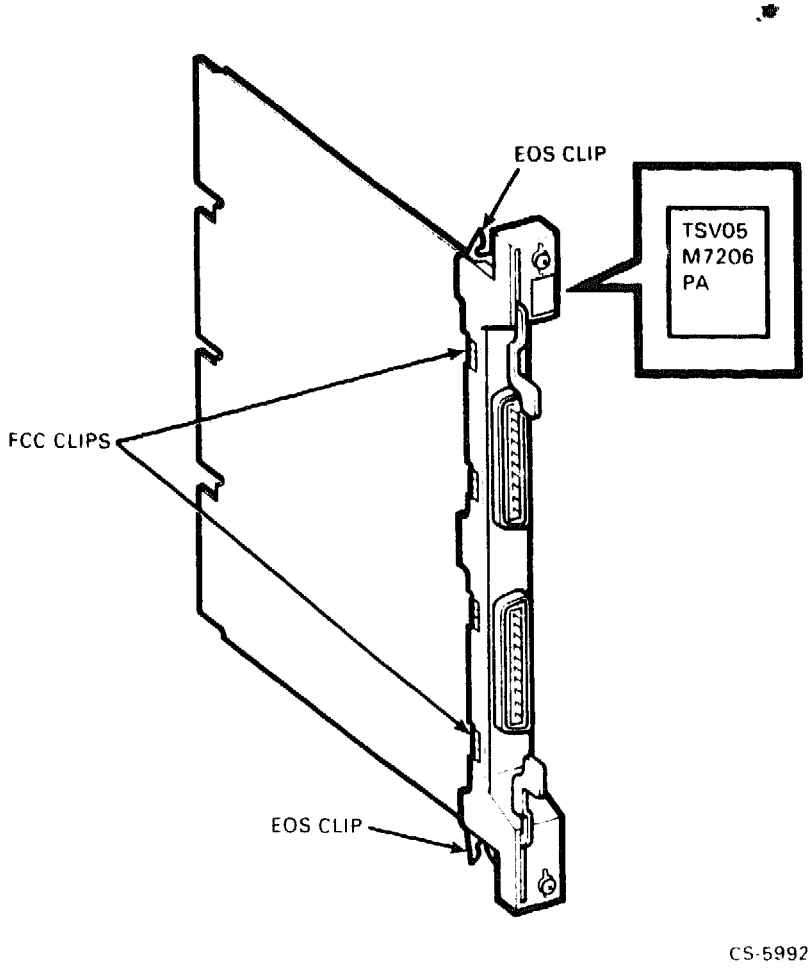


Figure 2-8 M7206-PA Module

2.2.5 Unpacking the Cable Kit (CK-TS05-15 or CK-TS05-16)

Open the shipping container and check its contents. The kit (Figure 2-9) should contain the following:

- Two individually boxed cables (P/N 17-01822-02 eight foot) or (P/N 17-01822-01 16 foot).
- Peel-off cable labels sufficient for marking both the two cables.
- One filler panel kit (P/N 70-24505-01)[2].
- One installation guide (EK-TSV05-IN).
- One #10 screw.
- Two tywraps.
- Two tywrap mounting clamps.

2.2.6 Unpacking the Other Small Cartons

Open the other soft box kit (P/N 70-224[illegible]8-00) and check its contents. The kit should contain the following.

- *TSV05 Installation Manual* (EK-TSV05-IN)
- *TSV05 Users Guide* (EK-TSV05-UG)
- *TSV05 Technical Manual* (EK-TSV05-TM)
- Tape cleaning kit
- Magnetic tape (2400 feet, blank)

If any item is damaged, missing, or incorrect, contact the dealer from whom the system was purchased.

[2] The filler panel kit should include two gap filler assemblies and four 1/4 inch flat-head machine screws.

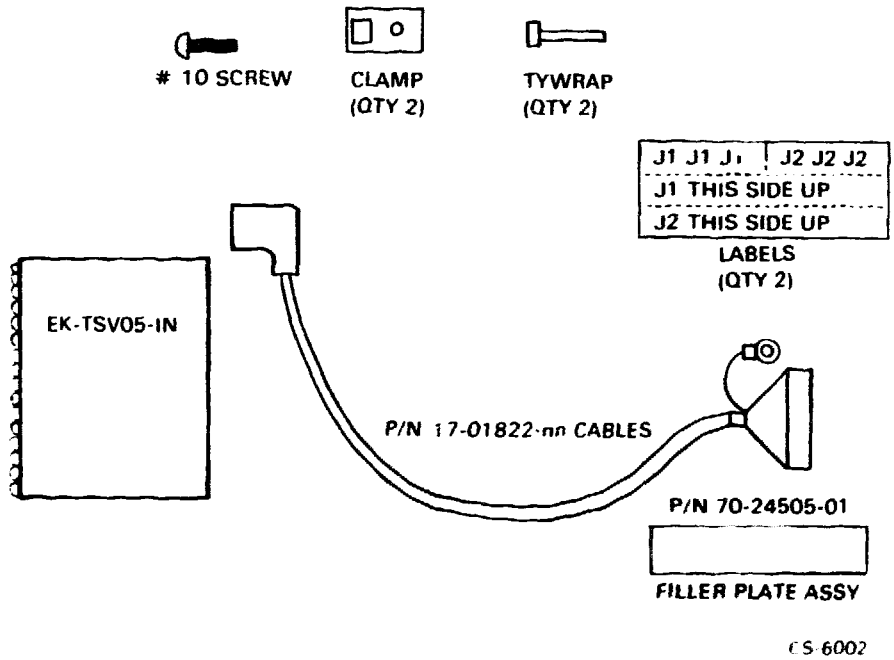


Figure 2-9 CK-TS05-nn Cable Kit Components

2.3 TAPE TRANSPORT CABINET INSTALLATION

NOTE

Installing the TSV05-SA subsystems in cabinets other than the H9642 cabinet may result in higher levels of EMI radiation.

2.3.1 Installing the Cabinet

The TSV05-SA tape transport model is intended to be mounted in a user-supplied or separately purchased cabinet. Refer to Appendix B for TSV05-SA rack mounting guidelines.

The TSV05-SE tape transport model is shipped mounted in an H9642 cabinet.

The TSV05-SE tape transport model is to be connected to another cabinet, then refer to Appendix D.

The TSV05-SK model is shipped with a cabinet top cover P/N 70-16864-00. Refer to Appendix D for top cover installation procedure.

2.3.2 Removing the Shipping Foam

The tape transport is shipped with foam cushions protecting the takeup hub and blower motor. These cushions must be removed before the unit is powered up. This requires opening the tape transport to the operator maintenance access position to remove the foam from around the takeup hub, and opening it to the service access position to remove two other pieces of foam.

2.3.2.1 Removing the Top Foam Pieces -

1. On TSV05-SE models, raise the top of the cabinet by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up (Figure 2-10).
2. Raise the top cover of the tape transport unit by reaching in through the front door and pushing upward on the front of the top cover. Prop the cover up using the nylon support that hangs from the left side of the cover (Figure 2-11).
3. Gently move the tachometer assembly away from the takeup hub (Figure 2-12). Remove the foam cushion. Carefully place the tachometer assembly back on the takeup hub.
4. Inspect and ensure that the tape path area is free of any foreign matter. With the cover still in the operator maintenance access position, remove the bottom foam pieces (Section 2.3.2.2).

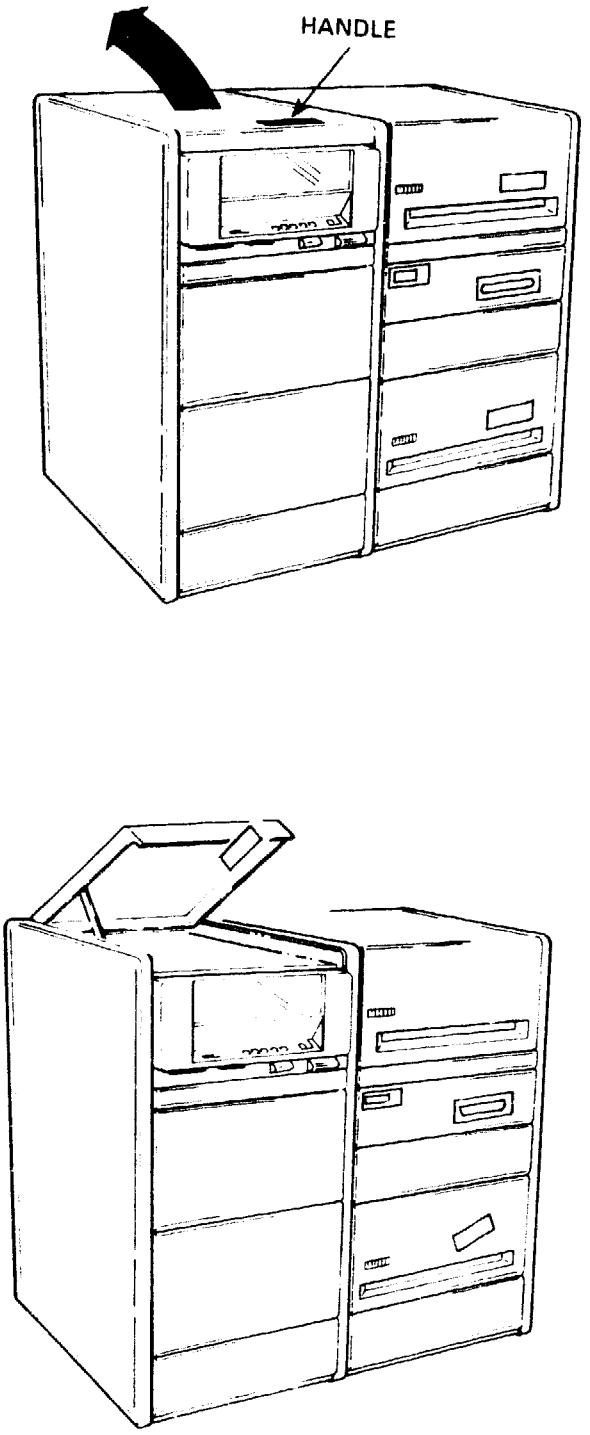


Figure 2-10 Cabinet Top Cover

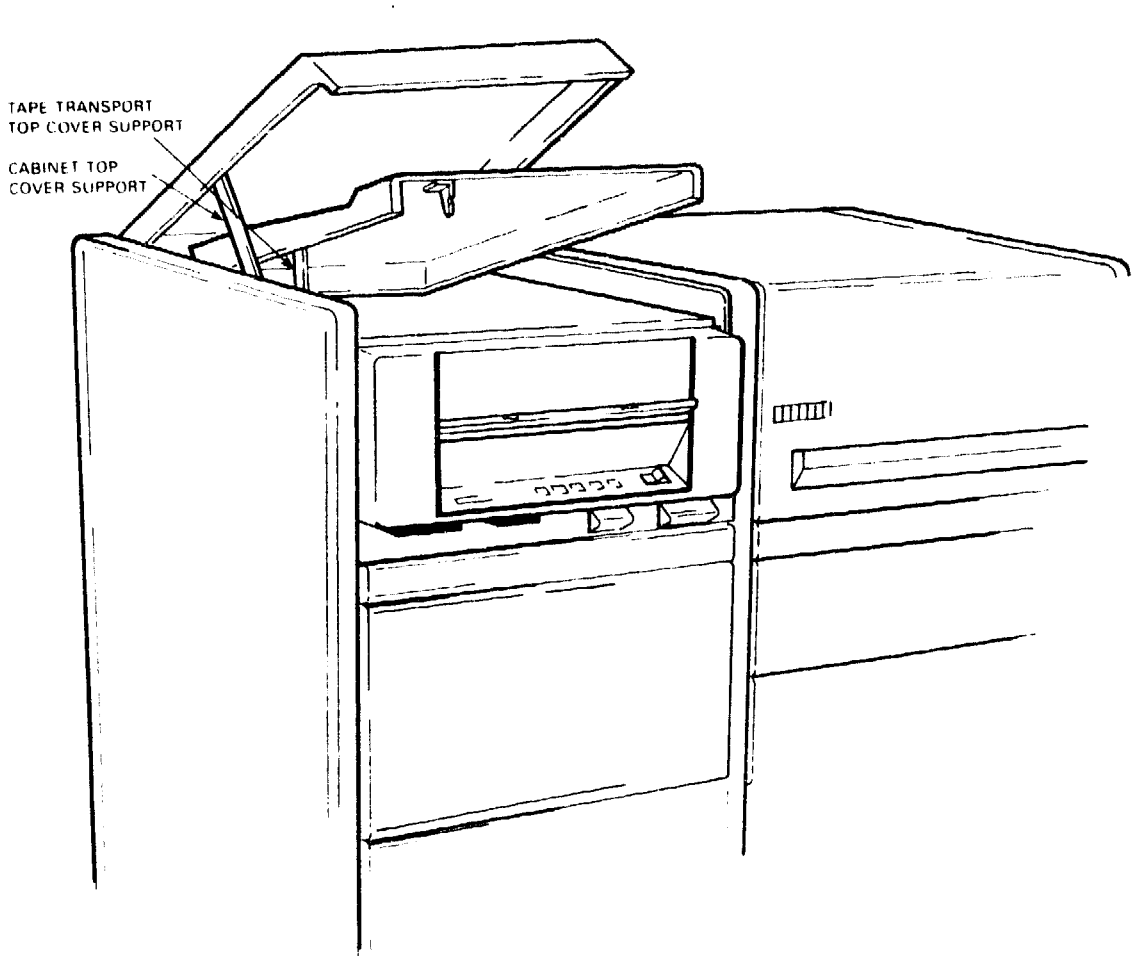


Figure 2-11 Tape Transport Top Cover

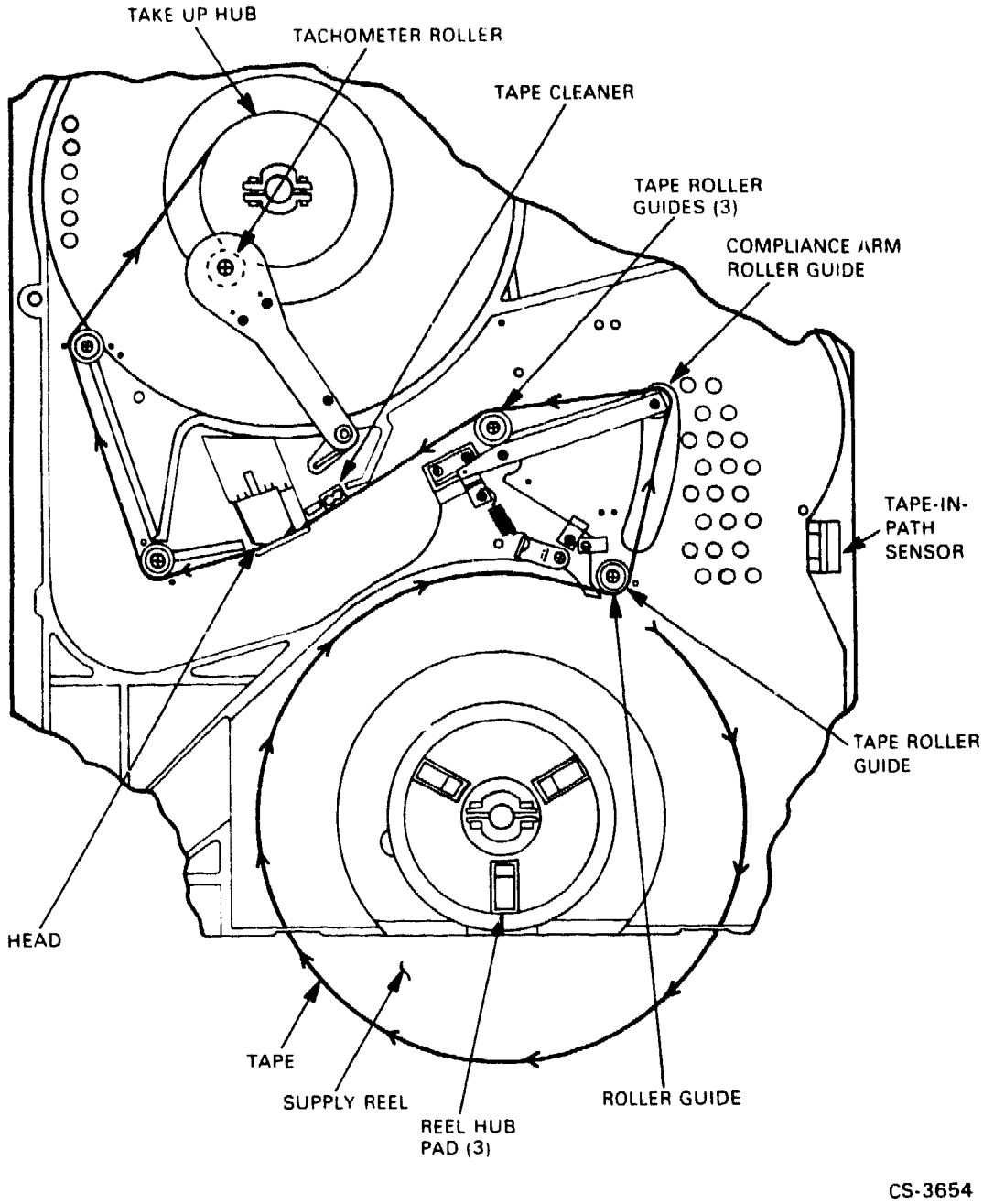


Figure 2-12 Tachometer and Takeup Hub

2.3.2.2 Removing the Bottom Foam Pieces -

NOTE

The Sandcast unit has a sandcasted top plate which is painted black, while the diecasted top plate has the appearance of a plain aluminum surface.

1. Loosen the two spring-loaded captive screws, located on each side (as viewed from the top of the TS05 tape transport unit), that secure the TS05 unit to the top rail assembly. (See Figure 2-13 if it is a Sandcast unit, or Figure 2-14 if it is a Diecast unit.)
2. Lower the top cover of the tape transport unit.

WARNING

Keep hands clear of corners of the tape unit while lifting. This is important to avoid brushing the mounting rails with your hands while lifting the unit, to prevent lacerations.

3. With both hands, grasp the lower front of the TS05 unit and lift the entire assembly to its maximum upright position. (This engages the locking mechanism automatically.)

WARNING

To eliminate the possibility of the tape unit dropping due to a failure in the locking mechanism, insert the supplied safety pin into the hole provided [2.5 cm (1.0 in)] above the locking mechanism on the top plate supporting slide, to prevent crushing your arms.

4. Carefully lower the TS05 unit approximately 2.5 cm (1.0 in). (This will activate the locking mechanism automatically.) Route the safety pin behind the supporting slide and across in front, and install it from left to right.

NOTE

Perform step 5 only if it is a Sandcast unit. Proceed to step 6 if it is a Diecast unit.

5. Release the drive/formatter module by pulling down on the two NyLok[3] fasteners that secure it to the bottom of the top plate assembly. When the NyLok fasteners are released, carefully lower the drive/formatter module as far as it will go.

[3] NyLok is a trademark of NyLok Fastener Corporation

6. Remove the sheet and block of foam from the unit.

7. Place the TS05 unit back to the operating position by reversing steps 1 through 5.

NOTE

To release the cabinet top cover support arm, it is necessary to raise the top cover slightly and move the top of the arm forward.

8. Close the top cover of the tape unit and the top cover of the cabinet.

2.3.3 Connecting Line Power

TSV05-SE and -SK models are equipped with cabinet power controllers. Before connecting the line power, perform the following checks:

1. Power switch on the front panel of the tape transport is in the 0 (OFF) position.
2. Power controller voltage rating is correct for your system.
3. Power controller circuit breaker switches are in the 0 (OFF) position.
4. Power controller LOCAL/REMOTE switch is in the LOCAL position. [4]

With the switches in these positions, unwind the power cable and plug it into the receptacle.

[4] On some power controllers, this switch is labeled A O B respectively. If this is the case, place the switch in the B position.

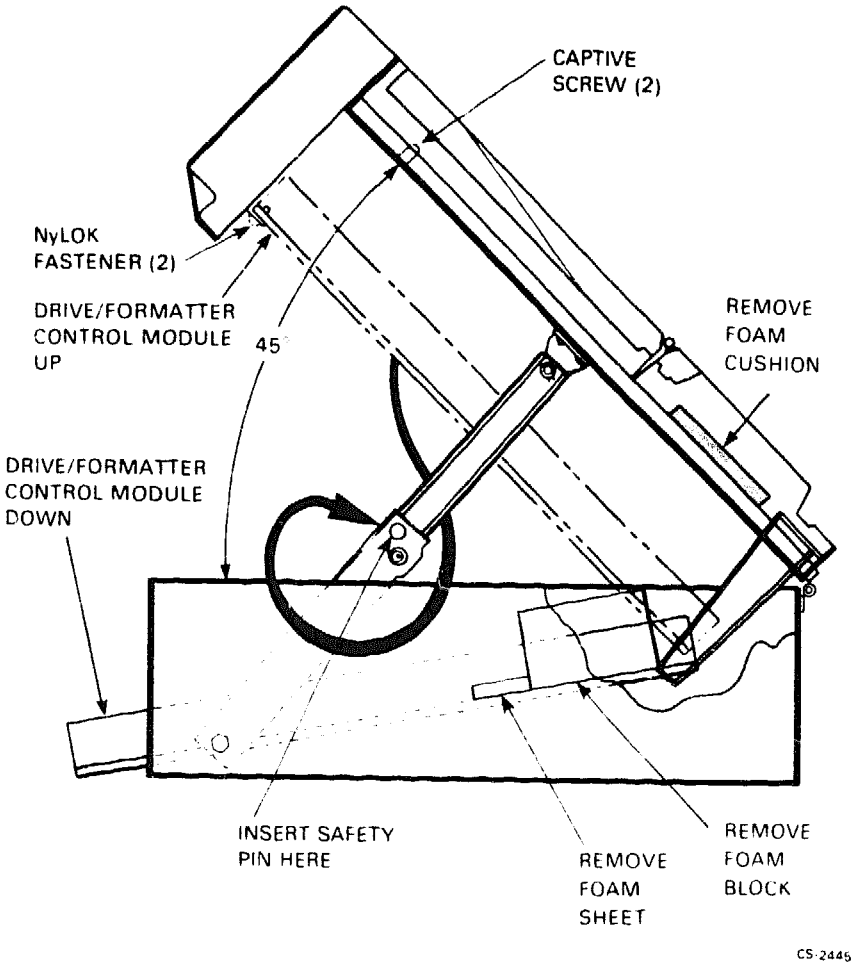


Figure 2-13 Service Access Position (Sandcast Unit)

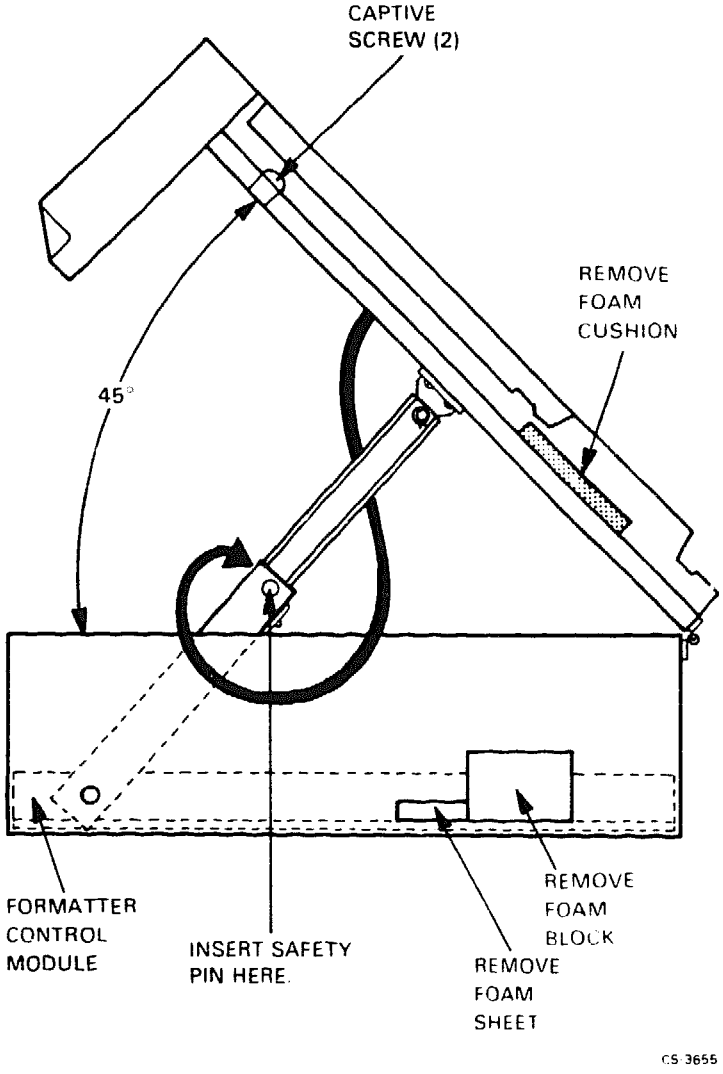


Figure 2-14 Service Access Position (Diecast Unit)

2.4 TAPE TRANSPORT CHECKOUT

The tape transport is tested by itself before being cabled to the bus interface/controller module. This standalone testing is performed with the line power controlled locally at the cabinet power controller[5]. After standalone operation has been verified, operation with the computer system is tested. For the tests in this section, the remote control cable remains unconnected.

2.4.1 Power-Up Test

1. Switch the circuit breaker switches on the cabinet power to the ON position. Observe that the power controller pilot lamp lights. Close the cabinet rear door.
2. On the tape transport front panel (Figure 2-15), press the POWER switch to the 1 (ON) position. Observe that all indicators light for approximately two seconds.
3. Observe that after two seconds all the indicators extinguish, and then the UNLOAD indicator lights.

If these indications have occurred, the tape transport unit has successfully completed the internal verification checks that it performs automatically at power-up. If the indications were different, there is a problem. Refer to the *TSV05 Pocket Service Guide* or call your local DIGITAL representative.

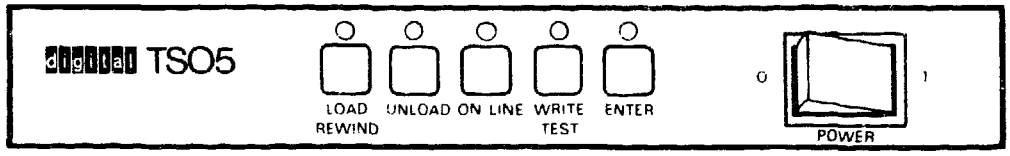


Figure 2-15 Front Panel Controls and Indicators

[5] If your cabinet does not have a power controller, simply connect power cable to the primary power outlet.

2.4.2 Tape Loading Test

This test verifies the ability of the TSV05 subsystem to automatically load a tape. It requires a tape that is blank except for the BOT and End-Of-Tape (EOT) markers. Refer to Figure 2-16 and proceed as follows.

CAUTION

Both the tape transport top cover and the front panel door are locked when a tape is loaded. Any attempt to force open either the cover or the door before the tape is unloaded will result in mechanical damage to the locking mechanism.

1. Ensure that the tape is wound completely onto the reel and that the end has been properly crimped.
2. Open the front panel door by gently pressing down on the top center area of the door.
3. Hold the tape with the file-protect ring side down and insert it into the transport unit, centering it on the hub.
4. Close the door.
5. Press the LOAD switch. This locks the cover and the door and begins the loading sequence.
6. Observe the LOAD indicator. It blinks while the tape is being loaded. After a maximum of 135 seconds, it stops blinking and remains lit. This indicates that the tape loading sequence is complete.

If the LOAD indicator does not stop blinking, or if the other indicators begin to blink, there is a problem. Unload the tape, check for a proper crimp, and retry the test. If the tape does not load, refer to the *TSV05 Pocket Service Guide* or to the manual loading instructions in Appendix B.

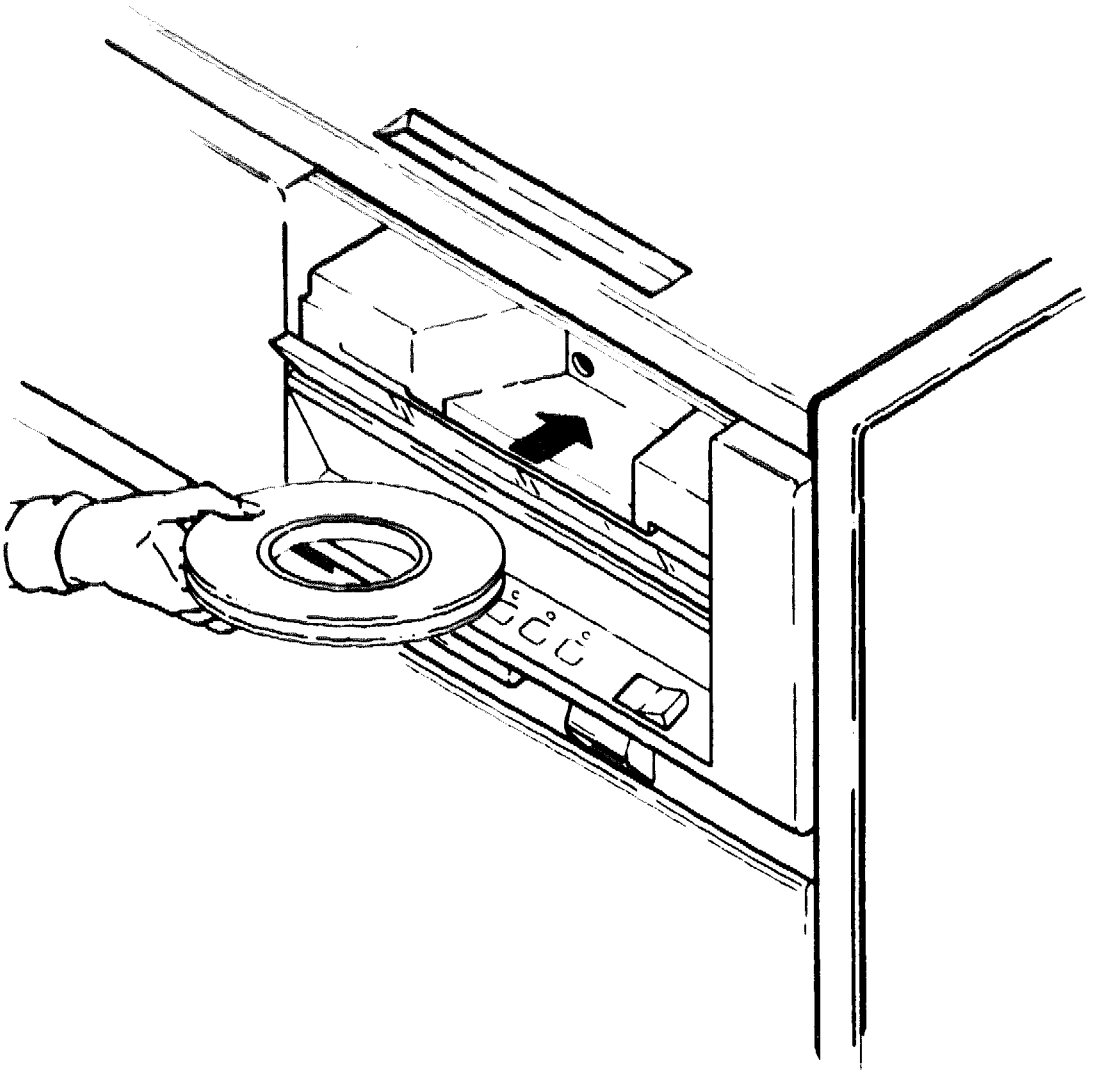


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Figure 2-16 Inserting Tape

2.4.3 Tape Movement Test

This test exercises the tape drive in both forward and reverse directions and at both high and low speeds.

NOTE

If you make an error and enter an illegal test sequence, or if you stop during the sequence and permit more than two seconds to pass before pressing the next switch in the sequence, the system aborts the test instruction and you must start the sequence from the beginning. An erroneous or aborted test instruction results in an expanding pattern of blinking.

1. Start the test by pressing the front panel control switches in the following sequence.
   a. TEST
   b. ENTER
   c. UNLOAD
   d. UNLOAD
   e. ENTER
2. The tape should begin to move after step e.
3. Observe the indicators. If, over a period of two minutes, they change their blinking value substantially, there is a problem. If the blinking remains about the same, the test is progressing successfully.
4. After two minutes, terminate the test by pressing the TEST key. This causes the tape to rewind (which may take several minutes) and the LOAD indicator to light.

If problems are encountered, refer to the *TSV05 Pocket Service Guide*.

2.4.4 Tape Unloading Test

This test verifies the ability of the tape unit to unload the tape automatically.

1. Press the UNLOAD switch.
2. Observe the UNLOAD indicator. It blinks to indicate that the tape is being unloaded. When the unloading process is complete, the UNLOAD indicator lights continuously, and the front panel door and top cover are unlocked. This should take a maximum of 15 seconds.
3. Open the front panel door and lift the tape reel out of the tape transport.
4. Close the door.
5. Press the tape transport POWER switch to the 0 (OFF) position.
6. Switch the circuit breaker switches on the cabinet power controller to the OFF position.

2.5 BUS INTERFACE/CONTROLLER MODULE PREPARATION

2.5.1 Checking the Configuration

NOTE

The M7206 module should be positioned as the next module after CPU and memory.

Complete the BA200 series enclosure configuration worksheet (Figure 2-17) to make sure you do not exceed the system limits for power and bus loads.

You may need to gain access to the modules installed in the system backplane before you configure the system. Refer to the system's documentation for further information on how to gain access to the system modules. To check the system configuration, perform the following steps.

1. On the configuration worksheet, list all the devices already installed in the system.
2. List all the devices you plan to install in the system.
3. Fill in the information for each device, using the device information listed in Table 2-1.
4. Add up the columns. Make sure the totals are within the limits for the enclosure.

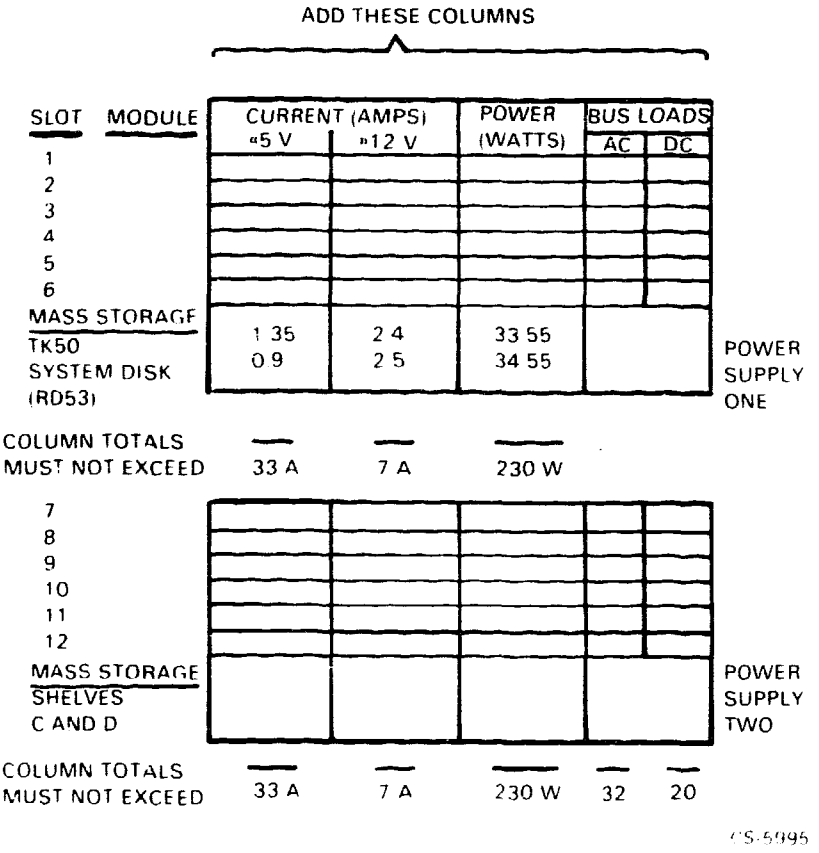


Figure 2-17 BA200 Series Configuration Worksheet

Table 2-1 Power and Bus Load Data

Option	Amps (Max)		Power(Max)	Bus Loads	
	+5 V	+12V	Watts	AC	DC
CXA16-M	1.6	200mA	10.4	3.0	0.5
CXB16-M	2.0	0.0	10.0	3.0	0.5
CXY08-M	1.8	300mA	12.6	3.2	0.5
DEQNA-SA	3.5	0.50	23.5	2.2	0.5
DPV11-SA	1.2	0.30	#2.6	1.0	1.0
DRQ3B-SA	4.5	0.0	22.5	2.0	1.0
DRV1W-SA	1.8	0.0	#2.0	2.0	1.0
DZQ11-SA	1.0	0.36	#2.3	1.4	0.5
IBQ01-SA	5.0	0.30	28.6	4.6	1.0
IEQ11-SA	3.5	0.0	17.5	2.0	1.0
KA620-AA	6.2	0.14	32.7	2.7	1.0
KA630-AA	6.2	0.14	32.7	2.7	1.0
KDJ11-BF	5.5	0.2	22.2	2.6	1.0
KDJ11-SA/SB	3.47	0.12	12.6	3.0	1.0
MRV11-D	1.6*	0.0	#8.0*	3.0	0.5
MS630-BB	1.8	0.0	#2.0	0.0	0.0
MS630-CA	3.1	0.0	15.5	0.0	0.0
MSV11-JD	3.74	0.0	18.7	2.7	0.5
MSV11-JE	4.1	0.0	20.5	2.7	0.5
MSV11-QA	2.4	0.0	12.0	2.0	1.0
RQDX3-M	2.48	0.06	13.1	1.2	0.5
TQK50	2.2	0.0	14.5	2.8	0.5
M2060-YA	5.3	0.0	26.5	0.0	0.0
RD53A-EA	0.2	2.5	34.5	0.0	0.0
RD54A-EA	1.3	1.34	22.6	0.0	0.0
TK50E-EA	1.35	2.4	35.6	0.0	0.0
TSV05 M7206-PA	6.5	0.0	24	3.0	1.0

* Value is for unpopulated module only

2.5.2 Placing the Module

2.5.2.1 Bus Continuity - Bus grant signals pass through each installed module through the A connectors of each slot. Figure 2-18 shows the bus grant routing. You must use a bus grant continuity card in vacant backplane slots to ensure bus continuity.

The M7206 uses the BIRQ4 line to request interrupt service. It does not monitor any of the higher-level interrupt request lines. Because of this, both the interrupt-request and DMA (non-processor request) priorities of the M7206 are selected by the position of the module on the bus. Devices closest to the CPU module have the highest priority.

The M7206 bus position is critical. The following list shows the sequence.

1. CPU module
2. Memory modules
3. M7206

2.5.2.2 Power Supplies - The BA200 series enclosure contains one or two separate 230 watt power supplies. For enclosures with two power supplies, the first (right side) power supply powers slots 1 through 6; the second (left side) power supply powers slots 7 through 12.

Each power supply in the enclosure must have a minimum 5 amp load on the 5 volt output to maintain regulation. If a power supply does not meet the minimum load requirement, you *must* install a load module (M9060-YA) in an open backplane slot that is powered by the power supply. The power supply will enter an error mode and shuts down the system, if the minimum load requirement was not adhered to. If a power supply meets or exce 's the minimum load requirement, you should remove an existing load module.

Refer to Section 2.6 for procedures used to install or remove modules.

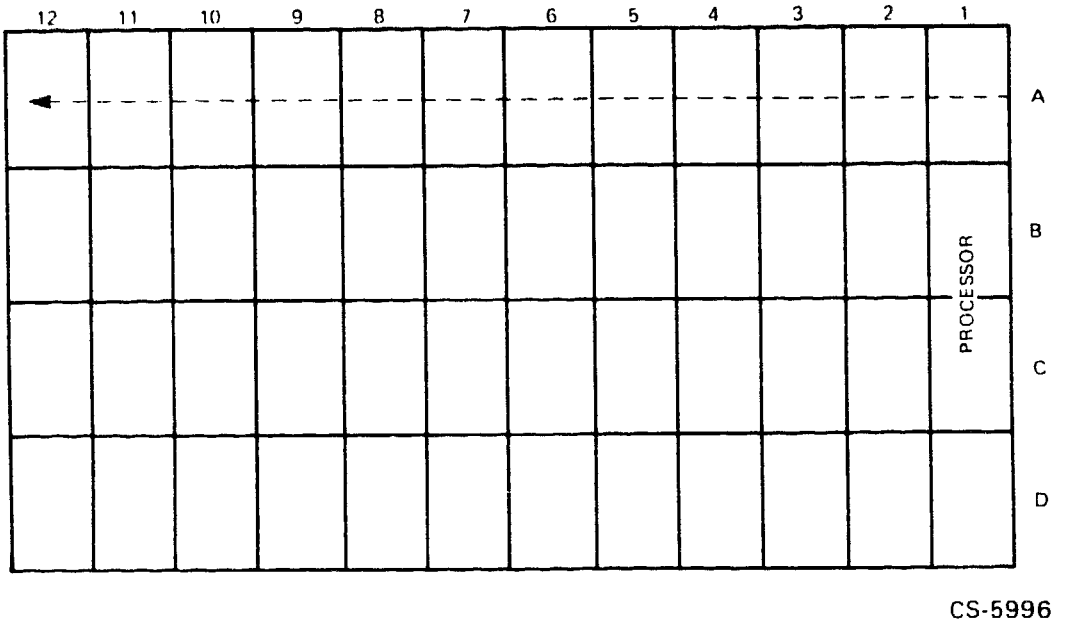


Figure 2-18 Bus Grant Continuity Path

2.5.3 Finding CSR Addresses and Interrupt Vectors

2.5.3.1 Micro/PDP-11 Systems - For information on how to find CSR addresses and interrupt vectors for modules in a Micro/PDP-11 system, refer to the *Micro/PDP-11 Systems Maintenance Guide*.

2.5.3.2 MicroVAX Systems - To find CSR addresses and interrupt vectors manually for modules in a MicroVAX system, see the *MicroVAX Systems Maintenance Guide*.

You may also use the CONFIG program in the MicroVMS or the VMS SYSGEN utility to determine the correct CSR address and interrupt vector for the modules in the system. When you type in a list of the devices in the system, CONFIG automatically provides CSR address and interrupt vector information. Table 2-2 lists the devices supported by this utility. Figure 2-19 is a sample SYSGEN utility display.

Table 2-2 Devices Supported by SYSGEN

Device	Enter at DEVICE Prompt	Device	Enter at DEVICE Prompt
CXA16	DHV11	DZV11	DZ11
CXY08	DHV11	IEQ11	IEQ11
DEQNA	QNA	KDA50	UDA
DHV11	DHV11	LPV11	LP11
DLVJ11	DJ11	RC25	UDA
DMV11-M	DMV11	RQDX2	UDA
DMV11-N	DMV11	RQDX3	UDA
DPV11	DPV11	RRD50	VDA
DRV11-WA	DR11W	TQK50	TU81
DZQ11	DZ11	TSV05	TS11

```
$MCR SYSGEN
SYSGEN> CONFIGURE
DEVICE> DHV11.2
DEVICE> DMV11
DEVICE> QNA
DEVICE> UDA.2
DEVICE> TU81
DEVICE> CTRL/Z

Device: UDA     Name:  PUA  CSR: 772150   Vector: 154    Support: yes
Device: TS11    Name:  MSA  CSR: 772520   Vector: 224    Support: yes
Device: QNA     Name:  XQA  CSR: 774440   Vector: 120    Support: yes
Device: DMV11   Name:  XDA  CSR: 760320*  Vector: 300*   Support: yes
Device: UDA     Name:  PUB  CSR: 760354*  Vector: 310*   Support: yes
Device: DHV11   Name:  TXA  CSR: 760500*  Vector: 320*   Support: yes
Device: DHV11   Name:  TXB  CSR: 760520*  Vector: 330*   Support: yes
```

Figure 2-19 SYSGEN Utility Display

To use the SYSGEN utility, type the following at the system command prompt:

MCR SYSGEN

Press <RETURN>.

The utility responds with the prompt

SYSGEN

At the prompt, type

CONFIGURE

Press <RETURN>.

The utility responds with the prompt

DEVICE

At this point, enter the abbreviation for each device already installed in the system and for each device you intend to install in the system. Table 2-2 lists the abbreviations.

Enter one abbreviation per line, then press <RETURN>. The **DEVICE** prompt prompts you for another entry. If you are installing more than one unit of a particular device, enter a comma and the number of devices after the abbreviation. For example, **DHV11,2** indicates two DHV11 modules.

After you have entered all devices, type <CTRL Z>. The program displays the following information for each device you entered.

- CSR address and vector
- The name assigned to the device by the operating system
- The operating system support status (yes or no)

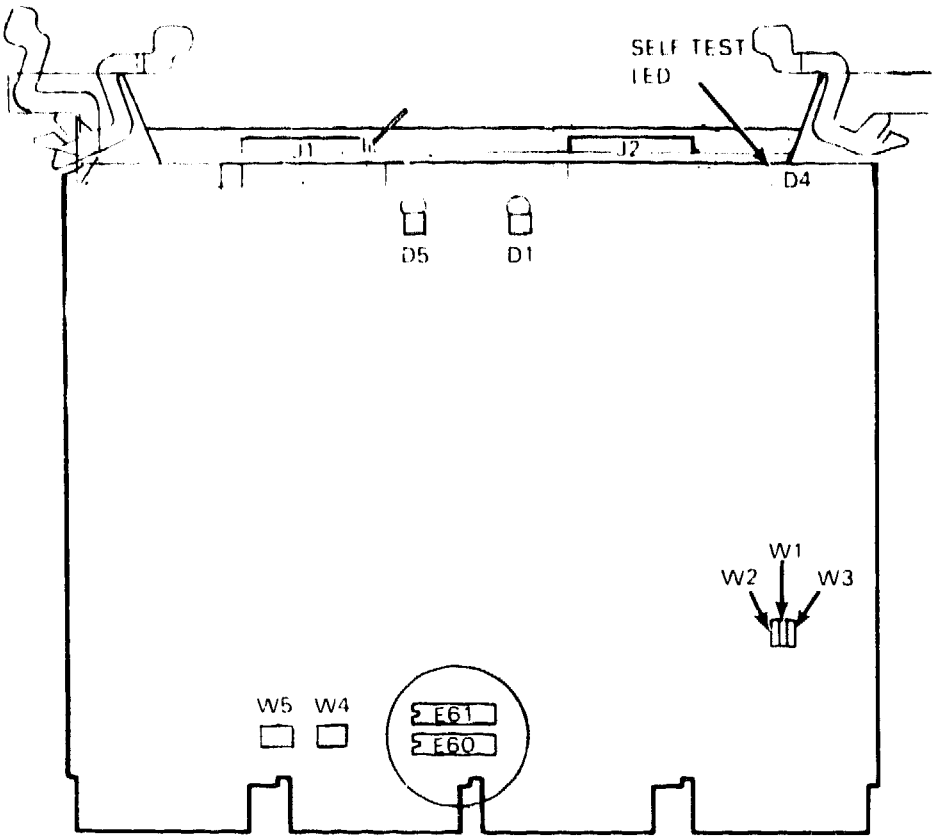
The program uses an asterisk (*) to indicate a floating address or vector. If there is more than one unit of a particular device, the first address refers to the first device to be installed. To exit from the SYSGEN utility, type <EXIT> at the SYSGEN prompt and press <RETURN>.

2.5.4 Configuring the TSV05

Before installing the TSV05 module, you must define two parameters by selecting them on the module on-board switchpacks. The parameters are listed below.

- Module address (CSR)
- Interrupt vector address

You select the CSR address and interrupt vector for the TSV05 by using DIP switches on the module Figure 2-20. The module uses a floating CSR address and interrupt vector. The M7206 is factory set to a CSR address of 772520 (octal) and an interrupt vector of 224 (octal). The factory settings are only correct if no other floating address or vector option is installed in the Micro ystem. Figure 2-21 and Table 2-3 show the factory settings.



VECTOR SWITCHPACK

	1	2	3	4	5	6	7	8	9	10	
ON	V8	V7	V6	V5	V4	V3	V2	S1	S0	A12	E58
OFF											

ADDRESS SWITCHPACK

	1	2	3	4	5	6	7	8	9	10	
ON	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	E57
OFF											

JUMPERS		AS SHIPPED
W1	BIRQ5	OUT
W2	BIRQ7	OUT
W3	BIRQ6	OUT
W4	BUS GRANT CONTINUITY	IN
W5	BUS GRANT CONTINUITY	IN
W6	SCLOCK ENABLE (USED DURING FACTORY REPAIR ONLY)	IN

CS-6097

Figure 2-20 M7206 Switch and Jumper Identification

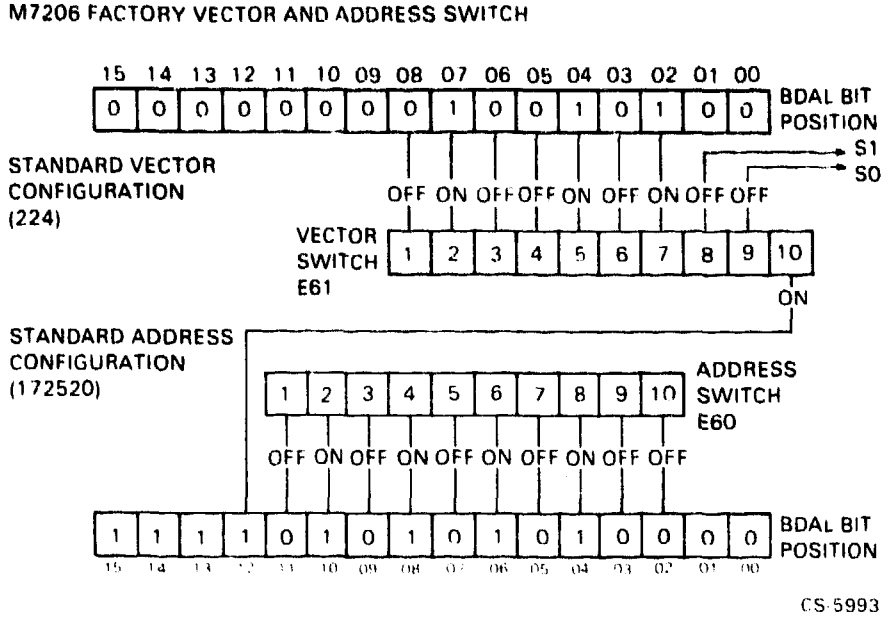


Figure 2-21 M7206 Vector and Address Switches

Table 2-3 M7206 Vector and Address Switch Description

S0	S1	Description
0	0	Auto speed control and no ID burst detect
0	1	No auto speed control and no PE ID burst detect
1	0	Auto speed control and no ID burst detect
1	1	Software driven contol auto speed and detection of ID burst

2.6 BUS INTERFACE/CONTROLLER MODULE INSTALLATION (M7206)

The M7206 bus interface/controller module plugs into a quad slot in the Q-bus backplane. It connects the Q-bus on the A and B sets of edge connectors (module fingers). It is shipped with the switches set for an interrupt vector of 224, and an address of 172520. If your system already uses this address, the M7206 module must be switched to other addresses. Refer to Figures 2-20 and 2-21 for information on switching the switchpacks. Refer to the *Microcomputers and Memories Handbook* or your system configurator for guidance in selecting new addresses.

For guidance in selecting the best backplane slot in which to install the M7206 module, refer to your system documentation or to the *Microcomputers and Memories Handbook*.

2.6.1 Testing the System

1. Test the existing system to make sure it is running properly. Run MicroVAX Diagnostic Monitor (MDM) for MicroVAX systems (Chapter 4), or run the XXDP+ Diagnostic for Micro/PDP-11 systems (Chapter 5).

CAUTION

Always remove the tape cartridge from the tape drive before turning the I/O power switch to OFF (0).

2. After the successful completion of the test, turn the I/O power switch off, and unplug the ac power cord from the wall outlet.

WARNING

Never work inside a system enclosure without first shutting off the system power, and unplugging the cord from the wall outlet.

2.6.2 Removing the Front Cover

The BA200 series pedestal system has a front cover with a three-position lock that controls access to the system controls. The controls are behind the window at the upper right of the cover. Remove the front cover as follows:

1. Insert the key into the lock at the front cover. Turn the key fully clockwise to the bottom position (Figure 2-22).
2. Slide the window down.
3. Release the cover by pulling out on the release latch (Figure 2-22).
4. Pull up on the front cover and remove it from the system (Figure 2-23).

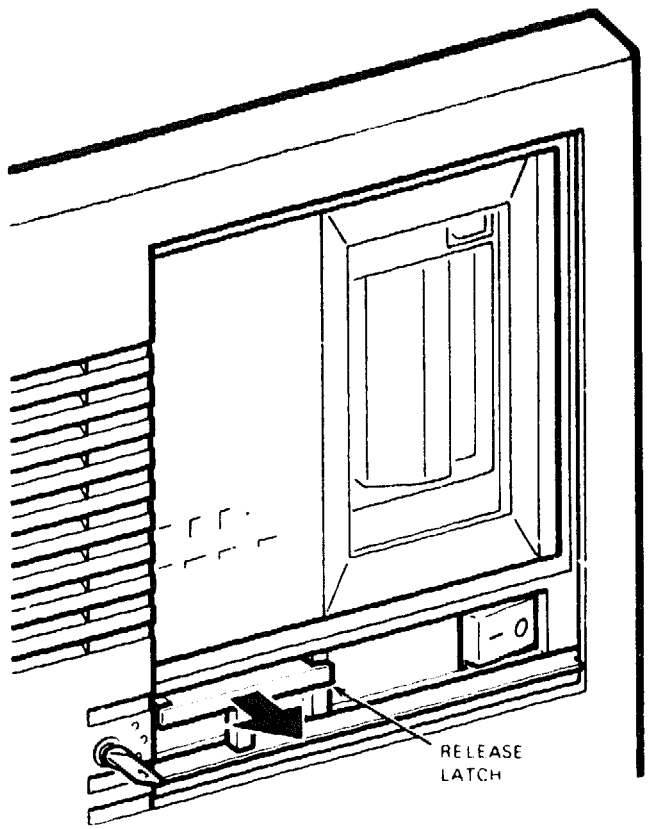


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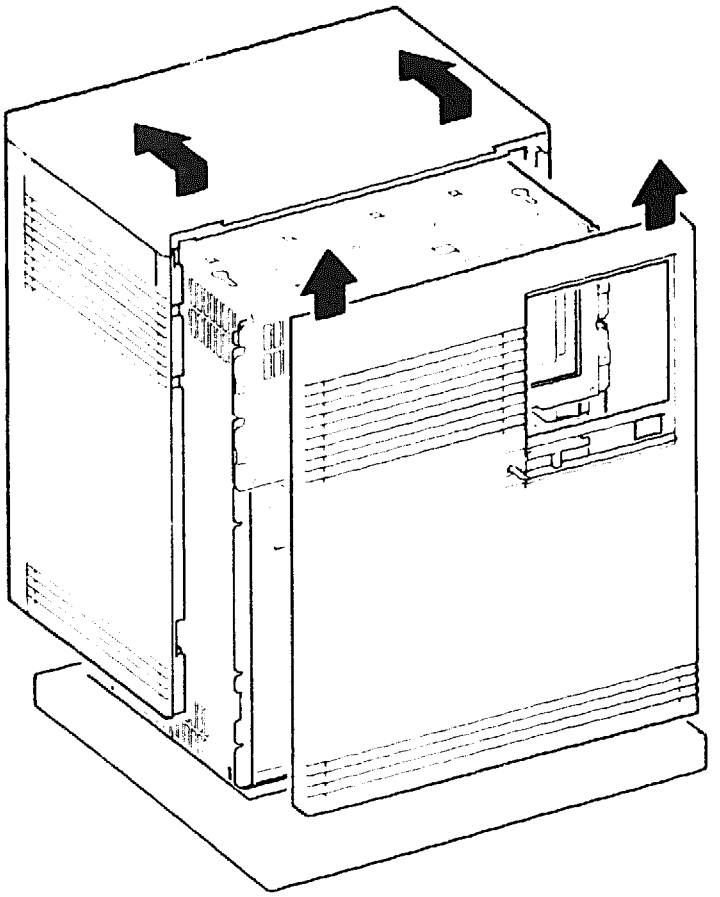
Figure 2-22 Unlocking the Front Cover



CS-6012

Figure 2-23 Removing the Front Cover

2.6.3 Removing Modules

You may now need to remove and reinstall existing modules before you install the M7206 module. If you do not need to relocate existing modules, proceed to Section 2.6.3.1.

CAUTION

Ensure that you are wearing a grounded anti-static wrist strap before removing or installing modules.

2.6.3.1 Modules with Handles - Use the following procedure to remove modules with handles.

1. Note the orientation of external cables connected to the module. Disconnect and label the cables.
2. Release the two 1/4-turn captive screws that hold the module's handle to the card cage (Figure 2-24).
3. Unlock the release levers by simultaneously pulling up on the top lever and pushing down on the bottom lever (Figure 2-25).
4. Pull out on the module's handle and remove it from the card cage.
5. If necessary, reinstall the module in its new location.
6. Reverse this procedure to install modules with handles. Do not fasten the 1/4-turn screws until you install the M7206 module.

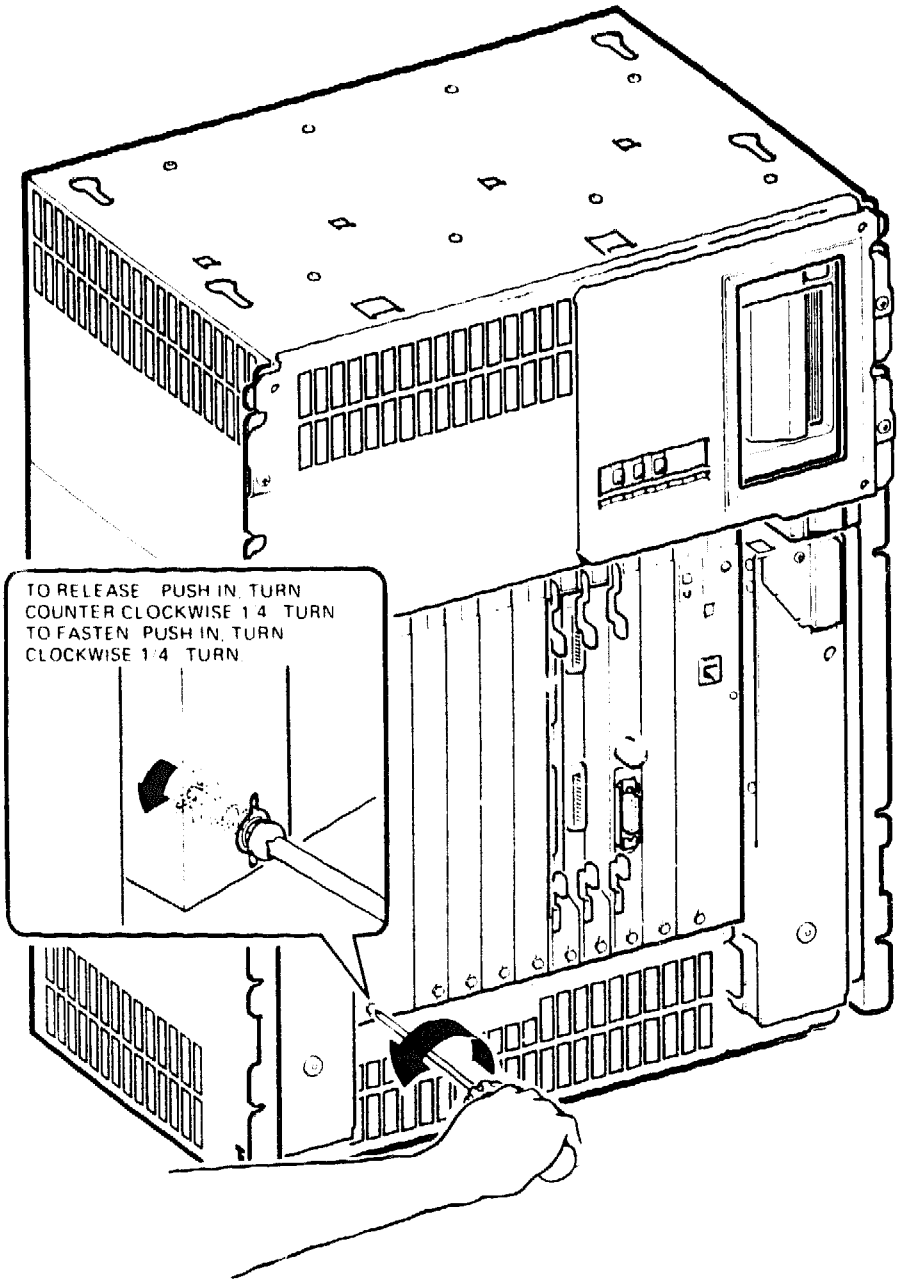
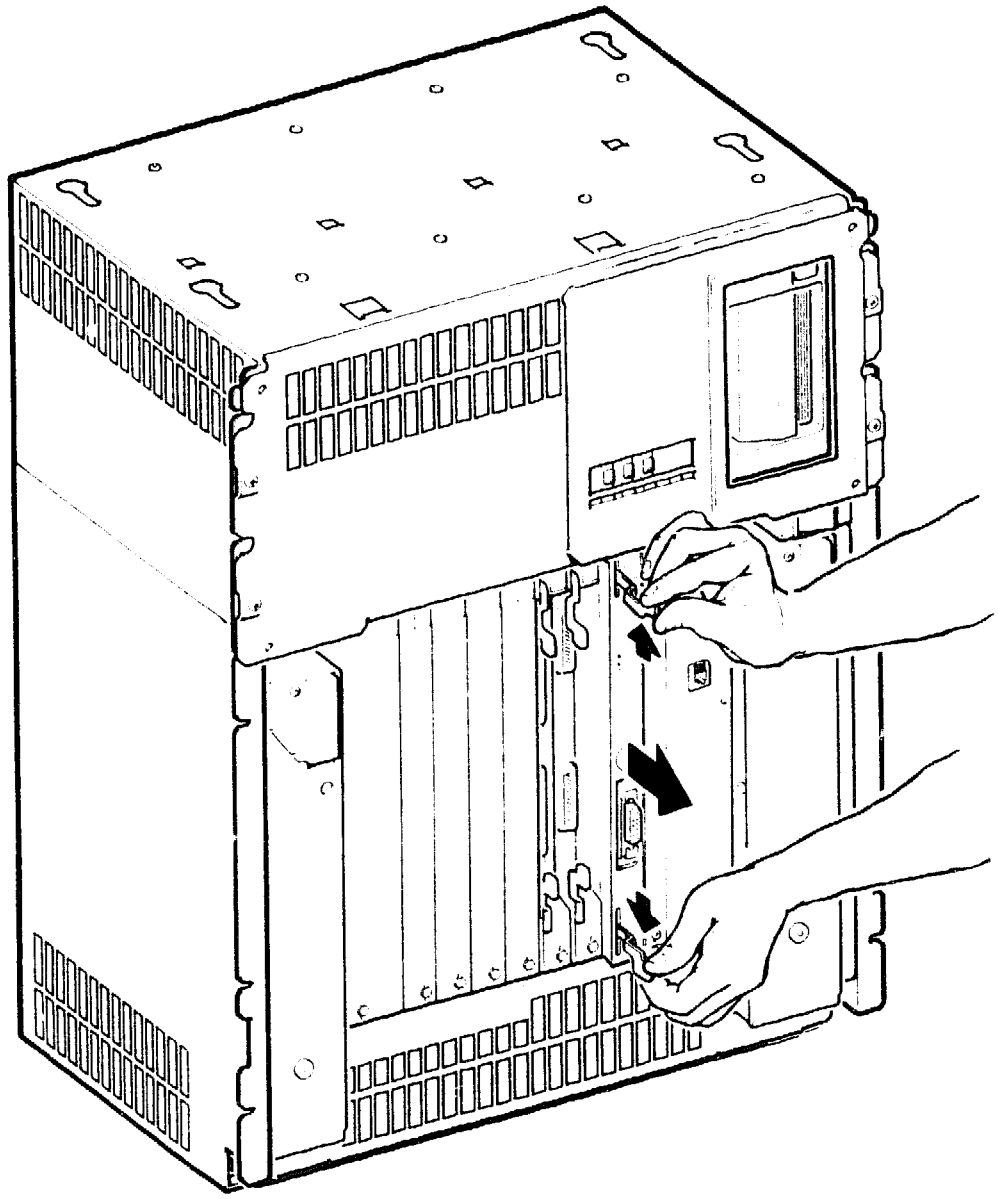


Figure 2-24 Releasing the Captive Screws



CS-5998

Figure 2-25 Unlocking the Release Levers

2.6.3.2 Modules with Blank Covers - Use the following procedure to remove modules with blank covers.

CAUTION

Ensure that any modules with plastic handles do not become caught under the edge of the blank cover. This action will prevent the proper installation of the blank cover.

1. Release the two 1/4-turn captive screws that hold the blank cover to the card cage (Figure 2-26).
2. Pull the blank cover away from the card cage.
3. Note the orientation of any internal cables connected to the module. Some connectors are not keyed. Carefully disconnect and label the internal cables.
4. Pull out on the module's plastic handle and remove it from the card cage.
5. If necessary, reinstall the module in its new location.
6. Reverse this procedure to install modules with blank covers. Do not fasten the 1/4-turn screws until you install the M7206 module.

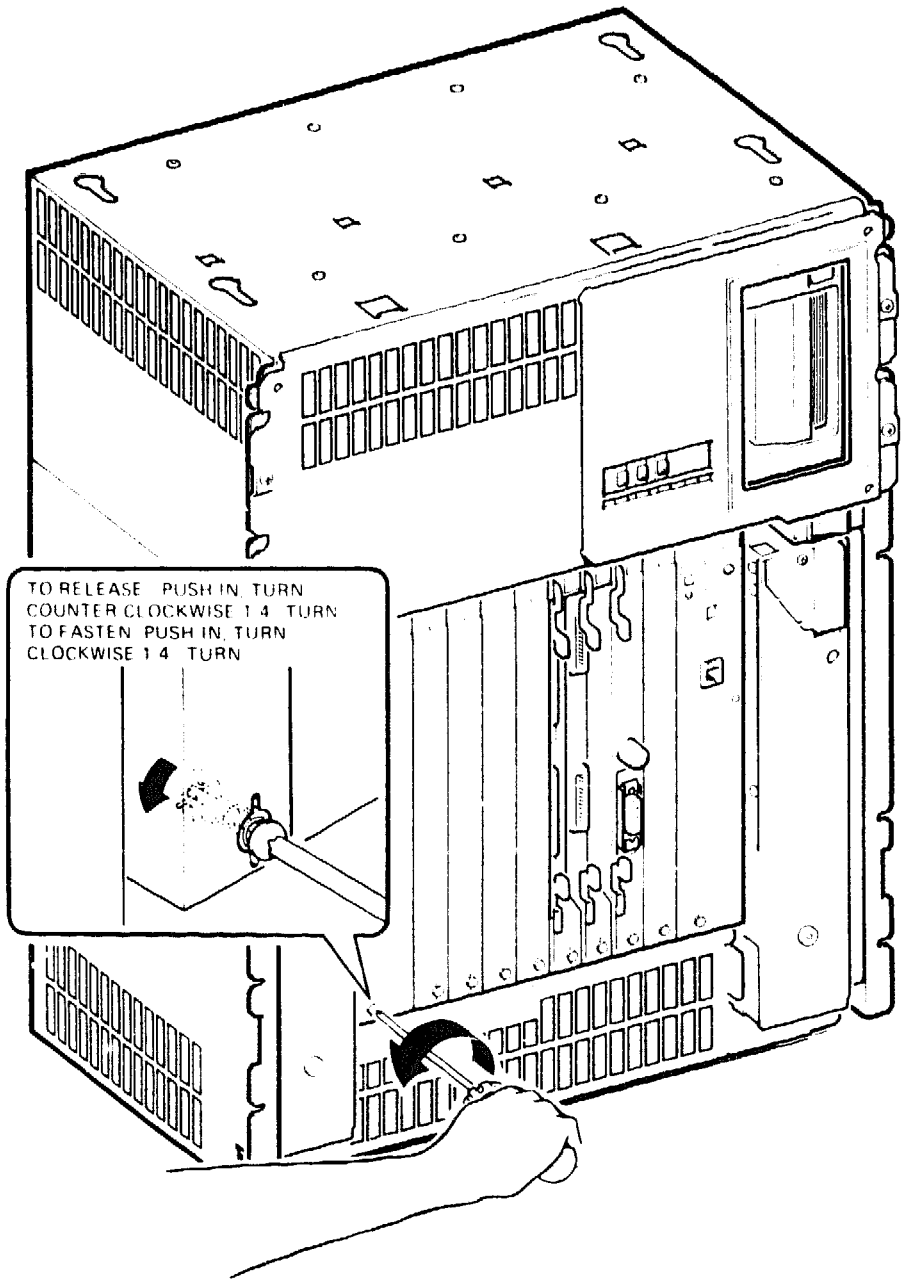


Figure 2-26 Removing the Blank Cover

2.6.4 Verifying the Ground Connections

When you install a module with a blank bulkhead cover next to a module with a flush handle or recessed handle, you must install a gap filler assembly between the modules to meet FCC regulations. Without the gap filler assembly, circuitry on the module is exposed.

Two gap filler assemblies (P/N 70-24505-01) are provided as part of the filler panel kit. Each gap filler assembly includes one gap filler and two screws. You may not need to install one, or both, of these assemblies.

NOTE

There should not be any open spaces between modules.

Before you install the M7206 module, verify the ground connections as follows:

1. Check to see if any recessed-handle module in the backplane has a module with a blank bulkhead cover or with a flush-handle in the slot immediately before or after it. If so, verify that a gap filler assembly is installed on the side of the blank bulkhead cover or the flush-handle that is next to the recessed-handle module. To accomplish this:
   - Place the blank bulkhead cover with the gap filler assembly on the card cage.
   - Insert the flush-handle module with the gap filler assembly attached into the card slot.
   - Do not fasten the 1/4-turn captive screws until you have installed the M7206 module.
2. Install the gap filler assembly (Figure 2-27), if needed, as follows:
   - Using the two screws and a gap filler assembly supplied with the filler panel kit (P/N 70-24505-01), attach the gap filler assembly to the top and bottom of the side of the blank bulkhead cover or the flush-handle that fits next to the recessed-handle module.
   - Make sure the gap filler assembly fits into the tab indentations on the blank bulkhead cover or the flush-handle.
3. Do not fasten the 1/4-turn screws until you install the M7206 module.

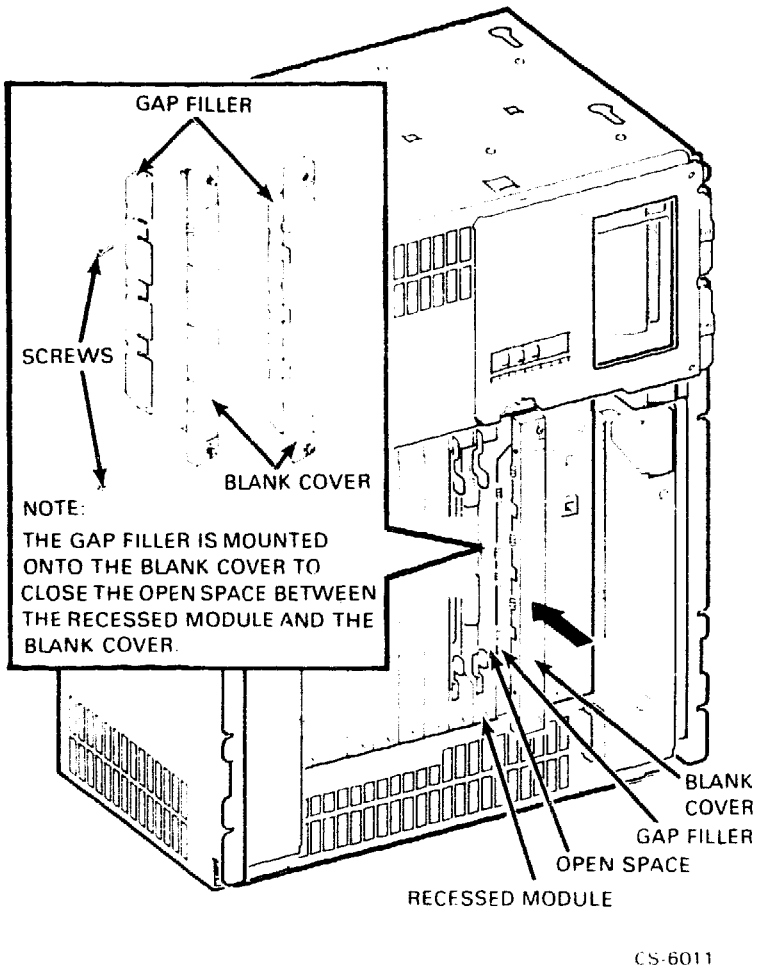


Figure 2-27 Attaching the Gap Filler Assembly

2.6.5 Installing the M7206 Module

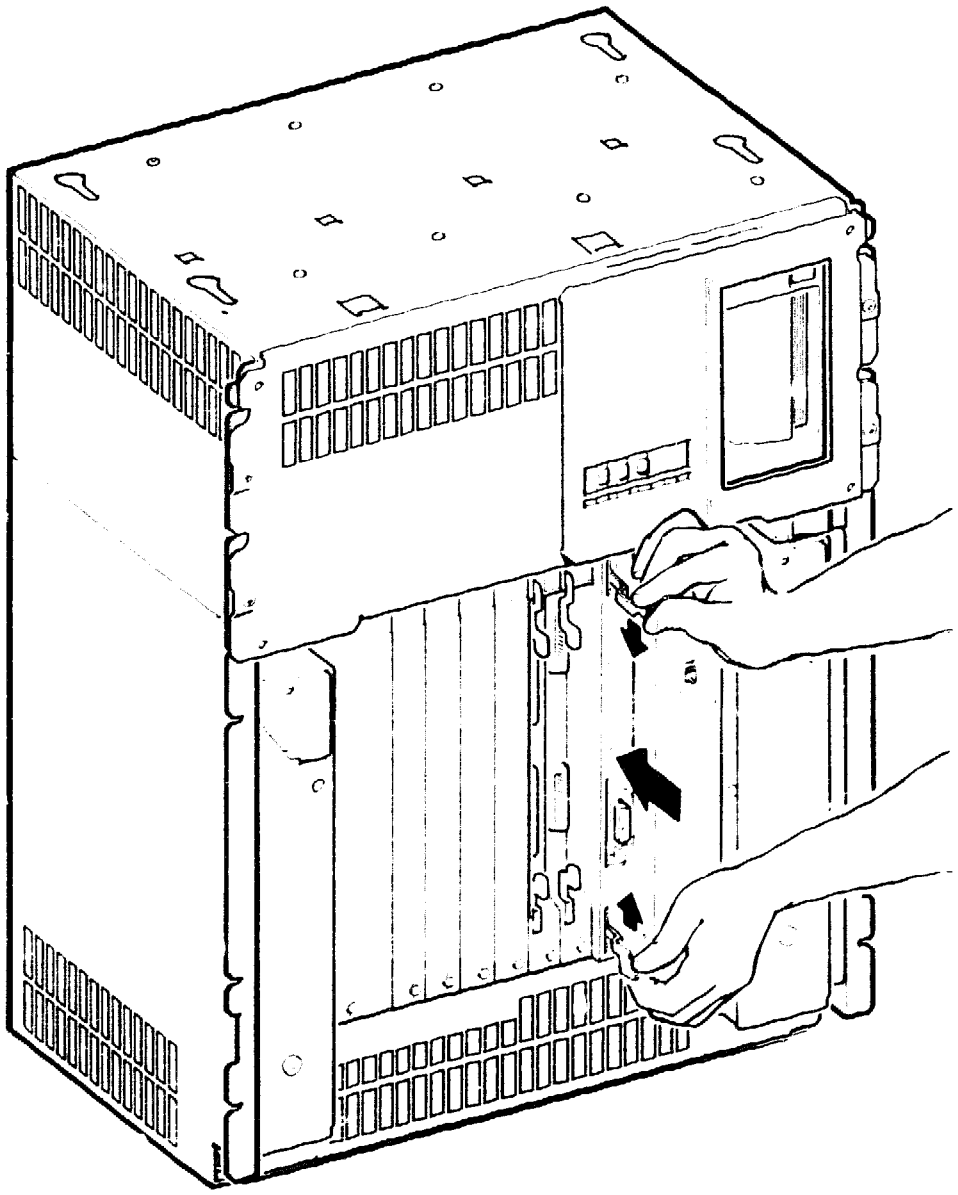
Use the following procedure to install modules with blank covers.

1. Select the card slot to insert the M7206 module.

CAUTION

Be careful not to snag the module's components on the card guides or adjacent modules.

2. Remove the blank cover or module at the chosen position.
3. Insert the M7206 module into the appropriate card slot (Figure 2-28).
4. Holding both the top and bottom release levers, lock the module in place by simultaneously pushing the top lever down and pulling the bottom lever up.
5. Make sure that bus grant continuity is maintained from the CPU to the last module in the backplane. Insert bus grant cards where needed.
6. Fasten the two 1/4-turn screws on the M7206 module, and also on the other modules and bulkhead covers in the system.



CS-6000

Figure 2-28 Inserting the Module

2.7 INTERCONNECTING CABLE INSTALLATION

Installation of the interconnecting cables includes the following procedures:

- Labeling the M7206 cables.
- Routing and connecting the M7206 cables.

2.7.1 Labeling the M7206 Module Cables

Use the following procedure to label the M7206 module cables.

1. Peel off the J1 J1 J1 label and wrap it around the round portion of one of the cables adjacent to the molded right angle connector.
2. Find the opposite end of the same cable and note the card edge connector marked with a white dot.
3. Peel off the label that says "J1 This Side Up" and place it directly on top of the white dot on the card edge connector.
4. Peel off the J2 J2 J2 label and wrap it around the round portion of the other cable adjacent to the molded right angle connector.
5. Find the opposite end of the same cable and note the card edge connector marked with a white dot.
6. Peel off the label that says "J2 This Side Up" and place it directly on top of the white dot on the card edge connector.

2.7.2 Routing and Connecting the M7206 Module Cables

Use the following procedure to complete the installation of the M7206 module cables.

1. Route the cable now labeled J2 up from the bottom of the BA200 series enclosure, and plug it into the lower (J2) connector on the M7206 module (Figure 2-29).
2. Using your fingers, snap the bail latches, one on top, one on the bottom, onto the right angle cable plug.
3. Route the cable now labeled J1 up from the bottom of the BA200 series enclosure, and plug it into the upper (J1) connector on the M7206 module.
4. Using your fingers, snap the bail latches, one on top, one on the bottom, onto the right angle cable plug.
5. Dress the cables to the rear of the TS05 tape transport.
6. Plug the cable labeled "J1 This Side Up" with the appropriate side up, onto the gold edge connector in the rear of the TS05 labeled P1.
7. Plug the cable labeled "J2 This Side Up" with the appropriate side up, onto the gold edge connector in the rear of the TS05 labeled P2. Using the #10 ground screw provided, connect the ground bonding wire from each cable to the ground screw threaded insert in the rear of the TS05 as shown in Figure 2-30.

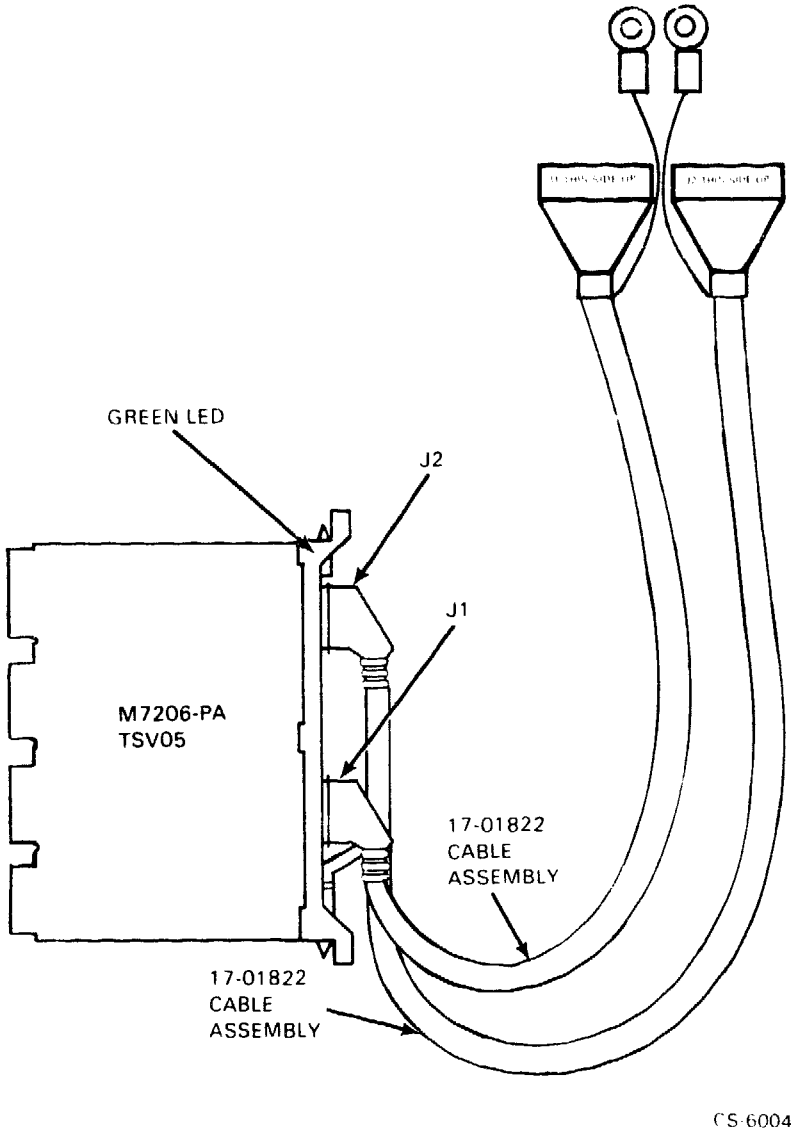


Figure 2-29 Ground Connections

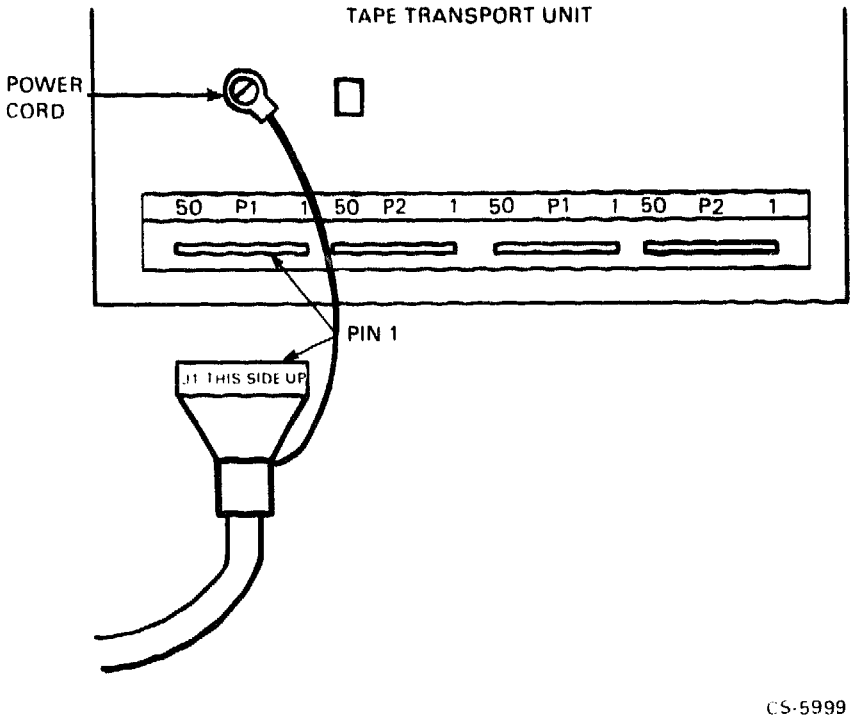
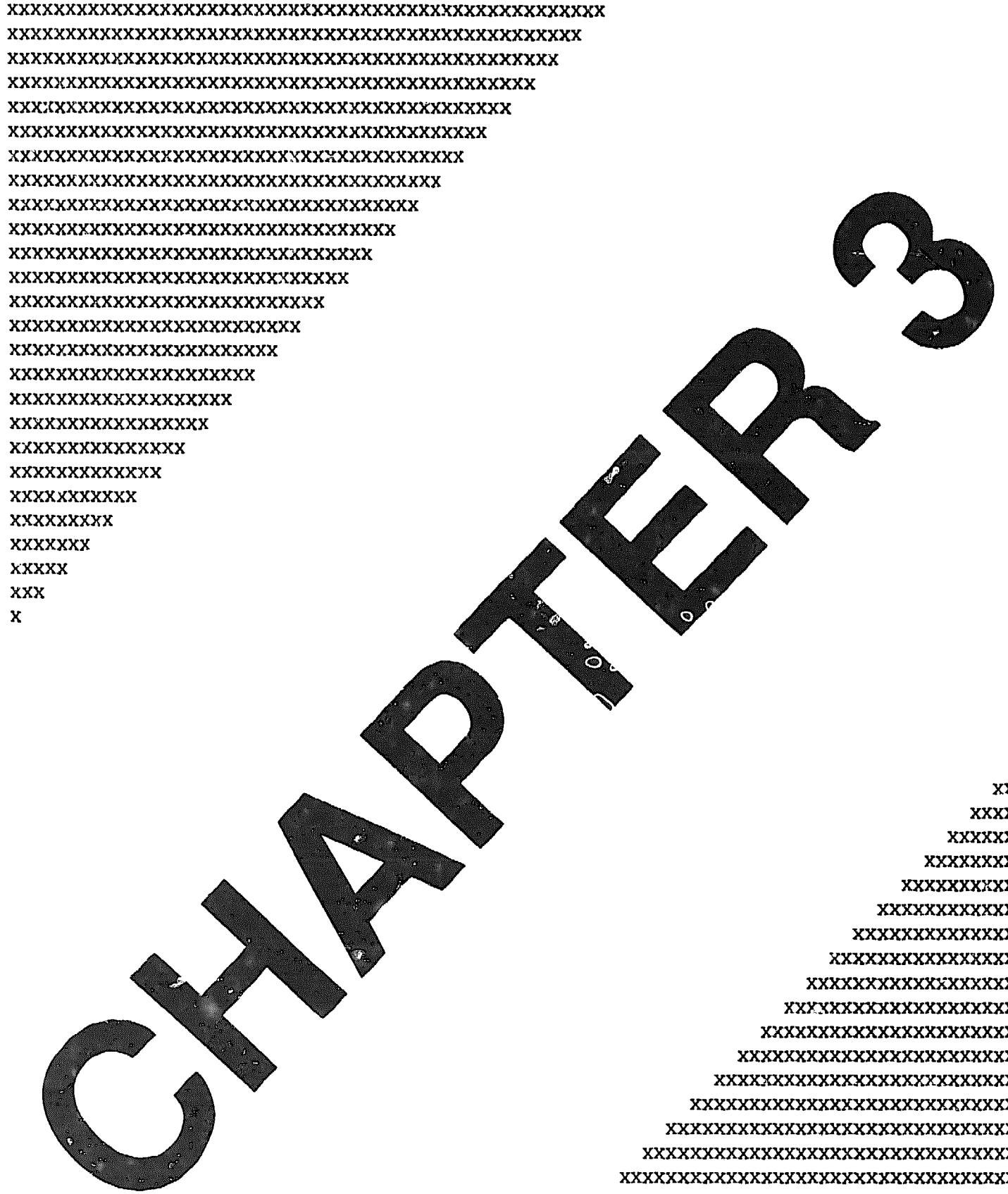


Figure 2-30 Cabling the Tape Transport

2.8 TSV05 SUBSYSTEM CHECKOUT

The TSV05 subsystem checkout procedure depends on the Micro system installed. Proceed to the applicable chapter to check out your TSV05 subsystem.

- PDP-11 processor (Chapter 4)
- MicroVAX II processor (Chapter 5)


CHAPTER 3

CHAPTER 3
TSV05-A/B INSTALLATION

NOTE

This chapter describes the 120V, 50/60 Hz rack (-A) and cabinet models (-B), but this description applies to all the other models.

Model	Applicability
-A	-AA, -AB, -AC, and AD
-B	-BA, -BB, -BC, and -BD

This chapter explains how to install a TSV05-A or TSV05-B tape transport subsystem in a Micro system enclosure other than the BA200-series enclosure. Chapter 2 explains how to install a TSV05 tape transport subsystem in a BA200-series enclosure. A section is devoted to each of the following:

1. Site preparation.
2. Unpacking and inspection.
3. TS05 tape transport installation.
4. Tape transport checkout.
5. Bus interface/controller installation.
6. Interconnecting cables installation.
7. TSV05 subsystem checkout.

NOTE

Before you unpack the cartons, inspect for signs of shipping damage. If the shipment has been damaged, call the dealer from whom the equipment was purchased. If the equipment is covered under "DIGITAL Transit Insurance", the DIGITAL representative will estimate the damage and put in a claim. If the equipment is not insured by "DIGITAL Transit Insurance", contact the carrier who handled the equipment and your own insurance company. DIGITAL Field Service is available on a per-call basis to make estimates of damage for any resulting insurance claims.

3.1 SITE PREPARATION

3.1.1 Space

All TSV05-A and TSV05-B subsystems models require room for access to the cabinet, the correct power receptacle, and an adequate flow of cooling air.

In addition, the TSV05-B subsystem cabinet models require a 597 mm (23.5 in) wide by 838 mm (33.0 in) deep by 1111 mm (43.75 in) high area of floor space that is capable of supporting a minimum of 121 kg (265 lbs). The cabinet is capable of supporting up to 205 kg (450 lbs).

3.1.2 Accessibility

A TSV05-B subsystem cabinet model requires sufficient space behind it for opening the rear door. If any expansion is anticipated, room in front of the cabinet will be required to allow future equipment to be pulled out of the cabinet for maintenance. Refer to Figure 3-1 for required dimensions.

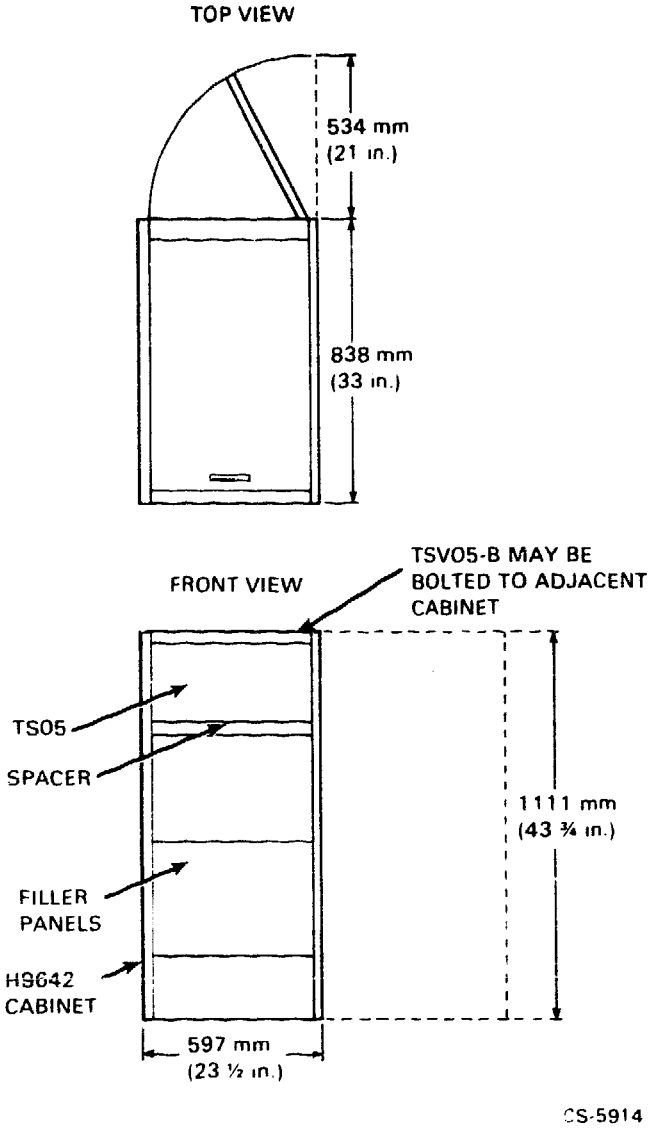


Figure 3-1 Cabinet Access Requirements

3.1.3 Power Receptacles

Ensure that the correct power receptacle is available (Figure 3-2). It should be capable of handling at least 270 watts required by the tape transport.

3.1.4 Cooling

The TSV05-A and TSV05-B subsystems require 1100 Btu per hour of cooling to be provided by the movement of room air through the cabinet.

3.1.5 Air Purity

The tape transport is equipped with internal filters to prevent dust from accumulating on the tape and tape heads. Nevertheless, it is good practice to avoid placing the cabinet in the path of a dust-laden current of air (such as beside a door).

Power Cord Color Code		**Pin Connection**	
Color	Function	L5-30P	6-15P
Brown	Hot	Brass	Brass 1
Blue	Neutral	Silver	Brass 2
Green/yellow	Ground	Ground	Ground

MODEL	PLUG	RECEPTACLE	CIRCUIT RATING
TSV05-BA TSV05-BC	SILVER — W BRASS — G NEMA #L5-30P DEC #12-11193	W G L5-30R 12-11194	120 V 24 A
TSV05-AB TSV05-AD TSV05-BB TSV05-BD	BRASS 2 — G BRASS 1 NEMA #6-15P DEC # 90-08853	G 6-15R 12-11204	220/240 V 12 A

CS-6017

Figure 3-2 Power Line Connections

3.2 UNPACKING AND INSPECTION

The TSV05-A is shipped in one large carton and one (or more) small carton(s). The TSV05-B is shipped as one skid-mounted carton and one (or more) smaller carton(s). The carton on the skid contains the TS05 tape transport cabinet. The smaller carton(s) contains the M7196 interface/controller module, the documentation and accessories, and two individually packaged cables. These smaller items may be shipped in one carton or two, depending on shipping requirements. Check the shipping documents to ensure that the correct model has been shipped. If anything is missing, damaged, or incorrect, contact the dealer from whom the equipment was ordered.

3.2.1 Tools and Working Space

The following tools are required for unpacking the TSV05-B subsystem:

1. Scissors
2. 9/16-inch wrench
3. 11/16-inch wrench
4. 3/4 inch wrench
5. 5/32-inch hex key

Also, a space of approximately 3 meters (10 feet) square is required for moving the cabinet off the shipping skid.

3.2.2 Unpacking the Cabinet

WARNING

Once the leveling feet are raised, the cabinet is free to roll on its casters. The cabinet is top-heavy and must be handled with care.

1. Cut the nylon straps and remove the cardboard tube (Figure 3-3). Remove the plastic bag.
2. Using a 9/16-inch wrench, remove the four shipping bolts that hold the cabinet to the skid (Figure 3-4).
3. Remove the metal hold-down brackets.
4. Using an 11/16-inch wrench, loosen the leveling feet locking nuts (Figure 3-5).
5. Using a 9/16-inch wrench, screw the leveling feet up into the cabinet base all the way.

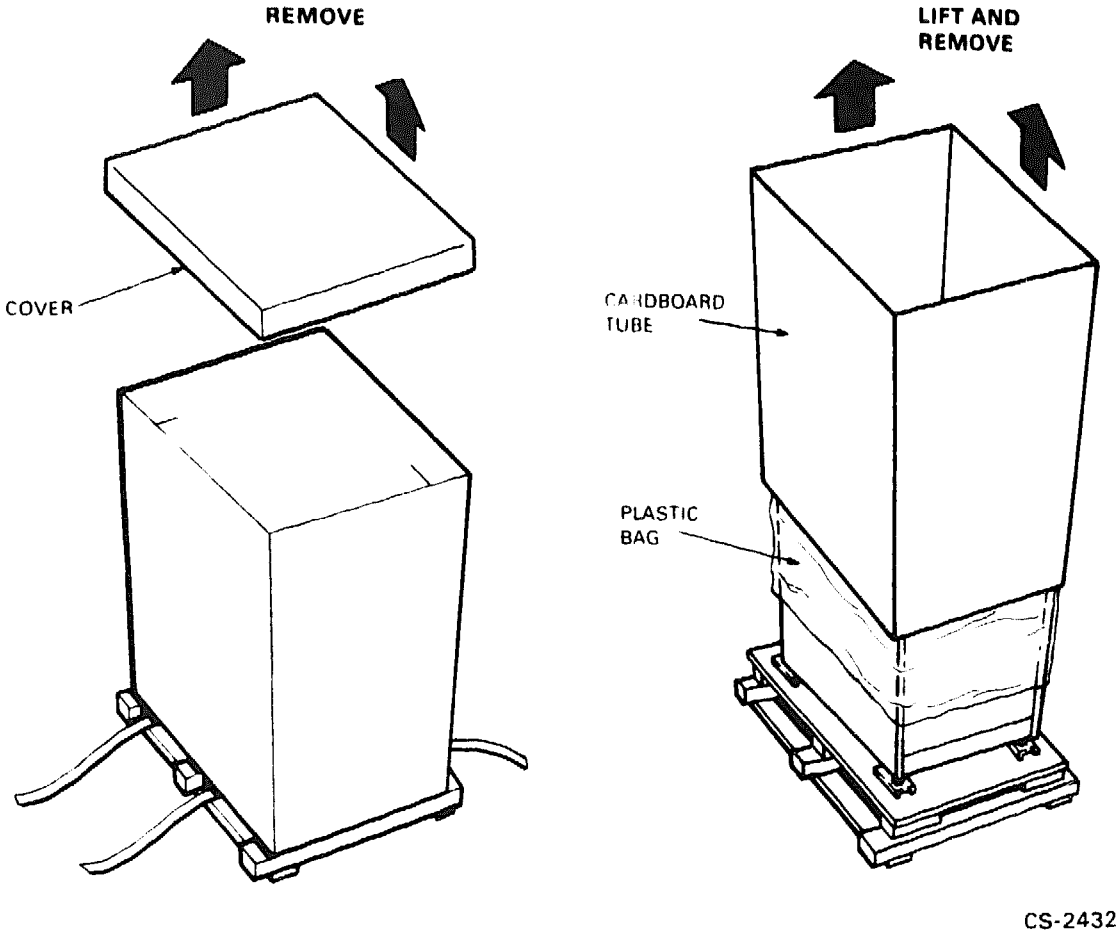


Figure 3-3 Cabinet Carton Removal

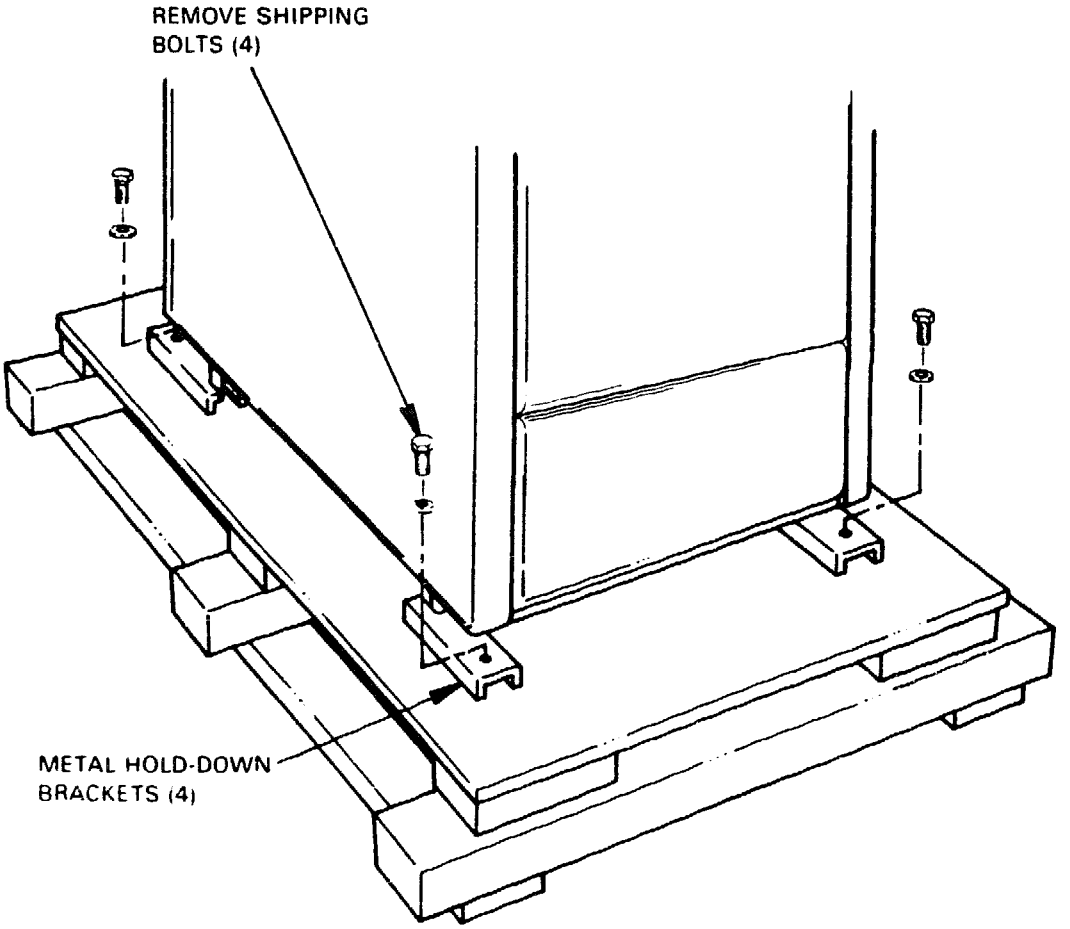
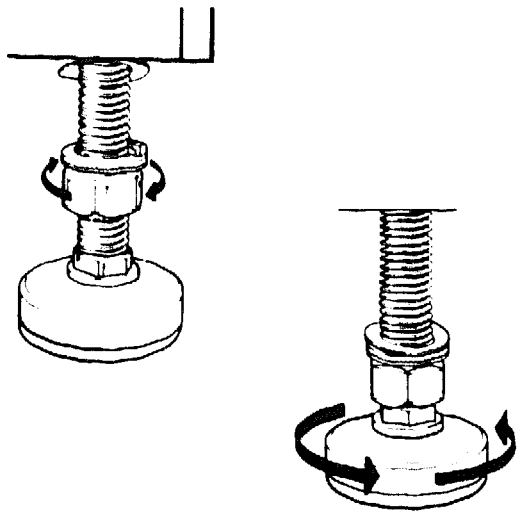


Figure 3-4 Cabinet Shipping Brackets

1. TURN NUT DOWN TO BOTTOM.

2. SCREW FOOT INTO CABINET FAR ENOUGH TO PERMIT CABINET TO BE ROLLED ON ITS CASTERS.



CS-2840

Figure 3-5 Raising Leveling Feet

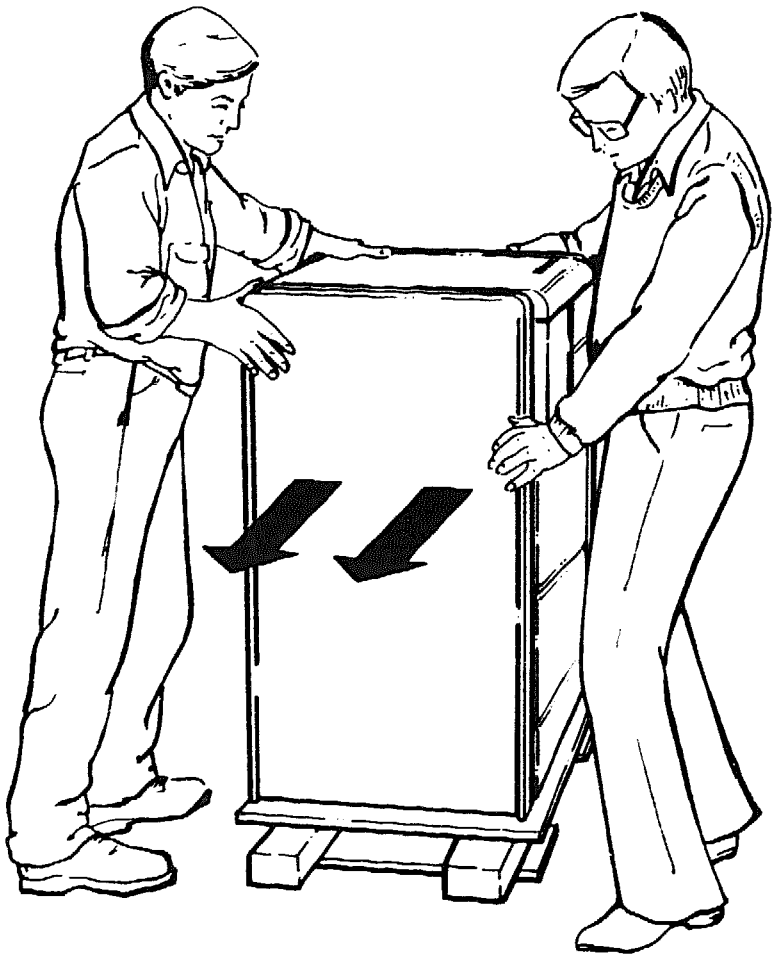
3.2.3 Deskidding the Cabinet

WARNING

Use sufficient manpower to move the cabinet off the skid.

The recommended procedure for removing the tape transport cabinet from the skid is as follows.

1. One person should stand in front of the cabinet while the other person stands behind it.
2. Grasp the cabinet by right top and by the left center (Figure 3-6).
3. Roll the cabinet off the side of the skid, taking care to prevent it from toppling over.
4. When the casters on the left side of the cabinet are on the floor, push the skid out from under the right side of the cabinet. Take care to prevent the cabinet from hitting the floor hard, or toppling.
5. Open the rear door using a 5/32-inch hex key (Figure 3-7) and verify that the envelope taped to the bottom of the cabinet contains the following:
   a. Remote cable (P/N 70-08288-8F).
   b. Intercabinet hardware (P/N 74-22224/74-22225).
   c. Four 1/4-20 x 2.75 inch bolts.
   d. Twelve 1/4-20 self-retaining nuts.



CS-7435

Figure 3-1 Deskidding the Cabinet

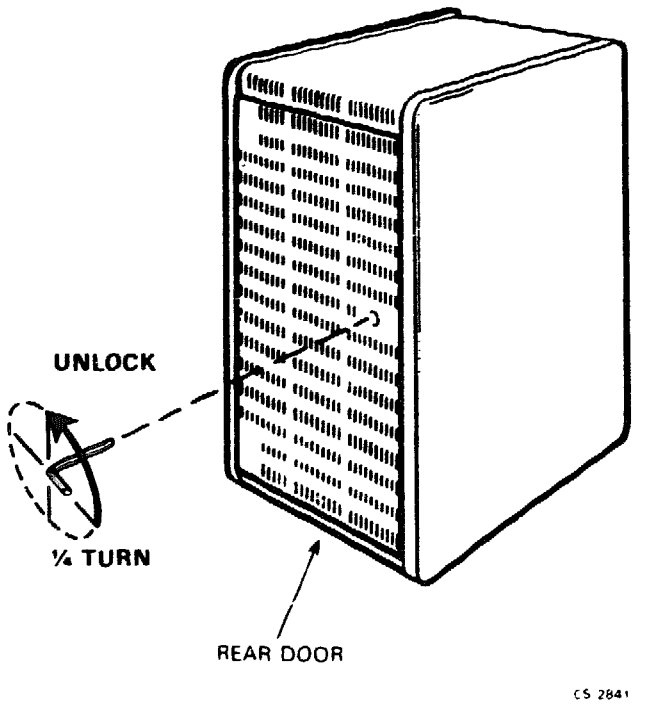


Figure 3-7 Opening Cabinet Door

3.2.4 Unpacking the TSV05 Installation Kit

CAUTION

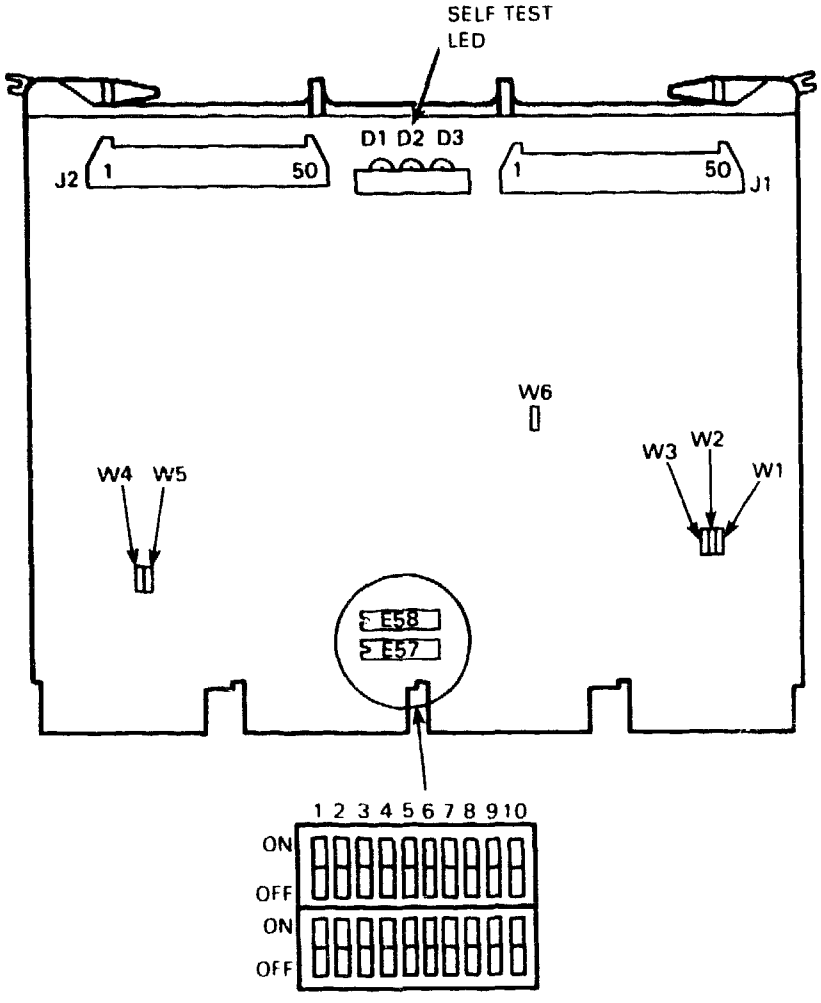
The TSV05 installation kit contains a module subject to electrostatic discharge (ESD). Put on ESD protective equipment[1] prior to unpacking the installation kit. Failure to do so can result in equipment damage.

NOTE

Do not dispose of the packing material until the module has been successfully installed and is operational.

1. Before you open the shipping container, look for external damage on the shipping container such as dents, holes, or crushed corners.
2. Put on your anti-static wrist strap.
3. Ground the wrist strap and anti-static mat. Use the anti-static mat for placement of the module.
4. Open the shipping container.
5. Remove the M7196 module from the anti-static bag.
6. Inspect the module for shipping damage. Check carefully for cracks, breaks, and loose components. Ensure that the seven PROMs are fully seated in their sockets.
7. Report any damage to the shipper and notify the DIGITAL representative.

[1] Antistatic kit (29-26246-00) is not included, but is part of the field service took kit.



NOTE:
FACTORY JUMPER CONFIGURATION IS:
W1, W2, AND W3 ARE REMOVED.
W4, W5, AND W6 ARE INSTALLED.

CS-5855

Figure 3-8 M7196 Module

3.2.5 Unpacking the Cable Kits

Open the shipping container and check its contents. Table 3-1 contains a list of the contents of the cable kits. Reference Table 3-1 and locate the configuration that was ordered. Locate the parts described for that configuration in the Parts List Breakdown.

Table 3-1 CK Kits and Parts List

Configuration	Configuration Descriptions
CK-TS05-11	TS05-A/B Cable Kit for BA123A (World Box Enclosure)
CK-TS05-12	TS05-A/B Cable Kit for OEM
CK-TS05-13	TS05-A Cable Kit for H9642 Deep Cabinet (H3490 I/O)
CK-TS05-14	TS05-A/B Cable Kit for BA23A (Pedestal Enclosure and TSV05 Cabinet)

Parts List Breakdown

Item	Part Number	Description	11	12	13	14
1	12-14614-02	Filter Con. 50 Pin	2	-	2	2
2	BC06L-1C	Cable, 1 ft 3 in	-	-	-	2
3	BC06L-03	Cable, 36 in	2	-	2	-
4	70-16855-12	Cable, 12 ft	2	-	-	2
5	70-16855-06	Cable, 6 ft	-	-	2	-
6	36-25190-01	Label, I.D.	1	-	1	1
7	37-00888-01	TKG Tab Kit CKTS05 (LND)	1	-	1	1
8	74-27575-01	Plate, Cover	-	-	-	1
9	70-16855-16	Cable, 16 in	-	2	-	-

3.2.6 Unpacking the Smaller Cartons

Open the smaller cartons and check that they contain the following:

1. M7196 bus interface/controller module.
2. Two interconnection cables (P/N 70-16855-08).
3. *TSV05 Tape Transport Installation Manual* (EK-TSV05-IN).
4. *TSV05 Tape Transport User's Guide* (EK-TSV05-UG).
5. *TSV05 Pocket Service Guide* (EK-TSV05-PS).
6. 26.7 centimeter (10.5 inch) magtape number (P/N 30-18709-08).
7. Tape cleaning kit P/N TUCO2.
8. TSV05 Field Maintenance Print Set (MP-01157).

Inspect each item. If any item is damaged, missing, or incorrect, contact the dealer from whom the system was purchased.

3.3 TAPE TRANSPORT CABINET INSTALLATION

NOTE

Installing the TSV05-A subsystems in cabinets other than the H9642 cabinet may result in higher levels of EMI radiation.

3.3.1 Installing the Cabinet

The TSV05-A tape transport model is intended to be mounted in a user-supplied or separately-purchased cabinet. Refer to Appendix B for TSV05-A rack mounting guidelines.

The TSV05-B tape transport model is shipped mounted in an H9642 cabinet that has no side panels, but has an expansion ring on the right side. This cabinet is intended to be connected to the left side of an H9642 cabinet. The TSV05-B subsystem can also be connected to computer systems that use H9612 cabinets.

The TSV05-B tape transport model is installed by removing the left side panel of the computer cabinet, installing the panel, just removed, to the left side of the tape transport cabinet, and then bolting the right side of the tape transport cabinet to the left side of the computer cabinet. Refer to Appendix C for the H9642/H9642 cabinet interconnection procedure, and to Appendix D for the H9612/H9642 cabinet interconnection procedure.

3.3.2 Removing the Shipping Foam

The tape transport is shipped with foam cushions protecting the takeup hub and blower motor. These cushions must be removed be fore the unit is powered up. This requires opening the tape transport to the operator maintenance access position to remove the foam from around the takeup hub, and opening it to the service access position to remove two other pieces of foam.

3.3.2.1 Removing the Top Foam Pieces -

1. On TSV05-B models, raise the top of the cabinet by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up (Figure 3-9).
2. Raise the top cover of the tape transport unit by reaching in through the front door and pushing upward on the front of the top cover. Prop the cover up using the nylon support that hangs from the left side of the cover (Figure 3-10).
3. Gently move the tachometer assembly away from the takeup hub (Figure 3-11). Remove the foam cushion. Carefully place the tachometer assembly back on the takeup hub.
4. Inspect and ensure that the tape path area is free of any foreign matter. With the cover still in the operator maintenance access position, remove the bottom foam pieces (Section 3.3.2.2).

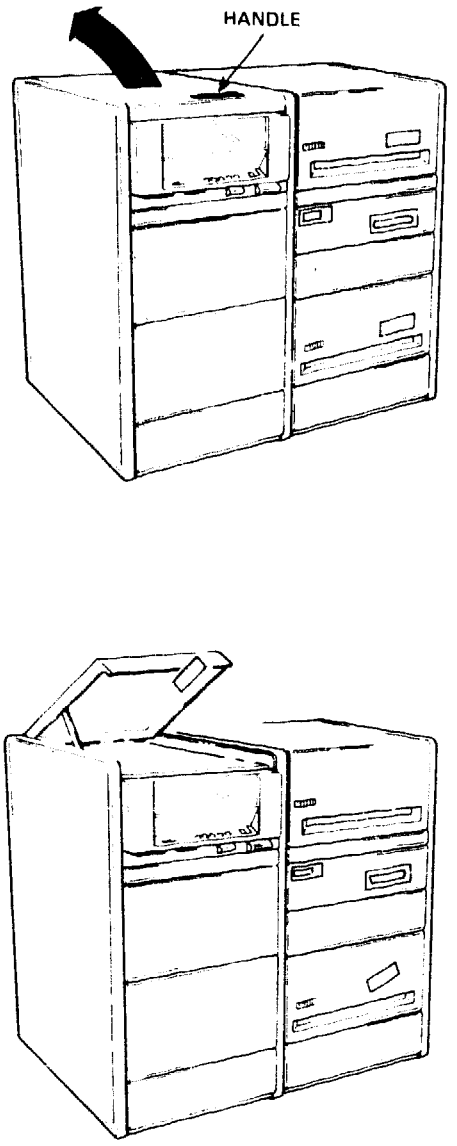


Figure 3-9 Cabinet Top Cover

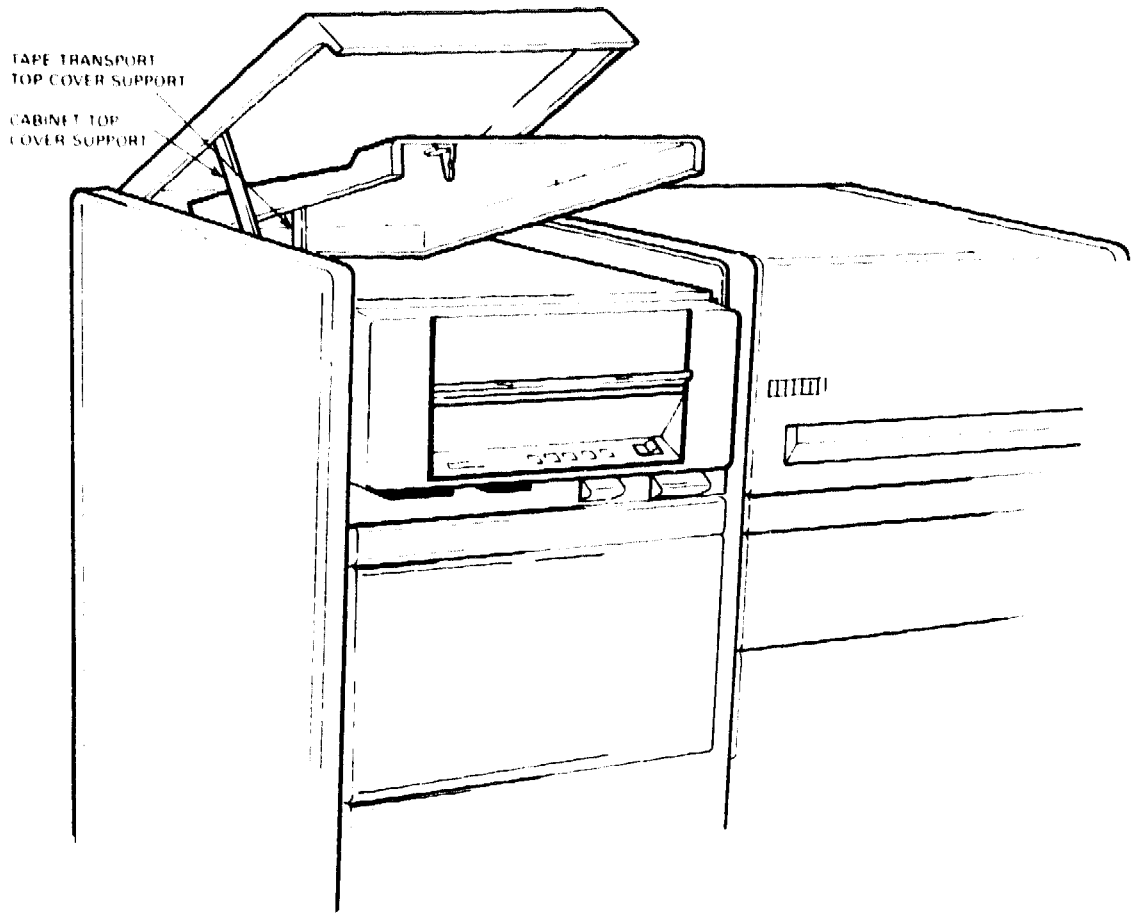


Figure 3-10 Tape Transport Top Cover

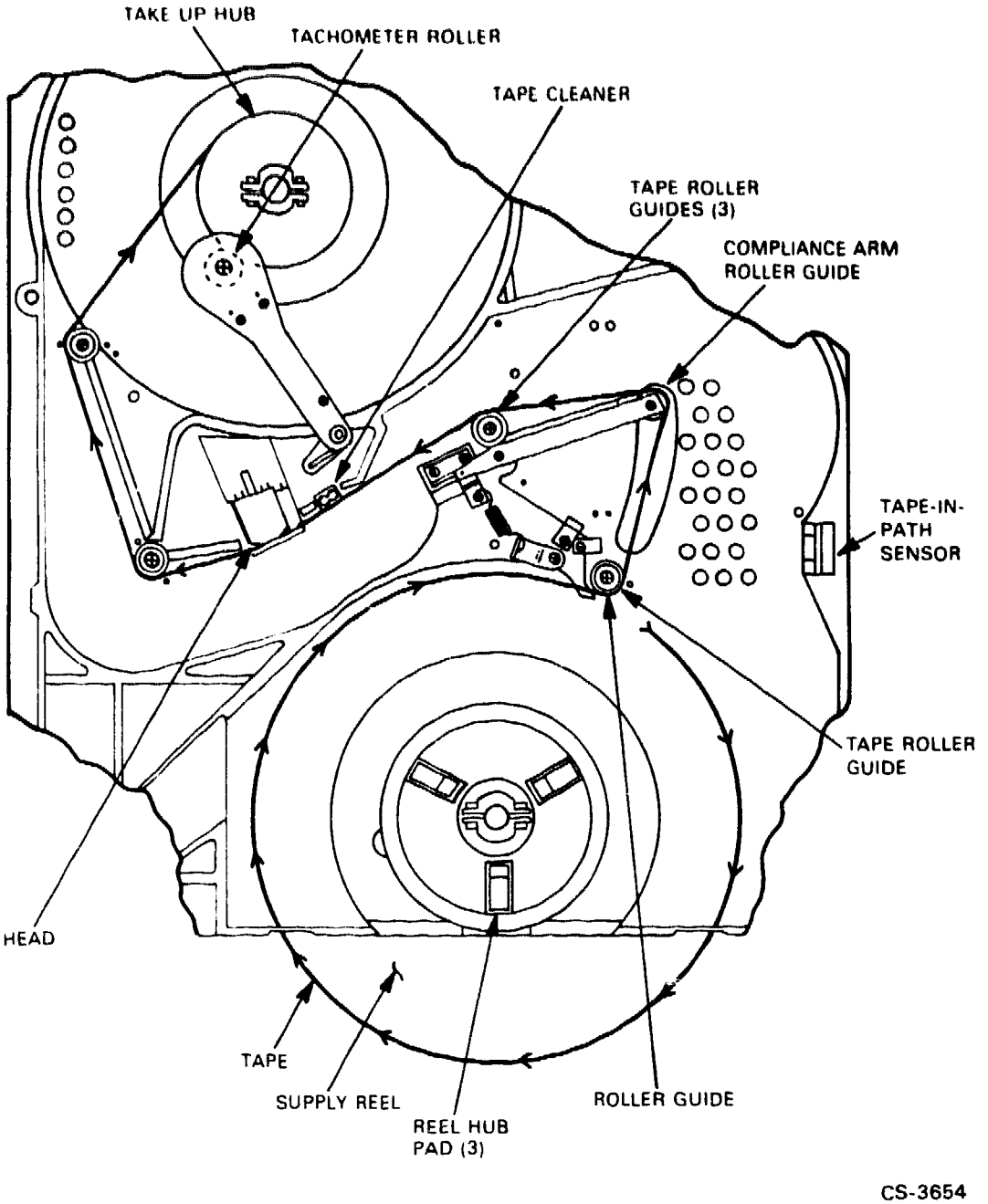


Figure 3-11 Tachometer and Takeup Hub

3.3.2.2 Removing the Bottom Foam Pieces -

NOTE

The Sandcast unit has a sandcasted top plate which is painted black, while the diecasted top plate has the appearance of a plain aluminum surface.

1. Loosen the two spring-loaded captive screws, located on each side (as viewed from the top of the TS05 tape transport unit) that secure the TS05 unit to the top rail assembly. (See Figure 3-12 if it is a Sandcast unit, or Figure 3-13 if it is a Diecast unit.)
2. Lower the top cover of the tape transport unit to prevent lacerations.

WARNING

Keep hands away from corners of the tape unit while lifting. This is important to avoid brushing the mounting rails with your hands while lifting the unit.

3. With both hands, grasp the lower front of the TS05 unit and lift the entire assembly to its maximum upright position (this engages the locking mechanism automatically).

WARNING

To eliminate the possibility of the tape unit dropping due to a failure in the locking mechanism, insert the supplied safety pin into the hole provided [2.5 cm (1.0 in)] above the locking mechanism on the top plate supporting slide.

4. Carefully lower the TS05 unit approximately 2.5 cm (1.0 in). This will activate the locking mechanism automatically. Route the safety pin behind the supporting slide and across in front, and install it from left to right.

NOTE

Perform step 5 only if it is a Sandcast unit. Proceed to step 6 if it is a Diecast unit.

5. Release the drive/formatter module by pulling down on the two NyLok[2] fasteners that secure it to the bottom of the top plate assembly. When the NyLok fasteners are released, carefully lower the drive/formatter module as far as it will go.

[2] NyLok is a trademark of NyLok Fastener Corporation

6. Remove the sheet and block of foam from the unit.

7 Place the TS05 unit back to the operating position by reversing steps 1 through 5.

NOTE

To release the cabinet top cover support arm, it is necessary to raise the top cover slightly and move the top of the arm forward.

8. Close the top cover of the tape unit and the top cover of the cabinet.

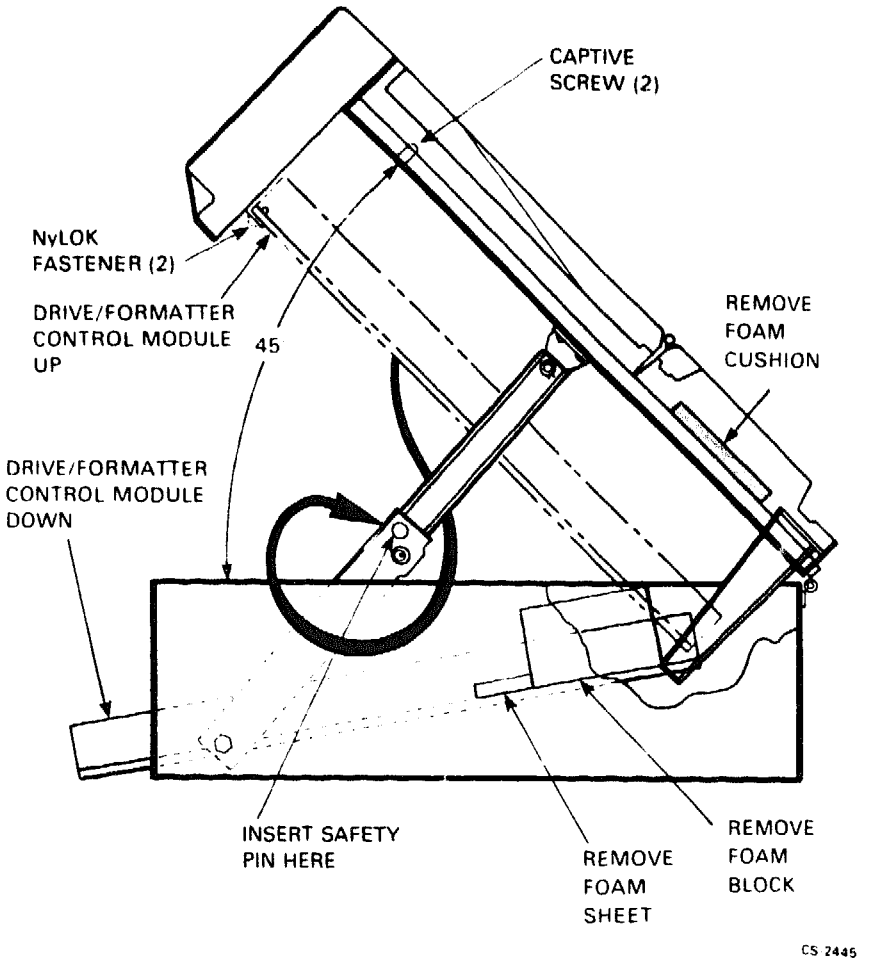


Figure 3-12 Service Access Position (Sandcast Unit)

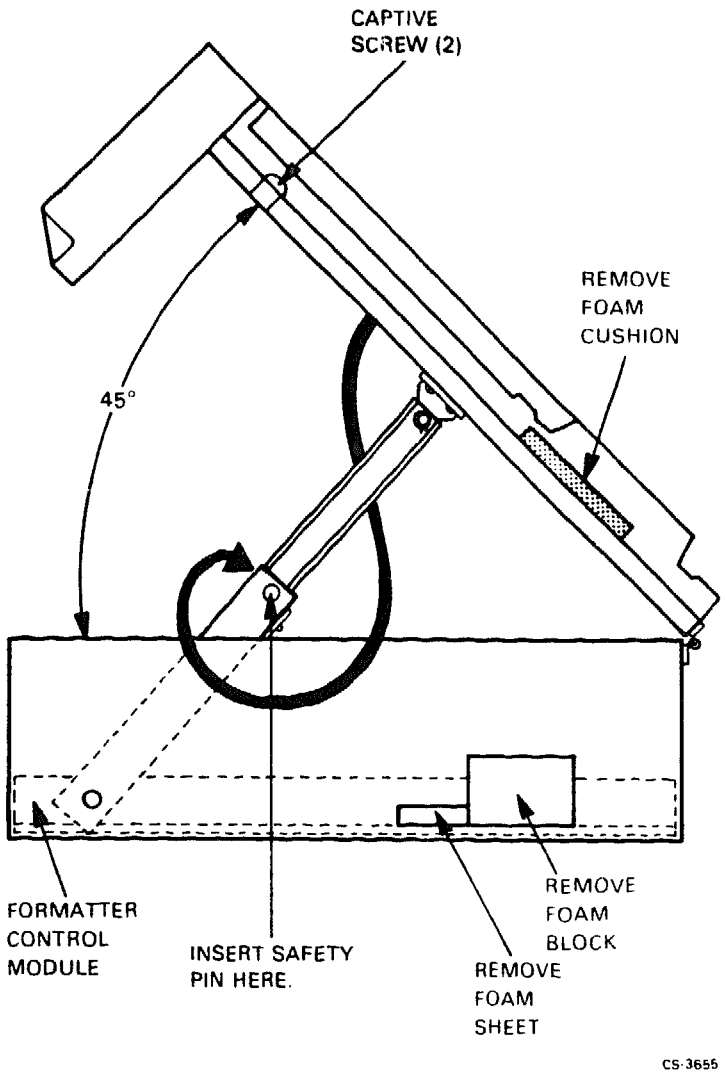


Figure 3-13 Service Access Position (Diecast Unit)

3.3.3 Connecting Line Power

TSV05-B models are equipped with cabinet power controllers. Before connecting the line power, perform the following checks.

1. Power switch on the front panel of the tape transport is in the 0 (OFF) position.
2. Power controller voltage rating is correct for your system.
3. Power controller circuit breaker switches are in the 0 (OFF) position.
4. Power controller LOCAL/REMOTE switch is in the LOCAL position. On some power controllers, the switch is labeled A O B respectively. If this is the case, place the switch in the B position.

With the switches in these positions, unwind the power cable and plug it into the receptacle.

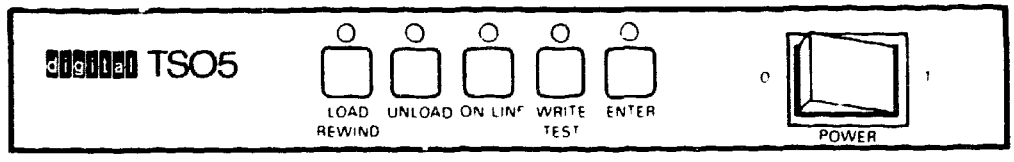
3.4 TAPE TRANSPORT CHECKOUT

The tape transport is tested by itself before being cabled to the bus interface/controller module. This standalone testing is performed with the line power controlled locally at the cabinet power controller[3]. After standalone operation has been verified, operation with the computer system is tested. At that point, the tape transport cabinet power is placed under the control of computer cabinet power controller by connecting the remote control cable. For the tests in this section, however, the remote control cable remains unconnected.

3.4.1 Power-Up Test

1. Switch the circuit breaker switches on the cabinet power to the ON position. Observe that the power controller pilot lamp lights. Close the cabinet rear door.
2. On the tape transport front panel (Figure 3-14), press the power switch to the 1 (ON) position. Observe that all indicators light for approximately two seconds.
3. Observe that after two seconds all the indicators extinguish, and then the UNLOAD indicator lights.

If these indications have occurred, the tape transport unit has successfully completed the internal verification checks that it performs automatically at power-up. If the indications were different, there is a problem. Refer to the *TSV05 Pocket Service Guide* or call your local DIGITAL Field Service representative.



CS-5994

Figure 3-14 Front Panel Controls and Indicators

[3] If your cabinet does not have a power controller, simply connect power cable to the primary outlet.

3.4.2 Tape Loading Test

This test verifies the ability of the TSV05 subsystem to automatically load a tape. It requires a tape that is blank except for the BOT and End-Of-Tape (EOT) markers. Refer to Figure 3-15 and proceed as follows.

CAUTION

Both the tape transport top cover and the front panel door are locked when a tape is loaded. Any attempt to force open either the cover or the door before the tape is unloaded will result in mechanical damage to the locking mechanism.

1. Ensure that the tape is wound completely onto the reel and that the end has been properly crimped.
2. Open the front panel door by gently pressing down on the top center area of the door.
3. Hold the tape with the file-protect ring side down, and insert it into the transport unit, centering it on the hub.
4. Close the door.
5. Press the LOAD switch. This locks the cover and the door and begins the loading sequence.
6. Observe the LOAD indicator. It blinks while the tape is being loaded. After a maximum of 135 seconds, it stops blinking and remains lit. This indicates that the tape loading sequence is complete.

If the LOAD indicator does not stop blinking, or if the other indicators begin to blink, there is a problem. Unload the tape, check for a proper crimp, and retry the test. If the tape does not load, refer to the *TSV05 Pocket Service Guide* or to the manual loading instructions in Appendix B.

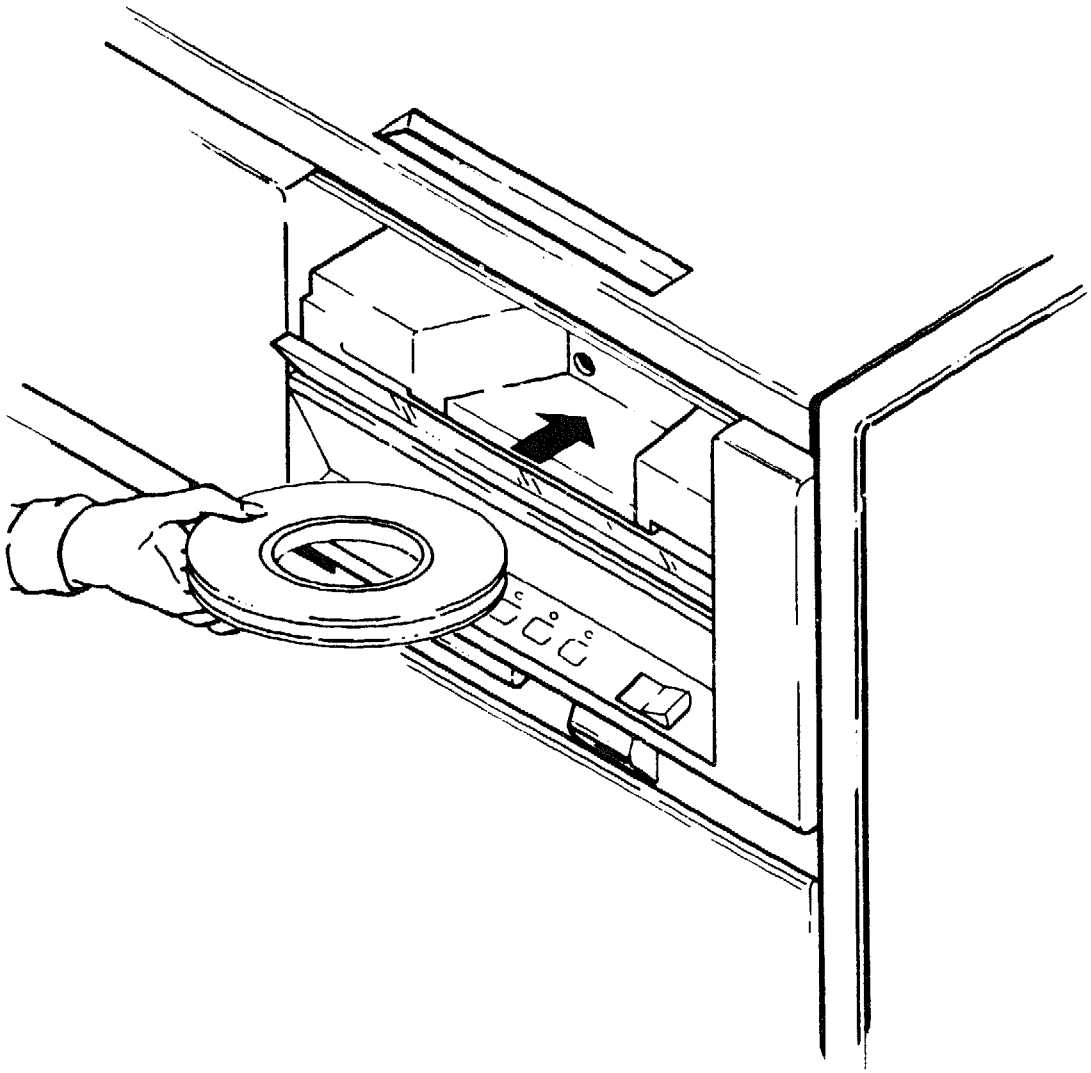


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Figure 3-15 Inserting Tape

3.4.3 Tape Movement Test

This test exercises the tape drive in both forward and reverse directions, and at both high and low speeds.

NOTE

If you make an error and enter an illegal test sequence, or if you stop during the sequence and permit more than two seconds to pass before pressing the next switch in the sequence, the system aborts the test instruction and you must start the sequence from the beginning. An erroneous or aborted test instruction results in an expanding pattern of blinking.

1. Start the test by pressing the front panel control switches in the following sequence.
   a. TEST
   b. ENTER
   c. UNLOAD
   d. UNLOAD
   e. ENTER
2. The tape should begin to move after step e.
3. Observe the indicators. If, over a period of two minutes, they change their blinking value substantially, there is a problem. If the blinking remains about the same, the test is progressing successfully.
4. After two minutes, terminate the test by pressing the TEST key. This causes the tape to rewind (which may take several minutes) and the LOAD indicator to light.

If problems are encountered, refer to the *TSV05 Pocket Service Guide*.

3.4.4 Tape Unloading Test

This test verifies the ability of the tape unit to unload the tape automatically.

1. Press the UNLOAD switch.
2. Observe the UNLOAD indicator. It blinks to indicate that the tape is being unloaded. When the unloading process is complete, the UNLOAD indicator lights continuously, and the front panel door and top cover are unlocked. This should take a maximum of 15 seconds.
3. Open the front panel door and lift the tape reel out of the tape transport.
4. Close the door.
5. Press the tape transport POWER switch to the 0 (OFF) position.
6. Switch the circuit breaker switches on the cabinet power controller to the OFF position.

3.5 INSTALLING THE CABLE KITS

Reference Table 3-2 and locate the configuration that was ordered.

Locate the parts described for that configuration in the Parts List Breakdown. Proceed to Filter Connector, Cable Connection, and Cabinet Mounting Instructions for that configuration as applicable.

Table 3-2 CK Kits and Parts List

Configuration	Configuration Descriptions
CK-TS05-11	TS05-A/B Cable Kit for BA123A (World Box Enclosure)
CK-TS05-12	TS05-A/B Cable Kit for OEM
CK-TS05-13	TS05-A Cable Kit for H9642 Deep Cabinet (H3490 I/O)
CK-TS05-14	TS05-A/B Cable Kit for BA23A (Pedestal Enclosure and TSV05 Cabinet)

PL Breakdowns

Item	Part Number	Description	Model (CK-TS05-n)			
			-11	-12	-13	-14
1	1214614-02	Filter Con. 50 Pin	2	-	2	2
2	BC06L-1C	Cable, 1 ft 3 in	-	-	-	2
3	BC06L-03	Cable, 36 in	2	-	2	-
4	70-16855-12	Cable, 12 ft	2	-	-	2
5	70-16855-06	Cable, 6 ft	-	-	2	-
6	36-25190-01	Label, I.D.	1	-	1	1
7	37-00888-01	TKG Tab Kit CKTS05 (LND)	1	-	1	1
8	74-27575-01	Plate, Cover	-	-	-	1
9	70-16855-16	Cable, 16 in	-	2	-	-

The following CK kit installation procedures are covered in this section:

- BA123A Enclosure (CK-TS05-11)
- H9642 Deep Cabinet with the H3490 rear I/O panel (CK-TS05-13)
- BA23A Pedestal Enclosure (CK-TS05-14)

3.5.1 Installing the Cable Kit for the BA123A Enclosure (CK-TS05-11)

- Remove the two filler panels from the rear I/O slots "J" and "H" (see Figure 3-16).
- Mount the filter connectors in cutouts "J" and "H".
- Install the P1 TSV05 label below the filter connector in cutout "J".
- Install the P2 TSV05 label below the filter connector in cutout "H".
- Proceed to Section 3.6.

3.5.2 Installing the TSV05-A Cable Kit for the H9642 Deep Cabinet (CK-TS05-13)

The H3490 rear I/O distribution panel is mounted on the rear of the H9642 cabinet (see Figure 3-17). When mounting to this panel:

- Remove the blank panels from the lower left side of the H3490 panel (cutouts "N" and "O").
- Mount the filter connectors in cutouts "N" and "O".
- Install the P1 TSV05 label over the filter connector in cutout "N".
- Install the P2 TSV05 label over the filter connector in cutout "O".
- Proceed to Section 3.6.

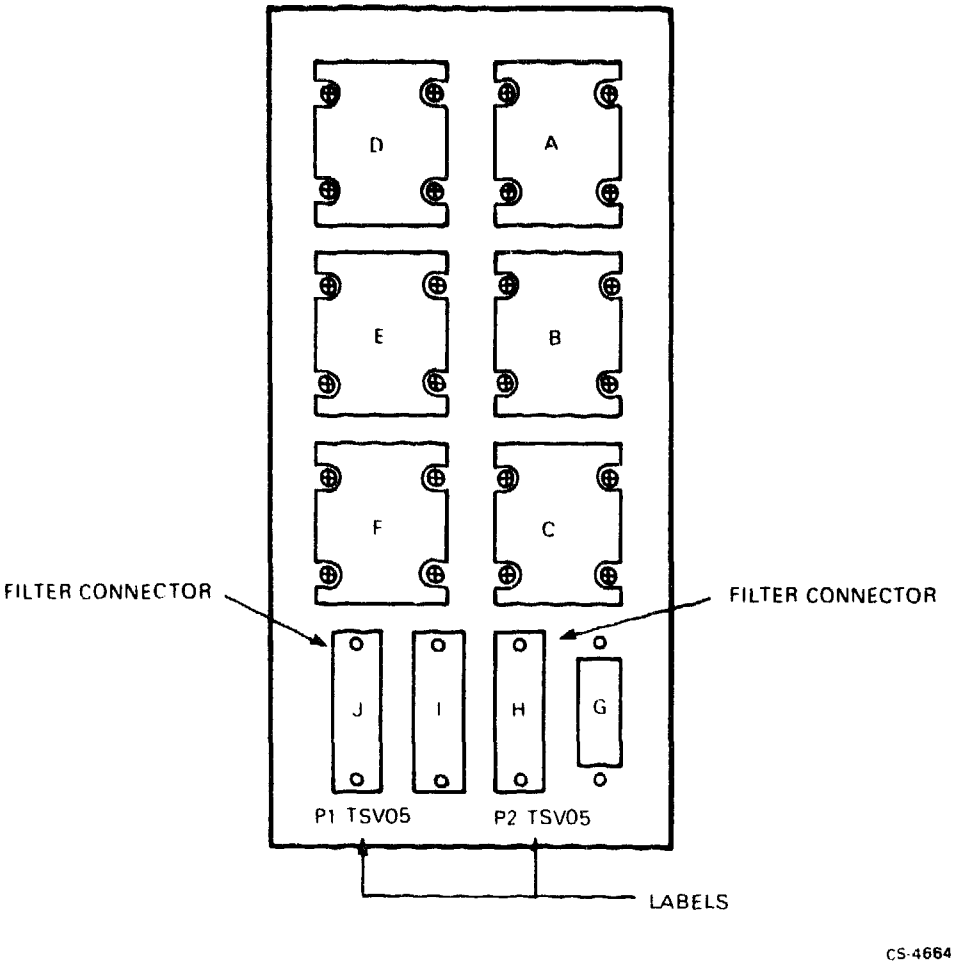


Figure 3-16 TSV05 Filter Connector Mounting BA123A

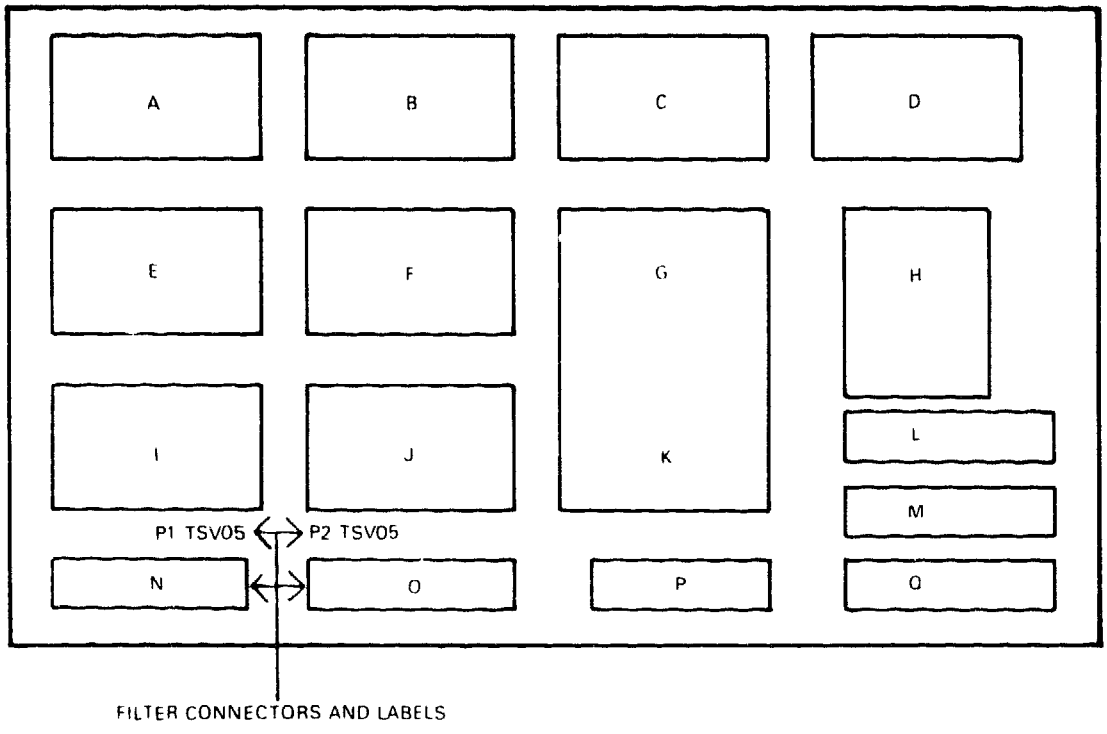


Figure 3-17 TSV05 Filter Connector Mounting, Deep Cabinet

3.5.3 Installing Cable Kit for the BA23A Enclosure (CK-TSV05-14)

Two configurations are possible, depending upon whether the CPU is in the pedestal, or the BA23A enclosure has or will have DECnet installed.

3.5.3.1 Installing the TVS05 Filter Connector (without DECnet) -

- Remove the two filter plates (PN 74-27575-01) covering the 50-pin connector expansion slots located on the bottom of the CPU I/O distribution panel located at the back of the CPU (see Figures 3-18 and 3-19).
- Install the filter connectors into the slots using the same screws.
- Label the connectors.
- Proceed to Section 3.6.

3.5.3.2 Installing the TVS05 Filter Connector (with DECnet) -

- Remove the two panels and the removable insert on the I/O distribution panel (refer to the *CPU Installation Manual* for panel insertion and removal instructions). See Figures 3-18 through 3-20.
- Locate the plastic bag containing the CPU (PN 74-27720-01). This CPU will contain three 50-pin expansion slots.
- Mount the two filter connectors in two of the slots.
- Mount the filter plate (PN 74-27575-01) in the third slot.
- Label the connectors.
- Mount the plate back into the CPU using the hardware provided in the kit.
- Proceed to Section 3.6.

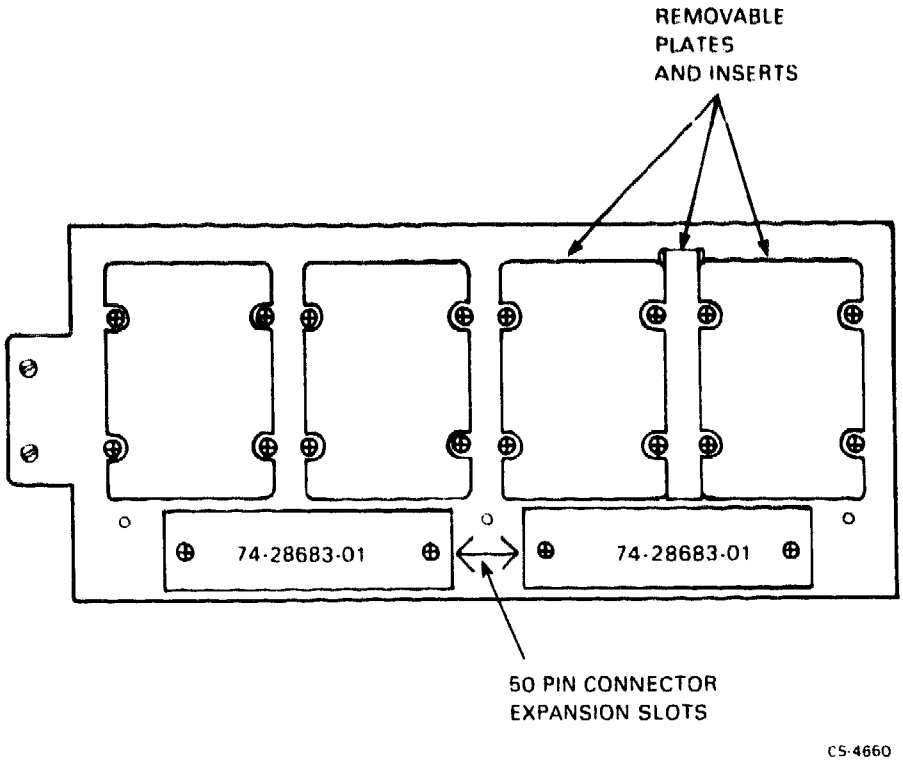


Figure 3-18 BA23A I/O Distribution Panel

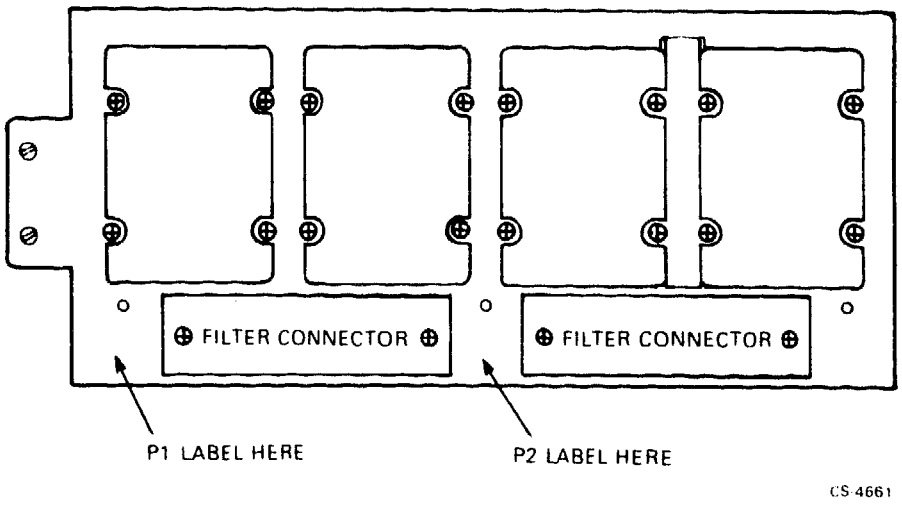


Figure 3-19 BA23A with TSV05 Filter Connector Mounting (without DECnet)

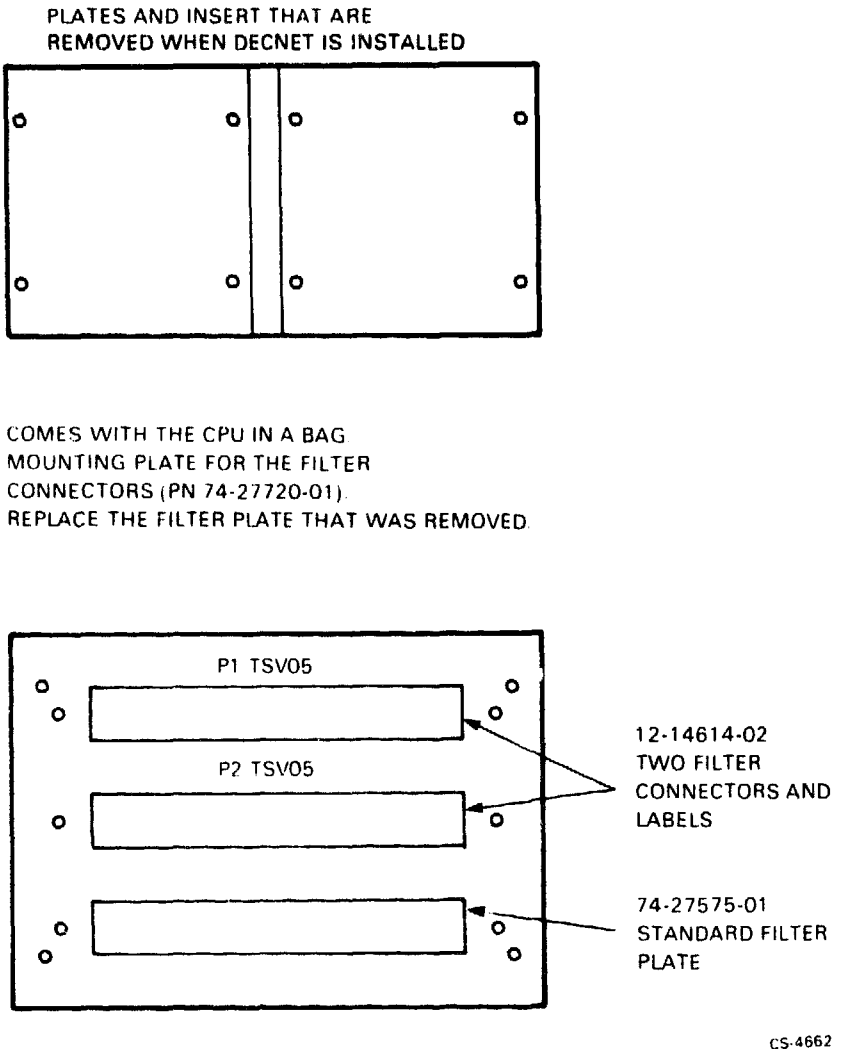


Figure 3-20 BA23A with TSV05 Filter Connector Mounting (with DECnet)

3.6 BUS INTERFACE/CONTROLLER MODULE INSTALLATION (M7196)

3.6.1 General Information

The M7196 bus interface/controller module plugs into a quad slot in the Q-bus backplane. It connects the Q-bus on the A and B sets of edge connectors (module fingers). It is shipped with the switches set for an interrupt vector of 224 and an address of 172520. If your system already uses this address, the M7196 module must be switched to other addresses. Refer to Figures 3-21 and 3-22 for information on switching the switchpacks on the M7196 module. Refer to the *Microcomputers and Memories Handbook* or your system configurator for guidance in selecting new addresses.

For guidance in selecting the best backplane slot in which to install the M7196 module, refer to your system documentation or to the *Microcomputers and Memories Handbook*.

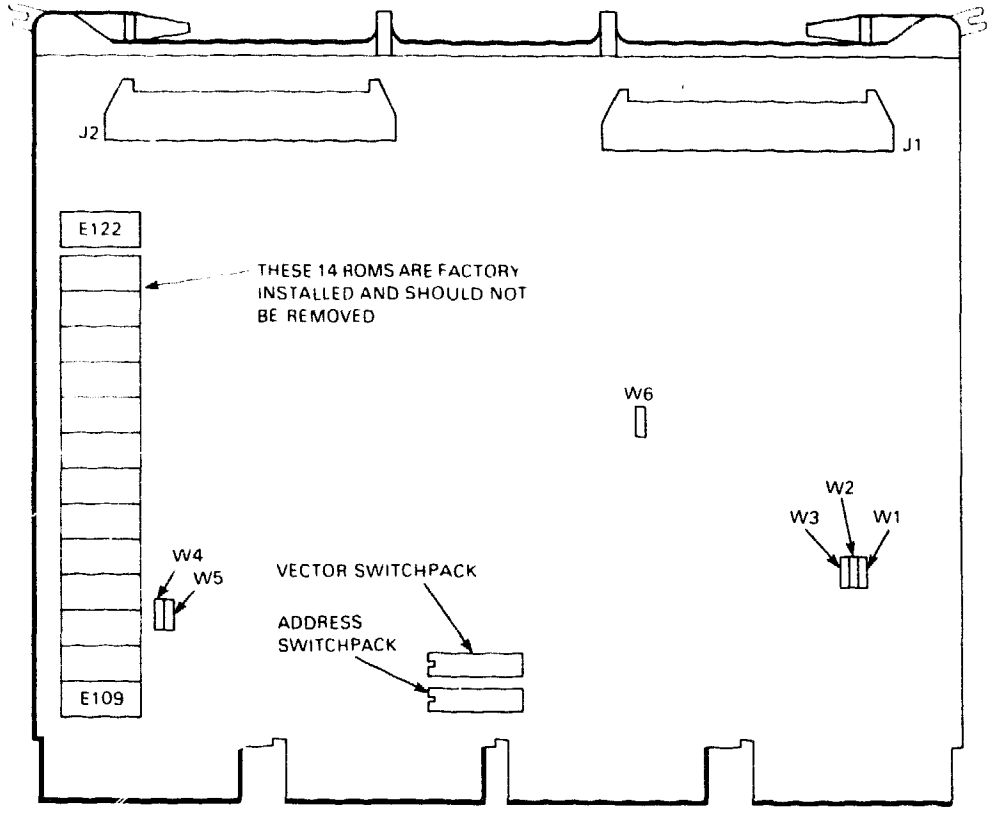
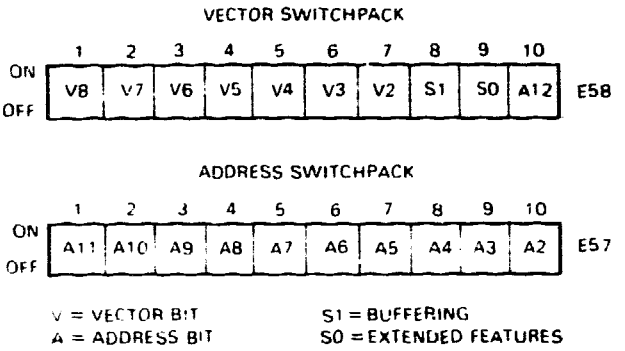


Figure 3-21 M7196 Switch and Jumper Identification



JUMPERS		AS SHIPPED
W1	BIRQ5	OUT
W2	BIRQ7	OUT
W3	BIRQ6	OUT
W4	BUS GRANT CONTINUITY	IN
W5	BUS GRANT CONTINUITY	IN
W6	SCLOCK ENABLE (USED DURING FACTORY REPAIR ONLY)	IN

CS-4681

Figure 3-22 M7196 Vector and Address Switches

3.6.2 Installing the Controller (M7196) and Cables

1. Locate the M7196 controller and remove it from its shipping box.
2. Locate the two sets of cables.
   a. One set has two different connectors at each end of the cables. These cables are labeled P/N 70-16855-XX (-XX indicates the length variation).
   b. The other sets have the same connectors at each end of the cables. These cables are labeled BC06L-XX (-XX indicates the variation).
3. Install one end of the BC06L-XX cables in the P1 and P2 connectors of the TSV05 controller board M7196 (see Figures 3-23 through 3-25).
4. Install the M7196 controller board in the last slot of the CPU backplane.

CAUTION

Do not remove a grant jumper in either slots 1, 2, or 3 or install the M7196 in any of those slots as they are for dual boards only. Installing a quad height board could damage the CPU or the quad height board.

5. Ensure that the cable connectors are seated into the connectors on the controller board before proceeding.
6. Connect the other end of the BC06L-XX cables to the filter connectors on the I/O distribution panel.

NOTE

The red stripe on the cables should be face down or to the right when installing the M7196 in the cabinet.

7. Connect the smaller connector on the P/N 70-16855-XX cables to the other end of the filter connectors.

NOTE

The red stripe on the P/N 70-16855-XX cables should be oriented in the same direction as the BC06L-XX cables.

8. Connect the other end of the P/N 70-16855-XX cables from J1 on the I/O distribution panel to J1 on the tape drive unit.
9. Connect the other end of the P/N 70-16855-XX cables from J2 on the I/O distribution panel, to J2 on the tape drive unit.

NOTE

The red stripe on the cables should go to the right when facing the tape drive from the rear.

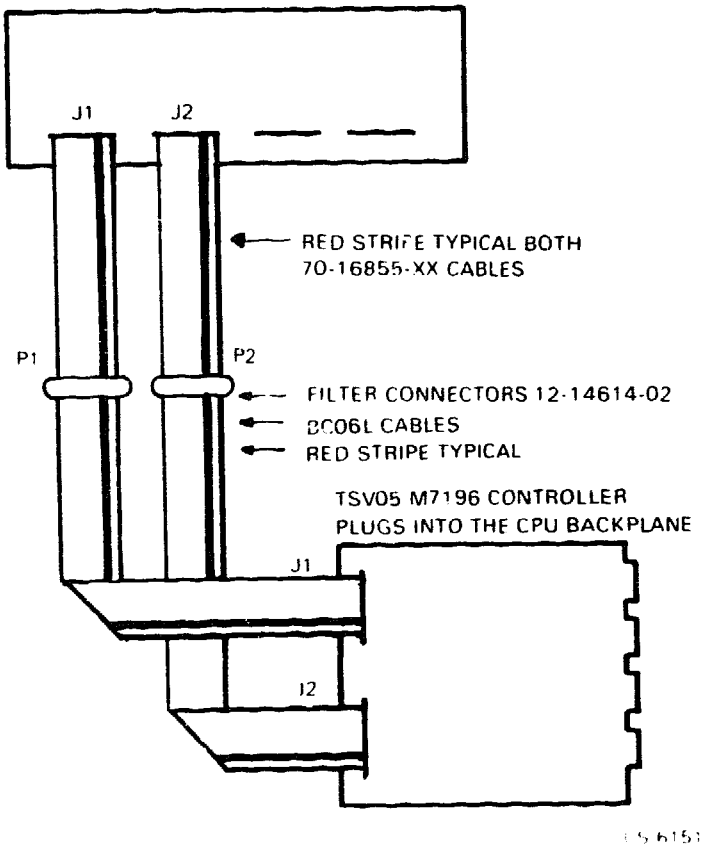


Figure 3-23 TSV05 Cable Configuration

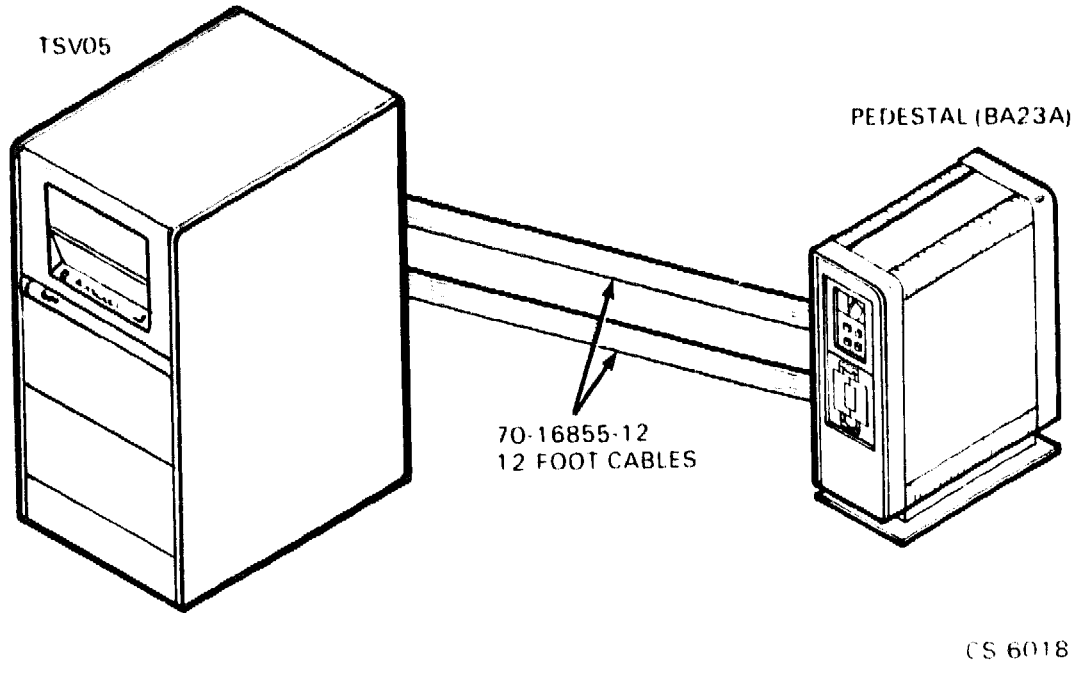


Figure 3-24 Configuring the TSV05 with the BA23A Pedestal

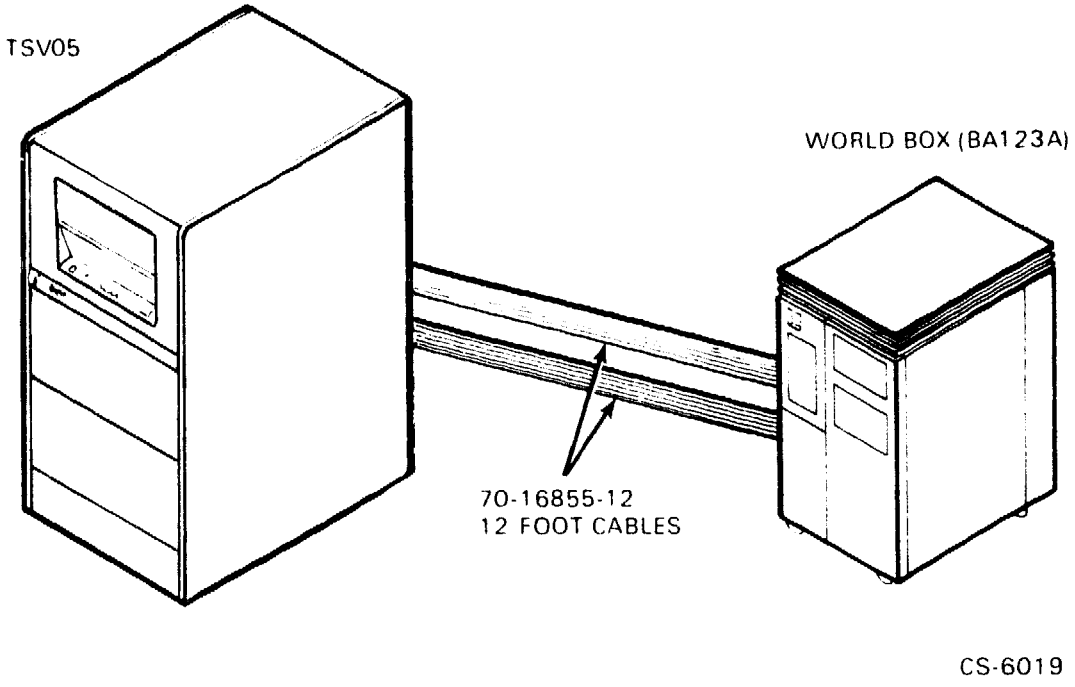


Figure 3-25 Configuring the TSV05 with the BA123A World Box

3.6.3 Connecting the Line Power Cord

The TSV05-B model is equipped with a cabinet power controller. Before connecting the line power, perform the following:

1. Place the POWER switch on the front panel of the tape transport in the 0 (off) position.
2. Ensure that the power controller voltage rating is correct for your system.
3. Place the power controller circuit breaker switch in the OFF position.
4. Place the controller LOCAL/REMOTE Switch[4] in the LOCAL position.
5. Unwind the line power cord and plug it into the receptacle.

3.7 CHECKING OUT THE TSV05 SUBSYSTEM

The TSV05 subsystem checkout procedure depends on the Micro system installed. Proceed to the applicable chapter to check out your TSV05 subsystem.

- PDP-11 processor (Chapter 4)
- MicroVAX II processor (Chapter 5)

[4] On some units, this switch is labeled A O B respectively. If this is the case, place the switch in the B position.


CHAPTER 4

CHAPTER 4
TSV05 CHECKOUT (PDP-11 PROCESSOR)

4.1 GENERAL INFORMATION

The TSV05 subsystem is tested in the following manner:

- Checking the interface/controller module LED indicators and voltage supply
- Running the diagnostic programs listed in Table 4-1.

These programs are available on the XXDP+ diagnostic software package that is shipped with the computer system. If your system is an earlier model and has the XXDP package instead of the XXDP+, contact your local DIGITAL representative for ordering information.

Table 4-1 TSV05 Subsystem Diagnostics

Program Title	File Name
Logic Test	CVTSA
Advanced Logic Test	CVTSB
Transport Test	CVTSC
Advanced Transport Test	CVTSD
Data Reliability Test	CVTSE
DEC-X11	XTSAA0

4.2 POWER-UP CHECKS

Complete the following steps to verify proper system power-up:

1. Set the POWER switch on the tape transport unit to the ON (1) position.
2. Switch on the computer system power and observe that the tape unit powers up with the system.
3. After a few seconds, all the tape unit indicators should be extinguished except for the the UNLOAD indicator.
4. Using a DVM, verify that the +5V power to the interface/controller module is within specification. Typically, the additional load of the interface/controller module lowers the power supply voltage slightly. Adjust if necessary.
5. Verify that the self-test LED on the interface/controller module (Figure 4-1) is blinking. This indicates that the interface/controller module self-test diagnostics are running. If other indications occur, there is a problem. Refer to the *TSV05 Pocket Service Guide* or contact your local DIGITAL Field Service representative.
6. Replace the access panel on the computer, and close the rear doors of the cabinets.

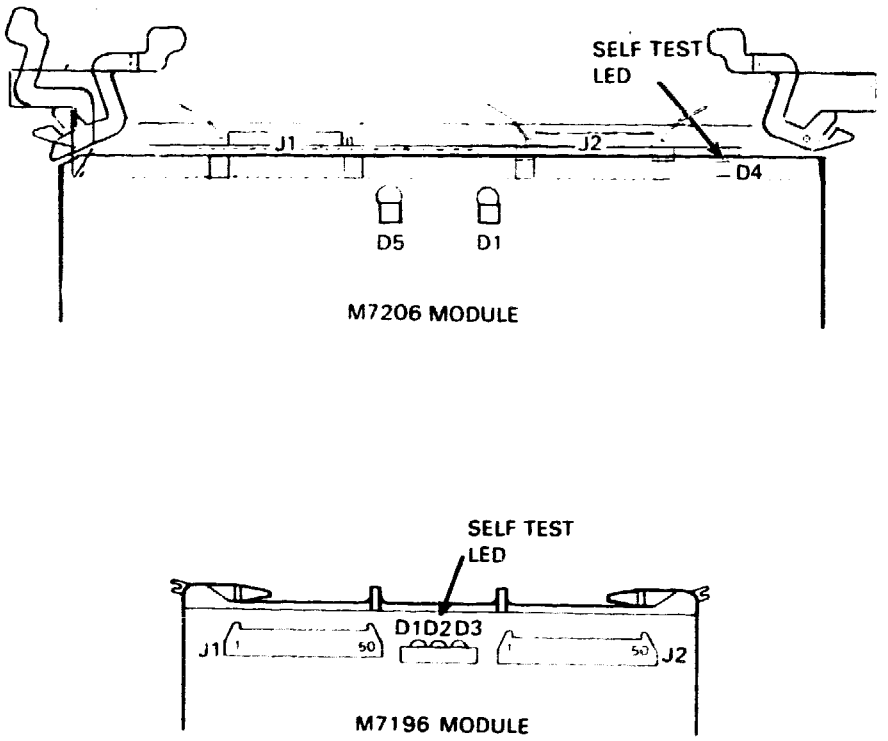


Figure 4-1 Locating the Interface/Control Module Self-Test LED

4.3 DIAGNOSTIC TESTS

4.3.1 System Setup

Complete the following steps prior to running each of the diagnostic tests listed in Table 4-1.

1. To prevent erroneous error indications, ensure that the tape transport is clean, and the blank tape is known to be of good quality.
2. Load the blank tape into the tape transport by:
   a. Opening the front panel access door.
   b. Inserting the tape reel, with the file-protect ring side down, and centering it on the hub.
   c. Closing the door.
   d. Pressing the LOAD switch.
   e. Waiting for the LOAD indicator to stop blinking and stay on continuously.
   f. Pressing the ON-LINE switch.
3. Load the computer system diagnostic disk pack or floppy.
4. Before running the tape subsystem diagnostics, run the system exerciser or diagnostics to verify that the computer is operating properly. For instructions on running the computer system tests, refer to the documentation for the system.

NOTE

The logic test and the advanced logic test (CVTSA and CVTSB) do not require a tape to be loaded in order to run. The other diagnostics, however, require the tape to be loaded and the tape subsystem to be on-line.

4.3.2 Diagnostic Test Procedures

Perform the following test procedures in order.

4.3.2.1 TSV05 Logic Test - This program tests the logic on the Q-bus interface/controller module. It checks the microprocessor, RAM, and various registers. It verifies that the computer can move data out to the module and receive status in from the module. After you have booted the XXDP+ disk (DL, DX, or DY) and answered the questions about the date, the processor, and the power line frequency, start the logic test as follows (operator responses are in italics).

```
.R VTSA?? <CR>
```

The system responds with a display similar to the following.

```
DIAG. RUN-TIME SERVICES
CVTSA-A-0
****TSV05 LOGIC DIAGNOSTIC****
UNIT IS TSV05
DR>
```

At this point, type in the following commands.

```
DR> START/FLAG:PNT:HOE <CR>
```

This instructs the program to start the test, display the test number as each of its 11 tests are executed, and halt it if an error is detected. The computer now asks the following:

```
CHANGE HW (L) ?
```

Type in a "Y" for yes:

```
CHANGE HW (L)? Y <CR>
```

The computer then asks:

```
# UNITS (D) ?
```

Type in a "1" to indicate that there is one tape unit:

```
# UNITS (D) ? 1 <CR>
```

The computer then displays the device address, the interrupt vector, and the interrupt priority. If you have left the interface/controller module in the configuration in which it was shipped, respond to these queries by typing a carriage return.

```
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (O) 172520? <CR>
INTERRUPT VECTOR (O) 224? <CR>
```

If, on the other hand, you have changed the switchpack settings on the interface/controller module, then you must type in the parameters you selected.

The computer then asks if you wish to change the software parameters:

```
CHANGE SW (L)
```

For the subsystem checkout, the answer to this question is "no".

```
CHANGE SW (L) ? N <CR>
```

After you have responded to these questions, the program starts testing the subsystem. The program runs continuously, repeating itself until it detects an error, or until you halt it. If the program halts because of an error, refer to the *CVTSAA TSV05 MAGTAPE Diagnostic User's Document* for a detailed description of the tests. For assistance, contact your local DIGITAL Field Service office.

After the program has made one pass through all the tests, halt it by pressing CONTROL C. This passes control of the system back to the diagnostic supervisor program. Then type "EXIT" to get back to the system monitor.

```
^C
DR> EXIT <CR>
```

4.3.2.2 Advanced Logic Test - This program verifies that the interface/controller module can get status and write characteristics from the computer memory, and that it can deposit message packets in the computer memory. It tests error detection circuits and verifies that the computer can initialize and write into the controller RAM memory. It checks the internal timers, buffers, and status and control logic. Also, it verifies that the controller can move signals to and from the cables that connect it to the tape transport unit.

Load this program as follows:

```
.R VTSB?? <CR>
```

After the program title is displayed and the diagnostic supervisor returns the DR prompt, enter the following command line.

```
DR> START/FLAG:PNT:HOE:UAM <CR>
```

The program responds by asking the same questions about hardware and software parameters as were asked by the logic test. Type in the same answers. After the last question is answered, the program starts running its tests (this one has 12 tests, with the last three not executed). It runs continuously until there is an error, or until you halt it. After one pass, halt the program by typing CONTROL C, and type EXIT to return to the system monitor.

```
^C
DR> EXIT <CR>
```

4.3.2.3 Tape Transport Test -

NOTE

The TS05 tape transport must be connected to the controller module, be powered up, have a tape loaded, have the write ring installed, and be ON LINE for the following tests.

This program verifies correct tape motion command decoding. It checks the basic operation of the rewind positioning command, the write data command, and the read forward and read reverse commands. It verifies that the system can space over records in forward and reverse directions, and that it can reread records. The ability of the subsystem to respond to error conditions is also tested. The program checks the commands for retrying to write data and tape marks. It also tests the skipping of tape marks in forward and reverse directions.

Load the program as follows:

.R VTSC?? <CR>

After the system displays the program title, enter the same command line and answers to the parameter questions as for the previous program (described in Chapter 2, Section 2.7.4). After one successful pass to the eight tests in this program, halt the program and exit to the system monitor.

4.3.2.4 Advanced Tape Transport Test - This program verifies the functioning of the No-Op, Initialize, and Erase commands. It checks that errors are indicated when no data is found on the tape, and it tests the data parity checking circuitry in both the controller and the tape transport electronics. It checks for the proper handling of the EOT status and tests the record buffering functions. It also checks that records and gaps written on the tape are the correct length.

Load the program as follows:

.R VTSD?? <CR>

After the title is displayed, enter the following command:

DR> START/FLAG:PNT:HOE <CR>

The program starts and runs its nine tests. After one successful pass, halt the program and exit to the system monitor.

4.3.2.5 Data Reliability Test - This program exercises and verifies the correct completion of all tape transport functions. It executes read and write commands a random number of times, with records of random length and data, for the entire tape.

Load the program by typing:

R VTSE?? <CR>

and then, after the title is displayed, enter the following:

DR> *START/FLAG:PNT:HOE <CR>*

NOTE

Magtape media typically will have several flaws per reel that will cause this diagnostic to indicate write errors or write retries due to bad tape spots. These types of errors do not indicate a problem with the subsystem.

The program then asks the following:

SELECT DRIVE 0-1 (0)?

Answer by typing 0 and a carriage return.

0<CR>

NOTE

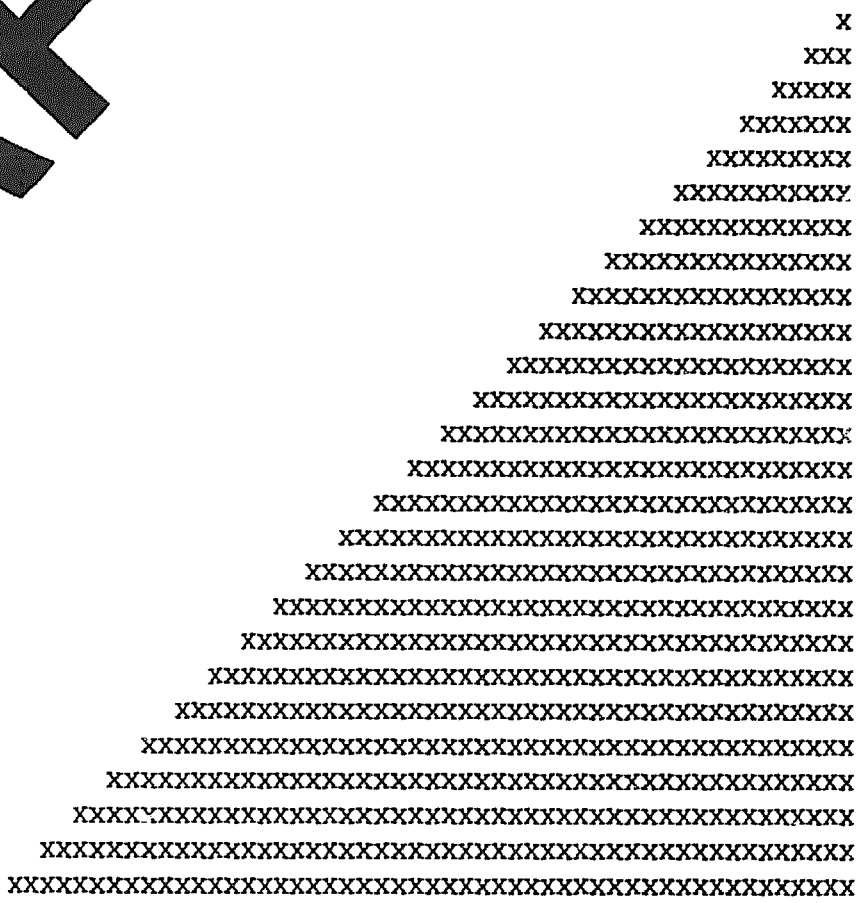
This program will run until an error is detected or until a CONTROL C is entered on the console.

4.4 ADDITIONAL TESTS

The tests described in the preceding sections provide a high confidence level that the TSV05 subsystem is functioning correctly. More exhaustive checks are available by allowing the diagnostic programs to run for more than one pass. The second pass of the program is more comprehensive than the first pass. All iterations after the first pass are the same; however, they are substantially longer than the first one. Running tests that cause tape motion for extended periods will require transport cleaning to prevent erroneous error reports. The logic type tape motion tests, when run continuously, can cause high tape wear to occur in the first few feet of tape. In these cases, errors due to faulty or worn tape do not indicate a failure.

Another test that may be run is the DEC/X11 runtime system exerciser. This test exercises the entire system to verify that there are no spurious interactions between various subsystems and components. There is an exerciser program module for each major system component, and these are linked together to create a system exerciser that is tailored to your system. The DEC/X11 module for the TSV05 subsystem is XTSAA0. Although this exerciser can be run by itself, its full value is not realized unless it is linked to and run with the system exerciser. For information about building a system exerciser to include the TSV05 subsystem, refer to the *DEC/X11 User Document* (AC-8240Z-MC).

CHAPTER 5



CHAPTER 5
TSV05 CHECKOUT (MicroVAX II PROCESSOR)

5.1 GENERAL INFORMATION

5.1.1 Prerequisites

- Functional MicroVAX II
- Functional Console Terminal

5.1.2 Hardware Requirements

- MicroVAX II Processor (256K words memory, minimum)
- TSV05 Magtape Subsystem (Drive and Controller)

5.1.3 Software Requirements

MDM Diagnostic Monitor

5.2 POWER-UP CHECKS

Complete the following power-up check steps:

1. Set the POWER switch on the tape transport unit to the ON (1) position.
2. Switch on the computer system power, and observe that the tape unit powers up with the system.
3. After a few seconds, all the tape unit indicators should be extinguished except for the the UNLOAD indicator.
4. Verify that the +5 V power to the interface/controller module is within specification. Typically, the additional load of the interface/controller module lowers the power supply voltage slightly. Adjust if necessary.
5. Verify that the self-test LED on the interface/controller module (Figure 5-1) is blinking. This indicates that the interface/controller module self-test diagnostics are running. If other indications occur, there is a problem. Refer to the *TSV05 Pocket Service Guide*, or contact your local DIGITAL representative.
6. Replace the access panel on the computer and close the rear doors of the cabinets.

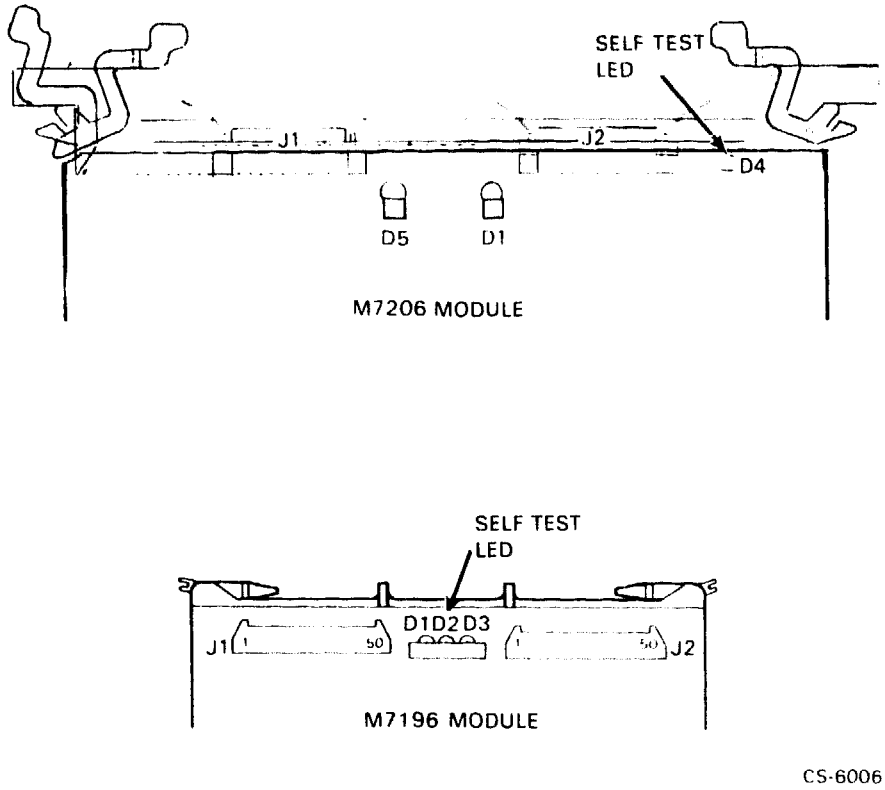


Figure 5-1 Locating the Bus Interface/Controller Module Self-Test LED

5.3 DIAGNOSTIC TEST

5.3.1 Loading MicroVAX Maintenance Software

- Turn the system OFF.
- Insert the MicroVAX Maintenance System software (minimum revision level MDM 118).
- Press the RESTART button.

  After pressing the RESTART button, the normal system startup message will appear. This startup message will then be followed by the MicroVAX Maintenance System Menu.
- Turn the tape drive power on. Load a tape with a write enable ring installed, and place drive on line.

5.3.2 Running the MicroVAX Maintenance Software (Customer Version)

1. Select Item Number 1 at the MicroVAX Maintenance System Menu to test the system.
2. Be sure that device MSA0: is recognized.
3. If no errors are detected, a "SYSTEM TEST PASSED" message will be displayed on the console. Follow the message instructions to exit the test.
4. When an error is detected, an error message will appear along with a description of the affected Field Replaceable Unit (FRU).
5. If the TSV05 tape drive is the FRU specified in the error message, refer to the *TSV05 Pocket Service Guide* for troubleshooting replacement instructions. Error reports include:

   a. Failing function (test step).

   b. Error number (a decimal indication of the unique error number within the diagnostic).

   c. FRU Identification.

   TSA DSL Pass number 1 Test number 5

   TSA - Error number 210

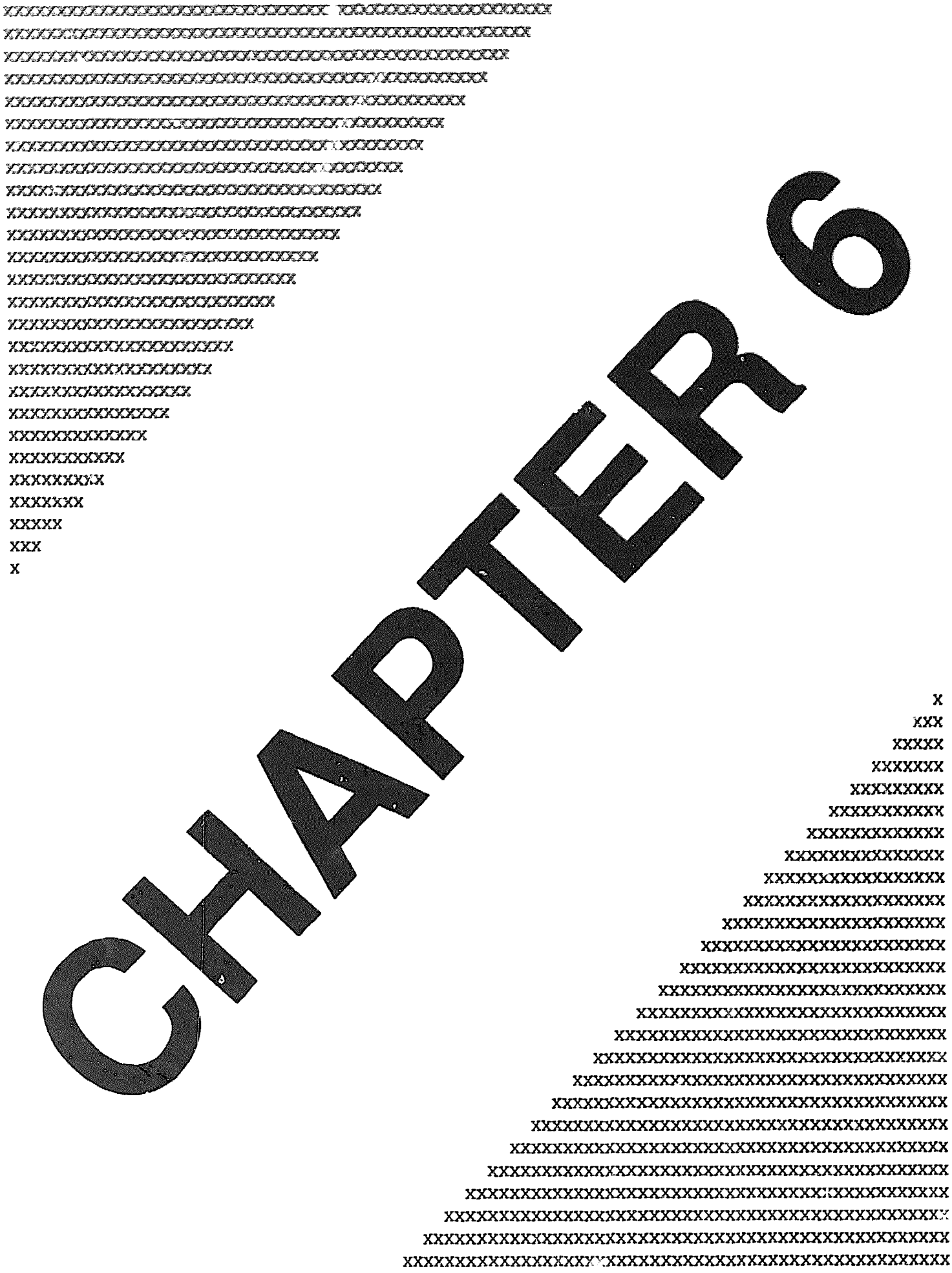
   Fatal exit DRIVE IS OFF LINE

   TSV05 DRIVE

   TSA ended with stopped

5.3.3 Running the MicroVAX Maintenance Software (Service Version)

Refer to the *MicroVAX Diagnostic Monitor User's Guide* to run the service version of the MicroVAX maintenance software.


CHAPTER 6

CHAPTER 6
OPERATION

System operations can be divided into various levels or categories of activities. At the most basic level are activities such as powering up and maintaining the system, loading the tape, and performing verification (confidence) checks on system operation. A second category of operating activities involves system generation. When the TSV05 subsystem is added to the computer system, the software operating system must be modified to include the handler for the tape transport subsystem. System generation requires building a new copy of the operating system. A third category of operating procedures covers the use of the software utility programs for operations such as copying data from one drive to another, updating files, and comparing one file to another. The most complex level of user activity involves designing programs that manipulate the internal workings of the tape transport subsystem. This chapter devotes sections to these categories of activities.

6.1 ROUTINE OPERATING PROCEDURES

6.1.1 Power-Up

On the tape transport front panel, press the POWER switch to its ON ("1") position. The indicators all light for approximately two seconds and then go out. The UNLOAD indicator then lights and stays on. At this point, the tape unit is ready to be loaded.

6.1.2 Loading the Tape

The TSV05 subsystem loads tape automatically unless the tape is in very bad condition. If data must be recovered from a tape that is crumpled or creased on the end, it may be necessary to load the tape manually. Refer to Appendix B for instructions on manual loading. For best load reliability, the Beginning Of Tape (BOT) leader should be crimped, using DIGITAL P/N 47-00038 (or equivalent). However, do not repeatedly crimp or remove excessive tape leader, as this causes the BOT marker to be too close to the tape end. Tape crimper P/N 47-00038 can be ordered from the Accessories and Supplies Group, as outlined in Section 6.1.8.2.

For normal tape loading, proceed as follows.

1. Ensure that the tape is wound completely onto the reel, and the file-protect ring is fully seated, if present on the reel.

NOTE

Most tapes have some form of stick-on TAB or rubber block to prevent the tape from unwinding during shipment or storage. These items must be removed so that the tape leader is free to unwind during the autoloading sequence. High levels of static electricity should also be avoided, since this prevents the tape leader from unwinding.

2. Open the front door panel by gently pressing down on the top center of the door (see Figure 6-1).
3. Hold the tape reel with the file-protect ring side down. Insert the reel into the transport unit, centering it on the hub.
4. Close the door.

CAUTION

Both the tape transport top cover and front panel door are locked when a tape is loaded. Any attempt to force open either the cover or the door before the tape is unloaded results in mechanical damage to the locking mechanism.

5. Press the LOAD/REWIND switch. This locks the cover and the door, and begins the loading sequence.
6. The LOAD indicator blinks while the tape is being loaded. Typically, after 30 seconds, the LOAD indicator stops blinking and remains lighted. This indicates that the tape is loaded and the TSV05 subsystem is ready to use.
7. Press the ON LINE switch to place the tape subsystem under the control of the host computer. The ON LINE indicator lights when the TSV05 subsystem is on-line. The ON LINE switch can be pressed immediately after the load switch.

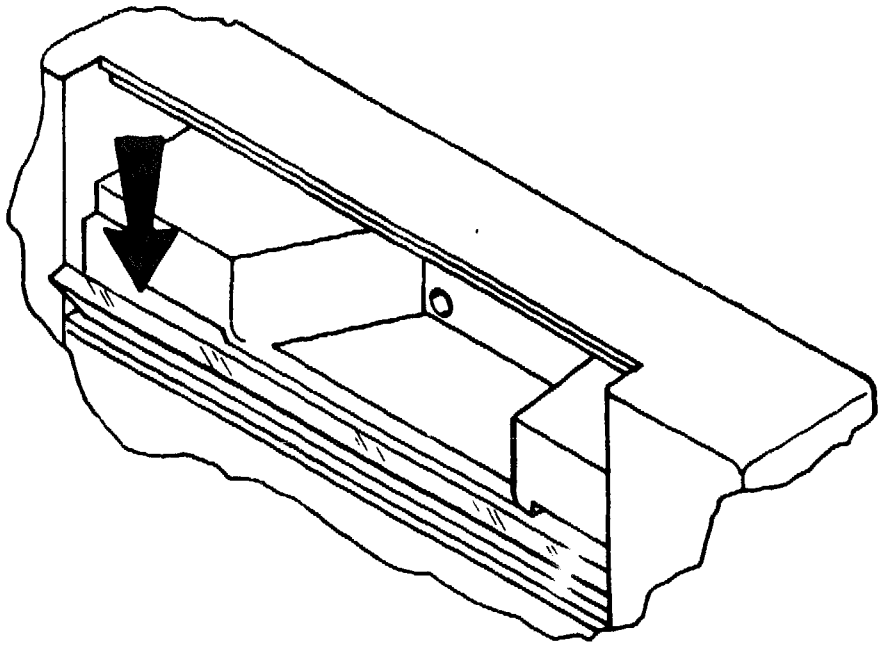


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Figure 6-1 Opening the Front Door Panel

6.1.3 Rewinding the Tape

It is not necessary to rewind the tape during normal operation, as all tape movement is under program control. Under unusual circumstances, however, such as a host system failure or a loss of communications with an upline host, you may wish to rewind the tape under local control. This is done as follows:

1. If the tape transport is on-line (indicated by the ON LINE indicator being ON), press the ON LINE switch once to switch off-line.
2. Press the REWIND switch. The LOAD/REWIND indicator blinks while the tape is rewound, and then remains on continuously when the BOT marker is reached.

6.1.4 Unloading the Tape

To unload a tape positioned at BOT, proceed as follows.

1. If the tape transport is on-line (indicated by the ON LINE indicator being ON), press the ON LINE switch once to switch off-line.
2. Press the UNLOAD switch. The UNLOAD indicator blinks while the tape is unloaded. When the unloading process is complete, the UNLOAD indicator lights continuously, and the front panel and top cover are unlocked. A typical unload sequence from BOT takes 15 seconds.
3. Open the front panel door (Figure 6-1) and lift the tape reel out of the tape transport.
4. Close the front panel door.

6.1.5 Restarting the Tape Transport

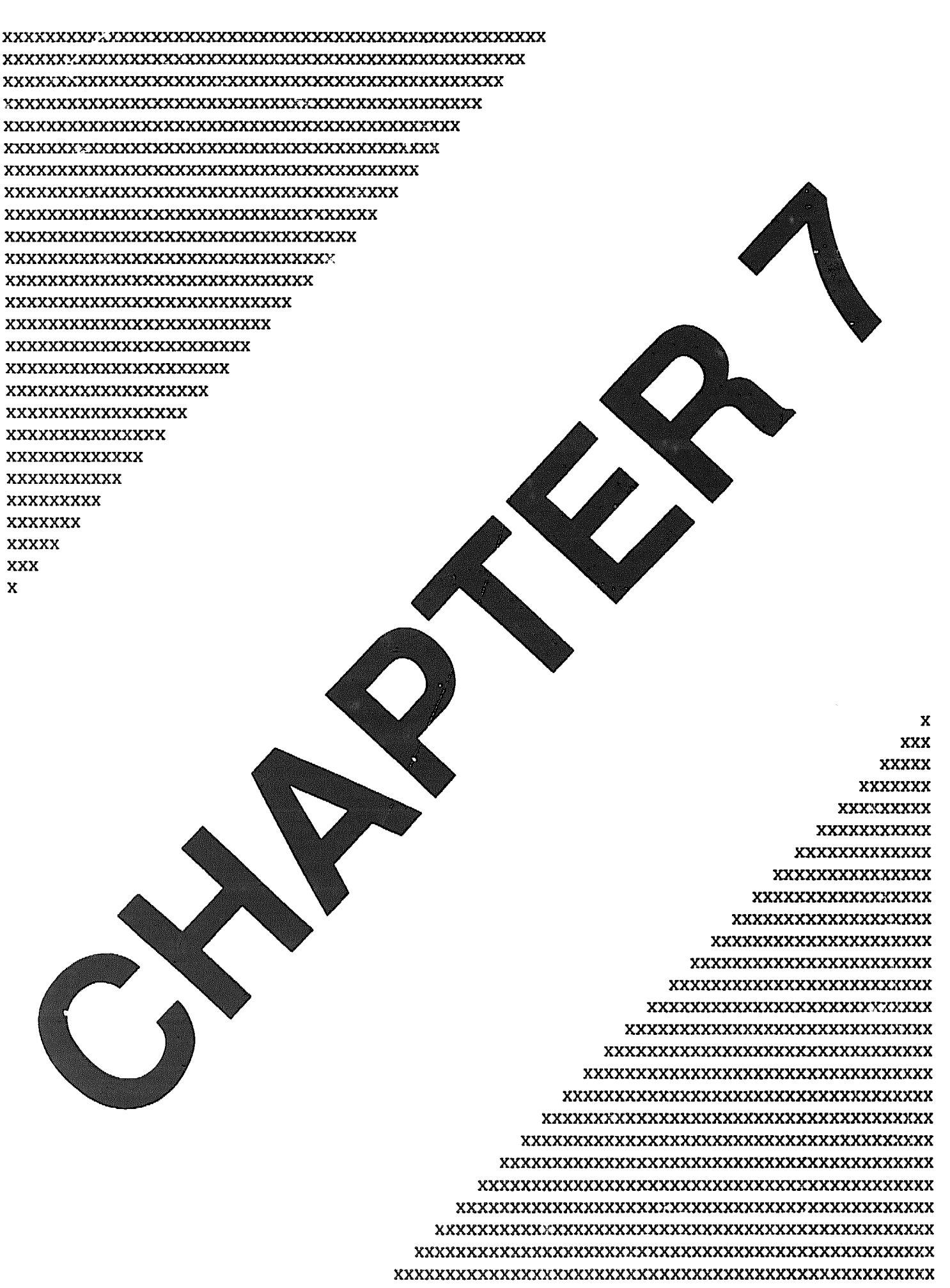
The TSV05 subsystem ceases operation in the event of a power failure, or if it detects a hard operational error.

6.1.5.1 Power Failure - When line power is interrupted, the tape transport automatically shuts down and tape motion stops without any physical damage to the tape. When line power is restored, the TSV05 subsystem powers up in the unload mode. Press either the LOAD or the UNLOAD switch.

If the LOAD switch is pressed, the LOAD/REWIND indicator blinks while the tape is reloaded to the BOT marker. When the BOT marker is reached, the LOAD/REWIND indicator remains on continuously, and the ON LINE switch can be pressed to return the tape transport to computer control.

If the UNLOAD switch is pressed, the UNLOAD indicator blinks while unloading is in progress. When the UNLOAD indicator remains lit continuously, the door can be opened and the tape removed.

6.1.5.2 Hard Errors - When the TSV05 subsystem encounters an error condition from which it cannot automatically recover, it stops tape movement and displays a series of blinks on the indicators. If this happens, switch the power OFF, switch it back ON again, and then press the UNLOAD switch. After the UNLOAD indicator stops blinking, remove the tape. At this point, it may be necessary to call either DIGITAL Field Service or refer to the *TSV05 Pocket Service Guide*.


CHAPTER 7

CHAPTER 7
MAINTENANCE

7.1 OPERATOR TROUBLESHOOTING

It may be possible to avoid a service call by making a few checks before reporting a condition as a problem. If the TSV05 subsystem is located in an area where several people may be using the tapes and equipment for different purposes, check the following.

1. If the tape transport does not power up, ensure that the power controller in the TSV05 subsystem has:
   a. Circuit breaker switches ON.
   b. REMOTE ON/OFF/LOCAL ON switch switched to LOCAL ON. This switch may also be labeled A,O,B. If that is the case, it should be in the B position.
   c. Remote control cable connected to DIGITAL power connector.
   d. Power controller pilot lamp lit.
2. If a tape does not load properly, ensure that:
   a. Tape is in reasonably good condition (if not, refer to manual loading procedure in Appendix B).
   b. Tape has a BOT marker located 4.9 +0.6 meters (16 +2 feet) per ANSI STDX3.40-1973.
   c. Front panel door is completely closed.
   d. The instructions on the loading label are followed.
3. If the subsystem is unable to write a file, ensure that the write enable ring is installed in the tape reel.
4. If intermittent problems occur involving the read/write functions, clean the tape path (see Chapter 6, Section 6.1.8, Customer Care).

If it is determined that the equipment is malfunctioning, record the symptoms of the malfunction to aid maintenance personnel in troubleshooting the system.

TSV05 maintenance activities, such as fault isolation and Field Replacement Unit (FRU) removal and replacement, are described in detail in the *TSV05 Pocket Service Guide* (EK-TSV05-PS).

7.2 CONFIDENCE CHECKS

There are three "confidence levels" established by testing. The basic level of confidence is established simply by powering up the system. Both the tape transport and the controller module perform internal self-test programs each time power is applied. Therefore, the ability of the TSV05 subsystem to power up and load tape establishes that it is probably in good working order.

A second, higher level of confidence is established by using the console terminal of the host computer system to check the status of the TSV05 subsystem. This is performed by using the appropriate operating system command to check device status (for example, on-line or off-line) or to call for a directory listing from a tape mounted in the TSV05 subsystem. If the subsystem powers up and loads tape properly, and if the operating system receives directory or status information from the TSV05 subsystem, then the probability that the system is working correctly is very high.

The highest level of confidence is established by running the Data Reliability Diagnostic Program (CVTSE in the XXDP diagnostic package) and the DEC/X11 exerciser.

7.3 CUSTOMER CARE

The person in charge of the TSV05 subsystem is normally responsible for the following tasks:

- Obtaining operating supplies including magnetic tape and cleaning supplies.
- Maintaining the required logs and report files consistently and accurately.
- Making the documentation available in a location convenient to the system users and maintainers.
- Ensuring that the exterior of the system and the surrounding area are kept clean.
- Ensuring that ac plugs are securely plugged in each time the equipment is used.
- Ensuring that preventive maintenance activities are performed at the suggested periods, or more often if usage and environment warrant.

7.3.1 Care of Magnetic Tape

The person responsible for the TSV05 subsystem ensures that system users exercise due care in the handling of magnetic tape. Basic rules of tape care are as follows.

- Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head. Keeping the tape clean is imperative.
- Always store tape reels inside containers when the tape is not in use. Keep empty containers tightly closed to guard against dust and dirt.
- Never touch the portion of tape between the BOT and End-of-Tape (EOT) markers; oil from fingers attracts dust and dirt.
- Never use a contaminated reel of tape since this spreads dirt to the clean tape reels and could adversely affect tape transport reliability.
- Always handle tape reels by the hub hole. Squeezing the reel flanges leads to tape edge damage when winding or unwinding tapes.
- Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.
- Do not place magnetic tape near line printers or other devices that produce paper dust.
- Do not place magnetic tape on top of the tape transport or in any other location where it may be affected by hot air.
- Do not store magnetic tape near electric motors.

7.3.2 Preventive Maintenance

The tape transport is a highly reliable precision instrument that provides years of trouble-free performance when properly maintained. For optimum performance and reliability, a planned and scheduled program of routine inspection and maintenance is essential. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is essential to proper tape transport operation. The frequency of maintenance operations varies with the environment and the degree to which the transport is used. Therefore, a rigid schedule for all machines is difficult to define. Cleaning after every eight hours of operation is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows that other periods are more suitable. Typically, new tapes or tapes near the end of their life produce the most oxide buildup within the tape transport and require more frequent cleaning. Table 7-1 shows the recommended frequency of maintenance activities. The replacement of filters and reel motors and the checkout of head wear is to be performed by DIGITAL Field Service personnel. Other activities are to be performed by the customer.

Before performing any cleaning operation, remove the supply reel and store it properly. When cleaning, be gentle but thorough.

Table 7-1 Suggested Preventive Maintenance

Maintenance Operation	Frequency	Quantity to Maintain
Clean Head, Guides, Roller Guides, Tape Path	Once per shift	-
Clean Tape Cleaner	Once per shift	1
Clean Reel-Hub Pads	Once per shift	3
Clean Tachometer Roller	Once per week	1
Check Head Wear	2,500 hours	1
Replace Reel Motors	10,000 hours	2
Check Air Filter	Every three months	1

7.3.2.1 Magnetic Tape Transport Cleaning Kit - A magnetic tape transport cleaning kit (TUC02, P/N 22-00012) has been carefully assembled to provide materials that do not harm tape equipment or leave any residue to interfere with data reliability. The hints contained in the following paragraphs aid in obtaining the very best results from the kit.

WARNING

When using DIGITAL magtape cleaning fluid, avoid excessive contact with the skin and eyes. Harmful if swallowed. Use the cleaning fluid only in a well ventilated area.

When cleaning tape equipment, never dip a dirty cleaning swab or wipe into the can.

Always keep the can of fluid tightly closed when not in use; the fluid evaporates rapidly when exposed to air.

CAUTION

Do not use acetone, lacquer thinner, or rubbing alcohol to clean the tape path and related parts.

If there is any unusually stubborn dirt deposit that resists the cleaner, try using a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with cleaning fluid to remove any residue.

If more cleaning materials, tape crimper (P/N 47-00038), or other items are required, forward orders for supplies, accessories, or documentation to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. Eastern Standard Time (U.S. customers only). New Hampshire, Alaska, and Hawaii customers should dial (603) 884-6660. Terms and conditions include net 30 days and F.O.B. Digital Equipment Corporation plant. Freight charges are prepaid by Digital Equipment Corporation and added to the invoice. Minimum order is $35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

7.3.2.2 Accessing the Tape Path Area - Raise the cabinet top cover by grasping the handle on the top cover and lifting (refer to Figure 7-1). When the top cover is raised far enough, the support arm latches to keep the cover up.

Raise the top cover of the tape transport unit by reaching in through the front panel door and pressing upward at the front area of the top cover.

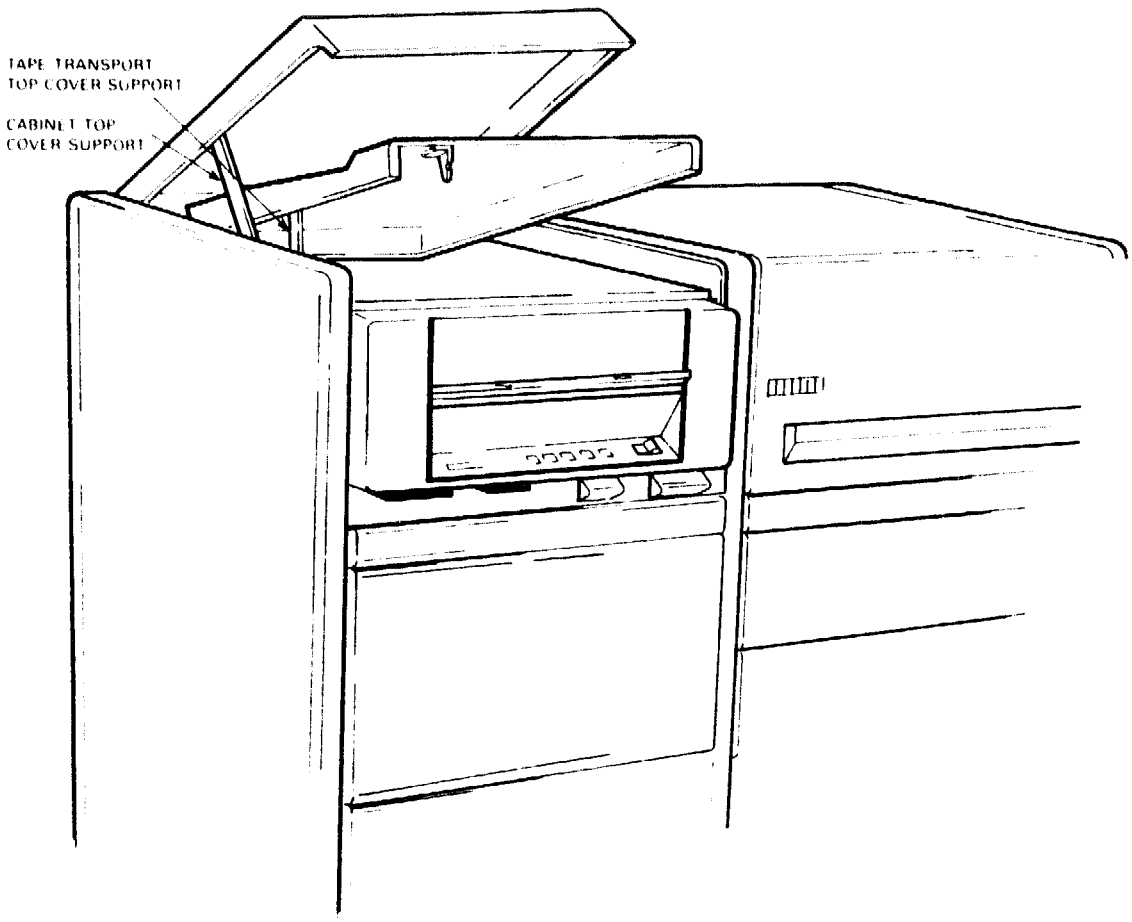


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Figure 7-1 Accessing the Tape Path Area

7.3.2.3 Cleaning the Tape Path and Related Parts - Using foam-tipped swabs soaked in cleaning fluid, gently wipe the following parts (refer to Figure 7-2):

- Read/write head
- Tachometer roller
- Tape cleaner

CAUTION

Exercise care to avoid damage to the sharp edges of the blades on the tape cleaner.

- Roller guides (quantity of five)

NOTE

When cleaning the roller guides, the cleaning fluid should contact only the tape-bearing surfaces. This prevents degreasing the roller guide bearing.

- Supply hub pawls (quantity of three)
- Tape path (use the supplied texwipes)

7.3.2.4 Cleaning the Housing - Clean the front panel door and control panel with Miller Stephenson Chemical Company MS-260, Windex™, or an equivalent commercial grade plastic cleaner. Use a clean, lint-free wipe material.

Windex™ is a trademark of The Drackett Products Company.

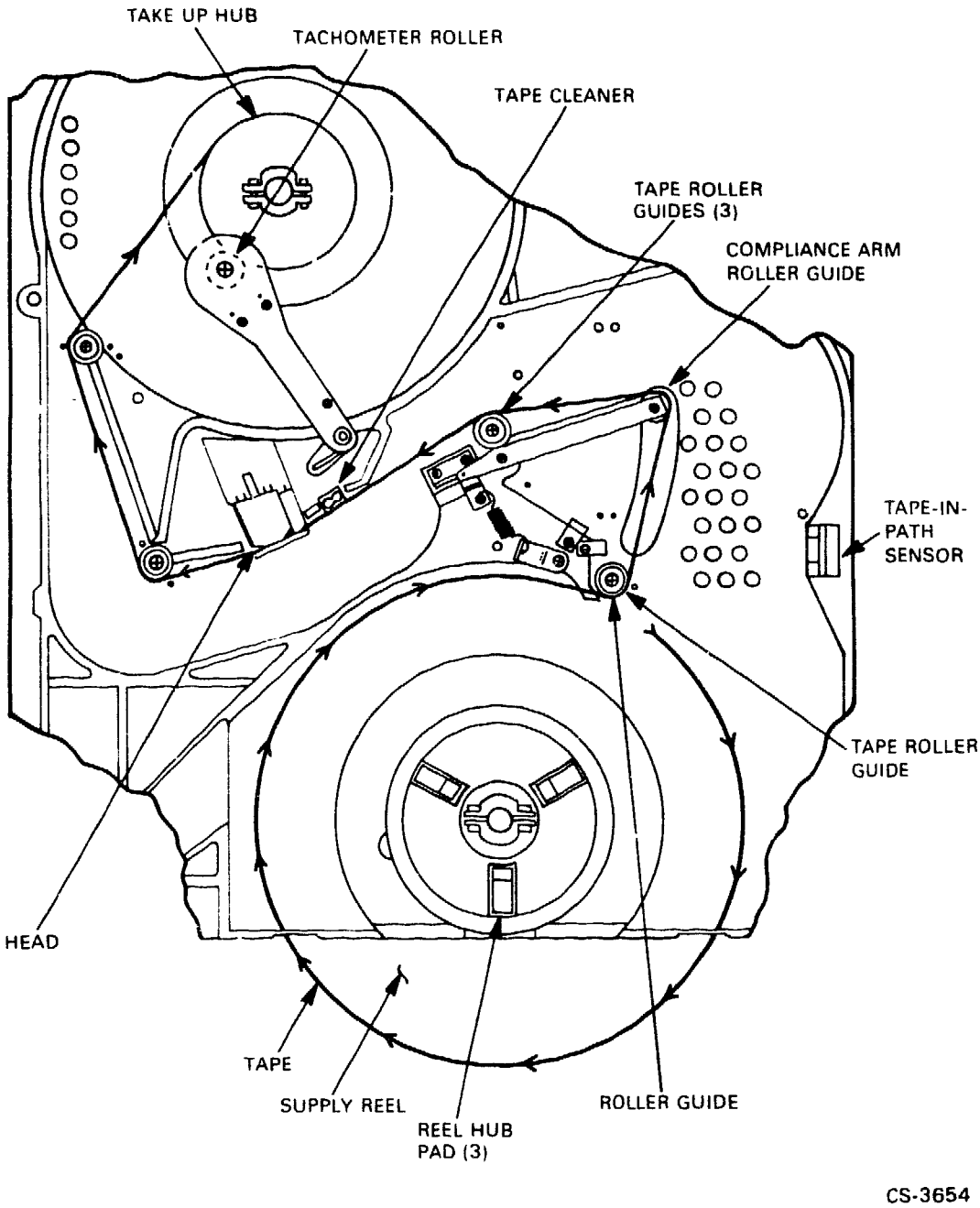
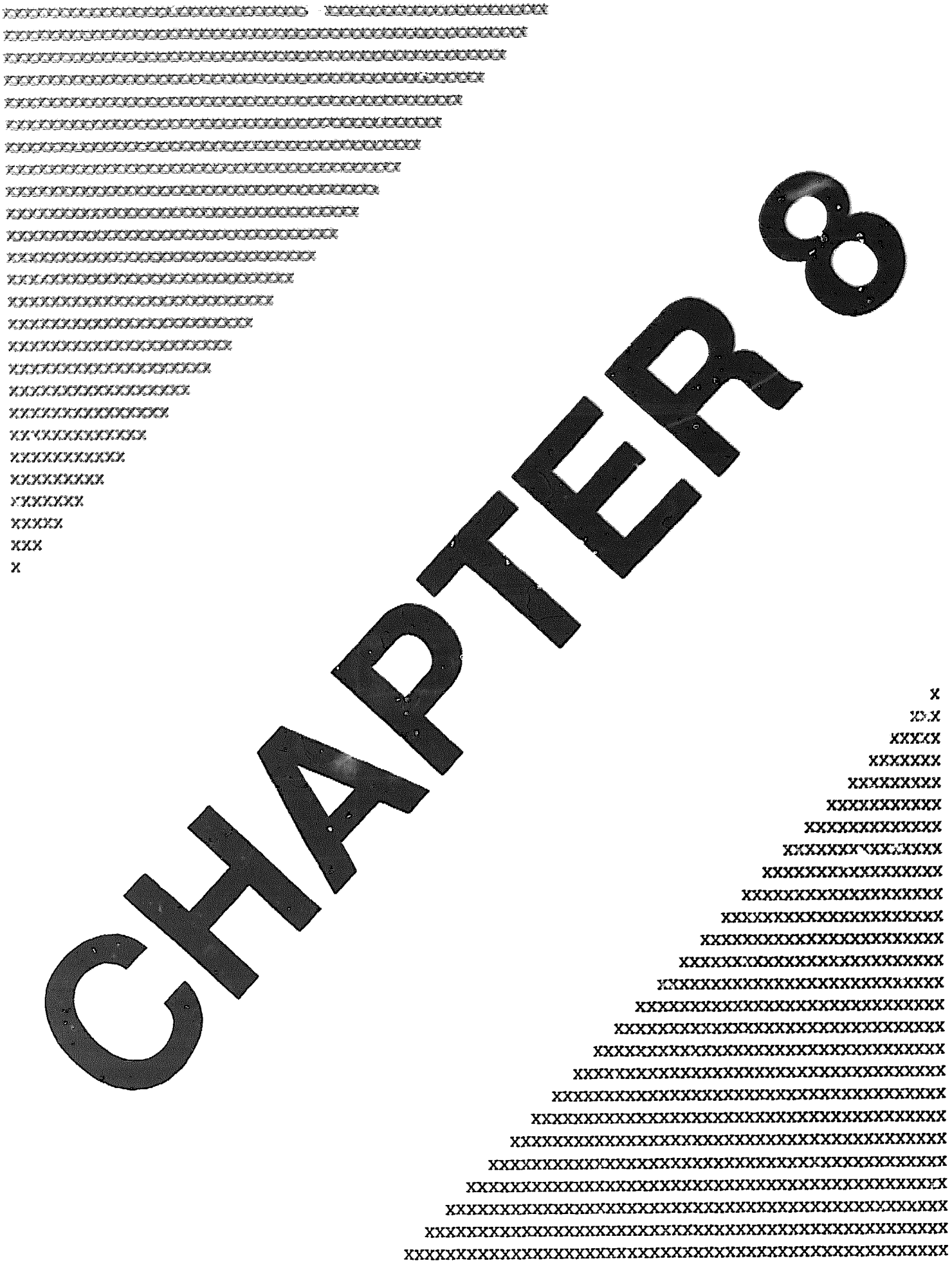


Figure 7-2 Tape Path and Related Parts


CHAPTER 8

CHAPTER 8
TSV05-S TECHNICAL DESCRIPTION

8.1 INTRODUCTION

8.1.1 Scope

This chapter describes the operation of the TSV05 subsystem in details necessary for diagnosing failures at the Field Replaceable Unit (FRU) level. Some aspects of the microprocessor hardware and firmware are described to the device and microcode level, where required for interpreting the results of the self-test diagnostic programs. Generally, however, the descriptions in this chapter are limited to the concept level.

8.1.2 Conventions

The *TSV05 Field Maintenance Print Set* (P/N MP-02347) is referenced in several sections in this chapter. The print set uses the following convention for signal identification:

- SOURCE
- SIGNAL NAME
- POLARITY

SOURCE indicates the print set sheet number on which the signal originates.

SIGNAL NAME is the functional name assigned to the signal. It may be a descriptive term or a mnemonic representation of the signal function.

POLARITY indicates the voltage level of the signal when it is in its TRUE (asserted) state. H indicates that the signal is at +3 volts when asserted, and at 0 volts when negated. Conversely, L indicates that the signal is at 0 volts when asserted, and +3 volts when negated. For example:

D10 MRST L

originates on print set sheet, performs a function that can be represented by the mnemonic MRST (master reset), and is in a logic LOW state (0 volt) when asserted.

The exception to this convention is the naming of bidirectional bus signals. No SOURCE identification appears on bus conductors, because they are asserted or negated from any of several sources.

8.1.3 Terminology

The following terms used in this manual are defined below.

1. Access Time — The time between the issuing of a tape read, write, or space command by the controller, and the reading or writing of the first character in the tape record.
2. BOT Marker — Beginning of Tape marker. This is a reflective strip placed on the tape 5 meters (16 feet) from the beginning of the tape.
3. Command Buffer — An area of contiguous 18-bit words in the host system memory space. I/O request packets are built in the command buffer and retrieved by the TSV05.
4. Command Delay — The elapsed time between the interrupt from the tape controller signifying the completion of an operation (that is, read or write) and the issuing of the next command to the controller by the operating software.
5. Command Packet (I/O Request Packet) — A set of control words issued from the CPU (that is, operating system, I/O driver, or diagnostic program) to the TSV05 to initiate and control operation.
6. Command Pointer — The high (most significant) 20 bits of a 22-bit modulo-4 address that points to a command packet located in memory.
7. Conventional, or Stop/Start, Technology — Operating characteristic of a tape drive that can rapidly accelerate and decelerate tape motion to allow the tape to come to rest with the read/write head positioned in the interrecord gap.
8. EOT Marker — End of Tape marker. This is a reflective strip placed on the tape 7.6 meters (25 feet) from the end of the tape.
9. Auto Speed Control — In this mode of operation, the algorithm in the firmware determines the rate of data transfer from the host to the tape subsystem. Depending on the data transfer rate, it locks the speed of the tape transport at 25 or 100 Inches Per Second (IPS).
10. Header Word — The header word is the first word of a command packet or a message packet.
11. Message Buffer — An area of contiguous words in CPU memory. The message packets are stored there by the TSV05.
12. Message Packet — A group of status words issued from the TSV05 to the CPU to indicate status of the tape transport and/or operation completed.
13. Modulo-4 Address — An address within the CPU memory that is evenly divisible by 4 (that is, octal 0, 4, 10, 14, 20, and so on).

14. Packet Protocol — Method of communication between CPU software and the TSV05 by means of areas in CPU memory, following the rules dictated by TS11/TS04 compatibility requirements. A "packet" is a contiguous series of words residing in CPU memory. The TSV05 accesses a command packet to receive command information, and stores a message packet (in a message buffer area in CPU memory) to provide status information to the software. This technique allows large amounts of information to be passed, while allowing the device to occupy only two hardware I/O addresses.

15. Q-22 — Q-bus containing signal connections for 22-bit addressing capability.

16. Record Buffering — Capability of the TSV05 to store an entire tape record (up to 3584 bytes in length) during read or write command sequences to allow overlapping of reel-to-reel tape repositioning with transfer of data to or from the CPU.

17. Reinstruct Time — The period of time following reading or writing the last character of a record allowed by a tape transport for a controller to issue the next command, in order to avoid slowing or stopping the tape.

18. Repositioning — A characteristic of the TS05 streaming tape drive whereby tape motion is halted and the tape is readied for the next operation by decelerating the tape in its current direction and bringing it to a stop, then accelerating and decelerating the tape in the opposite direction and bringing it to a stop. The tape is not stopped in the gap, as with conventional tape drives.

19. Streaming, or Reel-to-Reel, Technology — Operation of a tape transport without stopping in the interrecord gap. Requires that, for maximum efficiency, commands of similar type, speed, and direction be supplied by the controller within a relatively short "reinstruct" period. The TS05 tape transport operates in this fashion.

20. TSBA — TSV05 Bus Address Register. A read-only hardware register in the I/O address space.

21. TSDB — TSV05 Data Buffer Register. A write-only hardware register in the I/O address space.

22. TSSR — TSV05 Status Register. A read/write register in the I/O address space.

23. XSTn — Extended Status Register n. One of five status registers deposited intc the message buffer area.

8.2 GENERAL DESCRIPTION

The TSV05 Tape Transport Subsystem includes two major components: the M7206 interface/controller module, and the TS05 tape transport unit.

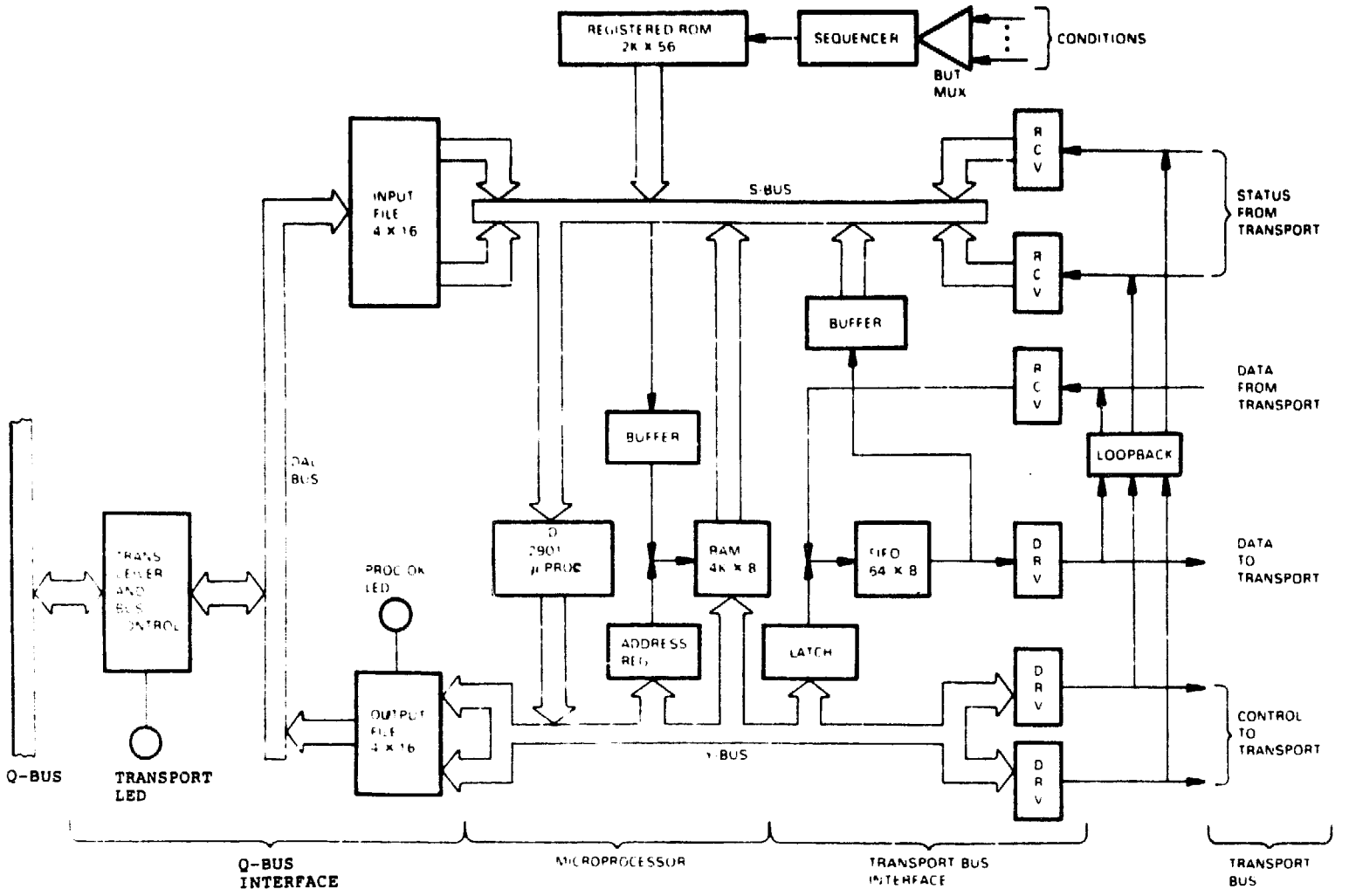
8.2.1 M7206 Q-Bus Interface/Controller Module

The M7206 interface/controller module has three functional areas of circuitry (Figure 8-1):

1. Q-bus Bus Interface
2. Microprocessor
3. Tape Transport Bus Interface

8.2.1.1 Q-Bus Interface - The Q-bus interface includes:

1. Transceivers and Bus Control — This circuitry handles the Q-bus protocol and the movement of addresses and data onto and off of the Q-bus conductor.
2. Input File — The input file contains data written to the M7206 interface/controller module from the host computer over the Q-bus. It includes:
   a. TSV05 data buffer register (TSDB).
   b. High byte of the TSV05 status register (TSSR).
   c. DMA data in register.
3. Output File — The output file contains data to be read by the host computer over the Q-bus. It includes:
   a. TSV05 bus address register (TSBA).
   b. TSV05 status register (TSSR).
   c. DMA data out register.



CS-6007

Figure 8-1 M7206 Q-Bus Interface/Controller Block Diagram

8.2.1.2 Microprocessor - The microprocessor includes:

1. Arithmetic Logic Unit (ALU) — This circuit comprises two 2901 bit slice microprocessor chips, and the associated logic devices necessary for performing the functions instructed by the microwords. The ALU operates on eight bits at a time.
2. S-Bus — The source, or input, bus carries the operands on which the 2901 ALU functions are performed.
3. Y-Bus — The Y, or output, bus carries the results of the ALU functions.
4. Random Access Memory (RAM) — The 4K x 8-bit RAM provides temporary storage area for microprocessor operations and also provides a 3K byte data buffer when the data buffering feature is enabled.
5. Address Register — This is loaded from the Y-Bus as necessary to specify a RAM address.
6. Buffer — This is used when a RAM address is specified by the EMIT field of the microword.
7. ROM — The 2K x 56-bit latched output ROM contains the microinstructions that control the microprocessor.
8. Sequencer and Branch Microtest (BUT) Multiplexer — This set of three 2911 sequencer chips provides 11 microprogram address lines to the ROMs. The BUT multiplexer enables the microprogram to select conditions for testing so as to allow the microprogram to modify the sequence of microinstructions.

8.2.1.3 Tape Transport Bus Interface - The tape transport bus interface includes:

1. First In First Out (FIFO) Register File — The 64 x 8-bit FIFO register file serves as a buffer for all data being transferred to or from the tape transport bus.
2. Latch — Latches are used on the microprocessor output bus for temporary storage of data and control functions.
3. Buffer — During microprocessor read operations, data is taken from the FIFO register file, passed through the buffer, and placed on the microprocessor input bus.
4. Receivers — These devices receive status and data signals from the tape transport bus.
5. Drivers — These devices transmit status and data signals onto the tape transport bus.
6. Loopback Circuitry — The loopback circuitry is used during maintenance diagnostic testing to test the transport bus drivers and receivers.

8.2.2 TS05 Tape Transport Unit

The TS05 tape transport unit has three main functional areas (Figure 8-2):

1. Data Formatter Interface
2. Microprocessor
3. Electromechanical Assemblies

8.2.2.1 Data Formatter Interface - The data formatter interface includes:

- Receivers — These devices receive data and control signals from the tape transport bus.
- Drivers — These devices transmit data and control signals onto the tape transport bus.
- Data Formatter Electronics — Under the control of the tape transport unit microprocessor, the data formatter circuits place data in the proper format on the tape, and reads data off the tape. Binary write data from the tape transport bus is routed directly to the formatter, where it is placed within the required format. The formatter electronics generate the necessary current profile to drive the write head. During read operations, the formatter performs read head amplification, data separation, skew buffering, error detection and, if necessary, error correction.

8.2.2.2 Microprocessor - The microprocessor includes:

1. ALU — A Z80 microprocessor chip performs ALU functions executing instructions stored in ROM.
2. ROM — Microinstructions for the operation of the tape transport unit are contained in the 8K x 8-bit ROM.
3. RAM — The 8 x 258-bit RAM provides temporary storage area for the microprocessor.
4. PIO Ports — The microprocessor uses four PIO ports to control and obtain feedback from the electromechanical assemblies.

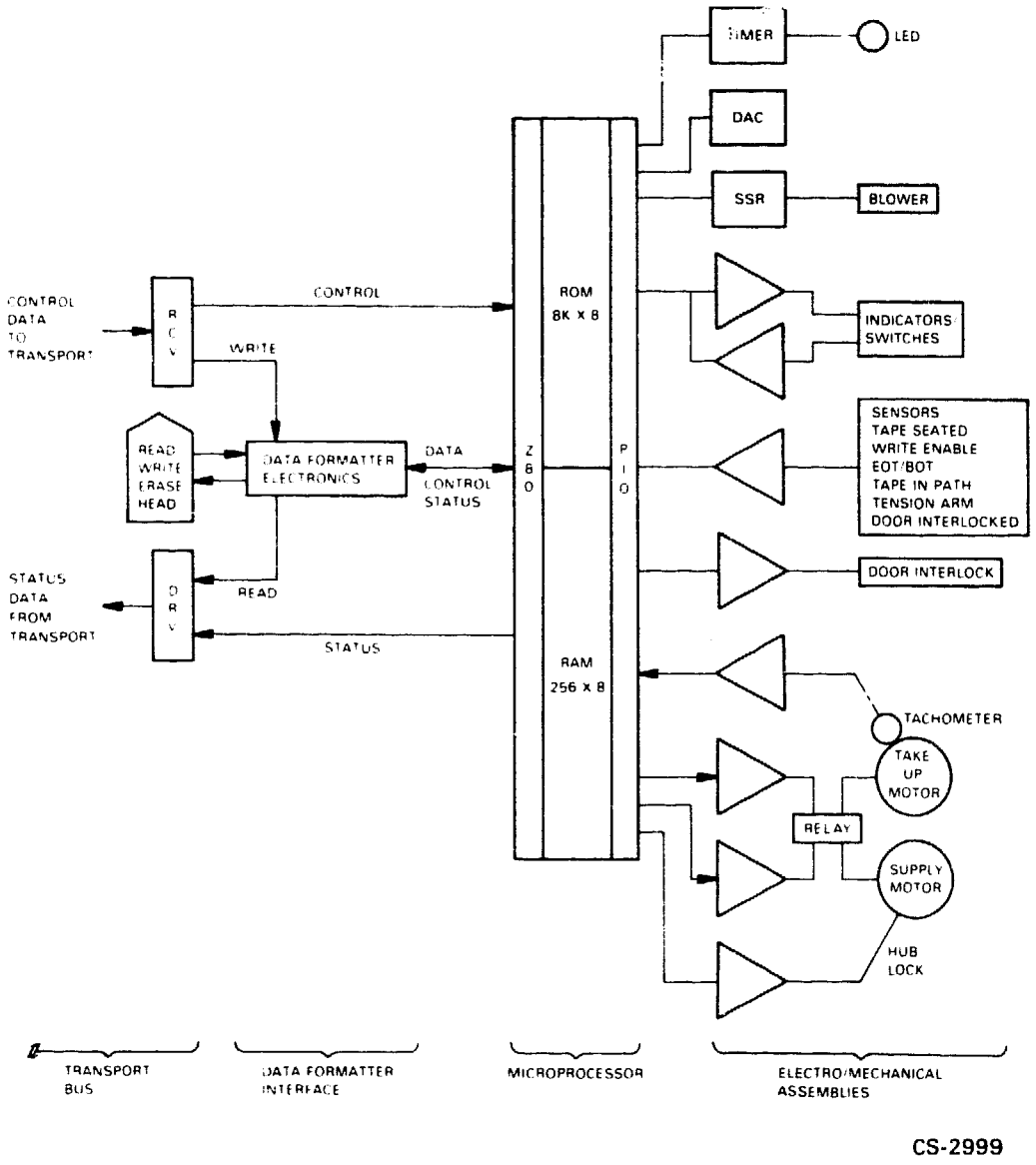


Figure 8-2 TS05 Tape Transport Block Diagram

8.2.2.3 Electromechanical Assemblies - The electromechanical assemblies include:

1. Timer — A watchdog timer is constantly pulsed by the microprocessor. If the microprocessor stops or if the power supply fails, the timer times out. This error condition lights a Light-Emitting Diode (LED) and shuts down the tape transport.
2. Digital-to-Analog Converter — By means of the VOUT signals, this drives the electric devices controlling the movement of the tape.
3. Analog-to-Digital Converter — By means of the VIN signals, this reads sensor voltages.
4. Solid-State Relay and Blower — The blower is turned on and off under the control of a PIO port.
5. Switches and Indicators — The front panel switches and indicators are directly controlled by the PIO port.
6. Sensors — The microprocessor monitors seven sensors:
   a. Tape reel seated
   b. Write enable ring
   c. End of tape photodiode
   d. Beginning of tape photodiode
   e. Tape in path photodiode
   f. Tension arm transducer
   g. Door interlocked
7. Door Interlock — This is a solenoid that locks the tape transport top cover and front door whenever tape is loaded.
8. Tachometer — This high resolution quadrature tachometer indicates tape speed and position.
9. Takeup Motor — The takeup motor moves the tape in the forward direction.
10. Motor Relay — This mechanical relay is closed under normal power ON conditions. If the watchdog timer times out, the relay opens. When this occurs, both the takeup and supply motors receive dynamic braking signals so as to stop the tape motion in a controlled manner.
11. Supply Motor — The supply motor moves the tape in the reverse direction.
12. Hub Lock Solenoid — This is actuated during the load operation to lock the supply reel onto the supply hub.

8.2.3 Major Data Flows

Each time the host computer system writes data to the tape subsystem, the data is both written on the tape and read off the tape. During write operations, the data is read off the tape immediately after it is written, in order to verify correct write operation. The writing and reading of data during a typical write operation proceeds as follows.

1. The host system software builds a command packet in its main memory specifying a write operation, the starting address of the data to be written, and the byte count. It then passes the address of this command packet to the M7206 interface/controller module.
2. The M7206 interface/controller module transfers the command packet from computer memory to its own logic, and identifies the operation to be performed. It then checks the tape transport unit to ensure that it is capable of performing the operation and that no error conditions exist. If the tape transport unit is ready, the controller instructs it to start tape motion.
3. The M7206 interface/controller module initiates a DMA transfer of the write data from computer memory to the controller DMA input file. From the input file, the data becomes available on the S-Bus.
4. The microprocessor takes data from the S-Bus and places it on the Y-Bus. From the Y-Bus, the data is held in a latch until it can be loaded into the FIFO register.
5. The data is loaded into the FIFO register and held for transfer to the tape transport unit.
6. When the tape is up to speed and the proper format characters are written on the tape, the tape transport logic requests the controller module to place data on the transport bus. (Thereinafter, the transport logic continues to request data as necessary to maintain the basic data rate until it is informed by the controller that the last data byte is in the FIFO.)
7. The data formatter electronics takes the data off the transport bus and converts it to the current profile required for driving the write head. The write head places the data on the tape.
8. When the tape being written by the write head reaches the read head, the read head reads the data off the tape and passes it back to the data formatter electronics.
9. The formatter electronics places the data on the transport bus, from which it is transferred to the M7206 interface/controller module for parity checking.
10. After the last byte of data has been written on the tape, the data formatter electronics writes the final format characters on the tape, and then places updated status information on the transport bus.

11. The M7206 interface/controller module recognizes that the tape transport has finished executing the write command, and it updates the message buffer (in the host computer memory) accordingly.

12. The controlling software checks the message buffer and finds that the TSV05 subsystem is ready for another command.

At this moment, the tape transport is still moving tape at the full read/write speed. If the controlling software issues another command of the same type within a short time (the reinstruct time), the TSV05 subsystem executes the command without having to stop and restart the tape. The TSV05 subsystem continues executing a stream of commands ("streaming") until the command type is changed or the reinstruct time is exceeded. Once a tape motion command falls outside the reinstruct time, however, the tape transport performs a tape repositioning cycle and then stops the tape.

8.3 FUNCTIONAL DESCRIPTION

This section describes the operation of the following:

- M7206 Q-Bus Interface/Controller Module
- M7206/TS05 Interface
- Tape Transport Unit

8.3.1 M7206 Q-Bus Interface/Controller Module Operation

The M7206 interface/controller module is compatible with the "MS" software at the device driver level. It uses an 8-bit bit slice microprocessor (200 nanosecond cycle time), 2K words of control store memory (56-bit words), and 4K bytes of RAM. The controller supports 16, 18, or 22 address lines, but not Q-bus parity. The block, or hog mode, DMA feature is not implemented. All critical time-dependent Q-bus register functions are handled in hardware. This relieves the microprocessor for packet protocol handling, buffer management, and tape drive control. The registers include:

1. TSDB (Data Buffer) — A write-only register used to load a command pointer address locating the command packet in host memory.
2. TSBA (Buffer Address) — A read-only register at the same I/O address as the TSDB. The TSBA reflects the main memory address being used by the controller.
3. TSSR (Status Register) — Indicates the status of the last completed command. The following three bits of this register are implemented in hardware.
   a. SSR (Subsystem Ready, <07>) — This bit is set after the controller (subsystem) has written a message buffer to system memory indicating that the controller is ready for a new command. (It is cleared on power up, then set. It is also cleared after the system writes the TSDB.)
   b. RMR (Register Modification Refused, <12>).
      - If the system (host) attempts to write the TSDB when the SSR is cleared, then the RMR bit is set.
      - If the subsystem is to do an attention (it can only do an attention if it controls the message buffer), and SSR has been set for a long period of time, then the subsystem must first clear SSR. If this occurs at the same time the system tries to write the TSDB, then RMR is set.
   c. SC (Special Condition, <15>) — If RMR is set, or if the command was not completed without incident, then the SC bit is set.

The operation of the M7206 interface/controller module is discussed in detail in the sections that follow. Refer to the *TSV05 Field Maintenance Print Set* (MP-02348-01) to identify the devices being discussed.

8.3.1.1 Q-Bus Interface (Sheets D1, D2, and D3) - The Q-bus interface circuitry includes the following.

1. Register Access Control — Access to the Q-bus registers is controlled primarily by a DC004 protocol chip and two Programmable Array Logic (PAL) devices (Table 8-1). Two I/O word registers are used for Q-bus transfers. These are the TSBA with TSDB (read and write), and the TSSR (read only; write resets the subsystem, although a write high byte is allowed by strapping). PAL01 and PAL02 are programmable AND-OR-INVERT gates, programmed to enable the DC005 bus transceivers and Q-bus registers at the proper time. Inputs to the PALs are primarily from the DC003 interrupt chip, the DC010 DMA control chip, and the Q-bus.

2. Q-bus Latch — When the host system performs a write operation to the tape transport subsystem, the exact operation is latched into a 74LS174. This is necessary to distinguish maintenance writes (TSDB high byte or TSDB low byte) from command operations (TSDB word writes).

3. Interrupt Control — The key device controlling interrupts is the DC003 interrupt control chip. The TSV05 subsystem uses only one interrupt. The interrupt is created by clearing and subsequently setting the ENA DAT input of the DC003. This is done under microprocessor control. (The clearing is necessary since the device input is usually still set from the previous interrupt.)

4. DMA Control — DMA transfers are handled by a DC010 control chip, a 74S112, and a 74LS174. A DMA transfer is initiated by loading the Non-Processor Request (NPR) latch and requesting service by means of D11 EMIT 11 H. This is done with OUT BYTE, OUT WORD, or IN WORD. As the transfer is initiated (by D11 EMIT 11 H and D8 NPR ENAB L), D3 NPR BSY H and D3 NPR REQ H are set. The D2 NPR BSY H line remains set until the DMA transfer is complete. As the DMA sequence progresses (under the control of the DC010), addresses and data are stored in the Q-bus access registers (print set Sheet D4). D2 RRPLY H sets and D3 NPR REQ H is cleared. D3 NPR BSY H is cleared as a result of D2 RRPLY H being negated, and the DMA cycle is complete.

   If, however, D3 XSYNC H (DC010 SYNC) is asserted for more than 12 microseconds, the NPR abort timer aborts the DMA transfer.

   During the DMA transfer cycle, all address and data register selection is performed by the two PALs.

5. SSR Interlock — For purposes of software compatibility, the microprocessor emulates the TS11 tape transport subsystem at the Q-bus interface. In order to offload some of this task from the microprocessor, three real-time bits in the TSSR are handled by the hardware. These are SSR, RMR, and SC. This hardware performs the following functions:

   a. Sets the RMR and SC bits to indicate an error if the host system writes the TSDB when the SSR bit is cleared. (Writes to the TSDB are not allowed when SSR is in the cleared state.)

   b. Clears SSR and RMR if the host system writes the TSDB while SSR is set.

   c. Sets D2 Q WRT H when the host system writes to the TSV05 subsystem. This is used by the microprocessor to ensure the correct states of SSR and RMR in the event of the host system and the microprocessor attempting to modify the SSR bit simultaneously.

   These three status bits are placed on the DAL lines (by way of the 74LS244 in location E51) under the control of the PALs.

6. Address Bit Logic — Address bits <21:16> are latched (in AM2908s in E38 and E37) and used to drive the Q-bus directly. These bits are used in conjunction with address bits <15:00> (which are stored in the register file) for the address of DMA transfers.

Table 8-1 PAL Maps

PAL 01 (Location E32)

Output	Input
~D1 QRA H =	~D1 SELO L + D2 ADREN H
~D1 QRB H =	~D1 SELO L + ~D1 SEL2 L + D2 ADREN H
~D1 QWA H =	~D1 SELO L
~D1 QWB H =	~D1 SELO L + ~D1 SEL2 L
~D1 PMRST L =	~D1 SEL2 L * ~D1 OUTLB L + D1 RINIT H
~D1 RCV H =	~D2 XDIN H * D1 OUTHB L * D1 OUTLB L * D1 RSYNC L +
	~D2 XDIN H * D1 SELO L * D1 SEL2 L * D1 RSYNC L +
	~D2 XDIN H * D1 OUTHB L * D1 OUTLB L * D2 ADREN H +
	~D2 XDIN H * D1 SELO L * D1 SEL2 L * D2 ADREN H
~D1 XMIT H =	~D2 DATEN L * ~D2 ADREN H * D1 INWD L +
	~D2 DATEN L * ~D2 ADREN H * D1 SELO L * D1 SEL2 L

PAL 02 (Location E31)

Output	Input
~D1 QGWHB L =	D2 SSR H * ~D1 OUTHB L * ~D1 SELO L +
	D2 SSR H * ~D1 OUTHB L * ~D1 SEL2 L + D2 XDIN H
~D1 QGWLB L =	D2 SSR H * ~D1 OUTLB L * ~D1 SELO L +
	D2 SSR H * ~D1 OUTLB L * ~D1 SEL2 L + D2 XDIN H
~D1 WTBT H =	~D2 OUT H * D2 BYT L + ~D2 OUT H * D2 DATEN L
~D2 ADREN H *	D2 BYT L + ~D2 ADREN H * D2 DATEN L
~D1 RDSTATQ L =	~D1 SEL2 L * ~D1 INWD L
~D1 RDREGQ L =	~D1 SELO L * ~D1 INWD L + D2 ADREN H + ~D2 DATEN L
~D1 WRTTSDB H =	D1 SELO L + D1 OUTHB L * D1 OUTLB L
~D1 BUSWRT H =	D1 OUTLB L * D1 OUTHB L + D2 SELO L * D1 SEL2 L

NOTE

PAL01 pin 18 (D2 RINIT H) and PAL02 pin 14 (D3 SSR H) are used as inputs. PAL01 pin 11 (D1 Mux 1 H) is not used. PAL16L8 devices, as shown in the above maps, define outputs as the not TRUE, that is, LOW driven, states.

8.3.1.2 CSR and Data Memory (Sheet D8) - The CSR and data memory circuitry includes the following:

1. Q-bus Access Registers — Control, status, and data transactions between the Q-bus and the tape transport subsystem are performed using the 74LS670 4-bit x 4-word register files. The registers shown on the right side of print set Sheet D3 hold all the TSV05-to-Q-bus data and the DMA address <15:00>. The registers shown in the middle hold TSV05-to-Q-bus data. Both sets of registers have independent address, read, and write controls. This allows them to be read and written independently, with no contention problems between the Q-bus and the microprocessor.

   Register selection is as follows:

   a. TSV05-to-Q-bus

      00 TSBA and DMA address IN or OUT <15:00>

      01 TSSR <15:00>

      10 Not used

      11 DMA data out <15:00>

   b. Q-bus-to-TSV05

      00 TSDB <15:00>

      01 TSSR <15:08> (See note)

      10 Not used

      11 DMA data in <15:00>

NOTE

A write low byte or write word from the Q-bus to the TSSR causes a master reset to the TSV05 subsystem. A write to the high byte of the TSSR does not cause a master reset. This register contains the boot bit and, if the EXTENDED FEATURES switch is ON, bits <18:21> of the TSDB.

2. RAM (55 nanosecond) — Two 4K by 4-bit RAMs are used for data memory. The inputs are from the Y-Bus and the outputs are to the S-Bus. The RAMs can be addressed from either the 12-bit EMIT field or the 12-bit address latch. A RAM read occurs during the entire 200 nanosecond microcycle. A RAM write occurs during the last 100 nanoseconds of the microcycle.

3. RAM Address Latch (74LS374, 74S241) — The address for the RAM are from either the 74LS374s or the 74S241s. The 74LS374s are loaded from the microprocessor Y-Bus. (Two load's are required to update all 12 bits.) The 74S241s are used to directly address the RAM from the current operating microinstruction.

8.3.1.3 Tape Unit Interface (Sheet D7) - The tape unit interface includes the following circuitry:

1. Tape Format and Control Out — This circuit comprises 74LS374 latches that hold the tape drive commands and associated latches.

2. Tape Data FIFO — The tape data FIFO is a 64 x 8-bit register having a 5 megahertz shift in shift out rate and a 4 microsecond fall-through time. The direction of tape data flow is determined by D3 SEL OUT H. Data is transferred to the tape as follows:

   a. The tape data in buffer '244) is disabled and the 74LS374 is enabled to supply data from t microprocessor. Tape data from the microprocessor is loaded into the 74LS374 on the second 100 nanoseconds of D10 T DAT OUT L. The pulse on D10 T DAT OUT L is delayed by one subsystem clock pulse (through 74S74) and then gated with D9 PSCLK L to produce a 100 nanosecond pulse that occurs during the second half of the subsystem clock period. This pulse is used to strobe data into the FIFO.

      The microprocessor uses D7 IN RDY L to monitor the input ready state of the FIFO.

   b. When the data reaches the bottom of the FIFO, D7 OUT RDY L asserts and indicates to the microprocessor that data is ready. The microprocessor then asserts D10 T DAT IN H to shift one byte of data into the tape data out register.

   c. The tape unit asserts D12 IWSTR each time it takes data. The FIFO is monitored for the presence of data. The empty state of the FIFO is indicated by D7 DAT OUT MISS H. If the FIFO becomes empty, D7 DAT OUT MISS H asserts and ILW (last word indicator) to the tape unit is set. If D7 OUT RDY L and D7 DAT OUT MISS H are true simultaneously, an error condition exists because ILW is sent to the tape unit even though there is still data in the FIFO. In this case, the entire buffer must be written to the tape again.

   d. The parity of the tape data out is monitored by a 74LS280. A parity bit (D7 IWP) is generated and sent to the tape unit.

   e. The parity of the tape data in is monitored by a 74LS280 and a 74LS112. A parity error is flagged by D7 PAR IN H.

3. Data is transferred from the tape as follows:

   a. The 74LS244 is enabled and the 74LS374 is disabled. D12 IRSTR from the tape unit indicates that data from the tape is ready. Its positive edge occurs 200 nanoseconds after the data is sent from the tape unit. This signal is delayed another 200 nanoseconds, then used to strobe data into the FIFO and latch any parity error from the 74LS280.

   b. When data reaches the bottom of the FIFO, D7 OUT RDY L is asserted, indicating that data is ready to be taken out of the FIFO.

   c. If the FIFO becomes full, D7 DAT IN MISS H is asserted on that D12 IRSTR.

   d. The microprocessor clears the FIFO by asserting D7 FRST L.

8.3.1.4 Program Sequencer and Tape Status In (Sheet D8) - The program sequencer and tape status in circuitry includes the following:

1. Tape Status In Logic — Tape status from the tape unit status lines is latched into 74LS34s at the subsystem clock rate. The 74LS34s are reset by the microprocessor using D4 T STAT RST L.

2. Program Sequencer — Three 2911s generate an 11-bit address (2K words) that sequences through the microinstruction ROMs. The 2911s can select an address from any of four sources.

   a. The EMIT field of the microinstruction. This is typically the branch address taken if a given condition is met as selected from the BUT multiplexer.

   b. An internal register holding an address from a previous EMIT field.

   c. An internal push/pop stack including control lines for nested subroutine linkages.

   d. An internal program counter. This usually contains the last address plus one.

   These 2911s are controlled directly by the microinstruction using D11 RO FE H, D11 RO SQ 1 H, D11 RO SQ 0 H and D11 RO D7 TEST INV H. Testing for conditional branching is supplied from the BUT multiplexer.

3. BUT Multiplexer — The BUT multiplexer is a condition code multiplexer that selects one of 23 conditions for the 2911 program sequencer. The selected output is first synchronized to the subsystem clock by a 74S74. The actual test selection is from the BUT field of the microinstruction.

8.3.1.5 Arithmetic Logic Unit (Sheet D9) - The ALU and its associated circuitry include the following devices:

1. 2901s — Two 2901 chips form the ALU and its 16 8-bit registers.

2. Subsystem Timing — A subsystem clock is produced by dividing the output of a 20 megahertz oscillator down to 5 megahertz. This goes to a timer and to other components. It also generates D9 DIS BUS L. This is a negative-going 25 nanosecond pulse, the leading edge of which coincides with the positive-going edge of D9 S CLK H (the subsystem clock). D6 DIS BUS L is used to disable all S-bus drivers for 25 nanoseconds before any of the drivers are given control. This prevents bus contention problems.

3. Timer — The 5 megahertz clock from the system timing circuit is divided by 256 to produce D9 TIMER A H. This in turn is divided by two to produce D9 TIMER B H. These signals are used by the microprocessor for timing the duration of functions (for example, for computing the length of tape passed).

8.3.1.6 Microprogram ROMs (Sheet D11) - Microprocessor instructions are contained in 56-bit words stored in a control store circuit. The control store comprises seven 2K x 8-bit ROMs. The ROMs are addressed by the 2911 program sequencer. This register allows the sequencer to look up the next instruction while the current instruction is being executed. For a description of the words, refer to Section 8.3.1.8.

8.3.1.7 Loopback Registers (Sheet D4) - Three 74LS244s perform the transport bus loopback function at the connectors, permitting board testing without the need for external loopback connectors.

8.3.1.8 Microprocessor Words - At the assembly level, the M7206 56-bit microinstructions are made up of four types of words.

1. Word 0 — ALU operations. This word occupies ROMs E95 and E101.
2. Word 1 — Register definitions and S-bus and Y-bus control. This word occupies ROMs E96 and E97.
3. Word 2 — Sequencer control and test selection. This word occupies ROMs E100 and E99.
4. Word 3 — EMIT field and Q-bus and strobe control fields. This word occupies ROMs E98 and E99.

The functions of these words are summarized in Figures 8-3 through 8-6 and Tables 8-2 through 8-5.

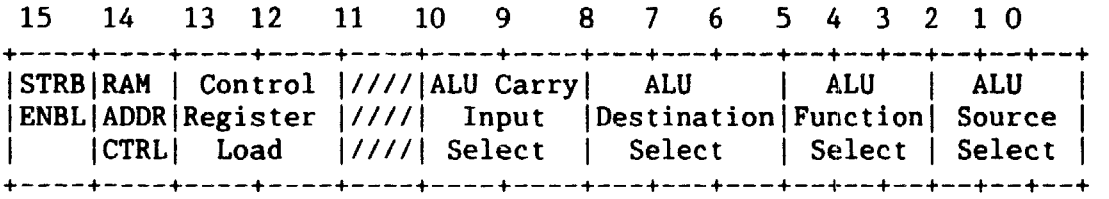


Figure 8-3 Word 0

Table 8-2 Word 0 - ALU Operations

ALU Source: [Bits (2:0)]

Decoded Operation Code	ALU Source Operands R	S
0	A	Q
1	A	B
2	0	Q
3	0	B
4	0	A
5	D	A
6	D	Q
7	D	0

ALU Function: [Bits (5:3)]

Decoded Operation Code	ALU Function
0	R Plus S
1	S Minus R
2	R Minus S
3	R Inclusive-OR S
4	R and S
5	Not-R AND S
6	R Exclusive-OR S
7	R Exclusive-NOR S (Equivalence)

ALU Destination: [Bits (8:6)]

Decoded Destination Code	RAM Shift	RAM Load	Q-Res Shift	Q-Res Load	Y Output
0	X	None	None	F > G	F
1	X	None	X	None	F
2	None	F > B	X	None	A
3	None	F > B	X	None	F
4	Down	F/2 >B	Down	Q/2 >Q	F
5	Down	F/2 >B	X	None	F
6	Up	2F > B	Up	2Q > Q	F
7	Up	2F > B	X	None	F

Table 8-2 Word 0 - ALU Operations (Cont)

ALU Carry Input Select: [Bits (10:9)]

Decoded Operation Code	Carry Input
0	0 (LOW)
1	1 (HIGH)
2	Saved Carry-Out from Previous Cycle
3	Complement of Carry-Out from Previous Cycle

Bit 11 D8 RO 2911 EMIT H is not used.

Control Register Load Select: [Bits (13:12)]

Decoded Operation Code	Register Load
0	No Load
1	Tape Command Out (from Y-Bus)
2	Tape Control Out (from Y-Bus)
3	DMA Enable and Control

RAM Address Control: [Bit 14]

Bit 14 = 0	RAM Address Supplied from EMIT
Bit 14 = 1	RAM Address Supplied from Y-Bus

Strobe Enable: [Bit 15]

When set (in a symbolic microinstruction), enables code in EMIT (10:8) to produce one of eight strobe pulses. In the hardware, the strobe is enabled by a LOW (0) signal.

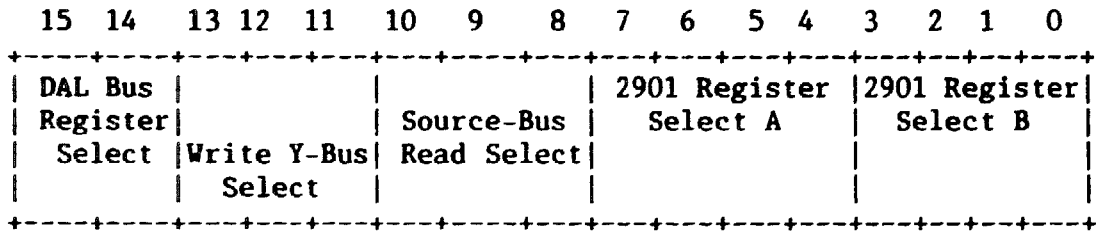


Figure 8-4 Word 1

Table 8-3 Word 1 - Register Definitions, S- and Y-Bus Control

Register Select: [Bits (7:0)]

The 2901 contains a 16 word dual-ported register RAM. These two groups of select bits enable one of 16 words for access.

NOTE

If both Read from RAM and Write to RAM are selected simultaneously, the Write to RAM takes precedence; data read from RAM (onto the S-Bus) is unpredictable.

SRC Bus Select: [Bits (10:8)]

Decoded Operation Code	SRC Bus Data Source
0	
1	RAM
2	FIFO (Tape Data In)
3	Tape Status 2 In
4	Tape Status 1 In
5	EMIT (7:0) (Literal Data)
6	DAL Bus Register (In-File) High Byte
7	DAL Bus Register (In-file) Low Byte

(Note that SRC code 0 is not used.)

Y-Bus Register Write: [Bits (13:11)]

(Data from the 2901 is written into the register selected by the following code.)

Decoded Operation Code	Register Written
0	NO-OP (No Register Loaded)
1	RAM
2	FIFO (Tape Data Out)
3	Extended DMA Address (Bits 18-21)
4	Memory (RAM) Address Register High Byte
5	Memory (RAM) Address Register Low Byte
6	DAL Bus Register (Out-File) High Byte
7	DAL Bus Register (Out-File) Low Byte

DAL-Bus Register (In-File and Out-File) Select: [Bits (15:14)]

Selects a 18-bit register in the input file for Reading and/or a 18-bit register in the output file for Writing.

Table 8-3 Word 1 - Register Definitions, S- and Y-Bus Control (Cont)

Assignments for Writing from Y-Bus:

Decoded Operation Code	Register Selected
0	TSBA and DMA Address
1	TSSR
2	2 is Not Used
3	DMA Data Out

Assignments for Reading onto S-Bus:

Operation Code	Register Selected
0	TSDB
1	TSSR
2	Not Used
3	DMA Data In

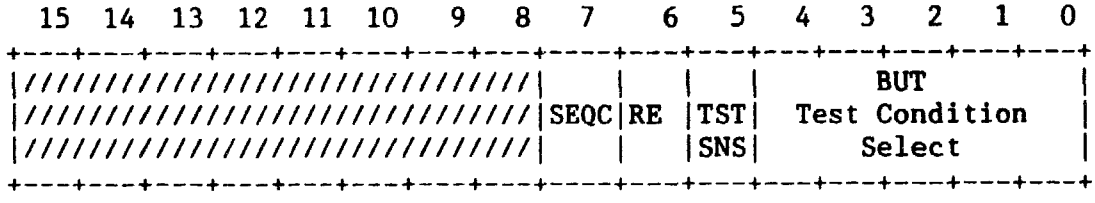


Figure 8-5 Word 2

Table 8-4 Word 2 - Sequencer Control and Test Select

Sequence Control [Bits (7:5)]

Bit 7 = Enables BUT test condition to effect sequencer operation. If the BUT condition is not met, the next microword is executed.

Bit 6 = Enables EMIT data into the internal address holding register.

Bit 5 = Inverts the conditional test, BUT, polarity.

BUT [Bits (4:0)]

Selects the condition to be tested to affect sequencer operation.

BUT Code	Signal	
SW0H	Switch 0 (E58-9)	ON (Extended Features Enable)
SW1H	Switch 1 (E58-8)	ON (Buffering Enable)
MRSTL	D7 MRST L	(Master RESET)
OVRH	D6 OVR H	(2901 ALU Arithmetic Overflow)
F7H	D6 F07 H	(Most-Significant Bit of 2901 ALU Output)
COUTH	D6 COUT H	(2901 ALU Carry-Out)
FEQ0	D6 F=0 H	(2901 ALU Output is 0)
TIMAH	D6 TIMER A H	(51.2 second Timer)
TIMBH	D6 TIMER A H	(102.4 second Timer)
SEL0L	D1 SEL 0 L	(Bus Access to TSDB/TSBA)
SEL2H	D1 SEL 2 H	(Bus Access to TSSR)
OUTLBL	D1 OUT LB L	(Bus Write into Low Byte)
OUTHBL	D1 OUT HB L	(Bus Write into High Byte)
QBWRTH	D1 QWRT H	(Flag Indicating TSDB Written)
DSEL2H	D1 SEL 2 H	(Previous Write was done to TSSRH)
SSRH	D2 SSR H	(Subsystem Ready Bit)
RMRH	D2 RMR H	(Register Modification Refused Bit)
NBSYH	D2 NPR BSY H	(NPR Busy - In Progress)
NXMH	D2 NPR ABORT H	(NXM Timer Timed Out)
ORDYL	D4 OUT RDY L	(FIFO Output Has Data)
MISSH	D4 DATA IN MISS H	(FIFO Input Overrun)
IRDYL	D4 IN RDY L	(FIFO Input Ready)
ILWL	D9 ILW L	(Last-Word Signal on Transport Bus - Should be Complement of MISSH)

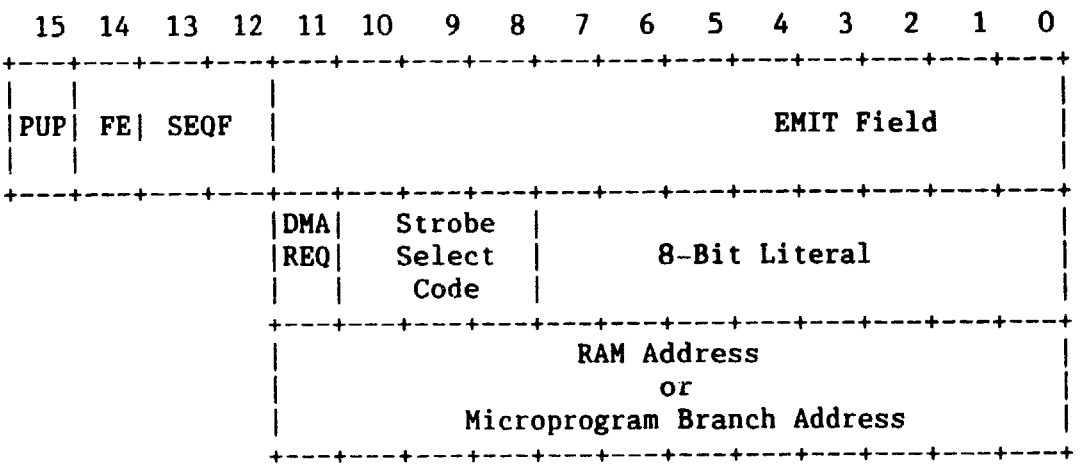


Figure 8-6 Word 3

Table 8-5 Word 3 - EMIT Field[1], Q-Bus and Strobe Control Fields

Control Bits	EMIT Function

Sequence Control [Bits (15:12)]

Bit 15 = 0 will pop, 1 will push data onto the stack if enabled.

Bit 14 = 1 will enable the push/pop function as determined by bit 11.

Bits 13:12 are decoded to determine the sequencer microaddress source.

0 = Program counter
1 = Address holding register
2 = Top of the push/pop stack
3 = Direct inputs, EMIT field

Word 0, Bit 14 — EMIT bits [11:0] represent a RAM address.

Word 2, Bit 06 Bits 9:8 — EMIT bits [11:0] represent a microprogram and branch address that is loaded into the sequencer.

Word 1, Bits 10:8 — EMIT bits [7:0] represent a literal data value typically used for masking during comparison commands.

Word 0, Bit 15 — EMIT bits [10:8] are decoded to make up eight strobe pulses.

Decoded Value	Strobe Pulse
0	Tape status reset
1	FIFO reset
2	Timer reset
3	Clear Q-Bus latch (TSDB written flag)
4	Set RMR flag
5	Clear RMR flag
6	Set SSR flag
7	Clear SSR flag

Word 0, Bits 13, 12 EMIT bit 11 initiates a DMA request sequence.

[1] The EMIT field represents a variable data word whose value is dependent on other control bits within the microword.

8.3.1.9 Microprocessor Chip Description - The M7206 interface/controller module uses three 2911 chips and two 2901 chips for its microprocessor.

2911

The 2911 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in PROM. In the TSV05 controller, three 2911s are interconnected to generate a 12-bit address (4096 words). Eleven bits of the address are used to address 2048 words.

The 2911 can select an address from any of four sources.

1. A set of external direct inputs.
2. Data from the D inputs stored in an internal register.
3. A four-word deep push/pop stack.
4. A program counter register (which usually contains the last address plus one).

The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. The outputs are three-state. A separate line can be used to force all outputs to zeros.

The 2911 signals are defined in Table 8-6.

Table 8-6 2911 Signal Definitions

Signal Name	Description
S0-1	Address source selection control lines. These lines are decoded as follows.

S1	S0	Y0-3 output source
L	L	Microprogram counter
L	H	Address/holding register
H	L	Push/pop stack
H	H	D0-3 direct inputs

FE-PUP — Push/pop stack control lines. These lines are decoded as follows.

FE	PUP	Push/pop stack change
H	X	No change
L	H	Increment stack pointer, then push current PC onto stack
L	L	Pop stack (decrement stack pointer)

RE	Internal address holding register enable line.
Z	Disables output lines Y0-3. Resets the microaddress to zero.
OE	Enables the output lines Y0-3; always TRUE.
CI	Carries input to the next stage.
D0-3	Direct data inputs.
CLK	Clock input.
Y0-3	Microaddress output lines.
CO	Carries output to the next stage.

2901

This is a 4-bit bipolar microprocessor slice designed as a high-speed cascadable element. Two such slices are cascaded together in the TSV05 controller, forming an 8-bit microprocessor data path.

The device consists of a 18-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding, and multiplexing circuitry. The 9-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable (the TSV05 controller cascades two with ripple carry), has three-state outputs, and provides various status flag outputs from the ALU. The 2901 signals are defined in Table 8-7.

Table 8-7 2901 Signal Definitions

Signal Name	Description
A0-3	The first of four address inputs to the register RAM used to select one register whose contents are displayed through an internal port.
B0-3	The second of four address inputs to the register RAM used to select one register whose contents are displayed through an internal port, and into which new data is written when the clock goes LOW.
I0-8	The nine instruction control lines. Used to determine what data sources are applied to the ALU, what function the ALU performs, and what data is deposited in the Q-register or the register RAM.
Q3 RAM3	A shift line at the MSB of the Q-register (Q3) and the register RAM (RAM3). Electrically, these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code indicates an up shift, the three-state outputs are enabled and the MSB of the Q-register is available on the Q3 pin and the MSB of the ALU output is available on the RAM3 pin. Otherwise, the three-state outputs are OFF (high impedance), and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q-register and the RAM.
Q0 RAM0	Shift lines like Q3 and RAM3, but at the LSB of the Q-register and RAM. These pins are tied to the Q3 and RAM3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q-register and ALU data.
D0-3	Direct data inputs. A 4-bit data field that can be selected as one of the ALU data sources for entering data into the device. D0 is the LSB.
Y0-3	The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register RAM, as determined by the destination code.
$\overline{OE}$	Output enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic 2's complement operation has overflowed into the sign bit.

Table 8-7 2901 Signal Definitions (Cont)

Signal Name	Description
F = 0	This is an open collector output that goes HIGH (OFF) if the data on the four ALU outputs F0-3 are all LOW. In positive logic, it indicates the result of an ALU operation is zero.
FE	The most significant ALU output bit.
CIN	The carry-in to the internal ALU.
COUT	The carry-out of the internal ALU.
CP	The clock input. The Q-register and register RAM outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM that compromises the "master" latches of the register RAM. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register RAM.

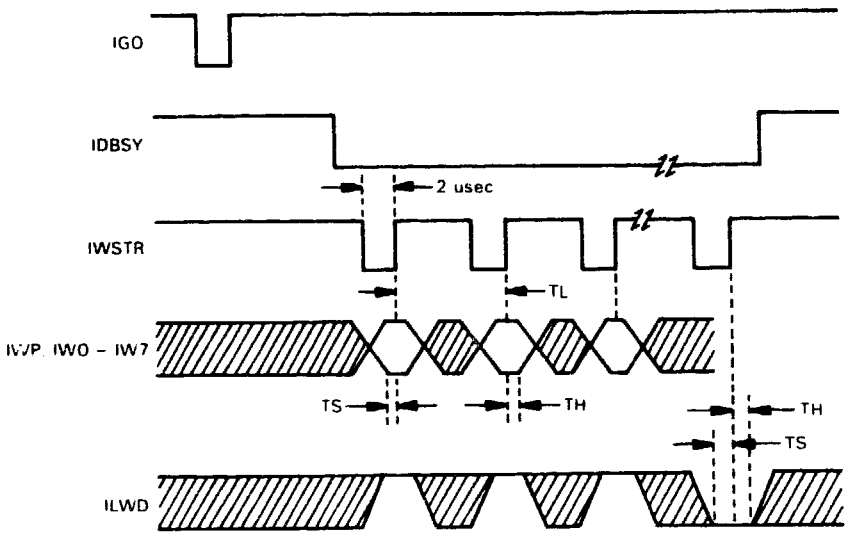
8.3.2 M7206/TS05 Interface

The M7206 interface/controller module connects to the TS05 tape transport unit with two 50-conductor cables. Electrically, these cables form a bus over which the two components communicate. The signal lines are terminated by 220/330 ohm resistor networks and carry standard TTL level signals. All interface signals are active LOW (0 volt = TRUE) unless specified otherwise in the descriptions that follow.

8.3.2.1 Interface to Tape Unit - Pin assignments and names of signals sent to the tape transport from the M7206 interface/controller module are listed in Table 8-8. All interface signal names begin with "I". Signal timing is indicated in Figures 8-7 through 8-9. The functions of the signals are as follows.

Table 8-8 Interface Signals to Tape Transport Unit

Plug No.	Live Pin	Ground Pin	Signal Description	Signal Name
P1	4	3	Last Word	ILWD
P1	6	5	Write Data 4	IW4
P1	8	7	Initiate Command	IGO
P1	10	9	Write Data 0	IWO
P1	12	11	Write Data 1	IW1
P1	16	15	Reserved	-
P1	18	17	Reverse	IREV
P1	20	19	Rewind	IREW
P1	22	21	Write Data Parity	IWP
P1	24	23	Write Data 7	IW7
P1	26	25	Write Data 3	IW3
P1	28	27	Write Data 6	IW6
P1	30	29	Write Data 2	IW2
P1	32	31	Write Data 5	IW5
P1	34	33	Write	IWRT
P1	36	35	Reserved	-
P1	38	37	Edit	IEDIT
P1	40	39	Erase	IERASE
P1	42	41	Write File Mark	IWFM
P1	14	13	Reserved	-
P1	46	45	Transport Address 0	ITADO
P2	18	17	Formatter Enable	IFEN
P2	24	23	Rewind/Unload	IRWU
P2	46	45	Transport Address 1	ITAD1
P2	48	47	Formatter Address	IFAD
P2	50	49	High-Speed Select	IHISP



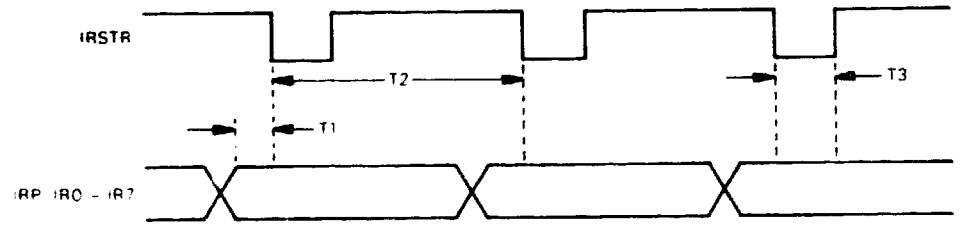
TS = 300 NANOSECONDS (MINIMUM)

TH = 0 NANOSECOND (MINIMUM)

TL = 25.00 MICROSECONDS @ 25 IPS
= 6.25 MICROSECONDS @ 100 IPS

CS-3000

Figure 8-7 Write Strobe Timing



T1 (MINIMUM) = 100 NANOSECONDS

T2 (MINIMUM) = 3.5 MICROSECONDS @ 100 IPS
= 14 MICROSECONDS @ 25 IPS

T2 (AVERAGE) = 6 MICROSECONDS @ 100 IPS
= 25 MICROSECONDS @ 25 IPS

T3 (NOMINAL) = 1 MICROSECOND

CS-3001

Figure 8-8 Read Strobe Timing

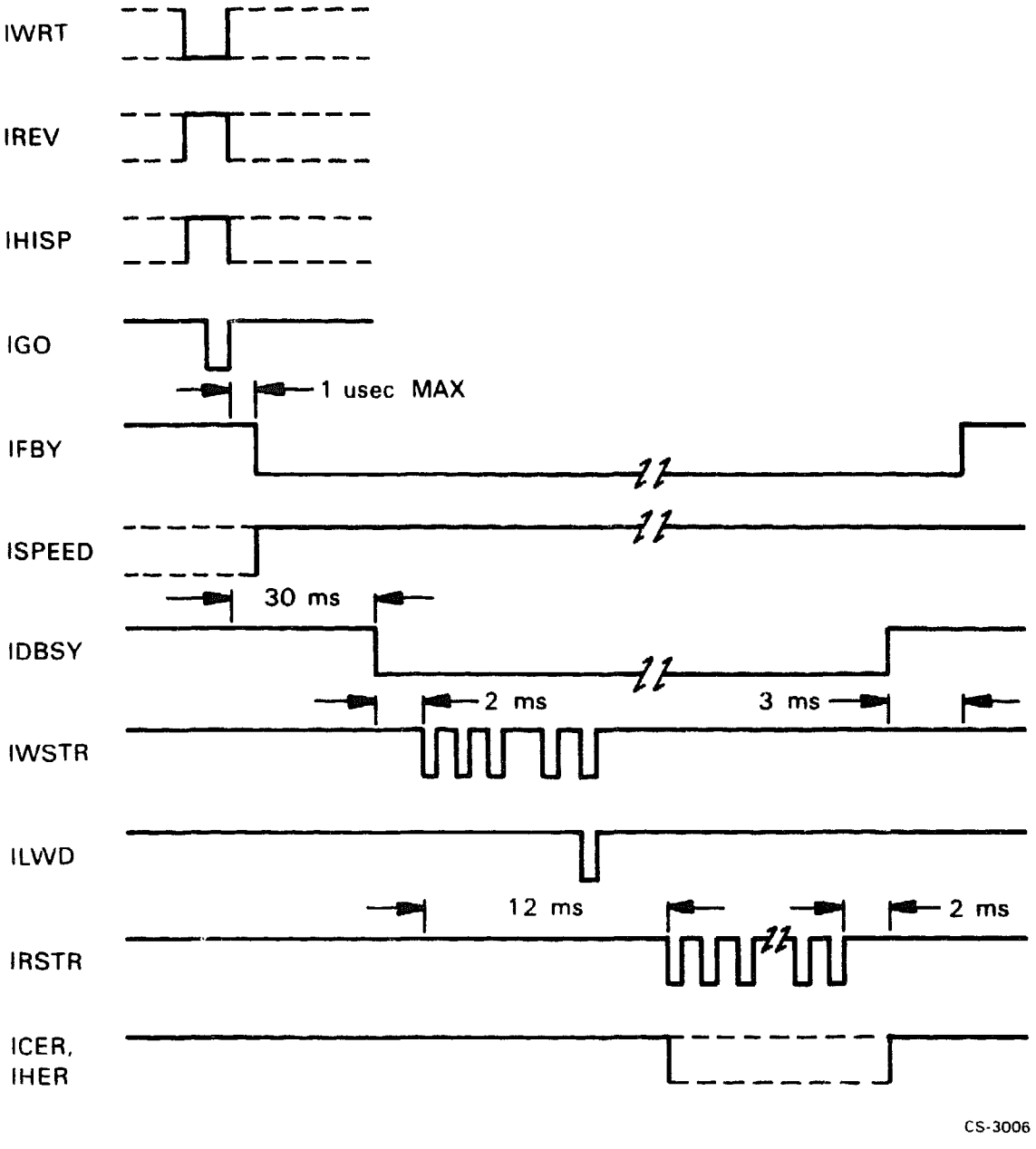


Figure 8-9 Write Forward [64 cm/s (25 in/s)]

IGO

This is a pulse of 1 microsecond minimum duration. The trailing edge initiates tape motion of the selected ready tape drive and latches the command into the formatter register. The commands are initiated by this pulse. The formatter address lines must be held constant from the leading edge of IGO until IFBY is negated.

IREW

A pulse of 1 microsecond minimum duration initiates a rewind in the selected ready (not at load point) tape drive. If the selected tape drive is at load point, the command is ignored. The rewind command does not use IFBY or IDBY. The IRWD status asserts within less than 1 microsecond, while IRDY is negated. A new command to this drive is delayed until the status IRDY is TRUE and IRWD is FALSE. The physical operation of a rewind involves running at 25 inches/second for about 51 centimeters (20 inches) in the forward direction before the reverse motion occurs. The drive runs reverse with the fastest reel motor near the microprocessor-controlled maximum speed. When the tape reaches BOT, the drive ramps down and returns to BOT where it stops, setting IBOT and IRDY, and resetting the IRWD status.

IRWU

This is a pulse of 1 microsecond minimum duration that:

1. Clears the ON-LINE flip-flop.
2. Generates a rewind.
3. Unloads the tape and unlocks the door.

The tape unit indicates IRDY and IONL are FALSE within 1 microsecond of the command.

ILWD

This is a flag associated with the last write data character. The setup time must be at least 300 nanoseconds before the trailing edge of IWST. There is no hold time requirement. This flag is also used to terminate the write command and variable length erase operation.

IFEN

For normal conditions, this signal must be asserted by the controller. This signal may be pulsed high (2 microseconds minimum) to reset a read, search, or write command run-away during DBSY. It is ignored when DBSY is FALSE. Command termination occurs within 50 milliseconds with a normal sequence, terminate rewind, unload, erase fixed, write file mark, or extended status command since these commands cannot "run away". By limiting the IFEN in this way, all "run aways" can be terminated in an orderly manner without loss of tape information.

IWP, IWO-7

These are write data. They must be set up with the same timing as ILWD. The tape track binary weight format is:

Head Physical - 1 2 3 4 5 6 7 8 9

Binary Weight - $2^2\ 2^0\ 2^4\ P\ 2^5\ 2^6\ 2^7\ 2^1\ 2^3$

R/W Data Bit - 5 7 3 P 2 1 0 6 4

IFAD, ITAD0, ITAD1

These are address lines to the tape drive. Address decoding is as follows.

Interface			Address Switches		
IFAD	**ITAD0**	**ITAD1**	**S1**	**S2**	**S4**
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

NOTE

Address lines must be set up a minimum of 1 microsecond before a command is issued or status is polled. Address zero is the only supported configuration.

IREV, IWRT, IWFM, IEDIT, IERASE

These lines are decoded to produce the commands. They must be set up a minimum of 300 nanoseconds before the trailing edge of IGO. Since they are latched in the tape drive, there is no hold time requirement.

IHISP

When IHISP is asserted, the tape drive operates at 100 inches/second. This line must be set up a minimum of 1 microsecond before the trailing edge of IGO. Since it is latched in the tape drive, there is no hold time requirement. Repositioning is automatic when switching speed, thereby delaying the first command by about 400 milliseconds.

RESERVED

These lines are reserved for future options.

8.3.2.2 Interface to Controller - Pin assignments and names of signals sent to the M7206 interface/controller module from the TS05 tape transport are listed in Table 8-9. The functions of the signals are as follows.

IFBY

This signal is asserted within 1 microsecond after the trailing edge of IGO, and is negated after command completion.

IDBY

This signal is asserted after any repositioning, and stays TRUE during the active execution of all commands initiated by IGO. On the trailing edge of this signal, another command of any type, direction, or speed can be given. There is no restriction as to type of direction, or speed. IDBY goes TRUE as soon as the MTST is positioned in the correct IRG, and a data record or file mark can occur. IDBY goes TRUE at least 100 microseconds before any data transfer, EOF, or block detection.

Table 8-9 Interface Signals to Controller

Plug No.	Live Pin	Ground Pin	Signal Description	Signal Name
P1	2	1	Formatter Busy	IFBY
P1	44	43	Reserved	-
P1	48	47	Read Data 2	IR2
P1	50	49	Read Data 3	IR3
P2	1	-	Read Data Parity	IRP
P2	2	-	Read Data 0	IR0
P2	3	-	Read Data 1	IR1
P2	4	-	Load Point	ILDP
P2	6	5	Read Data 4	IR4
P2	8	7	Read Data 7	IR7
P2	10	9	Read Data 6	IR6
P2	12	11	Hard Error	IHER
P2	14	13	File Mark	IFMK
P2	16	25	Identification	IDENT
P2	20	19	Read Data 5	IR5
P2	22	21	End of Tape	IEOT
P2	26	25	Reserved	-
P2	28	27	Ready	IRDY
P2	30	29	Rewinding	IRWD
P2	32	31	File Protect	IFPT
P2	34	33	Read Strobe	IRSTR
P2	36	35	Write Strobe	IWSTR
P2	38	37	Data Busy	IDBY
P2	40	39	High-Speed Status	ISPEED
P2	42	41	Corrected Error	ICER
P2	44	43	On-Line	IONL

IDENT

This signal is pulsed when reading or writing from load point and the PE identification burst is detected. The IDENT line is tested on the trailing edge of ILDP. When a write command is started at BOT, an ID burst of about 13 to 15 centimeters (5 to 6 inches) overlapping the BOT marker is generated. When a read command is executed, the recorded ID burst is sampled at about the leading edge of the BOT marker. An ID burst is detected by the presence of more than 80 character periods where only the P channel is recorded with other channels erased. The absence of an ID burst does not prevent the MTSU from reading an otherwise valid 1600 bits/inch tape.

IHER

This signal is pulsed if the record being written or read contains an uncorrectable error. The line goes LOW when an error is detected during IDBY. Error conditions asserting this line include:

1. Multitrack Dropout — Two or more tracks have analog envelopes dropping below the operating threshold before passing through the postamble.
2. Uncorrectable Parity Error — All tracks have valid envelopes but the parity is even and the postamble has not yet been detected. This error is caused by writing incorrect parity when the external write parity option is selected.
3. Nonzero Character in Postamble — The only allowable character in the postamble is a zero (with even parity). This is checked during the first 20 postamble character intervals.
4. Excessive Skew — This error detection is indirect. A character bit is lost, causing an unavoidable postamble detection failure and consequent parity error when entering the postamble.
5. Loss of Data Envelope After Postamble Detection — Twenty character intervals are allowed after the postamble to provide time for the postamble to end and envelope detectors to decay. At the end of this time, there must be at least eight quiescent data channels, or else an error is reported.

ICER

This signal is pulsed when a single track dropout is detected and error correction is in process. This occurs before IDBY goes FALSE. These pulses occur throughout the rest of the data block. They range in width from 100 nanoseconds to over 10 microseconds. These pulses must be latched to be sensed at the IDBY transition.

IFMK

This line is pulsed on a write verification or read operation when an IBM/ANSI compatible file mark is detected. This occurs prior to IDBY going FALSE. If a file mark is not detected during a file mark write operation, the bad file mark must be backspaced with a space reverse command and the file mark must be rewritten. For maximum data reliability, a file mark is detected using majority logic. A filemark is sensed when any two of three tracks that must be present (Channels 2, 6, and 7) are present for at least 15 character periods and all three of the erased channels (Channels 1, 3, and 4) are absent. This technique provides automatic dead track recovery of file marks.

IRDY

This signal indicates tape is tensioned and is not rewinding, offline, loading, or unloading. In the event of a hard fault shutdown, the drive goes off-line and not ready. This line is used to precondition any tape drive command.

IONL

This signal indicates the tape drive ON-LINE flip-flop is set. The drive is placed on-line during or after a tape load operation. This signal is negated within 1 microsecond of the reception of an unload command. When IONL is FALSE, IRDY is also FALSE. If the transport is manually placed off-line during a rewind operation, this signal remains TRUE until BOT is reached.

IRWD

This signal indicates the tape drive is in a rewind to beginning of tape sequence. The status goes TRUE within 1 microsecond of the rewind command and stays TRUE until the tape returns to BOT. IRDY is negated while the drive is rewinding.

IFPT

This signal indicates the loaded reel has no write permit ring, hence the write electronics are disabled, and write commands are prohibited. This status goes TRUE during the tape load sequence before the drive goes ready. This status is valid at all times once tape is loaded.

ILDP

This signal is asserted when the load point reflective marker is logically at the sensor. Since normal operation requires long ramps and repositions, when a command is executed at BOT the ILDP status remains TRUE during the repositioning. This is especially noticeable at 254 centimeters/second (100 inches/second) when ILDP remains TRUE for 0.5 second after a command. If a reverse command runs into BOT, a command reset occurs with ILDP being set. If an illegal reverse command occurs at BOT, ILDP remains TRUE but IFBY and IDBY sequence quickly (< 10 milliseconds) in order to retain compatibility with other commands. ILDP goes TRUE only at the end of a rewind, and is not set even when crossed over physically by the drive if the drive is "repositioning" and is not logically at the BOT marker.

IEOT

This signal is asserted to indicate the end of tape condition [less than 4.6 meters (15 feet) of tape remaining on the reel] and is negated to indicate that a rewind or reverse operation over the EOT marker has occurred. The signal is programmable to the extent that its assertion or negation can be delayed up to a maximum of three data blocks. That is, the end of tape reflective marker can be up to three data blocks pass the end of tape sensor before IEOT is switched.

ISPEED

This signal is asserted when the tape drive is operating in the high-speed mode. The signal is valid after IDBY goes TRUE for the associated command. This signal is latched until after the next IGO command.

IWSTR

This is a pulse, the trailing edge of which indicates that the character on the data lines has been written on tape and the next character is needed. The next character and last word flag must have a setup time of at least 300 nanoseconds before the trailing edge of IWSTR. The frequency of the IWSTR pulse is proportional to tape speed times bit density. The width of IWSTR is 2 microseconds nominal.

fw = V bits/inch

for example:

at 254 centimeters/seconds (100 inches/second) PE

fw = 160,000 bytes/second

IRSTR

This signal is a pulse indicating a read character is available to the interface. Note that although the average long-term transfer rate is the same as for write data, due to skew and velocity change the instantaneous rate is almost twice that of the write data. The fall of IDBY is used to indicate the end of a command since not all read and write commands produce read strobes. The width of IRSTR is 1 microsecond nominal.

IRP, IRO-7

These are data lines to the interface. The read data overlaps IRSTR by at least 500 nanoseconds.

RESERVED

These lines are reserved for future options.

8.3.3 TS05 Tape Transport Unit

The TSV05 subsystem tape transport unit (TS05A) responds to the transport bus control lines with status or data, depending on the command issued. The unit includes a microprocessor consisting of the following.

1. Z80 microprocessor chip
2. 8K x 8 ROM
3. 8 x 256 RAM
4. 4 x PIO

The microprocessor directly controls electromechanical subassemblies and indirectly controls the data formatter electronics. The actual read and write data are not directly controlled by the microprocessor.

8.3.3.1 Tape Transport Operation - The following sequence of events occur when the tape transport unit receives a write command over the transport bus from the M7206 interface/controller module.

1. The microprocessor checks that the tape is properly loaded, the transport is on-line, and the write enable ring is installed in the supply reel.
2. If these conditions are TRUE, the microprocessor switches on drive current to the takeup motor to begin forward tape motion. It uses feedback from the tachometer to ensure the proper forward startup ramp profile. During this startup, and during the remainder of the sequence, the microprocessor constantly scans the sensors. If it detects a fault condition, it causes a double blink of the front panel LEDs. Additionally, a fault condition causes a mechanical relay to deactuate, resulting in dynamic motor braking such that the tape is not damaged, and switches on the system failure LED.
3. At the end of the startup ramp, the tape is moving at its full read/write speed of 64 or 254 centimeters/second (25 or 100 inches/second). Nominal tape tension is maintained by a drag current provided to the supply motor. The microprocessor controls the drag current based on feedback from the tension arm transducer. The microprocessor continues to control tape speed and tension by analyzing feedback from the tachometer and tension arm transducer and controlling the drive and drag currents.
4. Using the tachometer feedback, the microprocessor determines the amount of tape moving past the read/write/erase heads. When a nominal 1.5 centimeter (0.6 inch) gap is present between the last record and the write head, the microprocessor directs the formatter to place the 40-character preamble on the tape and then write the data bytes obtained from the transport bus.

5. After the last data byte is written on the tape, the formatter writes the 40-character postamble on the tape, thus completing the record.

6. Tape motion continues at the full read/write speed another 1.5 centimeters (0.6 inch). If the tape transport microprocessor receives another command of the same type within the time it takes for the 1.5 centimeter (0.6 inch) gap to occur (the reinstruct time), tape motion continues and the command is executed. If, however, a different type of command or no command is received, the microprocessor begins a tape repositioning cycle.

Throughout this sequence, the microprocessor places operational or error status on the transport bus to the M7206 interface/controller module.

Signals used within the tape transport electronics are shown in the vendor print set and defined in Appendix E.

8.3.3.2 Tape Transport Microprocessor - The TS05 tape transport unit uses a single chip Z80 microprocessor. Its internal registers contain 208 bits of read/write memory that are accessible to the program. These registers include two sets of general-purpose registers that may be used individually as 8-bit registers or as 18-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of exchange instructions makes either set of main or alternate registers accessible to the program. The Z80 also contains a stack pointer, program counter, two index registers, a refresh counter register, and an interrupt register.

The Z80 PIO parallel I/O circuit is a programmable, dual-port device that provides a TTL compatible interface between peripheral events and the Z80 CPU. Each port has eight data bits and two handshaking signals, ready and strobe, that control data transfers.

The Z80 CTC counter/timer has four independent channels. Each channel is individually programmed with two words: a control word and a time constant word. The control word selects the operating mode, counter or timer, and selects operating parameters. The time constant word is a value between 1 and 256. The CTC provides general system requirements of event timing, interrupt and interval timing, and clock rate generation.

8.4 FIRMWARE DESCRIPTION

The TSV05 subsystem has four main areas of functionality implemented in firmware.

1. Diagnostic (power-up, main loop, TSDB byte wrap)
2. Attention handler
3. Get command
4. Process command

The relationship of these areas to one another is illustrated in Figure 8-10. This section describes each of these main functional areas. It also discusses troubleshooting with the diagnostics and the use of the boot code.

8.4.1 Diagnostic

8.4.1.1 Power-Up - The firmware of the M7206 interface/controller module includes self-test diagnostic code that is executed at power-up. The power-up diagnostic code tests the 2901-based microprocessor to the extent of assuring that it does hang or produce meaningless error indications. These diagnostics do not fully test the Q-bus interface or the tape transport bus interface. They run with or without the tape transport cables installed.

The power-up self-test diagnostics are started or restarted under the following conditions:

- After the bus initialize signal is negated due to a power-up or reset command, and
- After a write word type command into the TSSR.

Note that SSR is cleared whenever self-test diagnostics are running. Successful startup of the diagnostics is indicated by the PROC OK LED and the contents of the TSSR.

There are three LEDs located in the top center area of the M7206 interface/controller module. During the running of the firmware diagnostics, the LEDs have the following meanings.

- D5 = SSR — D5 is OFF when SSR = 1.
- D4 = PROC OK — D4 is ON during self-test. It blinks ring the main loop test if there are no errors.
- D1 = TRANSMIT — D1 is OFF during self-test. If it is ON continuously, it indicates that the M7206 is hanging the Q-bus.

The status of the self-test diagnostics is obtained by examining the contents of the TSSR (standard address is 772522). This register is updated at the beginning of each test. If a test fails, the processor stops at the failing test (except for test 13, the RAM test) and the TSSR contains the test number. The test number is read from the TSSR, and the diagnostics restarted. The meanings of the contents of the TSSR pertaining to the powerup self-test diagnostics are listed in Table 8-10. The octal representation of the low order bits gives the number of the failing test. Note that a test 13 failure may not be apparent until the main loop code has begun executing.

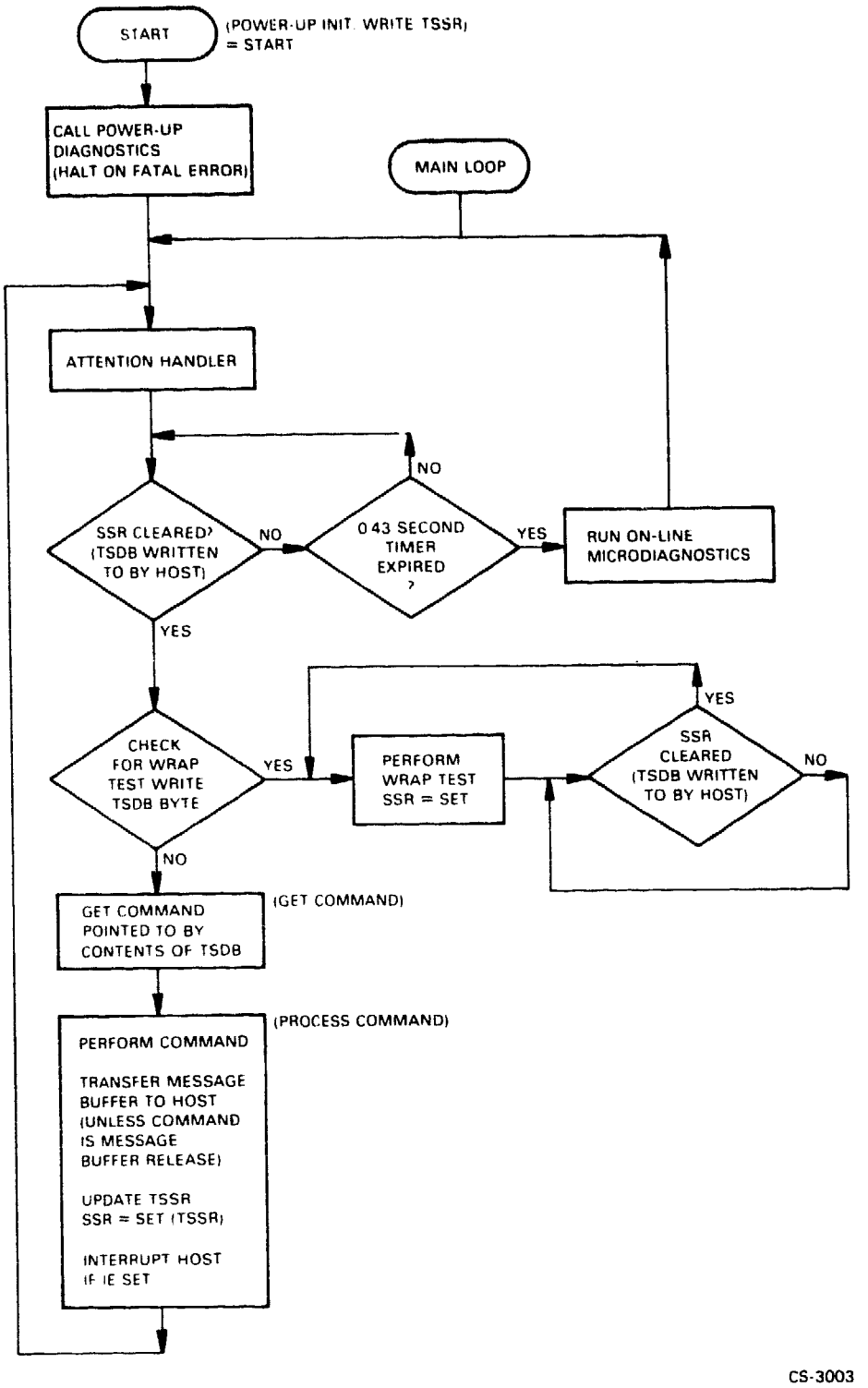


Figure 8-10 TSV05 Operation

Table 8-10 TSSR Contents for Power-Up Diagnostics

Test or State	TSSR Value	Bit Status	Comments
Start		Not accessible	INIT or write word to TSSR.
Test 17	066017	SSR = 0	Jump test. Other bits set in TSSR are for operating system compatibility.
Test 16	066016	SSR = 0	Conditional jump test.
Test 15	066015	SSR = 0	ALU sign test.
Test 14	066014	SSR = 0	ALU function test.
Test 13	066013	SSR = 0	RAM test. This TSSR value is present only if the main loop code is not entered properly. This test resets a hardware timer for use as a scope sync point at E83-1 pin 13 (D4 TIMER RST L). In the event of a failure, this test does not hang, but sets an internal error flag.
Initialize			No error checking performed.
Enter main loop	102313	SC = 1 NBA1 = 1 SSR = 1 OFL = 1	Test 13 (RAM test) failed.
	2300	NBA = 1 SSR = 1 OFL = 1	Power-up self-test diagnostics successfully completed.

8.4.1.2 Main Loop - After the successful completion of the power-up diagnostics, the main loop code begins executing. This is indicated by the center LED (PROC OK) blinking. Also, the TSSR contains the value 2300, indicating that NBA, OFF-LINE, and SSR are set (Table 8-11). If, however, the tape transport is cabled, loaded with tape and placed on-line, the TSSR contains 2200 and OFF-LINE is cleared. Note that the TSSR is not automatically updated by placing the tape transport on-line or off-line. In this case, the TSSR is updated after a bus initialize or a write word type command to the TSSR is issued.

Once the microprocessor enters the main loop, it checks to see if the TSDB has been written. If the TSDB was written (with the starting address of a command packet), the system executes the command and returns to the main loop (Figure 8-11). If the TSDB was not written, the microprocessor checks to see if a 430 millisecond timer has timed out. If it has not, the microprocessor checks again for the receipt of a command (write to the TSDB). If the 430 millisecond timer has timed out, the microprocessor executes the MICRO 1 and MICRO 2 diagnostic tests.

Table 8-11 TSSR Contents During Main Loop Diagnostics

Test or State	TSSR Value	Bit Status	Comments
Initialize			No error checking performed.
Enter main loop	2300	NBA = 1 SSR = 1 OFL = 1	This value pertains to the power-up diagnostic test results. 2300 indicates that the power-up diagnostics completed successfully.
Wait 430 ms	2300	NBA = 1 SSR = 1 OFL = 1	
MICRO 2	2300	NBA = 1 SSR = 1 OFL = 1	FIFO test. Failure sets an internal error flag.
MICRO 1	2300	NBA = 1 SSR = 1 OFL = 1	RAM test. Failure sets an internal error flag.

If an error is detected by either of the two diagnostics, the microprocessor sets an internal error flag and continues to loop, checking for commands and checking the timer. When a command does arrive, the microprocessor checks the status of the internal error flags before exiting the main loop to execute the command. The status at the point where program execution exits the main loop is obtained by examining the contents of the TSSR (Table 8-12). There are several possibilities.

1. If a valid command (other than write characteristics or write subsystem memory commands) is issued and the internal error flag is set, an immediate error occurs, resulting in SC = 1, SSR = 1, and TCC = 7.

2. If a valid write characteristics command or write subsystem memory command is issued, the microprocessor may be able to execute the command. If the command is executed successfully, SC = 0 and SSR = 1. If the command is not executed successfully, SC = 1, SSR = 1, and TCC = 3 or 7, depending on the type of failure.

3. If an invalid command is issued and the internal error flag is set, the subsystem attempts to report the status of the invalid command execution. In this case, the contents of the TSSR may be ambiguous, depending on the nature of the error and the command.

4. If the internal error flag is not set and there are no errors during command execution, the TSSR has SC = 0 and SSR = 1.

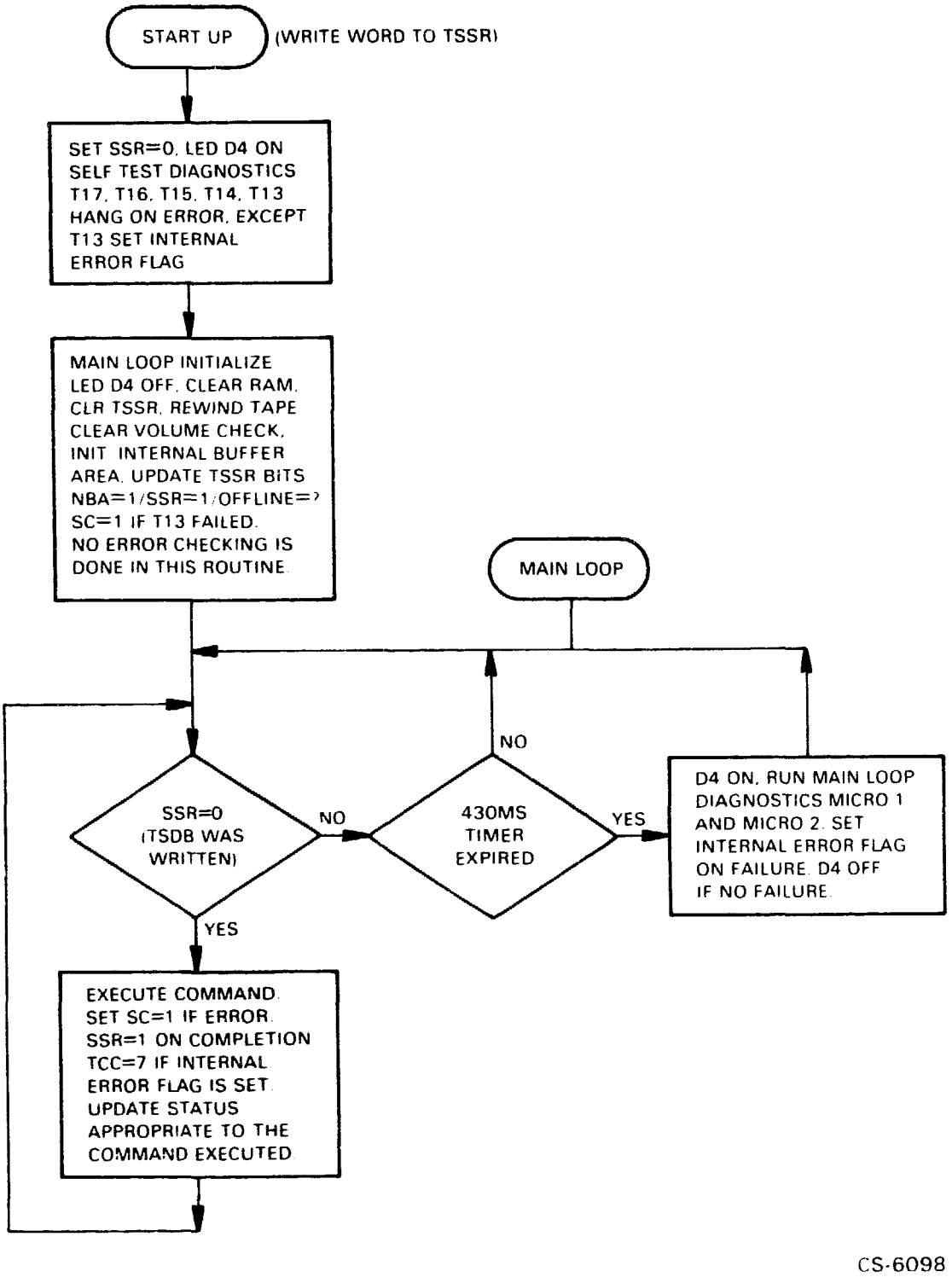


Figure 8-11 Diagnostic Flowchart

Table 8-12 TSSR Contents After Main Loop is Exited

Test or State	TSSR Value	Bit Status	Comments
Write TSDB Pointer	2200	NBA = 1 SSR = 1	The transport is on-line, there are no self-test errors, and a command can be issued. Since NBA = 1, the command must be a valid write characteristics command. SSR = 0 until command completion.
	200	SSR = 1 SC = 0	Successful completion of any command. A new command can be issued.
	1002XX	SC = 1 SSR = 1 TCC = X	Subsystem error resulted from last command. Refer to the TCC codes and message buffer.
	120216	SC = 1 SCE = 1 SSR = 1 TCC = 7	MICRO 1 RAM test failure. No message buffer was output. Since NBA = 0, a valid write characteristics command was issued issued prior to this command.
	100216	SC = 1 SSR = 1 TCC = 7	MICRO 2 FIFO test failure. A message buffer was output. If command was valid, XSTAT3H within that message buffer contains 002.

The first tests performed by the diagnostic software verify that all the power-up self-tests have run successfully. The results of these tests and the MICRO 1 and MICRO 2 tests are reported by means of the write subsystem memory command.

A message buffer is not outputted to memory if MICRO 1 (the RAM test) fails. If MICRO 2 (the FIFO test) fails, a message buffer is output and the high byte of XSTAT3 contains 002 if the command is valid.

Caution must be used when interpreting the TSSR and message buffer during failure modes, as the failure condition can corrupt this data.

To recover from these types of errors, a restart must be performed. Refer to Section 8.4.5.

8.4.1.3 TSDB Byte Wrap - A write byte operation to one byte of the TSDB automatically invokes a data wraparound test of the other byte of the TSDB. The subsystem ready bit must be set when the write byte instruction is issued. Subsystem ready is cleared during the test operation and reset upon test completion. At this point, another byte data pattern can be written into the unaccessed byte of the TSDB. TSDB byte wrap error testing is limited to checking that the correct data pattern is wrapped. To exit this diagnostic mode, a restart must be performed.

8.4.2 Attention Handler

The attention handler (indicated in Figure 8-10) is a body of code in firmware that performs the following functions.

1. It checks the state of the enable attentions interrupt (EAI) bit in the write characteristics command. If the bit is set, the handler continues. If EAI is clear, the attention handler is exited.
2. It checks the state of the diagnostic error flag. If the flag is set (as a result of an error during the main loop diagnostics), the handler jumps to step 4.
3. It checks the volume check flag (VCK). This flag is usually set by a change in the states of ON-LINE and OFF-LINE. If VCK is not set, program execution exits the attention handler.
4. It checks for the message buffer release condition, which results from the last command having been message buffer release. If the message buffer has not been released, the handler sets the attention pending flag. (This flag is checked by the process command subroutine).
5. It checks the SSR bit. If it is already cleared, this indicates a command pending. In this case, the handler sets the attention pending flag. The attention handler is then exited.
6. If the host CPU has not initiated a command by the time the attention handler reaches this point in its execution, then the SSR bit is still set. The program now clears the SSR bit. If the host CPU issues a command to the tape subsystem at this time, the RMR bit is automatically set.
7. Next, the attention handler updates the message buffer and transfers it to the host CPU. The handler then updates the TSSR with the appropriate FCC and TCC codes, and sets the SSR bit.
8. The handler checks the interrupt enable (IE) bit from the previous command (message buffer release). If IE is set, the handler interrupts the host CPU.
9. The attention handler is exited.

8.4.3 Get Command

When the host writes the TSDB, SSR clears, alerting the controller that a command is pending. The sequence for getting and accepting a command proceeds as follows.

1. The TSSR high byte is checked for a 1 in bit 7 (bit 15 of the word). (The hardware sets a flag to indicate that the TSSR was written prior to the writing of the TSDB.) If the boot bit is set, the following boot sequence occurs:

   a. Tape is rewound.

   b. One record or file mark is spaced over.

   c. 512 bytes of the next record is read and placed at starting address zero of the host.

   d. The TSSR is updated, indicating errors by setting SC = 1. SSR = 1 on completion.

   If the boot bit is not set, the get command routine bypasses the boot sequence.

2. If the boot bit is not set, the controller takes the command. The command consists of four words that are pointed to by the contents of the TSDB. Note that the contents of the TSDB was written previously by the host.

3. If a write characteristics command has not been written previously, the current command should be a write characteristics command. If these conditions are not met, the Need Buffer Address (NBA) bit remains set and the command is rejected. Command rejection causes the TSSR to be updated, SSR to be set, and the get command routine to be exited.

4. The routine checks the command for the state of the acknowledge (ACK) bit. If ACK is not set, then the last command should have been a message buffer release command.

   If these conditions are not met, then SSR is set, the host CPU is interrupted (if IE is set), and the get command routine is exited.

5. At this point, the command is ready to be processed by the process command routine.

8.4.4 Process Command

The process command routine interprets the command as follows.

1. If the command is not a valid command, the routine sets error bits and error codes. It also transfers the message buffer, updates the TSSR, sets SSR, and if IE is set, interrupts the host CPU. The process command routine is then exited.
2. If the clear volume check bit is set, the routine clears the volume check and also any attentions that were pending due to the volume check.
3. If the command is a write characteristics command, program control is passed to a separate area of code that clears the NBA bit in the TSSR, sets up characteristics parameters, and exits the routine.
4. If the command is an initialization command, the process command routine performs the following:
   a. Resets the tape drive.
   b. Checks for the previous occurrence of an error. If an error was detected previously during the running of the microdiagnostics, execution jumps to the beginning of the microcode.
   c. Transfers the message buffer.
   d. Updates the TSSR.
   e. Interrupts the host CPU (if the IE bit is set).
   f. Exits the routine.
5. If the command is a write subsystem memory command, then control passes to a routine unique to the diagnostics. After execution of the subsystem memory command routine, control returns to the process command routine, which then performs the following:
   a. Transfers the message buffer.
   b. Updates the TSSR.
   c. Sets SSR.
   d. Interrupts the host if IE is set.
   e. Exits the routine.
6. If an attention is pending, then the process command routine outputs the message buffer as an attention condition, without processing the command. It also performs the following:
   a. Updates the TSSR.
   b. Sets SSR.
   c. Interrupts the host if IE is set.
   d. Exits the routine.

7. If the command is a message buffer release command, then the routine sets the message buffer release flag, interrupts the host CPU (if IE is set), and exits.

8. If the command is a get status immediate command, the routine performs the following:

   a. Updates the message buffer.

   b. Outputs the message buffer.

   c. Updates the TSSR.

   d. Interrupts the host (if IE is set).

   e. Exits the routine.

9 At this point, processing of the command involves tape motion. The routine executes the command and then performs the following:

   a. Updates the message buffer.

   b. Outputs the message buffer.

   c. Updates the TSSR.

   d. Interrupts the host (if IE is set).

   e. Exits the routine.

8.4.5 Firmware Diagnostic Aids

8.4.5.1 Toggle In Routine - In the event that the unit does not respond to the TSSR address or if the firmware diagnostic must be restarted for troubleshooting purposes, the following toggle in type routine may be helpful. The starting address is 2000.

2000/	12706	(Set up R6 in case of traps)
2002/	1000	R6 = 1000
2004/	5000	CLR R0
2006/	12701	Set up delay value in R1
2010/	XXXXXX	Delay value (177777 = MIN/000000 = MAX TIME) - See NOTE
2012/	12737	Move word TSSR (start firmware diagnostics)
2014/	0	
2016/	172522	TSSR standard address
2020/	105200	Wait loop fixed
2022/	1376	Branch to 2020 until R0 = zero
2024/	5201	Wait loop variable
2026/	1374	Branch to 2020 until R1 = zero
2030/	763	Branch to 2000
4/	2000	(Restart on NXM, TSSR bus address is nonexistent.)
6/	0	
224/	226	(Halt address PC = 230, problem with interrupts or vectors.)
226/	0	

NOTE

The actual delay value used is dependent on the CPU type and the nature of the failure. If T17 through 13 fail, a short (177777) delay value can be used such that the oscilloscope is triggered more frequently. If a microdiagnostic fails, a long (174000) delay value must be used. In either case, the delay value must allow enough time for the failing diagnostic to run.

8.4.5.2 Startup - The firmware program startup is accomplished by either of the following:

1. Write to the TSSR.
2. Bus initialize.

On the trailing edge of a bus intialize signal (caused by power-up or a CPU command), the controller starts its firmware at microword location zero. (Refer to Figures 8-12 and 8-13, and to print set Sheet D8.) Signal D10 MRST L is asserted during the startup sequence, clearing all the address lines of the 2911 program sequencer. This sets the ROMs (Sheet D11) to location zero. D10 MRST L originates at E92 pin 9 (Sheet D10, middle right). It is derived from D2 PMRST L synchronized by D9 SCLK H. D9 SCLK H is a free-running clock with a period of approximately 200 nanoseconds. Signal D12 PMRST L (Sheet D2, upper left) originates at E4 pin 13, and is enabled in either of two ways:

1. Bus Initialize — D2 BINIT L arrives on pin AT2 and is received by the 8641 at E15 (Sheet 2, left center). This enables E4 pin 18.
2. Write TSSR Command — A write to the TSSR (standard address of 772522) causes SIGNAL MATCH (E36/48/49/50-3, Sheet D1, middle left) to go HIGH (TRUE). This signal results from the comparison of the bus address lines to the address switch. It enables the DC004 at location E18-19, which in turn decodes the bus control lines received by the 8641 transceivers at locations E1 and E15. The PAL01 in location E4 further decodes the bus control signals plus internal M7206 control signals to drive the D2 PMRST L line at E4 pin 13.

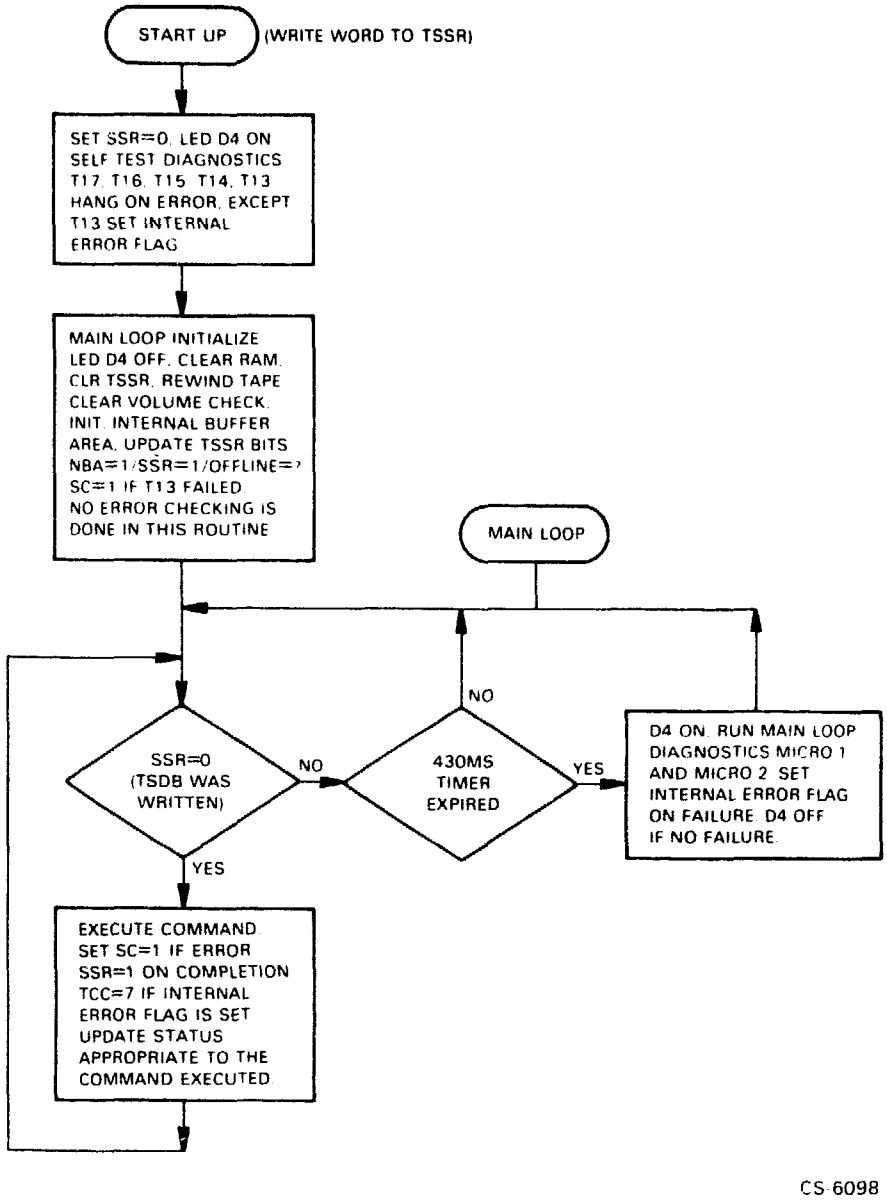
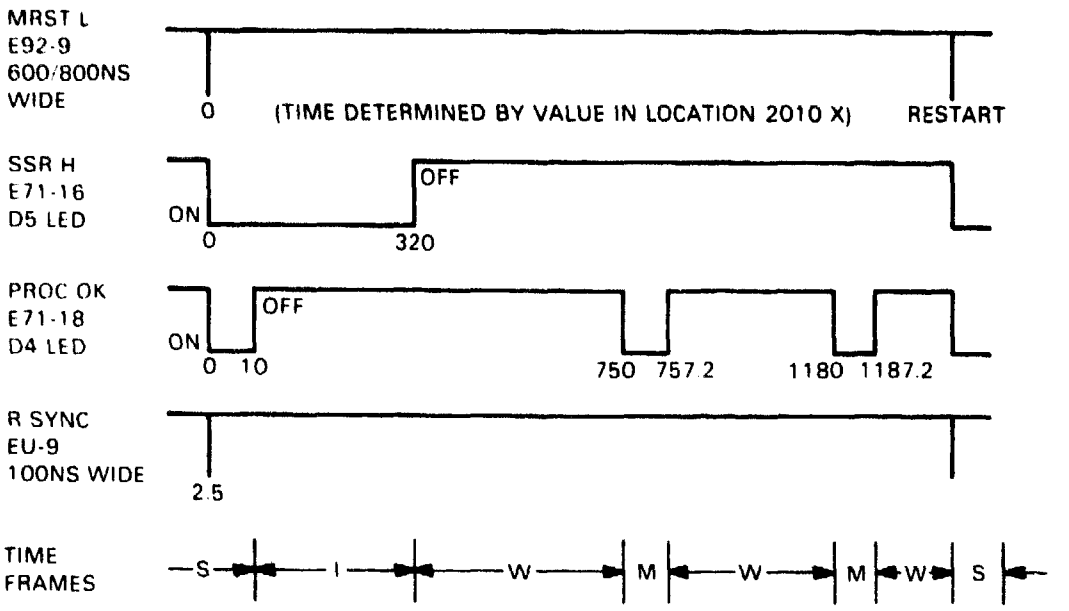


Figure 8-12 Firmware Diagnostic Flowchart



S = SELF TEST T17 THROUGH T13.
I = INITIALIZE. THIS TIME EXTENDS IF TAPE IS AVAILABLE TO REWIND.
W = 430ms WAIT TIMER. A COMMAND (TSDB WRITTEN SSR=0) EXITS HERE.
M = MICRO DIAGNOSTICS 1 AND 2.
IF NO COMMAND IS ISSUED, THE FIRMWARE REMAINS IN THE W AND M STATES.

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Figure 8-13 Firmware Diagnostic Timing

8.4.5.3 Boot Code - The boot code listed below is functionally equivalent to the "MS" boot code for the TSV05. Error handling is accomplished by checking the special conditions bit (bit 15) and, if it is set, retrying until there is no error. If an "MS" boot block exists on the tape and all the hardware is operating properly, the code listed below can boot RT11, RSX11, RSTS, and XXDP+ tapes. The real-time event clock should be disabled when this boot code is used to load diagnostics.

Upon exit from the boot routine, registers R0 through R4 normally contain the following.

R0 = 0	Unit number
R1 = 172522	TSSR address
R2 = 172520	TSBA/TSDB address
R3 = 010016	PC of "SM" +20

The boot code is as follows. The starting address is 10000.

```
                                        .=7776
007776  046523                          .WORD "SM"              Device ID
                                                                backwards

010000  012701  172522  START:  MOV TS05DB+2,R1      R1=TSSR
010004  010102                  MOV R1,R2           R2=TSSR
010006  005000                  CLR R0              Clear R0

010010  105711                  TSTB (R1)           Wait for SSR
010012  100376                  BPL .-1
010014  010704                  MOV PC,R4           R4=PC of
                                                    "SM"+20
010016  112737  000200  172523  MOVB #200,@#TS05DB+3 Write byte
                                                    bit 15

010024  005242                  INC -(R2)           Write into
                                                    TSDB

010026  105711                  TSTB (R1)           Wait for SSR
010030  100376                  BPL .-1

010032  005711                  TST (R1)            Test for error
010034  100761                  BMI START           If SC=1 retry
010036  005007                  CLR PC              Jump to zero
                                .END
```

8.4.6 Programming Example

The following toggle in type routine writes 100 bytes on tape, starting at memory location 4000, and then halts. No error checking or retries are performed. A tape (with write enable ring installed) must be loaded in the tape transport unit. The TSSR should contain 002200 at start-up. The starting address is 2000.

```
2000/005037   CLR TSSR     Initialize the subsystem.
2002/172522
2004/105737   TSTB TSSR    Wait for subsystem ready, wait for the
2006/172522                self-test diagnostics, including rewind,
                           to complete.
2010/100375
2012/012737   TSDB=1000    Perform the set characteristics command.
2014/001000                This clears NBA, bit 10, in the TSSR.
2016/172520
2020/105737   TSTB TSSR    Wait for subsystem ready.  Wait for the
2022/172522                write characteristics command to com-
                           plete.
2024/100375
2026/012737   TSDB=1600    Perform the write data command.  Tape
                           motion occurs.
2030/001600
2032/172520
2034/105737   TSTB TSSR    Wait for subsystem ready.  Wait for the
2036/172522                write data command to complete.
2040/100375
2042/000000   HALT         Tape is positioned approximately 8.9
                           centimeters (3.5 inches) forward of the
                           BOT marker.  The contents of the message
                           buffer, starting at address 1400, is ex-
                           amined to obtain subsystem status.
```

Placing 771 in address 2042 causes the program to run continuously. However, EOT is not detected.

The following is the write characteristics command packet and data area.

```
1000/140004   Write characteristics command
1002/001200   Low characteristics data address
1004/000000   High characteristics data address
1006/000010   Characteristics data length

1200/001400   Low message buffer address
1202/000000   High message buffer address
1204/000020   Message buffer length
1206/000000   Characteristic data
```

The following is the message buffer data area.

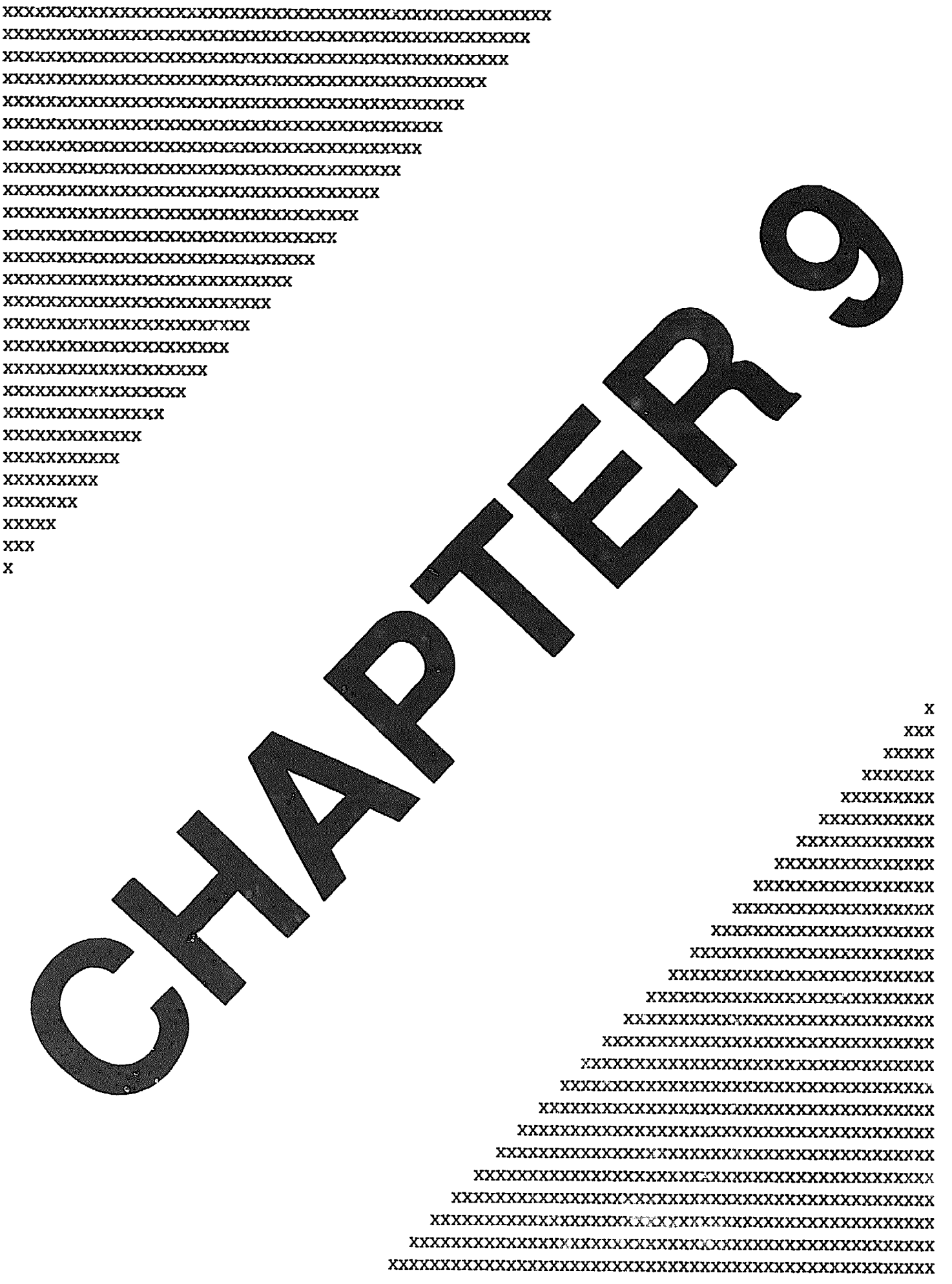
1400/??????	Message header word	Typically 100020
1402/??????	#Bytes following	Typically 000012
1404/??????	Residual byte count	Typically 000000
1406/??????	XSTAT0	Typically 000310
1410/??????	XSTAT1	Typically 000000
1412/??????	XSTAT2	Typically 100000
1414/??????	XSTAT3	Typically 000000
1416/------	XSTAT4	This word exists only if extended features are enabled. "#Bytes following" in address 1402 equals 000014 if XSTAT4 exists.

The following is the write command packet and data area.

1600/140005	Write data command
1602/004000	Low memory address
1604/000000	High memory address
1606/000100	Byte count
4000/??????	Data buffer
THRU/??????	
4076/??????	

Changing address 1600 to 140001 causes a read forward command to take 100 bytes of data from tape and place it in memory starting at location 4000.

When the program halts at PC location 2044, the TSSR should equal 200. Only subsystem ready is set. Other bits set indicate an error occured. The TSDB should contain 1416, pointing to the end of the message buffer data area. As shown in this example, it is possible in diagnostic error situations to place the CPU in console mode and determine where the message buffer is located by examining the TSDB and subtracting approximately 20. Caution must be exercised if this method is used, because the message buffer is updated if another command is issued or another routine utilizes the message buffer memory area.


CHAPTER 9

CHAPTER 9
TSV05-A/B TECHNICAL DESCRIPTION

9.1 INTRODUCTION

9.1.1 Scope

This chapter describes the operation of the TSV05 subsystem in details necessary for diagnosing failures at the Field Replaceable Unit (FRU) level. Some aspects of the microprocessor hardware and firmware are described to the device and microcode level, where required for interpreting the results of the self-test diagnostic programs. Generally, however, the descriptions in this chapter are limited to the concept level.

9.1.2 Conventions

The *TSV05 Field Maintenance Print Set* (MP-01157) is referenced in several sections in this chapter. The print set uses the following convention for signal identification:

- SOURCE
- SIGNAL NAME
- POLARITY

SOURCE indicates the print set sheet number on which the signal originates.

SIGNAL NAME is the functional name assigned to the signal. It may be a descriptive term or a mnemonic representation of the signal function.

POLARITY indicates the voltage level of the signal when it is in its TRUE (asserted) state. H indicates that the signal is at +3 volts when asserted, and at 0 volts when negated. Conversely, L indicates that the signal is at 0 volts when asserted, and +3 volts when negated. For example:

D7 MRST L

originates on print set sheet D7, performs a function that can be represented by the mnemonic MRST (master reset), and is in a logic LOW state (0 volt) when asserted.

The exception to this convention is the naming of bidirectional bus signals. No SOURCE identification appears on bus conductors, because they are asserted or negated from any of several sources.

9.1.3 Terminology

The following terms used in this manual are defined below.

1. Access Time — The time between the issuing of a tape read, write, or space command by the controller, and the reading or writing of the first character in the tape record.

2. BOT Marker — Beginning of Tape marker. This is a reflective strip placed on the tape 5 meters (16 feet) from the beginning of the tape.

3. Command Buffer — An area of contiguous 18-bit words in the host system memory space. I/O request packets are built in the command buffer and retrieved by the TSV05.

4. Command Delay — The elapsed time between the interrupt from the tape controller signifying the completion of an operation (that is, read or write) and the issuing of the next command to the controller by the operating software.

5. Command Packet (I/O Request Packet) — A set of control words issued from the CPU (that is, operating system, I/O driver, or diagnostic program) to the TSV05 to initiate and control operation.

6. Command Pointer — The high (most significant) 16 bits of an 18-bit modulo-4 address that points to a command packet located in memory. In extended operation, "command pointer" refers to the high 20 bits of a 22-bit modulo-4 address that points to a command packet located in memory.

7. Conventional, or Stop/Start, Technology — Operating characteristic of a tape drive that can rapidly accelerate and decelerate tape motion to allow the tape to come to rest with the read/write head positioned in the interrecord gap.

8. EOT Marker — End of Tape marker. This is a reflective strip placed on the tape 7.6 meters (25 feet) from the end of the tape.

9. Extended Feature — Mode of operation of the TSV05 subsystem that extends the functionality of the subsystem beyond that allowed by TS11/TS04 compatibility. Includes 22-bit memory addressing, and additional status and functions. Requires the use of special software, which is not supplied and/or does not exist.

10. Header Word — The header word is the first word of a command packet or a message packet.

11. Message Buffer — An area of contiguous words in CPU memory. The message packets are stored there by the TSV05.

12. Message Packet — A group of status words issued from the TSV05 to the CPU to indicate status of the tape transport and/or operation completed.

13. Modulo-4 Address — An address within the CPU memory that is evenly divisible by 4 (that is, octal 0, 4, 10, 14, 20, and so on).

14. Packet Protocol — Method of communication between CPU software and the TSV05 by means of areas in CPU memory, following the rules dictated by TS11/TS04 compatibility requirements. A "packet" is a contiguous series of words residing in CPU memory. The TSV05 accesses a command packet to receive command information, and stores a message packet (in a message buffer area in CPU memory) to provide status information to the software. This technique allows large amounts of information to be passed, while allowing the device to occupy only two hardware I/O addresses.

15. Q-22 — Q-bus containing signal connections for 22-bit addressing capability. Used on the PDP-11/23B computer system.

16. Record Buffering — Capability of the TSV05 to store an entire tape record (up to 3584 bytes in length) during read or write command sequences to allow overlapping of reel-to-reel tape repositioning with transfer of data to or from the CPU.

17. Reinstruct Time — The period of time following reading or writing the last character of a record allowed by a tape transport for a controller to issue the next command, in order to avoid slowing or stopping the tape.

18. Repositioning — A characteristic of the TS05 streaming tape drive whereby tape motion is halted and the tape is readied for the next operation by decelerating the tape in its current direction and bringing it to a stop, then accelerating and decelerating the tape in the opposite direction and bringing it to a stop. The tape is not stopped in the gap, as with conventional tape drives.

19. Streaming, or Reel-to-Reel, Technology — Operation of a tape transport without stopping in the interrecord gap. Requires that, for maximum efficiency, commands of similar type, speed, and direction be supplied by the controller within a relatively short "reinstruct" period. The TS05 tape transport operates in this fashion.

20. TSBA — TSV05 Bus Address Register. A read-only hardware register in the I/O address space.

21. TSDB — TSV05 Data Buffer Register. A write-only hardware register in the I/O address space.

22. TSSR — TSV05 Status Register. A read/write register in the I/O address space.

23. XSTn — Extended Status Register n. One of five status registers deposited into the message buffer area.

9.2 GENERAL DESCRIPTION

The TSV05 Tape Transport Subsystem includes two major components: the M7196 interface/controller module, and the TS05 tape transport unit.

9.2.1 M7196 Q-Bus Interface/Controller Module

The M7196 interface/controller module has three functional areas of circuitry (Figure 9-1):

1. Q-Bus Interface
2. Microprocessor
3. Tape Transport Bus Interface

9.2.1.1 Q-Bus Interface - The Q-bus interface includes:

1. Transceivers and Bus Control — This circuitry handles the Q-bus protocol and the movement of addresses and data onto and off of the Q-bus conductor.
2. Input File — The input file contains data written to the M7196 interface/controller module from the host computer over the Q-bus. It includes:
   a. TSV05 data buffer register (TSDB).
   b. High byte of the TSV05 status register (TSSR).
   c. DMA data in register.
3. Output File — The output file contains data to be read by the host computer over the Q-bus. It includes:
   a. TSV05 bus address register (TSBA).
   b. TSV05 status register (TSSR).
   c. DMA data out register.

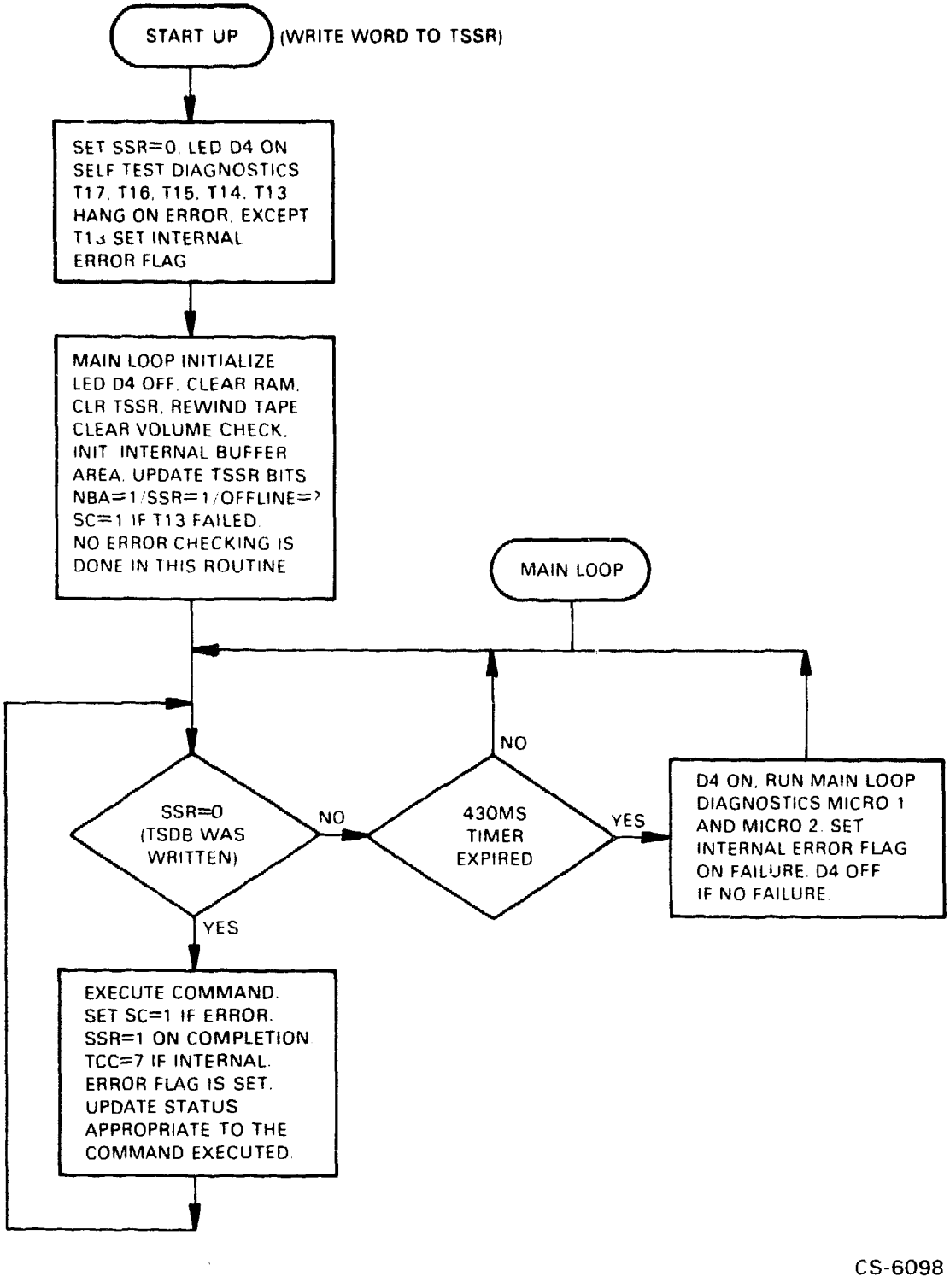


Figure 9-1 M7196 Q-Bus Interface/Controller Block Diagram

9.2.1.2 Microprocessor - The microprocessor includes:

1. Arithmetic Logic Unit (ALU) — This circuit comprises two 2901 bit slice microprocessor chips and the associated logic devices necessary for performing the functions instructed by the microwords. The ALU operates on eight bits at a time.

2. S-Bus — The source, or input, bus carries the operands on which the 2901 ALU functions are performed.

3. Y-Bus — The Y, or output, bus carries the results of the ALU functions.

4. Random Access Memory (RAM) — The 4K x 8-bit RAM provides temporary storage area for microprocessor operations and also provides a 3K byte data buffer when the data buffering feature is enabled.

5. Address Register — This is loaded from the Y-bus as necessary to specify a RAM address.

6. Buffer — This is used when a RAM address is specified by the EMIT field of the microword.

7. Pipeline Register — The pipeline register stores all 56 bits of the microword from the Read Only Memory (ROM). The outputs of this register are applied as control functions to all elements of the controller.

8. ROM — The 2K x 58-bit ROM contains the microinstructions that control the microprocessor.

9. Sequencer and Branch Microtest (BUT) Multiplexer — This set of three 2911 sequencer chips provides 11 microprogram address lines to the ROMs. The BUT multiplexer enables the microprogram to select conditions for testing so as to allow the microprogram to modify the sequence of microinstructions.

9.2.1.3 Tape Transport Bus Interface - The tape transport bus interface includes:

1. First In First Out (FIFO) Register File — The 64 x 8-bit FIFO register file serves as a buffer for all data being transferred to or from the tape transport bus.

2. Latch — Latches are used on the microprocessor output bus for temporary storage of data and control functions.

3. Buffer — During microprocessor read operations, data is taken from the FIFO register file, passed through the buffer, and placed on the microprocessor input bus.

4. Receivers — These devices receive status and data signals from the tape transport bus.

5. Drivers — These devices transmit status and data signals onto the tape transport bus.

6. Loopback Circuitry — The loopback circuitry is used during maintenance diagnostic testing to test the transport bus drivers and receivers.

9.2.2 TS05 Tape Transport Unit

The TS05 tape transport unit has three main functional areas (Figure 9-2):

1. Data Formatter Interface
2. Microprocessor
3. Electromechanical Assemblies

9.2.2.1 Data Formatter Interface - The data formatter interface includes:

- Receivers — These devices receive data and control signals from the tape transport bus.
- Drivers — These devices transmit data and control signals onto the tape transport bus.
- Data Formatter Electronics — Under the control of the tape transport unit microprocessor, the data formatter circuits place data in the proper format on the tape, and reads data off the tape. Binary write data from the tape transport bus is routed directly to the formatter, where it is placed within the required format. The formatter electronics generate the necessary current profile to drive the write head. During read operations, the formatter performs read head amplification, data separation, skew buffering, error detection and, if necessary, error correction.

9.2.2.2 Microprocessor - The microprocessor includes:

1. ALU — A Z80 microprocessor chip performs ALU functions executing instructions stored in ROM.
2. ROM — Microinstructions for the operation of the tape transport unit are contained in the 8K x 8-bit ROM.
3. RAM — The 8 x 258-bit RAM provides temporary storage area for the microprocessor.
4. PIO Ports — The microprocessor uses four PIO ports to control and obtain feedback from the electromechanical assemblies.

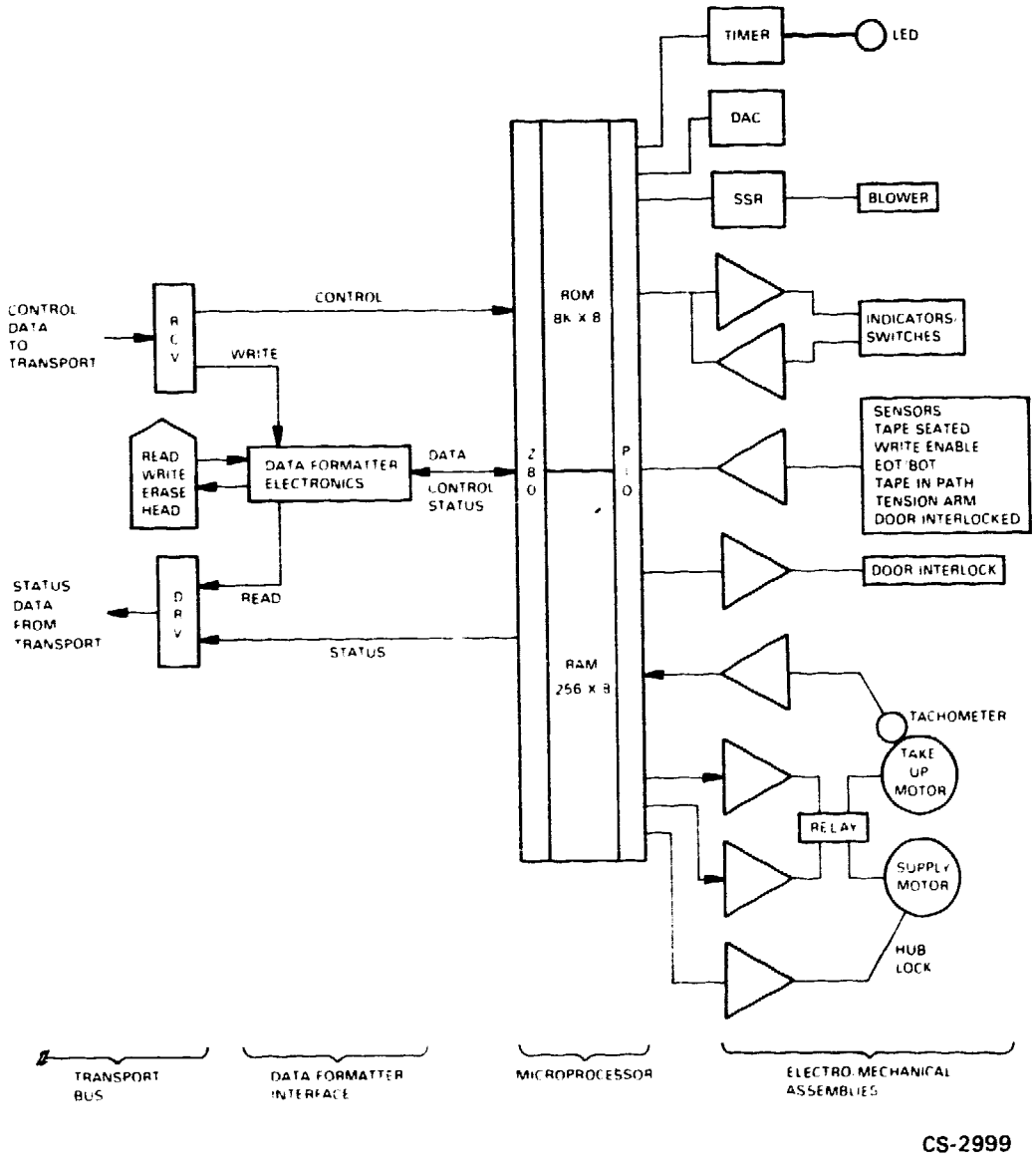


Figure 9-2 TS05 Tape Transport Block Diagram

9.2.2.3 Electromechanical Assemblies - The electromechanical assemblies include:

1. Timer — A watchdog timer is constantly pulsed by the microprocessor. If the microprocessor stops or if the power supply fails, the timer times out. This error condition lights a Light-Emitting Diode (LED) and shuts down the tape transport.
2. Digital-to-Analog Converter — By means of the VOUT signals, this drives the electric devices controlling the movement of the tape.
3. Analog-to-Digital Converter — By means of the VIN signals, this reads sensor voltages.
4. Solid-State Relay and Blower — The blower is turned on and off under the control of a PIO port.
5. Switches and Indicators — The front panel switches and indicators are directly controlled by the PIO port.
6. Sensors — The microprocessor monitors seven sensors:
   a. Tape reel seated
   b. Write enable ring
   c. End of tape photodiode
   d. Beginning of tape photodiode
   e. Tape in path photodiode
   f. Tension arm transducer
   g. Door interlocked
7. Door Interlock — This is a solenoid that locks the tape transport top cover and front door whenever tape is loaded.
8. Tachometer — This high resolution quadrature tachometer indicates tape speed and position.
9. Takeup Motor — The takeup motor moves the tape in the forward direction.
10. Motor Relay — This mechanical relay is closed under normal power ON conditions. If the watchdog timer times out, the relay opens. When this occurs, both the takeup and supply motors receive dynamic braking signals so as to stop the tape motion in a controlled manner.
11. Supply Motor — The supply motor moves the tape in the reverse direction.
12. Hub Lock Solenoid — This is actuated during the load operation to lock the supply reel onto the supply hub.

9.2.3 Major Data Flows

Each time the host computer system writes data to the tape subsystem, the data is both written on the tape and read off the tape. During write operations, the data is read off the tape immediately after it is written, in order to verify correct write operation. The writing and reading of data during a typical write operation proceeds as follows.

1. The host system software builds a command packet in its main memory specifying a write operation, the starting address of the data to be written, and the byte count. It then passes the address of this command packet to the M7196 interface/controller module.
2. The M7196 interface/controller module transfers the command packet from computer memory to its own logic, and identifies the operation to be performed. It then checks the tape transport unit to ensure that it is capable of performing the operation and that no error conditions exist. If the tape transport unit is ready, the controller instructs it to start tape motion.
3. The M7196 interface/controller module initiates a DMA transfer of the write data from computer memory to the controller DMA input file. From the input file, the data becomes available on the S-Bus.
4. The microprocessor takes data from the S-Bus and places it on the Y-Bus. From the Y-Bus, the data is held in a latch until it can be loaded into the FIFO register.
5. The data is loaded into the FIFO register and held for transfer to the tape transport unit.
6. When the tape is up to speed and the proper format characters are written on the tape, the tape transport logic requests the controller module to place data on the transport bus. (Thereinafter, the transport logic continues to request data as necessary to maintain the basic data rate until it is informed by the controller that the last data byte is in the FIFO.)
7. The data formatter electronics takes the data off the transport bus and converts it to the current profile required for driving the write head. The write head places the data on the tape.
8. When the tape being written by the write head reaches the read head, the read head reads the data off the tape and passes it back to the data formatter electronics.
9. The formatter electronics places the data on the transport bus, from which it is transferred to the M7196 interface/controller module for parity checking.
10. After the last byte of data has been written on the tape, the data formatter electronics writes the final format characters on the tape, and then places updated status information on the transport bus.

11. The M7196 interface/controller module recognizes that the tape transport has finished executing the write command, and it updates the message buffer (in the host computer memory) accordingly.

12. The controlling software checks the message buffer and finds that the TSV05 subsystem is ready for another command.

At this moment, the tape transport is still moving tape at the full read/write speed. If the controlling software issues another command of the same type within a short time (the reinstruct time), the TSV05 subsystem executes the command without having to stop and restart the tape. The TSV05 subsystem continues executing a stream of commands ("streaming") until the command type is changed or the reinstruct time is exceeded. Once a tape motion command falls outside the reinstruct time, however, the tape transport performs a tape repositioning cycle and then stops the tape.

9.3 FUNCTIONAL DESCRIPTION

This section describes the operation of the following:

- M7196 Q-Bus Interface/Controller Module
- M7196/TS05 Interface
- Tape Transport Unit

9.3.1 M7196 Q-Bus Interface/Controller Module Operation

The M7196 interface/controller module is compatible with the "MS" software at the device driver level. It uses an 8-bit bit slice microprocessor (200 nanosecond cycle time), 2K words of control store memory (58-bit words), and 4K bytes of RAM. The controller supports 16, 18, or 22 address lines, but not Q-bus parity. The block, or hog mode, DMA feature is not implemented. All critical time-dependent Q-bus register functions are handled in hardware. This relieves the microprocessor for packet protocol handling, buffer management, and tape drive control. The registers include:

1. TSDB (Data Buffer) — A write-only register used to load a command pointer address locating the command packet in host memory.
2. TSBA (Buffer Address) — A read-only register at the same I/O address as the TSDB. The TSBA reflects the main memory address being used by the controller.
3. TSSR (Status Register) — Indicates the status of the last completed command. The following three bits of this register are implemented in hardware.
   a. SSR (Subsystem Ready, <07>) — This bit is set after the controller (subsystem) has written a message buffer to system memory indicating that the controller is ready for a new command. (It is cleared on power-up, then set. It is also cleared after the system writes the TSDB.)
   b. RMR (Register Modification Refused, <12>).
      - If the system (host) attempts to write the TSDB when the SSR is cleared, then the RMR bit is set.
      - If the subsystem is to do an attention (it can only do an attention if it controls the message buffer), and SSR has been set for a long period of time, then the subsystem must first clear SSR. If this occurs at the same time the system tries to write the TSDB, then RMR is set.
   c. SC (Special Condition, <15>) — If RMR is set, or if the command was not completed without incident, then the SC bit is set.

The operation of the M7196 interface/controller module is discussed in detail in the sections that follow. Refer to the TSV05 Field Maintenance Print Set (MP-01157) to identify the devices being discussed.

9.3.1.1 Q-Bus Interface (Sheets D1 and D2) - The Q-bus interface circuitry includes the following.

1. Register Access Control — Access to the Q-bus registers is controlled primarily by a DC004 protocol chip and two Programmable Array Logic (PAL) devices (Table 9-1). Two I/O word registers are used for Q-bus transfers. These are the TSBA with TSDB (read and write), and the TSSR (read only; write resets the subsystem, although a write high byte is allowed by strapping). PAL01 and PAL02 are programmable AND-OR-INVERT gates, programmed to enable the DC005 bus transceivers and Q-bus registers at the proper time. Inputs to the PALs are primarily from the DC003 interrupt chip, the DC010 DMA control chip, and the Q-bus.

2. Q-Bus Latch — When the host system performs a write operation to the tape transport subsystem, the exact operation is latched into a 74LS174. This is necessary to distinguish maintenance writes (TSDB high byte or TSDB low byte) from command operations (TSDB word writes).

3. Interrupt Control — The key device controlling interrupts is the DC003 interrupt control chip. The TSV05 subsystem uses only one interrupt. The interrupt is created by clearing and subsequently setting the ENA DAT input of the DC003. This is done under microprocessor control. (The clearing is necessary since the device input is usually still set from the previous interrupt.)

4. DMA Control — DMA transfers are handled by a DC010 control chip, a 74S112, and a 74LS174. A DMA transfer is initiated by loading the Non-Processor Request (NPR) latch and requesting service by means of D7 EMIT 11 H. This is done with OUT BYTE, OUT WORD, or IN WORD. As the transfer is initiated (by D7 EMIT 11 H and D7 NPR ENAB L), D2 NPR BSY H and D2 NPR REQ H are set. The D2 NPR BSY H line remains set until the DMA transfer is complete. As the DMA sequence progresses (under the control of the DC010), addresses and data are stored in the Q-bus access registers (print set Sheet D3). D1 RRPLY H sets and D2 NPR REQ H is cleared. D2 NPR BSY H is cleared as a result of D1 RRPLY H being negated, and the DMA cycle is complete.

   If, however, D2 XSYNC H (DC010 SYNC) is asserted for more than 12 microseconds, the NPR abort timer aborts the DMA transfer.

   During the DMA transfer cycle, all address and data register selection is performed by the two PALs.

5. SSR Interlock — For purposes of software compatibility, the microprocessor emulates the TS11 tape transport subsystem at the Q-bus interface. In order to offload some of this task from the microprocessor, three real-time bits in the TSSR are handled by the hardware. These are SSR, RMR, and SC. This hardware performs the following functions:

   a. Sets the RMR and SC bits to indicate an error if the host system writes the TSDB when the SSR bit is cleared. (Writes to the TSDB are not allowed when SSR is in the cleared state.)

   b. Clears SSR and RMR if the host system writes the TSDB while SSR is set.

   c. Sets D1 Q WRT H when the host system writes to the TSV05 subsystem. This is used by the microprocessor to ensure the correct states of SSR and RMR in the event of the host system and the microprocessor attempting to modify the SSR bit simultaneously.

   These three status bits are placed on the DAL lines (by way of the 74LS244 in location E33) under the control of the PALs.

6. Address Bit Logic — Address bits <21:16> are latched (in AM2908s in E29 and E30) and used to drive the Q-bus directly. These bits are used in conjunction with address bits <15:00> (which are stored in the register file) for the address of DMA transfers.

Table 9-1 PAL Maps

PAL 01 (Location E32)

Output	Input
~D1 QRA	H =~D1 SEL0 L + D2 ADREN H
~D1 QRB	H =~D1 SEL0 L +~D1 SEL2 L + D2 ADREN H
~D1 QWA	H =~D1 SEL0 L
~D1 QWB	H =~D1 SEL0 L +~D1 SEL2 L
~D1 PMRST	L =~D1 SEL2 L *~D1 OUTLB L + D1 RINIT H
~D1 RCV	H =~D2 XDIN H * D1 OUTHB L * D1 OUTLB L * D1 RSYNC L +
	~D2 XDIN H * D1 SEL0 L * D1 SEL2 L * D1 RSYNC L +
	~D2 XDIN H * D1 OUTHB L * D1 OUTLB L * D2 ADREN H +
	~D2 XDIN H * D1 SEL0 L * D1 SEL2 L * D2 ADREN H
~D1 XMIT	H =~D2 DATEN L *~D2 ADREN H * D1 INWD L +
	~D2 DATEN L *~D2 ADREN H * D1 SEL0 L * D1 SEL2 L

PAL 02 (Location E31)

Output	Input
~D1 QGWHB	L = D2 SSR H *~D1 OUTHB L *~D1 SEL0 L +
	D2 SSR H *~D1 OUTHB L *~D1 SEL2 L + D2 XDIN H
~D1 QGWLB	L = D2 SSR H *~D1 OUTLB L *~D1 SEL0 L +
	D2 SSR H *~D1 OUTLB L *~D1 SEL2 L + D2 XDIN H
~D1 WTBT	H =~D2 OUT H * D2 BYT L +~D2 OUT H * D2 DATEN L +
	~D2 ADREN H * D2 BYT L +~D2 ADREN H * D2 DATEN L
~D1 RDSTATQ	L =~D1 SEL2 L *~D1 INWD L
~D1 RDREGQ	L =~D1 SEL0 L *~D1 INWD L + D2 ADREN H +~D2 DATEN L
~D1 WRTTSDB	H = D1 SEL0 L + D1 OUTHB L * D1 OUTLB L
~D1 BUSWRT	H = D1 OUTLB L * D1 OUTHB L + D2 SEL0 L * D1 SEL2 L

NOTE

PAL01 pin 18 (D1 RINIT H) and PAL02 pin 14 (D2 SSR H) are used as inputs. PAL01 pin 11 (D5 SW0 H) is not used. PAL16L8 devices, as shown in the above maps, define outputs as the not TRUE, that is, LOW driven, states.

9.3.1.2 CSR and Data Memory (Sheet D3) - The CSR and data memory circuitry includes the following:

1. Q-Bus Access Registers — Control, status, and data transactions between the Q-bus and the tape transport subsystem are performed using the 74LS670 4-bit x 4-word register files. The registers shown in the left column of devices on the right side of print set Sheet D3 hold all the TSV05-to-Q-bus data and the DMA address <15:00>. The registers shown on the right hold Q-bus-to-TSV05 data. Both sets of registers have independent address, read, and write controls. This allows them to be read and written independently, with no contention problems between the Q-bus and the microprocessor.

   Register selection is as follows:

   a. TSV05-to-Q-Bus

      00 TSBA and DMA address IN or OUT <15:00>

      01 TSSR <15:00>

      10 Not used

      11 DMA data out <15:00>

   b. Q-Bus-to-TSV05

      00 TSDB <15:00>

      01 TSSR <15:08> (See note)

      10 Not used

      11 DMA data in <15:00>

NOTE

A write low byte or write word from the Q-bus to the TSSR causes a master reset to the TSV05 subsystem. A write to the high byte of the TSSR does not cause a master reset. This register contains the boot bit and, if the EXTENDED FEATURES switch is ON, bits <18:21> of the TSDB.

2. RAM (55 nanosecond 6147P) — Eight 4K by 1-bit RAMs are used for data memory. The inputs are from the Y-Bus and the outputs are to the S-Bus. The RAMs can be addressed from either the 12-bit EMIT field or the 12-bit address latch. A RAM read occurs during the entire 200 nanosecond microcycle. A RAM write occurs during the last 100 nanoseconds of the microcycle.

3. RAM Address Latch (74LS374, 74S241) — The address for the RAM are from either the 74LS374s or the 74S241s. The 74LS374s are loaded from the microprocessor Y-Bus. (Two loads are required to update all 12 bits.) The 74S241s are used to directly address the RAM from the current operating microinstruction.

9.3.1.3 Tape Unit Interface (Sheet D4) - The tape unit interface includes the following circuitry:

1. Tape Format and Control Out -- This circuit comprises 74LS374 latches that hold the tape drive commands and associated latches.

2. Tape Data FIFO -- The tape data FIFO is a 64 x 8-bit register having a 5 megahertz shift in shift out rate and a 4 microsecond fall-through time. The direction of tape data flow is determined by D4 SEL OUT H. Data is transferred to the tape as follows:

   a. The tape data in buffer (74LS244) is disabled and the 74LS374 is enabled to supply data from the microprocessor. Tape data from the microprocessor is loaded into the 74LS374 on the second 100 nanoseconds of D7 T DAT OUT L. The pulse on D7 T DAT OUT L is delayed by one subsystem clock pulse (through 74S74) and then gated with D6 PSCLK L to produce a 100 nanosecond pulse that occurs during the second half of the subsystem clock period. This pulse is used to strobe data into the FIFO.

      The microprocessor uses D4 IN RDY L to monitor the input ready state of the FIFO.

   b. When the data reaches the bottom of the FIFO, D4 OUT RDY L asserts and indicates to the microprocessor that data is ready. The microprocessor then asserts D4 T DAT IN H to shift one byte of data into the tape data out register.

   c. The tape unit asserts D9 IWSTR each time it takes data. The FIFO is monitored for the presence of data. The empty state of the FIFO is indicated by D4 DAT OUT MISS H. If the FIFO becomes empty, D4 DAT OUT MISS H asserts and ILW (last word indicator) to the tape unit is set. If D4 OUT RDY L and D4 DAT OUT MISS H are true simultaneously, an error condition exists because ILW is sent to the tape unit even though there is still data in the FIFO. In this case, the entire buffer must be written to the tape again.

   d. The parity of the tape data out is monitored by a 74LS280. A parity bit (D9 IWP) is generated and sent to the tape unit.

   e. The parity of the tape data in is monitored by a 74LS280 and a 74LS112. A parity error is flagged by D4 PAR IN H.

3. Data is transferred from the tape as follows:

   a. The 74LS244 is enabled and the 74LS374 is disabled. D9 IRSTR from the tape unit indicates that data from the tape is ready. Its positive edge occurs 200 nanoseconds after the data is sent from the tape unit. This signal is delayed another 200 nanoseconds, then used to strobe data into the FIFO and latch any parity error from the 74LS280.

   b. When data reaches the bottom of the FIFO, D4 OUT RDY L is asserted, indicating that data is ready to be taken out of the FIFO.

   c. If the FIFO becomes full, D4 DAT IN MISS H is asserted on that D9 IRSTR.

   d. The microprocessor clears the FIFO by asserting D7 FRST L.

9.3.1.4 Program Sequencer and Tape Status In (Sheet D5) - The program sequencer and tape status in circuitry includes the following:

1. Tape Status In Logic — Tape status from the tape unit status lines is latched into 74LS34s at the subsystem clock rate. The 74LS34s are reset by the microprocessor using D7 T STAT RST L.

2. Program Sequencer — Three 2911s generate an 11-bit address (2K words) that sequences through the microinstruction ROMs. The 2911s can select an address from any of four sources.

   a. The EMIT field of the microinstruction. This is typically the branch address taken if a given condition is met as selected from the BUT multiplexer.

   b. An internal register holding an address from a previous EMIT field.

   c. An internal push/pop stack including control lines for nested subroutine linkages.

   d. An internal program counter. This usually contains the last address plus one.

   These 2911s are controlled directly by the microinstruction using D7 FE H, D7 SQ 1 H, D7 SQ 0 H, and D7 TEST INV H. Testing for conditional branching is supplied from the BUT multiplexer.

3. BUT Multiplexer — The BUT multiplexer is a condition code multiplexer that selects one of 23 conditions for the 2911 program sequencer. The selected output is first synchronized to the subsystem clock by a 74S74. The actual test selection is from the BUT field of the microinstruction.

9.3.1.5 Arithmetic Logic Unit (Sheet D6) - The ALU and its associated circuitry include the following devices.

1. 2901s — Two 2901 chips form the ALU and its 16 8-bit registers.

2. Subsystem Timing — A subsystem clock is produced by dividing the output of a 20 megahertz oscillator down to 5 megahertz. This goes to a timer and to other components. It also generates D6 DIS BUS L. This is a negative-going 25 nanosecond pulse, the leading edge of which coincides with the positive-going edge of D6 S CLK H (the subsystem clock). D6 DIS BUS L is used to disable all S-Bus drivers for 25 nanoseconds before any of the drivers are given control. This prevents bus contention problems.

3. Timer — The 5 megahertz clock from the system timing circuit is divided by 256 to produce D6 TIMER A H. This in turn is divided by 2 to produce D6 TIMER B H. These signals are used by the microprocessor for timing the duration of functions (for example, for computing the length of tape passed).

9.3.1.6 Pipeline Registers (Sheet D7) - The pipeline registers hold the current microinstruction that is to be executed. The microinstruction is loaded into the pipeline register directly from the ROMs by the system clock. This register allows the sequencer to look up the next instruction, while the current instruction is being executed.

9.3.1.7 Microprogram ROMs (Sheet D8) - Microprocessor instructions are contained in 56-bit words stored in a control store circuit. The control store comprises fourteen 2K x 4-bit ROMs. The ROMs are addressed by the 2911 program sequencer. For a description of the words, refer to Section 9.3.1.9.

9.3.1.8 Loopback Registers (Sheet D9) - Three 74LS244s perform the transport bus loopback function at the connectors, permitting board testing without the need for external loopback connectors.

9.3.1.9 Microprocessor Words - At the assembly level, the M7196 58-bit microinstructions are made up of four types of words.

1. Word 0 — ALU operations. This word occupies ROMs E115, E116, E111, and E112.
2. Word 1 — Register definitions and S-Bus and Y-Bus control. This word occupies ROMs E113, E114, E109, and E110.
3. Word 2 — Sequencer control and test selection. This word occupies ROMs E117, E119, and E120.
4. Word 3 — EMIT field and Q-Bus and strobe control fields. This word occupies ROMs E118, E121, and E122.

The functions of these words are summarized in Figures 9-3 through 9-6 and Tables 9-2 through 9-5.

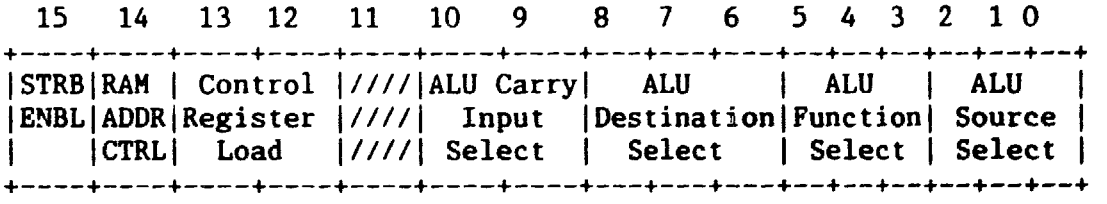


Figure 9-3 Word 0

Table 9-2 Word 0 - ALU Operations

ALU Source: [Bits (2:0)]

Decoded Operation Code	ALU Source Operands R	S
0	A	Q
1	A	B
2	0	Q
3	0	B
4	0	A
5	D	A
6	D	Q
7	D	0

ALU Function: [Bits (5:3)]

Decoded Operation Code	ALU Function
0	R Plus S
1	S Minus R
2	R Minus S
3	R Inclusive-OR S
4	R and S
5	Not-R and S
6	R Exclusive-OR S
7	R Exclusive-NOR S (Equivalence)

ALU Destination: [Bits (8:6)]

Decoded Destination Code	RAM Shift	RAM Load	Q-Res Shift	Q-Res Load	Y Output
0	X	None	None	F > G	F
1	X	None	X	None	F
2	None	F > B	X	None	A
3	None	F > B	X	None	F
4	Down	F/2 >B	Down	Q/2 >Q	F
5	Down	F/2 >B	X	None	F
6	Up	2F > B	Up	2Q > Q	F
7	Up	2F > B	X	None	F

Table 9-2 Word 0 - ALU Operations (Cont)

ALU Carry Input Select: [Bits (10:9)]

Decoded Operation Code	Carry Input
0	0 (LOW)
1	1 (HIGH)
2	Saved Carry-Out from Previous Cycle
3	Complement of Carry-Out from Previous Cycle

Bit 11 D8 RO 2911 EMIT H is not used.

Control Register Load Select: [Bits (13:12)]

Decoded Operation Code	Register Load
0	No Load
1	Tape Command Out (from Y-Bus)
2	Tape Control Out (from Y-Bus)
3	DMA Enable and Control

RAM Address Control: [Bit 14]

Bit 14 = 0	RAM Address Supplied from EMIT
Bit 14 = 1	RAM Address Supplied from Y-Bus

Strobe Enable: [Bit 15]

When set (in a symbolic microinstruction), enables code in EMIT (10:8) to produce one of eight strobe pulses. In the hardware, the strobe is enabled by a LOW (0) signal.

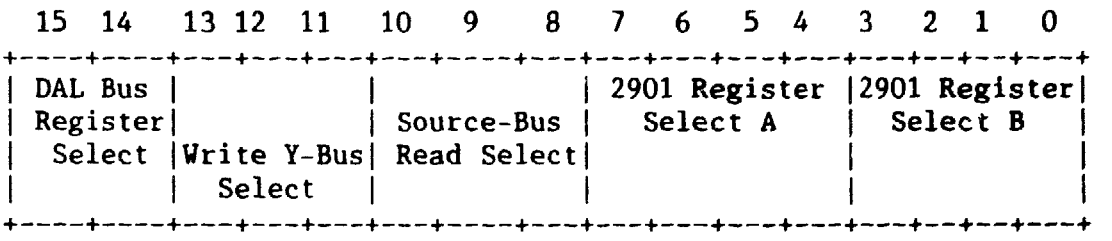


Figure 9-4 Word 1

Table 9-3 Word 1 - Register Definitions, S- and Y-Bus Control

Register Select: [Bits (7:0)]

The 2901 contains a 16 word dual-ported register RAM. These two groups of select bits enable one of 16 words for access.

NOTE

If both Read from RAM and Write to RAM are selected simultaneously, the Write to RAM takes precedence; data read from RAM (onto the S-Bus) is unpredictable.

SRC Bus Select: [Bits (10:8)]

Decoded Operation Code	SRC Bus Data Source
0	
1	RAM
2	FIFO (Tape Data In)
3	Tape Status 2 In
4	Tape Status 1 In
5	EMIT (7:0) (Literal Data)
6	DAL Bus Register (In-File) High Byte
7	DAL Bus Register (In-file) Low Byte

(Note that SRC code 0 is not used.)

Y-Bus Register Write: [Bits (13:11)]

(Data from the 2901 is written into the register selected by the following code.)

Decoded Operation Code	Register Written
0	NO-OP (No Register Loaded)
1	RAM
2	FIFO (Tape Data Out)
3	Extended DMA Address (Bits 18-21)
4	Memory (RAM) Address Register High Byte
5	Memory (RAM) Address Register Low Byte
6	DAL Bus Register (Out-File) High Byte
7	DAL Bus Register (Out-File) Low Byte

Table 9-3 Word 1 - Register Definitions, S- and Y-Bus Control (Cont)

DAL-Bus Register (In-File and Out-File) Select: [Bits (15:14)]

Selects a 18-bit register in the input file for Reading and/or a 18-bit register in the output file for Writing.

Assignments for Writing from Y-Bus:

Decoded Operation Code	Register Selected
0	TSBA and DMA Address
1	TSSR
2	2 is Not Used
3	DMA Data Out

Assignments for Reading onto S-Bus:

Operation Code	Register Selected
0	TSDB
1	TSSR
2	Not Used
3	DMA Data In

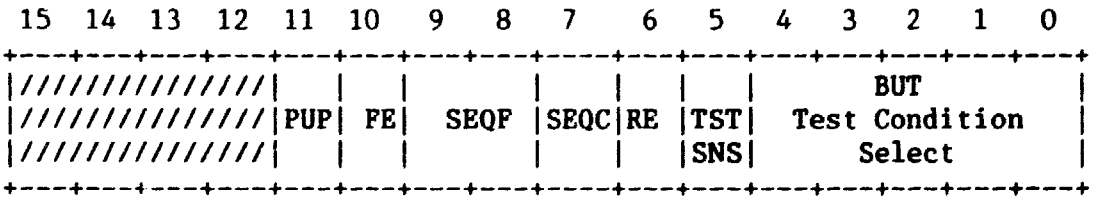


Figure 9-5 Word 2

Table 9-4 Word 2 - Sequencer Control and Test Select

Sequence Control [Bits (11:5)]

Bit 11 = 0 will pop, 1 will push data onto the stack if enabled.

Bit 10 = 1 will enable the push/pop function as determined by bit 11.

Bits 9:8 are decoded to determine the sequencer microaddress source.

0 = Program counter
1 = Address holding register
2 = Top of the push/pop stack
3 = Direct inputs, EMIT field

Bit 7 = Enables BUT test condition to effect sequencer operation. If the BUT condition is not met, the next microword is executed.

Bit 6 = Enables EMIT data into the internal address holding register.

Bit 5 = Inverts the conditional test, BUT, polarity.

BUT [Bits (4:0)]

Selects the condition to be tested to affect sequencer operation.

BUT Code		Signal
SW0H	Switch 0 (E58-9)	ON (Extended Features Enable)
SW1H	Switch 1 (E58-8)	ON (Buffering Enable)
MRSTL	D7 MRST L	(Master RESET)
OVRH	D6 OVR H	(2901 ALU Arithmetic Overflow)
F7H	D6 F07 H	(Most-Significant Bit of 2901 ALU Output)
COUTH	D6 COUT H	(2901 ALU Carry-Out)
FEQ0	D6 F=0 H	(2901 ALU Output is 0)

BUT Code		Signal
TIMAH	D6 TIMER A H	(51.2 second Timer)
TIMBH	D6 TIMER A H	(102.4 second Timer)
SEL0L	D1 SEL 0 L	(Bus Access to TSDB/TSBA)
SEL2H	D1 SEL 2 H	(Bus Access to TSSR)
OUTLBL	D1 OUT LB L	(Bus Write into Low Byte)
OUTHBL	D1 OUT HB L	(Bus Write into High Byte)
QBWRTH	D1 QWRT H	(Flag Indicating TSDB Written)

Table 9-4 Word 2 - Sequencer Control and Test Select (Cont)

BUT Code		Signal
DSEL2H	D1 SEL 2 H	(Previous Write was done to TSSRH)
SSRH	D2 SSR H	(Subsystem Ready Bit)
RMRH	D2 RMR H	(Register Modification Refused Bit)
NBSYH	D2 NPR BSY H	(NPR Busy - In Progress)
NXMH	D2 NPR ABORT H	(NXM Timer Timed Out)
ORDYL	D4 OUT RDY L	(FIFO Output Has Data)
MISSH	D4 DATA IN MISS H	(FIFO Input Overrun)
IRDYL	D4 IN RDY L	(FIFO Input Ready)
ILWL	D9 ILW L	(Last-Word Signal on Transport Bus - Should be Complement of MISSH)

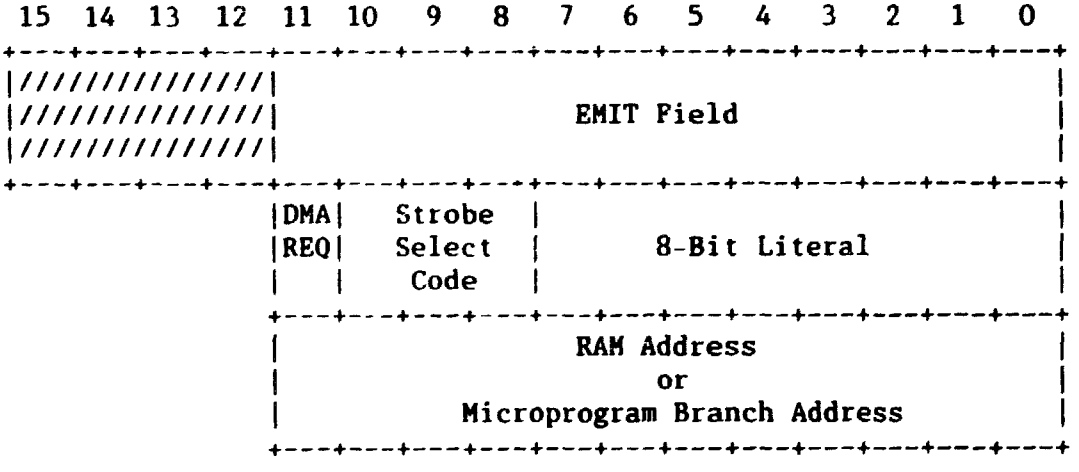


Figure 9-6 Word 3

Table 9-5 Word 3 - EMIT Field*, Q-Bus and Strobe Control Fields

Control Bits	EMIT Function
Word 0, Bit 14	EMIT bits [11:0] represent a RAM address.
Word 2, Bit 06 Bits 9:8	EMIT bits [11:0] represent a microprogram and branch address that is loaded into the sequencer.
Word 1, Bits 10:8	EMIT bits [7:0] represent a literal data value typically used for masking during comparison commands.
Word 0, Bit 15	EMIT bits [10:8] are decoded to make up eight strobe pulses.

Decoded Value	Strobe Pulse
0	Tape status reset
1	FIFO reset
2	Timer reset
3	Clear Q-bus latch (TSDB written flag)
4	Set RMR flag
5	Clear RMR flag
6	Set SSR flag
7	Clear SSR flag

Word 0, Bits 13, 12	EMIT bit 11 initiates a DMA request sequence.

* The EMIT field represents a variable data word whose value is dependent on other control bits within the microword.

9.3.1.10 Microprocessor Chip Description - The M7196 interface/controller module uses three 2911 chips and two 2901 chips for its microprocessor.

2911

The 2911 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in PROM. In the TSV05 controller, three 2911s are interconnected to generate a 12-bit address (4096 words). Eleven bits of the address are used to address 2048 words.

The 2911 can select an address from any of four sources.

1. A set of external direct inputs.
2. Data from the D inputs stored in an internal register.
3. A four-word deep push/pop stack.
4. A program counter register (which usually contains the last address plus one).

The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. The outputs are three-state. A separate line can be used to force all outputs to zeros.

The 2911 signals are defined in Table 9-6.

Table 9-6 2911 Signal Definitions

Signal Name	Description
S0-1	Address source selection control lines. These lines are decoded as follows. S1 S0 Y0-3 output source L L Microprogram counter L H Address/holding register H L Push/pop stack H H D0-3 direct inputs
FE-PUP	Push/pop stack control lines. These lines are decoded as follows. FE PUP Push/pop stack change H X No change L H Increment stack pointer, then push current PC onto stack L L Pop stack (decrement stack pointer)
RE	Internal address holding register enable line.
Z	Disables output lines Y0-3. Resets the microaddress to zero.
OE	Enables the output lines Y0-3; always TRUE.
CI	Carries input to the next stage.
D0-3	Direct data inputs.
CLK	Clock input.
Y0-3	Microaddress output lines.
CO	Carries output to the next stage.

2901

This is a 4-bit bipolar microprocessor slice designed as a high-speed cascadable element. Two such slices are cascaded together in the TSV05 controller, forming an 8-bit microprocessor data path.

The device consists of a 18-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding, and multiplexing circuitry. The 9-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable (the TSV05 controller cascades two with ripple carry), has three-state outputs, and provides various status flag outputs from the ALU. The 2901 signals are defined in Table 9-7.

Table 9-7 2901 Signal Definitions

Signal Name	Description
A0-3	The first of four address inputs to the register RAM used to select one register whose contents are displayed through an internal port.
B0-3	The second of four address inputs to the register RAM used to select one register whose contents are displayed through an internal port, and into which new data is written when the clock goes LOW.
I0-8	The nine instruction control lines. Used to determine what data sources are applied to the ALU, what function the ALU performs, and what data is deposited in the Q-register or the register RAM.
Q3 RAM3	A shift line at the MSB of the Q-register (Q3) and the register RAM (RAM3). Electrically, these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code indicates an up shift, the three-state outputs are enabled and the MSB of the Q-register is available on the Q3 pin and the MSB of the ALU output is available on the RAM3 pin. Otherwise, the three-state outputs are OFF (high impedance), and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q-register and the RAM.
Q0 RAM0	Shift lines like Q3 and RAM3, but at the LSB of the Q-register and RAM. These pins are tied to the Q3 and RAM3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q-register and ALU data.
D0-3	Direct data inputs. A 4-bit data field that can be selected as one of the ALU data sources for entering data into the device. D0 is the LSB.
Y0-3	The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register RAM, as determined by the destination code.
$\overline{OE}$	Output enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic 2's complement operation has overflowed into the sign-bit.
F = 0	This is an open collector output that goes HIGH (OFF) if the data on the four ALU outputs F0-3 are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

Table 9-7 2901 Signal Definitions (Cont)

Signal Name	Description
FE	The most significant ALU output bit.
CIN	The carry-in to the internal ALU.
COUT	The carry-out of the internal ALU.
CP	The clock input. The Q-register and register RAM outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM that compromises the "master" latches of the register RAM. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register RAM.

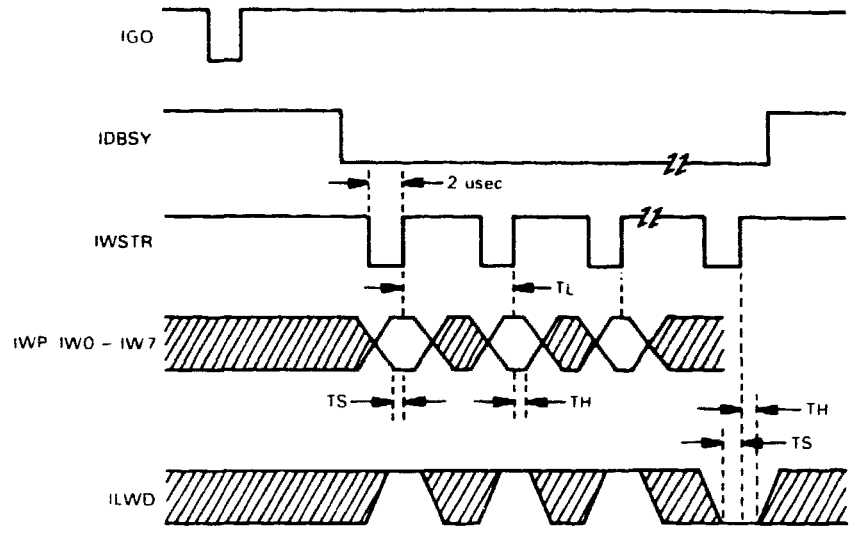
9.3.2 M7196/TS05 Interface

The M7196 interface/controller module connects to the TS05 tape transport unit with two 50-conductor ribbon cables. Electrically, these cables form a bus over which the two components communicate. The signal lines are terminated by 220/330 ohm resistor networks and carry standard TTL level signals. All interface signals are active LOW (0 volt = TRUE) unless specified otherwise in the descriptions that follow.

9.3.2.1 Interface to Tape Unit - Pin assignments and names of signals sent to the tape transport from the M7196 interface/controller module are listed in Table 9-8. All interface signal names begin with "I". Signal timing is indicated in Figures 9-7 through 9-9. The functions of the signals are as follows.

Table 9-8 Interface Signals to Tape Transport Unit

Plug No.	Live Pin	Ground Pin	Signal Description	Signal Name
P1	4	3	Last Word	ILWD
P1	6	5	Write Data 4	IW4
P1	8	7	Initiate Command	IGO
P1	10	9	Write Data 0	IWO
P1	12	11	Write Data 1	IW1
P1	16	15	Reserved	-
P1	18	17	Reverse	IREV
P1	20	19	Rewind	IREW
P1	22	21	Write Data Parity	IWP
P1	24	23	Write Data 7	IW7
P1	26	25	Write Data 3	IW3
P1	28	27	Write Data 6	IW6
P1	30	29	Write Data 2	IW2
P1	32	31	Write Data 5	IW5
P1	34	33	Write	IWRT
P1	36	35	Reserved	-
P1	38	37	Edit	IEDIT
P1	40	39	Erase	IERASE
P1	42	41	Write File Mark	IWFM
P1	14	13	Reserved	-
P1	46	45	Transport Address 0	ITADO
P2	18	17	Formatter Enable	IFEN
P2	24	23	Rewind/Unload	IRWU
P2	46	45	Transport Address 1	ITAD1
P2	48	47	Formatter Address	IFAD
P2	50	49	High-Speed Select	IHISP



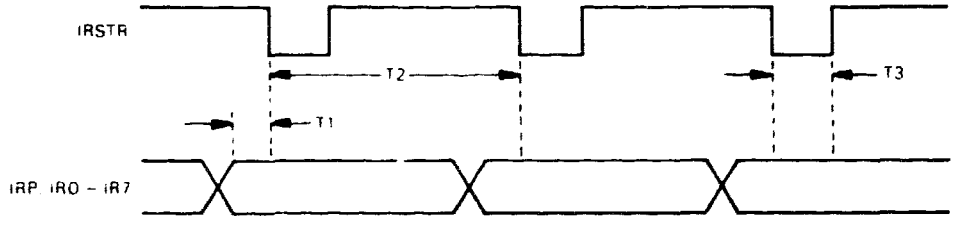
TS = 300 NANOSECONDS (MINIMUM)

TH = 0 NANOSECOND (MINIMUM)

TL = 25.00 MICROSECONDS @ 25 IPS
= 6.25 MICROSECONDS @ 100 IPS

CS-3000

Figure 9-7 Write Strobe Timing



T1 (MINIMUM) = 100 NANOSECONDS

T2 (MINIMUM) = 3.5 MICROSECONDS @ 100 IPS
= 14 MICROSECONDS @ 25 IPS

T2 (AVERAGE) = 6 MICROSECONDS @ 100 IPS
= 25 MICROSECONDS @ 25 IPS

T3 (NOMINAL) = 1 MICROSECOND

CS-3001

Figure 9-8 Read Strobe Timing

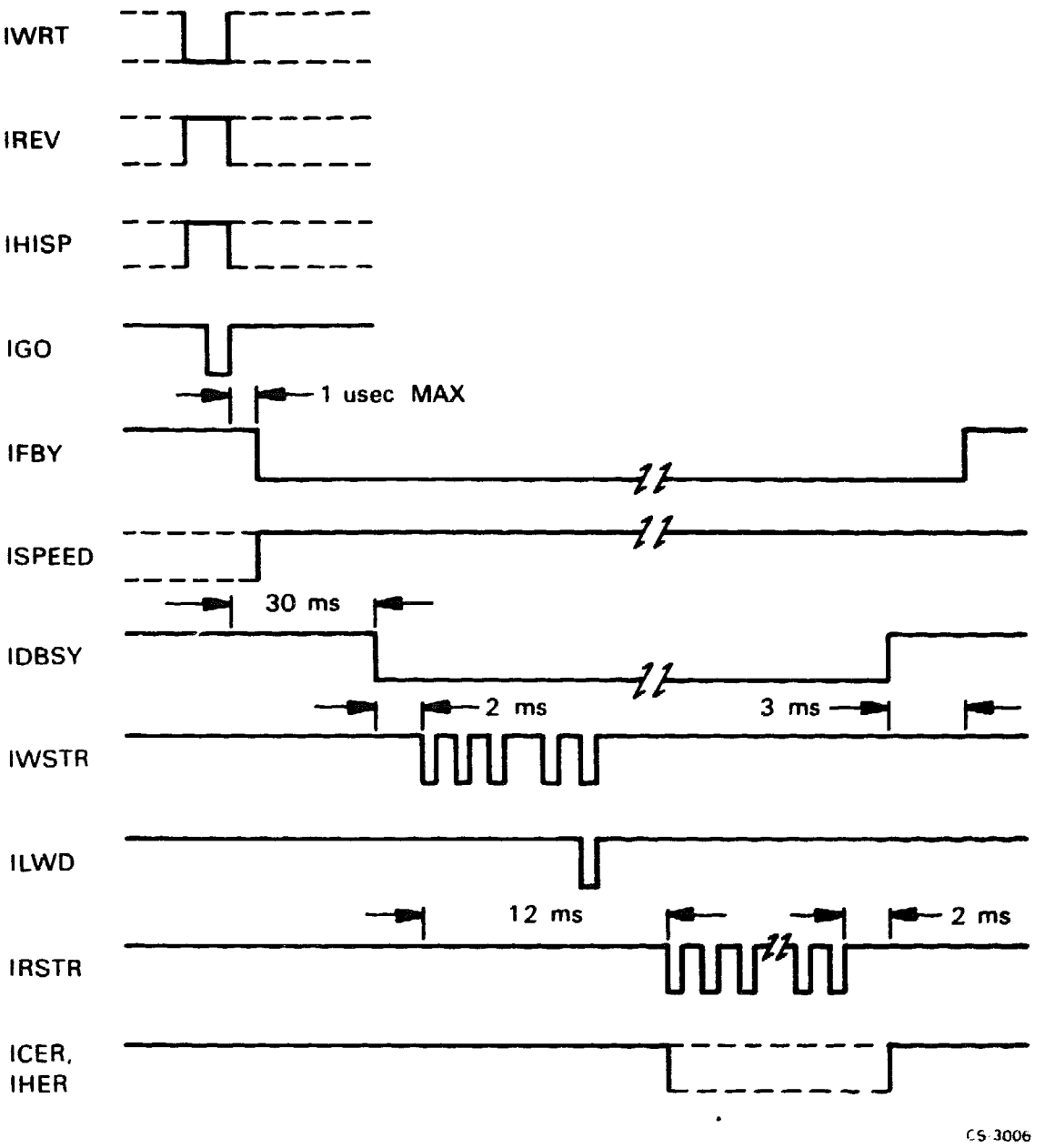


Figure 9-9 Write Forward [64 cm/s (25 in/s)]

IGO

This is a pulse of 1 microsecond minimum duration. The trailing edge initiates tape motion of the selected ready tape drive and latches the command into the formatter register. The commands are initiated by this pulse. The formatter address lines must be held constant from the leading edge of IGO until IFBY is negated.

IREW

A pulse of 1 microsecond minimum duration initiates a rewind in the selected ready (not at load point) tape drive. If the selected tape drive is at load point, the command is ignored. The rewind command does not use IFBY or IDBY. The IRWD status asserts within less than 1 microsecond, while IRDY is negated. A new command to this drive is delayed until the status IRDY is TRUE and IRWD is FALSE. The physical operation of a rewind involves running at 25 inches/second for about 51 centimeters (20 inches) in the forward direction before the reverse motion occurs. The drive runs reverse with the fastest reel motor near the microprocessor-controlled maximum speed. When the tape reaches BOT, the drive ramps down and returns to BOT where it stops, setting IBOT and IRDY, and resetting the IRWD status.

IRWU

This is a pulse of 1 microsecond minimum duration that:

1. Clears the ON-LINE flip-flop.
2. Generates a rewind.
3. Unloads the tape and unlocks the door.

The tape unit indicates IRDY and IONL are FALSE within 1 microsecond of the command.

ILWD

This is a flag associated with the last write data character. The setup time must be at least 300 nanoseconds before the trailing edge of IWST. There is no hold time requirement. This flag is also used to terminate the write command and variable length erase operation.

IFEN

For normal conditions, this signal must be asserted by the controller. This signal may be pulsed high (2 microseconds minimum) to reset a read, search, or write command run-away during DBSY. It is ignored when DBSY is FALSE. Command termination occurs within 50 milliseconds with a normal sequence, terminate rewind, unload, erase fixed, write file mark, or extended status command since these commands cannot "run away". By limiting the IFEN in this way, all "run aways" can be terminated in an orderly manner without loss of tape information.

IWP, IWO-7

These are write data. They must be set up with the same timing as ILWD. The tape track binary weight format is:

Head Physical - 1 2 3 4 5 6 7 8 9

Binary Weight - 22 20 24 P 25 26 27 21 23

R/W Data Bit - 5 7 3 P 2 1 0 6 4

IFAD, ITAD0, ITAD1

These are address lines to the tape drive. Address decoding is as follows.

Interface			Address Switches		
IFAD	ITAD0	ITAD1	S1	S2	S4
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

NOTE

Address lines must be set up a minimum of 1 microsecond before a command is issued or status is polled. Address zero is the only supported configuration.

IREV, IWRT, IWFM, IEDIT, IERASE

These lines are decoded to produce the commands. They must be set up a minimum of 300 nanoseconds before the trailing edge of IGO. Since they are latched in the tape drive, there is no hold time requirement.

IHISP

When IHISP is asserted, the tape drive operates at 100 inches/second. This line must be set up a minimum of 1 microsecond before the trailing edge of IGO. Since it is latched in the tape drive, there is no hold time requirement. Repositioning is automatic when switching speed, thereby delaying the first command by about 400 milliseconds.

RESERVED

These lines are reserved for future options.

9.3.2.2 Interface to Controller - Pin assignments and names of signals sent to the M7196 interface/controller module from the TS05 tape transport are listed in Table 9-9. The functions of the signals are as follows.

IFBY

This signal is asserted within 1 microsecond after the trailing edge of IGO, and is negated after command completion.

IDBY

This signal is asserted after any repositioning, and stays TRUE during the active execution of all commands initiated by IGO. On the trailing edge of this signal, another command of any type, direction, or speed can be given. There is no restriction as to type of direction, or speed. IDBY goes TRUE as soon as the MTSU is positioned in the correct IRG, and a data record or file mark can occur. IDBY goes TRUE at least 100 microseconds before any data transfer, EOF, or block detection.

Table 9-9 Interface Signals to Controller

Plug No.	Live Pin	Ground Pin	Signal Description	Signal Name
P1	2	1	Formatter Busy	IFBY
P1	44	43	Reserved	-
P1	48	47	Read Data 2	IR2
P1	50	49	Read Data 3	IR3
P2	1	-	Read Data Parity	IRP
P2	2	-	Read Data 0	IR0
P2	3	-	Read Data 1	IR1
P2	4	-	Load Point	ILDP
P2	6	5	Read Data 4	IR4
P2	8	7	Read Data 7	IR7
P2	10	9	Read Data 6	IR6
P2	12	11	Hard Error	IHER
P2	14	13	File Mark	IFMK
P2	16	25	Identification	IDENT
P2	20	19	Read Data 5	IR5
P2	22	21	End of Tape	IEOT
P2	26	25	Reserved	-
P2	28	27	Ready	IRDY
P2	30	29	Rewinding	IRWD
P2	32	31	File Protect	IFPT
P2	34	33	Read Strobe	IRSTR
P2	36	35	Write Strobe	IWSTR
P2	38	37	Data Busy	IDBY
P2	40	39	High-Speed Status	ISPEED
P2	42	41	Corrected Error	ICER
P2	44	43	On-Line	IONL

IDENT

This signal is pulsed when reading or writing from load point and the PE identification burst is detected. The IDENT line is tested on the trailing edge of ILDP. When a write command is started at BOT, an ID burst of about 13 to 15 centimeters (5 to 6 inches) overlapping the BOT marker is generated. When a read command is executed, the recorded ID burst is sampled at about the leading edge of the BOT marker. An ID burst is detected by the presence of more than 80 character periods where only the P channel is recorded with other channels erased. The absence of an ID burst does not prevent the MTSU from reading an otherwise valid 1600 bits/inch tape.

IHER

This signal is pulsed if the record being written or read contains an uncorrectable error. The line goes LOW when an error is detected during IDBY. Error conditions asserting this line include:

1. Multitrack Dropout — Two or more tracks have analog envelopes dropping below the operating threshold before passing through the postamble.
2. Uncorrectable Parity Error — All tracks have valid envelopes but the parity is even and the postamble has not yet been detected. This error is caused by writing incorrect parity when the external write parity option is selected.
3. Nonzero Character in Postamble — The only allowable character in the postamble is a zero (with even parity). This is checked during the first 20 postamble character intervals.
4. Excessive Skew — This error detection is indirect. A character bit is lost, causing an unavoidable postamble detection failure and consequent parity error when entering the postamble.
5. Loss of Data Envelope After Postamble Detection — Twenty character intervals are allowed after the postamble to provide time for the postamble to end and envelope detectors to decay. At the end of this time, there must be at least eight quiescent data channels, or else an error is reported.

ICER

This signal is pulsed when a single track dropout is detected and error correction is in process. This occurs before IDBY goes FALSE. These pulses occur throughout the rest of the data block. They range in width from 100 nanoseconds to over 10 microseconds. These pulses must be latched to be sensed at the IDBY transition.

IFMK

This line is pulsed on a write verification or read operation when an IBM/ANSI compatible file mark is detected. This occurs prior to IDBY going FALSE. If a file mark is not detected during a file mark write operation, the bad file mark must be backspaced with a space reverse command and the file mark must be rewritten. For maximum data reliability, a file mark is detected using majority logic. A filemark is sensed when any two of three tracks that must be present (Channels 2, 6, and 7) are present for at least 15 character periods and all three of the erased channels (Channels 1, 3, and 4) are absent. This technique provides automatic dead track recovery of file marks.

IRDY

This signal indicates tape is tensioned and is not rewinding, off-line, loading, or unloading. In the event of a hard fault shutdown, the drive goes off-line and not ready. This line is used to precondition any tape drive command.

IONL

This signal indicates the tape drive ON-LINE flip-flop is set. The drive is placed on-line during or after a tape load operation. This signal is negated within 1 microsecond of the reception of an unload command. When IONL is FALSE, IRDY is also FALSE. If the transport is manually placed off-line during a rewind operation, this signal remains TRUE until BOT is reached.

IRWD

This signal indicates the tape drive is in a rewind to beginning of tape sequence. The status goes TRUE within 1 microsecond of the rewind command and stays TRUE until the tape returns to BOT IRDY is negated while the drive is rewinding.

IFPT

This signal indicates the loaded reel has no write permit ring, hence the write electronics are disabled, and write commands are prohibited. This status goes TRUE during the tape load sequence before the drive goes ready This status is valid at all times once tape is loaded.

ILDP

This signal is asserted when the load point reflective marker is logically at the sensor. Since normal operation requires long ramps and repositions, when a command is executed at BOT the ILDP status remains TRUE during the repositioning. This is especially noticeable at 254 centimeters/second (100 inches/second) when ILDP remains TRUE for 0.5 second after a command. If a reverse command runs into BOT, a command reset occurs with ILDP being set. If an illegal reverse command occurs at BOT, ILDP remains TRUE but IFBY and IDBY sequence quickly (< 10 milliseconds) in order to retain compatibility with other commands. ILDP goes TRUE only at the end of a rewind, and is not set even when crossed over physically by the drive if the drive is "repositioning" and is not logically at the BOT marker.

IEOT

This signal is asserted to indicate the end of tape condition [less than 4.6 meters (15 feet) of tape remaining on the reel] and is negated to indicate that a rewind or reverse operation over the EOT marker has occurred. The signal is programmable to the extent that its assertion or negation can be delayed up to a maximum of three data blocks. That is, the end of tape reflective marker can be up to three data blocks pass the end of tape sensor before IEOT is switched.

ISPEED

This signal is asserted when the tape drive is operating in the high-speed mode. The signal is valid after IDBY goes TRUE for the associated command. This signal is latched until after the next IGO command.

IWSTR

This is a pulse, the trailing edge of which indicates that the character on the data lines has been written on tape and the next character is needed. The next character and last word flag must have a setup time of at least 300 nanoseconds before the trailing edge of IWSTR. The frequency of the IWSTR pulse is proportional to tape speed times bit density. The width of IWSTR is 2 microseconds nominal.

$$fw = V \text{ bits/inch}$$

for example:

at 254 centimeters/seconds (100 inches/second) PE

fw = 160,000 bytes/second

IRSTR

This signal is a pulse indicating a read character is available to the interface. Note that although the average long-term transfer rate is the same as for write data, due to skew and velocity change the instantaneous rate is almost twice that of the write data. The fall of IDBY is used to indicate the end of a command since not all read and write commands produce read strobes. The width of IRSTR is 1 microsecond nominal.

IRP, IRO-7

These are data lines to the interface. The read data overlaps IRSTR by at least 500 nanoseconds.

RESERVED

These lines are reserved for future options.

9.3.3 TS05 Tape Transport Unit

The TSV05 subsystem tape transport unit (TS05A) responds to the transport bus control lines with status or data, depending on the command issued. The unit includes a microprocessor consisting of the following.

1. Z80 microprocessor chip
2. 8K x 8 ROM
3. 8 x 256 RAM
4. 4 x PIO

The microprocessor directly controls electromechanical subassemblies and indirectly controls the data formatter electronics. The actual read and write data are not directly controlled by the microprocessor.

9.3.3.1 Tape Transport Operation - The following sequence of events occur when the tape transport unit receives a write command over the transport bus from the M7196 interface/controller module.

1. The microprocessor checks that the tape is properly loaded, the transport is on-line, and the write enable ring is installed in the supply reel.
2. If these conditions are TRUE, the microprocessor switches on drive current to the takeup motor to begin forward tape motion. It uses feedback from the tachometer to ensure the proper forward startup ramp profile. During this startup, and during the remainder of the sequence, the microprocessor constantly scans the sensors. If it detects a fault condition, it causes a double blink of the front panel LEDs. Additionally, a fault condition causes a mechanical relay to deactuate, resulting in dynamic motor braking such that the tape is not damaged, and switches on the system failure LED.
3. At the end of the startup ramp, the tape is moving at its full read/write speed of 64 or 254 centimeters/second (25 or 100 inches/second). Nominal tape tension is maintained by a drag current provided to the supply motor. The microprocessor controls the drag current based on feedback from the tension arm transducer. The microprocessor continues to control tape speed and tension by analyzing feedback from the tachometer and tension arm transducer and controlling the drive and drag currents.
4. Using the tachometer feedback, the microprocessor determines the amount of tape moving past the read/write/erase heads. When a nominal 1.5 centimeter (0.6 inch) gap is present between the last record and the write head, the microprocessor directs the formatter to place the 40-character preamble on the tape and then write the data bytes obtained from the transport bus.

5. After the last data byte is written on the tape, the formatter writes the 40-character postamble on the tape, thus completing the record.

6 Tape motion continues at the full read/write speed another 1.5 centimeters (0.6 inch). If the tape transport microprocessor receives another command of the same type within the time it takes for the 1.5 centimeter (0.6 inch) gap to occur (the reinstruct time), tape motion continues and the command is executed. If, however, a different type of command or no command is received, the microprocessor begins a tape repositioning cycle.

Throughout this sequence, the microprocessor places operational or error status on the transport bus to the M7196 interface/controller module.

Signals used within the tape transport electronics are shown in the vendor print set and defined in Appendix E.

9.3.3.2 Tape Transport Microprocessor - The TS05 tape transport unit uses a single chip Z80 microprocessor. Its internal registers contain 208 bits of read/write memory that are accessible to the program. These registers include two sets of general-purpose registers that may be used individually as 8-bit registers or as 18-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of exchange instructions makes either set of main or alternate registers accessible to the program. The Z80 also contains a stack pointer, program counter, two index registers, a refresh counter register, and an interrupt register.

The Z80 PIO parallel I/O circuit is a programmable, dual-port device that provides a TTL compatible interface between peripheral events and the Z80 CPU. Each port has eight data bits and two handshaking signals, ready and strobe, that control data transfers.

The Z80 CTC counter/timer has four independent channels. Each channel is individually programmed with two words: a control word and a time constant word. The control word selects the operating mode, counter or timer, and selects operating parameters. The time constant word is a value between 1 and 256. The CTC provides general system requirements of event timing, interrupt and interval timing, and clock rate generation.

9.4 FIRMWARE DESCRIPTION

The TSV05 subsystem has four main areas of functionality implemented in firmware.

1. Diagnostic (power up, main loop, TSDB byte wrap)
2. Attention handler
3. Get command
4. Process command

The relationship of these areas to one another is illustrated in Figure 9-10. This section describes each of these main functional areas. It also discusses troubleshooting with the diagnostics and the use of the boot code.

9.4.1 Diagnostic

9.4.1.1 Power-Up - The firmware of the M7196 interface/controller module includes self-test diagnostic code that is executed at power-up. The power-up diagnostic code tests the 2901-based microprocessor to the extent of assuring that it does hang or produce meaningless error indications. These diagnostics do not fully test the Q-bus interface or the tape transport bus interface. They run with or without the tape transport cables installed.

The power-up self-test diagnostics are started or restarted under the following conditions:

- After the bus initialize signal is negated due to a power-up or reset command, and
- After a write word type command into the TSSR.

Note that SSR is cleared whenever self-test diagnostics are running. Successful startup of the diagnostics is indicated by the PROC OK LED and the contents of the TSSR.

There are three LEDs located in the top center area of the M7196 interface/controller module. During the running of the firmware diagnostics, the LEDs have the following meanings.

- D1 = SSR — D1 is OFF when SSR = 1.
- D2 = PROC OK — D2 is ON during self-test. It blinks during the main loop test if there are no errors.
- D3 = TRANSMIT — D3 is OFF during self-test. If it is ON continuously, it indicates that the M7196 is hanging the Q-bus.

The status of the self-test diagnostics is obtained by examining the contents of the TSSR (standard address is 772522). This register is updated at the beginning of each test. If a test fails, the processor stops at the failing test (except for test 13, the RAM test) and the TSSR contains the test number. The test number is read from the TSSR, and the diagnostics restarted. The meanings of the contents of the TSSR pertaining to the power-up self-test diagnostics are listed in Table 9-10. The octal representation of the low order bits gives the number of the failing test. Note that a test 13 failure may not be apparent until the main loop code has begun executing.

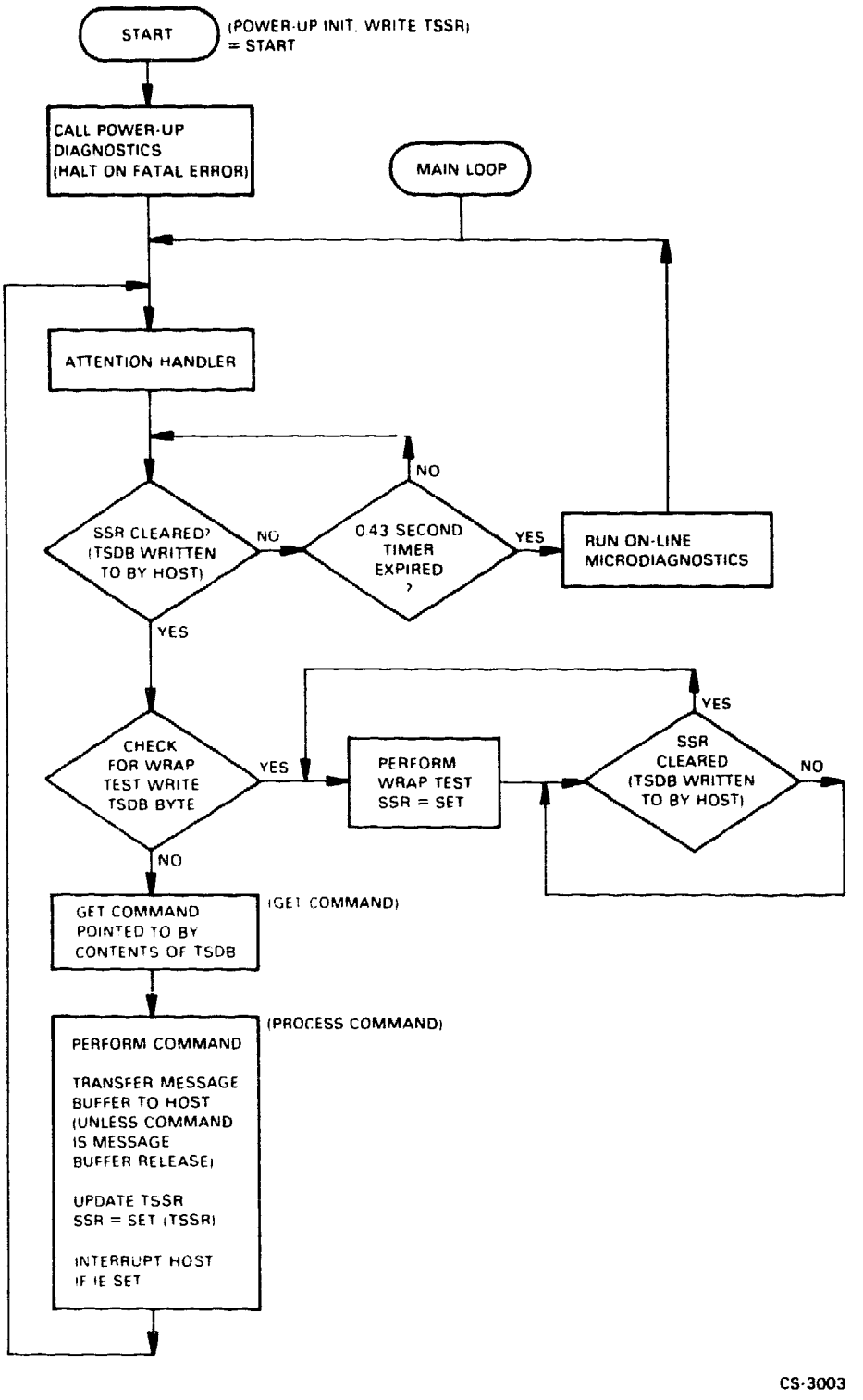


Figure 9-10 TSV05 Operation

Table 9-10 TSSR Contents for Power-Up Diagnostics

Test or State	TSSR Value	Bit Status	Comments
Start		Not accessible	INIT or write word to TSSR.
Test 17	066017	SSR = 0	Jump test. Other bits set in TSSR are for operating system compatibility.
Test 16	066016	SSR = 0	Conditional jump test.
Test 15	066015	SSR = 0	ALU sign test.
Test 14	066014	SSR = 0	ALU function test.
Test 13	066013	SSR = 0	RAM test. This TSSR value is present only if the main loop code is not entered properly. This test resets a hardware timer for use as a scope sync point at E20 pin 13 (D7 TIMER RST L). In the event of a failure, this test does not hang, but sets an internal error flag.
Initialize			No error checking performed.
Enter main loop	102313	SC = 1 NBA1 = 1 SSR = 1 OFL = 1	Test 13 (RAM test) loop failed.
	2300	NBA = 1 SSR = 1 OFL = 1	Power-up self-test diagnostics successfully completed.

9.4.1.2 Main Loop - After the successful completion of the power-up diagnostics, the main loop code begins executing. This is indicated by the center LED (PROC OK) blinking. Also, the TSSR contains the value 2300, indicating that NBA, OFF-LINE, and SSR are set (Table 9-11). If, however, the tape transport is cabled, loaded with tape and placed on-line, the TSSR contains 2200 and OFF-LINE is cleared. Note that the TSSR is not automatically updated by placing the tape transport on-line or off-line. In this case, the TSSR is updated after a bus initialize or a write word type command to the TSSR is issued.

Once the microprocessor enters the main loop, it checks to see if the TSDB has been written. If the TSDB was written (with the starting address of a command packet), the system executes the command and returns to the main loop (Figure 9-11). If the TSDB was not written, the microprocessor checks to see if a 430 millisecond timer has timed out. If it has not, the microprocessor checks again for the receipt of a command (write to the TSDB). If the 430 millisecond timer has timed out, the microprocessor executes the MICRO 1 and MICRO 2 diagnostic tests.

Table 9-11 TSSR Contents During Main Loop Diagnostics

Test or State	TSSR Value	Bit Status	Comments
Initialize			No error checking performed.
Enter main loop	2300	NBA = 1 SSR = 1 OFL = 1	This value pertains to the power-up diagnostic test results. 2300 indicates that the power-up diagnostics completed successfully.
Wait 430 ms	2300	NBA = 1 SSR = 1 OFL = 1	
MICRO 2	2300	NBA = 1 SSR = 1 OFL = 1	FIFO test. Failure sets an internal error flag.
MICRO 1	2300	NBA = 1 SSR = 1 OFL = 1	RAM test. Failure sets an internal error flag.

If an error is detected by either of the two diagnostics, the microprocessor sets an internal error flag and continues to loop, checking for commands and checking the timer. When a command does arrive, the microprocessor checks the status of the internal error flags before exiting the main loop to execute the command. The status at the point where program execution exits the main loop is obtained by examining the contents of the TSSR (Table 9-12). There are several possibilities.

1. If a valid command (other than write characteristics or write subsystem memory commands) is issued and the internal error flag is set, an immediate error occurs, resulting in SC = 1, SSR = 1, and TCC = 7.
2. If a valid write characteristics command or write subsystem memory command is issued, the microprocessor may be able to execute the command. If the command is executed successfully, SC = 0 and SSR = 1. If the command is not executed successfully, SC = 1, SSR = 1, and TCC = 3 or 7, depending on the type of failure.
3. If an invalid command is issued and the internal error flag is set, the subsystem attempts to report the status of the invalid command execution. In this case, the contents of the TSSR may be ambiguous, depending on the nature of the error and the command.
4. If the internal error flag is not set and there are no errors during command execution, the TSSR has SC = 0 and SSR = 1.

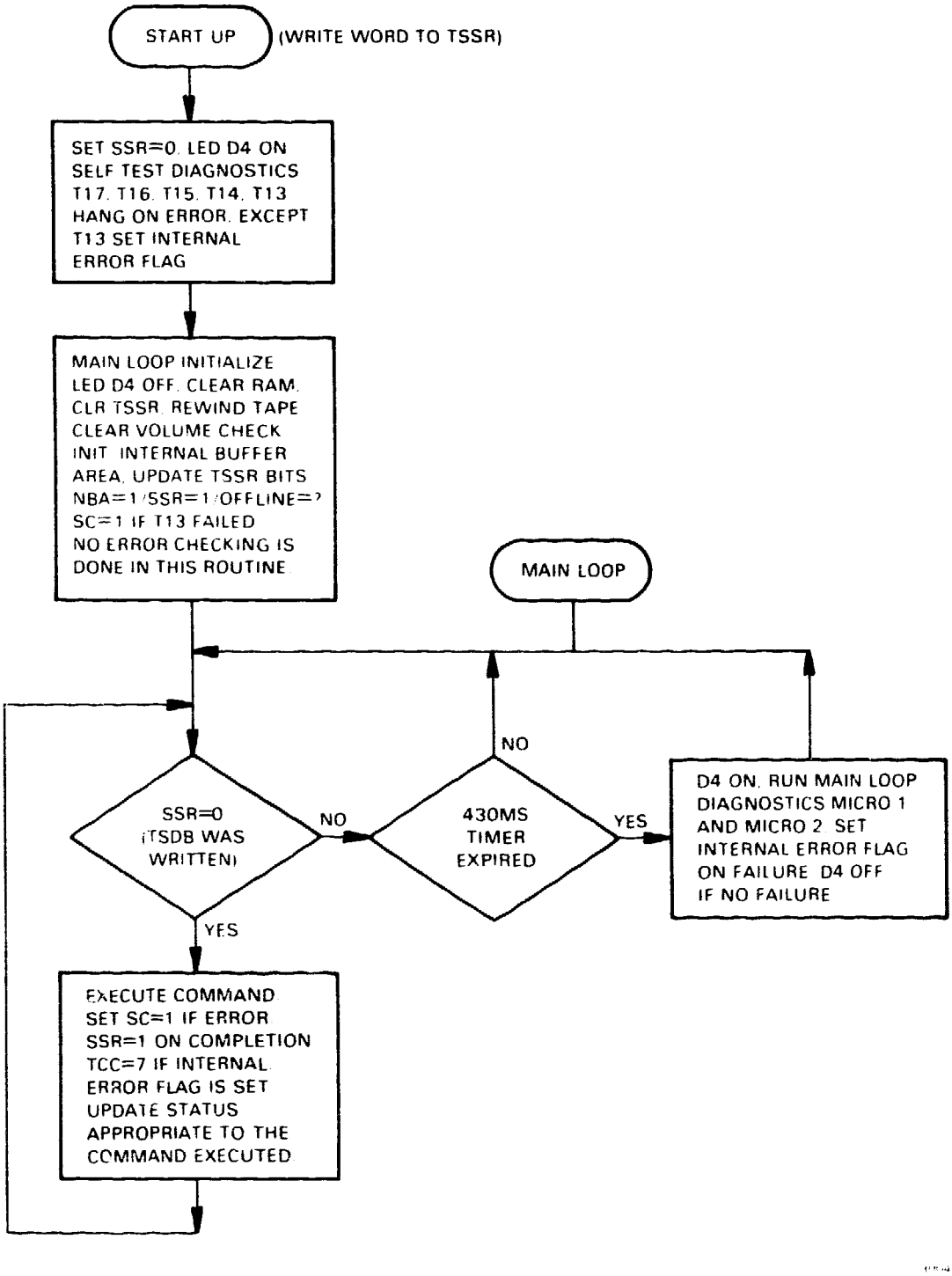


Figure 9-11 Diagnostic Flowchart

Table 9-12 TSSR Contents After Main Loop is Exited

Test or State	TSSR Value	Bit Status	Comments
Write TSDB Pointer	2200	NBA = 1 SSR = 1	The transport is on-line, there are no self-test errors, and a command can be issued. Since NBA = 1, the command must be a valid write characteristics command. SSR = 0 until command completion.
	200	SSR = 1 SC = 0	Successful completion of any command. A new command can be issued.
	1002XX	SC = 1 SSR = 1 TCC = X	Subsystem error resulted from command. Refer to last command. Refer to the TCC codes and message buffer.
	120216	SC = 1 SCE = 1 SSR = 1 TCC = 7	MICRO 1 RAM test failure. No message buffer was output. Since NBA = 0, a valid write characteristics command was issued prior to this command.
	100216	SC = 1 SSR = 1 TCC = 7	MICRO 2 FIFO test failure. A message buffer was output. If command was valid, XSTAT3H within that message buffer contains 002.

The first tests performed by the diagnostic software verify that all the power-up self-tests have run successfully. The results of these tests and the MICRO 1 and MICRO 2 tests are reported by means of the write subsystem memory command.

A message buffer is not outputted to memory if MICRO 1 (the RAM test) fails. If MICRO 2 (the FIFO test) fails, a message buffer is outputted and the high byte of XSTAT3 contains 002 if the command is valid.

Caution must be used when interpreting the TSSR and message buffered during failure modes, as the failure condition can corrupt this data.

To recover from these types of errors, a restart must be performed. Refer to Section 9.4.5.

9.4.1.3 TSDB Byte Wrap - A write byte operation to one byte of the TSDB automatically invokes a data wraparound test of the other byte of the TSDB. The subsystem ready bit must be set when the write byte instruction is issued. Subsystem ready is cleared during the test operation and reset upon test completion. At this point, another byte data pattern can be written into the unaccessed byte of the TSDB. TSDB byte wrap error testing is limited to checking that the correct data pattern is wrapped. To exit this diagnostic mode, a restart must be performed.

9.4.2 Attention Handler

The attention handler (indicated in Figure 9-10) is a body of code in firmware that performs the following functions.

1. It checks the state of the enable attentions interrupt (EAI) bit in the write characteristics command. If the bit is set, the handler continues. If EAI is clear, the attention handler is exited.
2. It checks the state of the diagnostic error flag. If the flag is set (as a result of an error during the main loop diagnostics), the handler jumps to step 4.
3. It checks the volume check flag (VCK). This flag is usually set by a change in the states of ON-LINE and OFF-LINE. If VCK is not set, program execution exits the attention handler.
4. It checks for the message buffer release condition, which results from the last command having been message buffer release. If the message buffer has not been released, the handler sets the attention pending flag. (This flag is checked by the process command subroutine).
5. It checks the SSR bit. If it is already cleared, this indicates a command pending. In this case, the handler sets the attention pending flag. The attention handler is then exited.
6. If the host CPU has not initiated a command by the time the attention handler reaches this point in its execution, then the SSR bit is still set. The program now clears the SSR bit. If the host CPU issues a command to the tape subsystem at this time, the RMR bit is automatically set.
7. Next, the attention handler updates the message buffer and transfers it to the host CPU. The handler then updates the TSSR with the appropriate FCC and TCC codes, and sets the SSR bit.
8. The handler checks the interrupt enable (IE) bit from the previous command (message buffer release). If IE is set, the handler interrupts the host CPU.
9. The attention handler is exited.

9.4.3 Get Command

When the host writes the TSDB, SSR clears, alerting the controller that a command is pending. The sequence for getting and accepting a command proceeds as follows.

1. The TSSR high byte is checked for a 1 in bit 7 (bit 15 of the word). (The hardware sets a flag to indicate that the TSSR was written prior to the writing of the TSDB.) If the boot bit is set, the following boot sequence occurs:

   a. Tape is rewound.

   b. One record or file mark is spaced over.

   c. 512 bytes of the next record is read and placed at starting address zero of the host.

   d. The TSSR is updated, indicating errors by setting SC = 1. SSR = 1 on completion.

   If the boot bit is not set, the get command routine bypasses the boot sequence.

2. If the boot bit is not set, the controller takes the command. The command consists of four words that are pointed to by the contents of the TSDB. Note that the contents of the TSDB was written previously by the host.

3. If a write characteristics command has not been written previously, the current command should be a write characteristics command. If these conditions are not met, the Need Buffer Address (NBA) bit remains set and the command is rejected. Command rejection causes the TSSR to be updated, SSR to be set, and the get command routine to be exited.

4. The routine checks the command for the state of the acknowledge (ACK) bit. If ACK is not set, then the last command should have been a message buffer release command. If these conditions are not met, then SSR is set, the host CPU is interrupted (if IE is set), and the get command routine is exited.

5. At this point, the command is ready to be processed by the process command routine.

9.4.4 Process Command

The process command routine interprets the command as follows.

1. If the command is not a valid command, the routine sets error bits and error codes. It also transfers the message buffer, updates the TSSR, sets SSR, and if IE is set, interrupts the host CPU. The process command routine is then exited.

2. If the clear volume check bit is set, the routine clears the volume check and also any attentions that were pending due to the volume check.

3. If the command is a write characteristics command, program control is passed to a separate area of code that clears the NBA bit in the TSSR, sets up characteristics parameters, and exits the routine.

4. If the command is an initialization command, the process command routine performs the following:

   a. Resets the tape drive.

   b. Checks for the previous occurrence of an error. If an error was detected previously during the running of the microdiagnostics, execution jumps to the beginning of the microcode.

   c. Transfers the message buffer.

   d. Updates the TSSR.

   e. Interrupts the host CPU (if the IE bit is set).

   f. Exits the routine.

5. If the command is a write subsystem memory command, then control passes to a routine unique to the diagnostics. After execution of the subsystem memory command routine, control returns to the process command routine, which then performs the following:

   a. Transfers the message buffer.

   b. Updates the TSSR.

   c. Sets SSR.

   d. Interrupts the host if IE is set.

   e. Exits the routine.

6. If an attention is pending, then the process command routine outputs the message buffer as an attention condition, without processing the command. It also performs the following:

   a. Updates the TSSR.

   b. Sets SSR.

   c. Interrupts the host if IE is set.

   d. Exits the routine.

7. If the command is a message buffer release command, then the routine sets the message buffer release flag, interrupts the host CPU (if IE is set), and exits.

8. If the command is a get status immediate command, the routine performs the following:

   a. Updates the message buffer.

   b. Outputs the message buffer.

   c. Updates the TSSR.

   d. Interrupts the host (if IE is set).

   e. Exits the routine.

9. At this point, processing of the command involves tape motion. The routine executes the command and then performs the following:

   a. Updates the message buffer.

   b. Outputs the message buffer.

   c. Updates the TSSR.

   d. Interrupts the host (if IE is set).

   e. Exits the routine.

9.4.5 Firmware Diagnostic Aids

9.4.5.1 Toggle In Routine - In the event that the unit does not respond to the TSSR address or if the firmware diagnostic must be restarted for troubleshooting purposes, the following toggle in type routine may be helpful. The starting address is 2000.

```
2000/  12706   (Set up R6 in case of traps)
2002/   1000   R6=1000
2004/   5000   CLR R0
2006/  12701   Set up delay value in R1
2010/ XXXXXX   Delay value (177777=MIN/000000=MAX TIME) - See NOTE
2012/  12737   Move word TSSR (start firmware diagnostics)
2014/      0
2016/ 172522   TSSR standard address
2020/ 105200   Wait loop fixed
2022/   1376   Branch to 2020 until R0=zero
2024/   5201   Wait loop variable
2026/   1374   Branch to 2020 until R1=zero
2030/    763   Branch to 2000

   4/   2000   (Restart on NXM, TSSR bus address is nonexistent.)
   6/      0
 224/    226   (Halt address PC=230, problem with interrupts or
                vectors.)
 226/      0
```

NOTE

The actual delay value used is dependent on the CPU type and the nature of the failure. If T17 through 13 fail, a short (177777) delay value can be used such that the oscilloscope is triggered more frequently. If a microdiagnostic fails, a long (174000) delay value must be used. In either case, the delay value must allow enough time for the failing diagnostic to run.

9.4.5.2 Startup - The firmware program startup is accomplished by either of the following:

1. Write to the TSSR.
2. Bus initialize.

On the trailing edge of a bus initialize signal (caused by power-up or a CPU command), the controller starts its firmware at microword location zero. (Refer to Figures 9-12 and 9-13, and to print set Sheet D5.) Signal D7 MRST L is asserted during the startup sequence, clearing all the address lines of the 2911 program sequencer. This sets the ROMs (Sheet D8) to location zero. D7 MRST L originates at E101 pin 12 (Sheet D7, bottom center). It is derived from D1 PMRST L synchronized by D6 SCLK H. D6 SCLK H is a free-running clock with a period of approximately 200 nanoseconds. Signal D1 PMRST L (Sheet D1, center) originates at E32 pin 13, and is enabled in either of two ways:

1. Bus Initialize -- D1 BINIT L arrives on pin AT2 and is received by the 8641 at E1 (Sheet 1, left center). This enables E32 pin 18.
2. Write TSSR Command -- A write to the TSSR (standard address of 772522) causes SIGNAL MATCH (E43/E44/E45/E48-3, Sheet D1, left) to go HIGH (TRUE). This signal results from the comparison of the bus address lines to the address switch. It enables the DC004 at location E15-19, which in turn decodes the bus control lines received by the 8641 transceivers at locations E1 and E2. The PAL01 in location E32 further decodes the bus control signals plus internal M7196 control signals to drive the D1 PMRST L line at E32 pin 13.

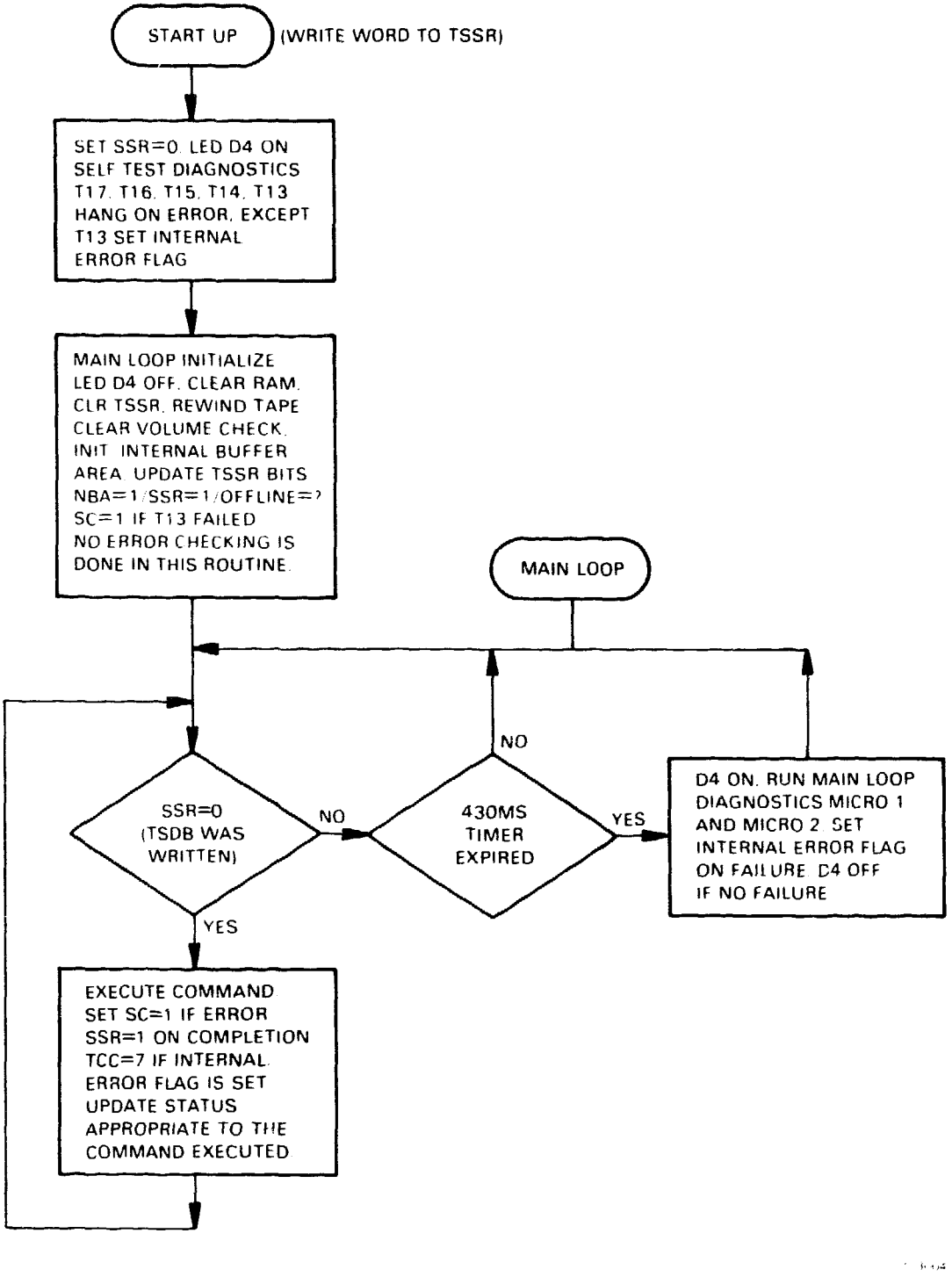
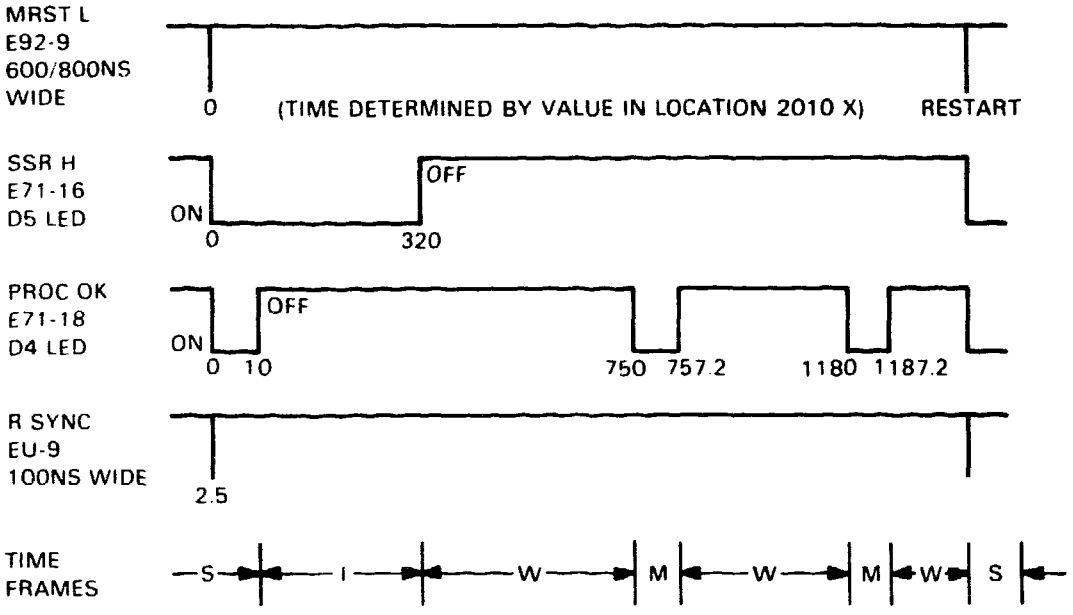


Figure 9-12 Firmware Diagnostic Flowchart



S = SELF TEST T17 THROUGH T13.
I = INITIALIZE. THIS TIME EXTENDS IF TAPE IS AVAILABLE TO REWIND.
W = 430ms WAIT TIMER. A COMMAND (TSDB WRITTEN SSR=0) EXITS HERE.
M = MICRO DIAGNOSTICS 1 AND 2
IF NO COMMAND IS ISSUED, THE FIRMWARE REMAINS IN THE W AND M STATES

CS 3005

Figure 9-13 Firmware Diagnostic Timing

9.4.5.3 Boot Code - The boot code listed below is functionally equivalent to the "MS" boot code for the TSV05. Error handling is accomplished by checking the special conditions bit (bit 15) and, if it is set, retrying until there is no error. If an "MS" boot block exists on the tape and all the hardware is operating properly, the code listed below can boot RT11, RSX11, RSTS, and XXDP+ tapes. The real-time event clock should be disabled when this boot code is used to load diagnostics.

Upon exit from the boot routine, registers R0 through R4 normally contain the following.

R0 = 0	Unit number
R1 = 172522	TSSR address
R2 = 172520	TSBA/TSDB address
R3 = 010016	PC of "SM" + 20

The boot code is as follows. The starting address is 10000.

```
                                        .=7776
007776  046523                          .WORD "SM"              Device ID
                                                                backwards

010000  012701  172522  START:  MOV TS05DB+2,R1          R1=TSSR
010004  010102                  MOV R1,R2               R2=TSSR
010006  005000                  CLR R0                  Clear R0

010010  105711                  TSTB (R1)               Wait for SSR
010012  100376                  BPL .-1
010014  010704                  MOV PC,R4               R4=PC of
                                                        "SM"+20
010016  112737  000200  172523  MOVB #200,@#TS05DB+3    Write byte
                                                        bit 15

010024  005242                  INC -(R2)               Write into
                                                        TSDB

010026  105711                  TSTB (R1)               Wait for SSR
010030  100376                  BPL .-1

010032  005711                  TST (R1)                Test for error
010034  100761                  BMI START               If SC=1 retry
010036  005007                  CLR PC                  Jump to zero
                                .END
```

9.4.6 Programming Example

The following toggle in type routine writes 100 bytes on tape, starting at memory location 4000, and then halts. No error checking or retries are performed. A tape (with write enable ring installed) must be loaded in the tape transport unit. The TSSR should contain 002200 at start-up. The starting address is 2000.

```
2000/005037   CLR TSSR     Initialize the subsystem.
2002/172522
2004/105737   TSTB TSSR    Wait for subsystem ready, wait for the
2006/172522                self-test diagnostics, including rewind,
                           to complete.
2010/100375
2012/012737   TSDB=1000    Perform the set characteristics command.
2014/001000                This clears NBA, bit 10, in the TSSR.
2016/172520
2020/105737   TSTB TSSR    Wait for subsystem ready. Wait for the
2022/172522                write characteristics command to com-
                           plete.
2024/100375
2026/012737   TSDB=1600    Perform the write data command. Tape
                           motion occurs.
2030/001600
2032/172520
2034/105737   TSTB TSSR    Wait for subsystem ready. Wait for the
2036/172522                write data command to complete.
2040/100375
2042/000000   HALT         Tape is positioned approximately 8.9
                           centimeters (3.5 inches) forward of the
                           BOT marker. The contents of the message
                           buffer, starting at address 1400, is ex-
                           amined to obtain subsystem status.
```

Placing 771 in address 2042 causes the program to run continuously. However, EOT is not detected.

The following is the write characteristics command packet and data area.

```
1000/140004   Write characteristics command
1002/001200   Low characteristics data address
1004/000000   High characteristics data address
1006/000010   Characteristics data length

1200/001400   Low message buffer address
1202/000000   High message buffer address
1204/000020   Message buffer length
1206/000000   Characteristic data
```

The following is the message buffer data area.

1400/??????	Message header word	Typically 100020
1402/??????	#Bytes following	Typically 000012
1404/??????	Residual byte count	Typically 000000
1406/??????	XSTAT0	Typically 000310
1410/??????	XSTAT1	Typically 000000
1412/??????	XSTAT2	Typically 100000
1414/??????	XSTAT3	Typically 000000
1416/— — —	XSTAT4	This word exists only if extended features are enabled. "#Bytes following" in address 1402 equals 000014 if XSTAT4 exists.

The following is the write command packet and data area.

1600/140005	Write data command
1602/004000	Low memory address
1604/000000	High memory address
1606/000100	Byte count
4000/??????	Data buffer
THRU/??????	
4076/??????	

Changing address 1600 to 140001 causes a read forward command to take 100 bytes of data from tape and place it in memory starting at location 4000.

When the program halts at PC location 2044, the TSSR should equal 200. Only subsystem ready is set. Other bits set indicate an error occurred. The TSDB should contain 1416, pointing to the end of the message buffer data area. As shown in this example, it is possible in diagnostic error situations to place the CPU in console mode and determine where the message buffer is located by examining the TSDB and subtracting approximately 20. Caution must be exercised if this method is used, because the message buffer is updated if another command is issued or another routine utilizes the message buffer memory area.

CHAPTER 10

CHAPTER 10
TSV05 PROGRAMMING PROTOCOL TECHNICAL DESCRIPTION

The TSV05 subsystem follows the same programming protocol as the TS11/TS04 subsystem. The nature of the TS05 tape transport dictates that some status bits are redefined. In addition, the TSV05 subsystem has special features not available in the TS11/TS04 subsystem.

10.1 OVERVIEW

The functions listed in Table 10-1 make up the TSV05 Subsystem Command Set. These commands utilize "command packets" stored in the computer system memory to operate the tape transport and transfer data. Some commands have various subcommands, termed "modes". The interface device registers are used to initiate command packet processing and retrieve basic status. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data). A detailed description of the commands is provided in Section 10.4.

The TSV05 subsystem has four device registers that occupy only two Q-bus word locations: a Data Buffer (TSDB), a Bus Address Register (TSBA), a Status Register (TSSR), and an Extended Data Buffer (TSDBX). The TSDB is an 18-bit register that is parallel loaded from the Q-bus, or from the TSV05 controller module itself. A 16-bit portion of this register is used as a word buffer register; it is written into by the CPU to initiate and operate, and it is written into by the controller logic itself to store data to be transmitted to Q-bus memory during a Direct Memory Access (DMA) cycle. The TSDB can be loaded from the Q-bus by three different transfers from the CPU.

Two transfers are for maintenance purposes (byte transfer, and DATOB at high byte or low byte), and the third is for the normal (word) operation (DATO) to initiate an operation. This register is write only, and is not cleared at power on, subsystem initialize, or bus initialize. This register can be loaded without the tape transport connected, since all controller functions reside within the interface/controller module.

Commands are not written to the TSV05 Q-bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used in the TSV05 subsystem to retrieve words in memory called the "command packet". The words in the command packet instruct the system as to the function to be performed. These words contain any function parameters such as bus address, byte count, record count, and modifier flags.

The TSBA is an 18-bit register (22 bits when the high byte of the TSSR is written to) that is parallel-loaded from the TSDB every time the TSDB is loaded. TSDB bits 16-02 load into TSBA bits 16-02, TSDB bits 01 and 00 load into TSBA bits 17 and 16, and zeros are loaded into TSBA bits 01 and 00 (thereby specifying a modulo-4 address). TSBA bits 17 and 16 are displayed in TSSR bits 09 and 08, respectively. (TSDB can be extended to 22 bits by first loading TSDB bits 18-22 into the high byte of TSSR. The extended features switch (E58-9) must be ON* or else bits 18-22 are ignored). The TSBA register is incremented or decremented by two for DMA word transfers, or by one for DMA byte transfers. The two major purposes of the TSBA register are as follows.

- The TSBA is used as a command pointer, pointing to the "functional device registers" (command and message buffers). These are located somewhere in Q-bus address space. The contents loaded into the TSDB when the TSV05 subsystem is the bus slave is considered the command pointer. In this mode, the TSV05 subsystem receives data (command buffer words) and stores them internally on the interface/controller module for storage and/or execution.
- The TSBA is used as a data pointer (bus address for DMA), pointing to data buffer areas located somewhere in the Q-bus address space. In this mode, the controller loads TSBA with data pointer information from internal storage. The contents are then used to point to data buffer areas while transferring tape data between CPU memory and the tape transport. The data pointer is extended to 22 bits (18-21 are zeros) if the TSSR high byte is not first loaded, or if the extended features switch (E58-9) is OFF*.

The TSSR is a 16-bit register that is updated only from the controller module internal logic. It cannot be modified from the Q-bus. In this register, major system status is observed.

The tape transport, when on-line, is under control of the microprocessor and related microcode within the controller module. When the transport is off-line, the transport is under control of its own internal logic, which can in turn be controlled by the operator using switches on the front panel.

Before the TSV05 subsystem begins a function, the Q-bus must assemble a command packet in main memory. The command packet is always four words long, although not all commands use all four of the words in the packet. The words in the command packet may be thought of as the contents of several registers:

- Command Register (CMDR).
- Data Pointer Register (DPR).
- Positive Byte Count Register (BPCR).

* M7196 only. M7206 is in extended features mode at all times.

The CMDR contains the machine language representation of one of the commands listed in Table 10-1. The DPR contains the address of the data to be manipulated. The DPR consists of two words: a low-order address word containing bits 16-00, and a high-order address word containing either bits 17-16 (for 18-bit addressing) or bits 21-16 (for 22-bit addressing). In the 18-bit addressing mode, bits 01-00 of the DPR high-order address word are used to specify bits 17-16 of the address. If the extended features switch is on, the 22-bit addressing mode can be used*.

In this case, bits 06-00 of the DPR high-order address word are used to specify address bits 21-16. When the command being used does not involve a data operation, the two DPR words are not used in the command packet (see Figure 10-1).

The BPCR contains the number of items to be manipulated during the operation specified by the command. In a packet that includes DPR words, the BPCR word follows the DPR word. If a packet does not involve a data operation, the BPCR word, if present, follows the command words.

Message packets are issued by the controller module and built in the host CPU memory space. Subsystem operation requires a message buffer address to be supplied on a write characteristics command. This command must be the first command issued to the subsystem after an initialize. Otherwise, all other commands are rejected.

The command pointer must be an address on a modulo-4 boundary (that is, beginning at octal 0, 4, 10, 14, and so on).

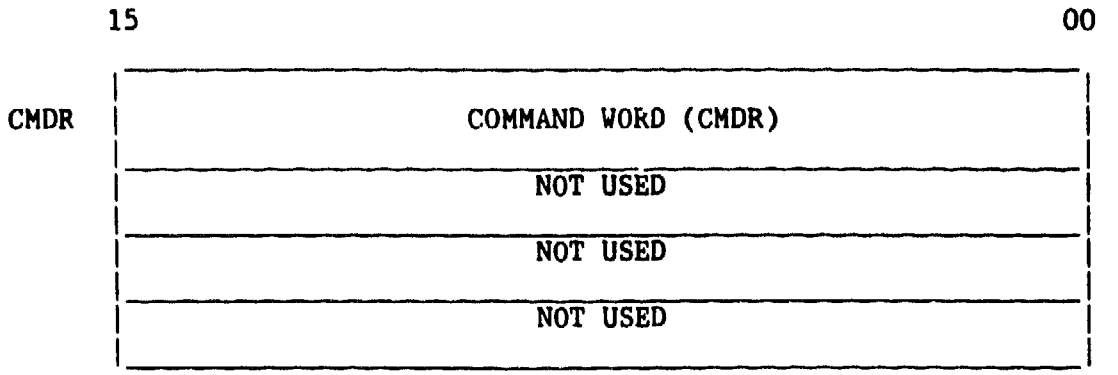
The DPR is eventually loaded into TSBA to be used as the Q-bus address for DMA transfers. The BPCR is used to indicate the number of bytes (8 bits of data per byte) to be moved to or from the transport during a data transfer. It is also used to specify the number of records in a space record command or the number of files in a skip tape marks command. The CMDR specifies the function to be executed by the subsystem.

* M7196 only. M7206 is in extended features mode at all times.

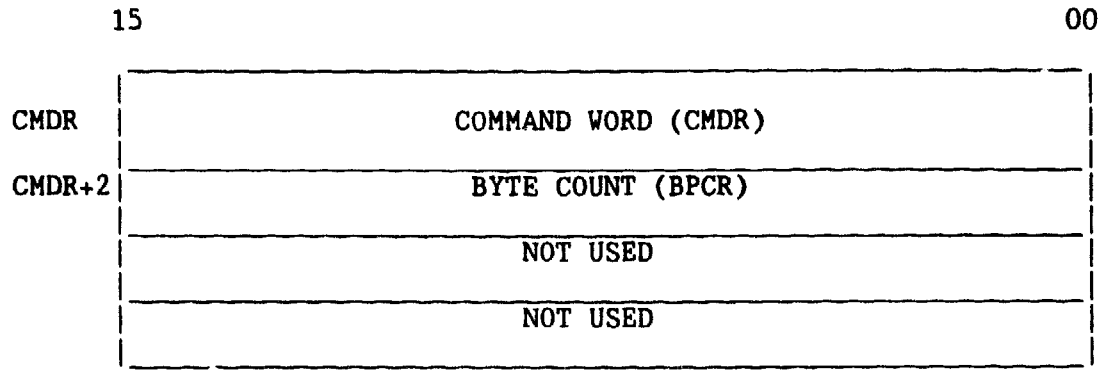
Table 10-1 TSV05 Assigned Command Modes

Command Name	Mode Name/Description
GET STATUS	Get Status (update the Extended Status registers in the message buffer in memory)
READ	Read Next (Forward) Read Previous (Reverse) Reread Previous (Space Reverse, Read Forward) Reread Next (Space Forward, Read Reverse)
WRITE CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
WRITE	Write Data Write Data Retry (Space Reverse, Erase, Write Data)
POSITION	Space Records Forward Space Records Reverse Skip Tape Marks Forward Skip Tape Marks Reverse Rewind
FORMAT	Write Tape Mark Erase Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
CONTROL	Message Buffer Release Rewind and Unload Clean Tape (handled as a NO-OP) Rewind with Immediate Interrupt*
INITIALIZE	Controller/Drive Initialize
WRITE SUBSYSTEM MEMORY	Diagnostic function. Allows test sequences and data patterns to be entered into the controller.

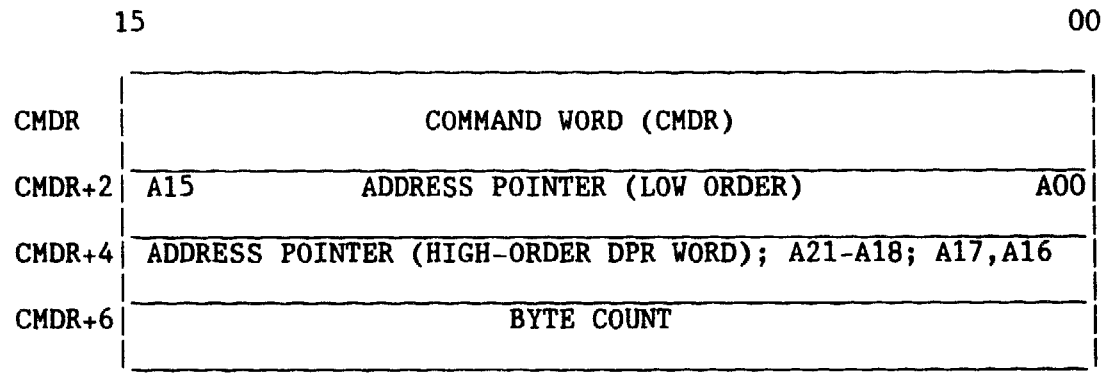
* Extended function, not part of the TS11/TS04 repertoire.



a. One-Word Type



b. Two-Word Type



c. Four-Word Type

Figure 10-1 Command Packet Types

10.2 REGISTERS

The TSV05 subsystem contains four hardware device registers on the controller module, and also five "remote" device registers that the controller maintains in a message buffer area of the Q-bus memory. The hardware registers are:

- TSBA
- TSDB
- TSSR
- TSDBX

The remote registers set up in Q-bus memory are extended status registers 0-4 (XST0-4). Register formats and bit definitions are presented in the sections that follow.

10.2.1 Bus Address Register (TSBA)

The TSBA is a read-only hardware register located at the first I/O register address. In normal operating mode, it displays the low-order 16 bits of the memory address to be used or being used by the controller to access system main memory (for example, for command buffer fetch, message buffer store, or data transfer). In maintenance mode, it displays data from the "wraparound" tests invoked by writing into TSDB. Figure 10-2 illustrates the TSBA, and Table 10-2 defines the bits.

Q-bus Address + 0 -- Read-Only

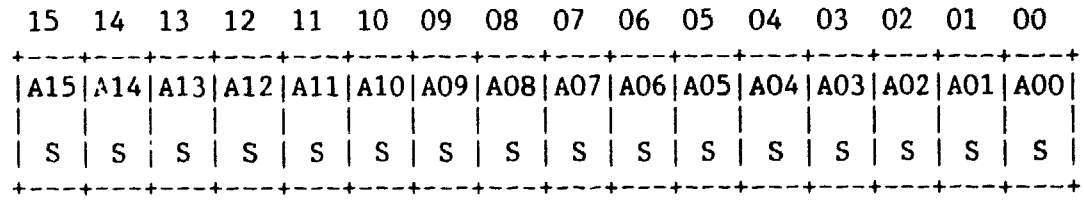


Figure 10-2 TSBA Register Format

Table 10-2 TSBA Register Bit Definitions

Bit	Name	Definition
15	A15	Bus address bit 15
14	A14	Bus address bit 14
13	A13	Bus address bit 13
12	A12	Bus address bit 12
11	A11	Bus address bit 11
10	A10	Bus address bit 10
09	A09	Bus address bit 09
08	A08	Bus address bit 08
07	A07	Bus address bit 07
06	A06	Bus address bit 06
05	A05	Bus address bit 05
04	A04	Bus address bit 04
03	A03	Bus address bit 03
02	A02	Bus address bit 02
01	A01	Bus address bit 01
00	A00	Bus address bit 00

Address bits 15 through 00 normally reflect the low-order 16 bits of the 22-bit address used by the controller to access Q-bus memory. They are loaded by:

1. The CPU when writing a word into TSDB, to define the address of the command buffer for the next operation. TSDB<15:02> are copied into TSBA<15:02>, and TSBA<01:00> are set to "0".
2. The CPU writing into the high byte (DATOB) of TSDB (for a maintenance function). TSDB bits 16-08 are copied into both bytes of TSBA. Data for bits 07-00 is TSDB<15:08>. TSDB bits 08 and 09 are copied into TSSR bits 08 and 09 (A16, A17).
3. The CPU writing into the low byte (DATOB) of TSDB (for a maintenance function). TSDB bits 07-00 are copied to TSBA<07:00>. TSBA <15:08> is then loaded from TSDB bits 07-00.
4. The CPU writing a word (DATO) into TSDB in maintenance mode. (Maintenance mode is entered as a result of Step 2 or 3 above.)
5. The controller, for specifying bits 16-00 of a DMA address. TSBA is not modified by initialize.

10.2.2 Data Buffer Register (TSDB)

The TSDB is, externally, a 16-bit write-only register that is parallel-loaded from the Q-bus. Internally it is a 22-bit register. It can be loaded from the CPU by four different types of transfers. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte); these place the controller into maintenance mode, which is cleared only by an initialize, and causes the internal data wraparound functions. The third is for maintenance purposes (DATO word when in maintenance mode). The fourth is for normal operation (DATO word when not in maintenance mode) to specify a command pointer. The 4-bit extension to TSDB is written at the high byte of the TSSR location. These address bits are ignored if the extended features switch is OFF. The extension is cleared after it is issued once, and so must be reloaded if extended addressing is used on subsequent command pointers. (It must be loaded before the TSDB is loaded.) It is also cleared by initialize.

The controller responds whenever the TSDB location is written to, but is loaded only when the SSR bit in the TSSR register is set (if SSR is clear, the Register Modification Refused (RMR) bit in TSSR is set). Writing into TSDB clears SSR. After a DATO or DATOB to TSDB (for maintenance data wraparound), SSR momentarily clears, then sets when the data wraparound is performed. An initialize should be performed (that is, write into TSSR) in order to use the controller again for normal operation. Note that entering maintenance mode (by performing a DATOB to either byte of the TSDB) causes the Need Buffer Address (NBA) bit in TSSR to be set, and automatic running of the idle-time on line microdiagnostics to be inhibited

The TSDB register is illustrated in Figure 10-3, and the bits are listed and defined in Table 10-3.

Q-bus Address + 0 -- Write-Only

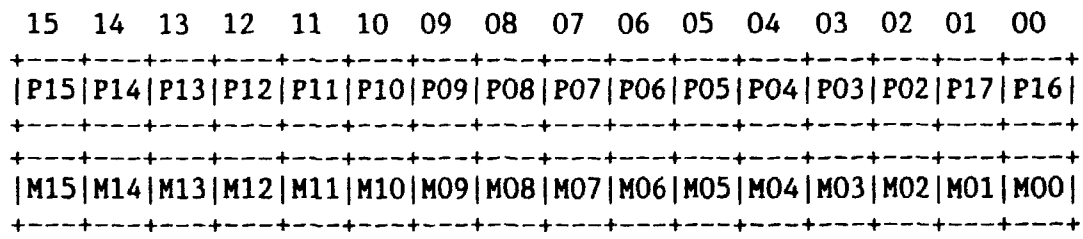


Figure 10-3 TSDB Register Format

Table 10-3 TSDB Register Bit Definitions

Bit	Name	Definition
15-02 01-00	P<15:02> P<17:16> (DATO) Word, Normal Mode)	Command Pointer Bits 17-02 — When the TSDB is written as a word, and SSR = 1 and the controller is not in maintenance mode, the data is loaded into bits 17-02 of both the TSBA output file register (for reading onto the Q-bus) and an internal TSBA register, and command processing commences. TSBA bits 01-00 are cleared to "0" (modulo-4 address). In addition, the extended TSDB register (TSDBX) is loaded into TSBA bits 21-18; TSDBX must be loaded before TSDB.
15-08	M<15:08> (DATOB to High Byte)	Maintenance Data Bits 15-08 for Wraparound to TSBA — If the wraparound is correct, M<15:08> appears in both bytes of TSBA. A DATOB to TSDB places the controller into maintenance mode.
07-00	M<07:00> (DATOB to Low Byte)	Maintenance Data Bits 07-00 for Wraparound to TSBA — If the wraparound is correct, M<07:00> appears in both TSBA<07:00> and TSBA<15:08>. A DATOB to TSDB places the controller into maintenance mode.
15-00	M<15:00> (DATO Bits Word in Main- tenance Mode)	Maintenance Data Bits 15-00 — This function can be used for specifying the address used in the low-byte data wrap test. Bits 15-12 are reserved for future maintenance functions and should be written to "0".

10.2.3 Status Register (TSSR)

TSSR is a 16-bit register. Although defined as a read/write register, its contents cannot be directly modified by the Q-bus. It can be read to examine status, but writing into it causes a hardware initialize of the controller. (A DATOB to the high byte only of the TSSR, however, loads the extended TSDBX.) The contents of the register is modified by the controller. The register format is illustrated in Figure 10-4. Table 10-4 gives the register bit definitions. If the initialize diagnostic fails, this register has alternate bit definitions.

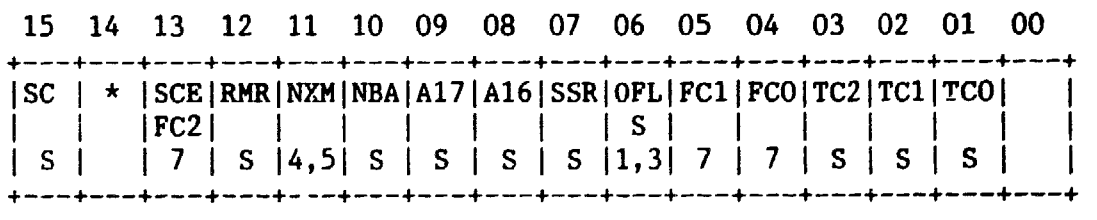


Figure 10-4 TSSR Register Format

Table 10-4 TSSR Register Bit Definitions

Bit	Name	Code	Definition
15	SC	S	Special Condition — When set, indicates that the last command was not completed without incident: either an error was detected, or an exception condition (that is, tape mark on read, reverse motion at BOT, and so on) occurred. Also set by the error bits in TSSR: RMR and NXM. Indicates that the Termination Class (TC) bits are nonzero (unless RMR is the only error — see RMR). Cleared by initialize unless a self-test error is detected, in which case SC is set.
14	*	—	Not used in TSV05, UPE in TS11.
13	SCE	FC2 7	Sanity Check Error — Set when the controller detects an internal failure. This is considered serious enough so that a message buffer is not sent out. SPE in TS11.
12	RMR	S	Register Modification Refused — Set when the TSDB is written from the Q-bus and Subsystem Ready (SSR) is not set. Causes the SC bit to be set, but no TC (the TSV05 never sees the data written), because on a system with no bugs, RMR can be set if TSDB is written while an ATTN message is being output. If ATTNs are not enabled, RMR setting indicates a fatal controller problem or a software bug.
11	NXM	4,5	Nonexistent Memory — Set when trying to do a DMA transfer to/from a memory location that does not exist (does not respond within 12 μs). May occur when fetching a command packet, fetching or storing data, or storing the message packet.
10	NBA	S	Need Buffer Address — When set, indicates that the TSV05 needs a message buffer address. Set by initialize and performing a DATOB to the TSDB (that is, to enter maintenance mode). Cleared during the write characteristics command (if a valid address was given). If NBA = 1 and any command other than write characteristics is given, the operation is terminated with function reject.
09-08	A<17:16>	S	Address Bits 17-16 — A17 and A16 display bits 17 and 16 of the internal TSBA register, which holds a command pointer or DMA address. Loaded from TSDB bits 01-00 when TSDB is written.

Table 10-4 TSSR Register Bit Definitions (Cont)

Bit	Name	Code	Definition
07	SSR	S	Subsystem Ready — When set, indicates that the TSV05 is not busy, and is ready to accept a new command pointer. Cleared by writing the TSDB. Also cleared by initialize, then set by the controller if the basic microdiagnostics are successfully passed.
06	OFL	S 1,3	Off-Line — When set, indicates that the TS05 tape transport is off-line and unavailable for any tape motion commands. This bit can cause a TC of 1 (on an ATTN interrupt) or 3 [results in Nonexecutable Function (NEF) status]. This bit does not indicate the current status of the tape transport (updated on command completions).
05-04	FC<01:00>	7	Fatal Termination Class Code — Used to indicate the type of fatal error that occurred on the TSV05. The code is valid only when the SC bit is set and the TC code bits are all set (111); they are clear otherwise. The FCs are:

Code	Meaning
0	Internal diagnostic failure. See the error code byte (XST3) for the failed function. Initialize must be issued for the controller to accept further commands.
1	Reserved
2	Not Used
3	Reserved for detection of power down on transport (not currently implemented).

Table 10-4 TSSR Register Bit Definitions (Cont)

Bit	Name	Code	Definition
03-01	TC<02:00>	S	Termination Class Code — This 3-bit field acts as a word offset value whenever an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The conditions in each class have similar significance and recovery procedures (as applicable). The codes are:

Code	Meaning
0	Normal Termination
1	Attention Condition
2	Tape Status Alert
3	Function Reject
4	Recoverable Error - tape position is one record down tape from start of function.
5	Recoverable Error — Tape not moved.
6	Unrecoverable Error — Tape position lost.
7	Fatal Controller Error — (see fatal class codes).

00	-	-	Not Used

10.2.4 Extended Data Buffer Register (TSDBX)

The TSDBX is a write-only hardware byte register located at the fourth byte address of the TSV05 I/O register block. This address corresponds to the high-order byte of the TSSR register. The TSDBX is used to specify the most significant four bits of a 22-bit command pointer address, and also to allow an automatic tape boot sequence to be performed.

TSDBX is written only by a byte-access (DATOB) cycle addressed to the high byte of TSSR. If the extended features switch (E58-9) is OFF* when TSDBX is written, only the boot bit is examined; the other bits are ignored.

Figure 10-5 illustrates the format of TSDBX, and Table 10-5 describes each bit.

Assume the extended features switch (E58-9) is ON. Once written, the contents of the least-significant four bits of TSDBX are transferred to bits 18 through 21 of the internal TSBA register for use as a command pointer. The low order 18 bits of the command pointer are specified by writing into the TSDB register, which starts operation and then clears TSDBX. Therefore, a subsequent load of only the TSDB specifies a 22-bit command pointer address, with the high order four bits equal to zero.

For the TSDBX register to be properly written, the SSR bit in TSSR must be set; if it is not, the RMR bit is set and no modification to TSDBX occurs. When the TSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked for, before TSDB is written.

Writing the TSDB begins processing on TSDBX. If the boot bit is not set, the command pointed to by the 22-bit TSDB is retrieved, and command processing begins. If the boot bit is set, SSR remains clear until the boot sequence is complete or until an error occurs.

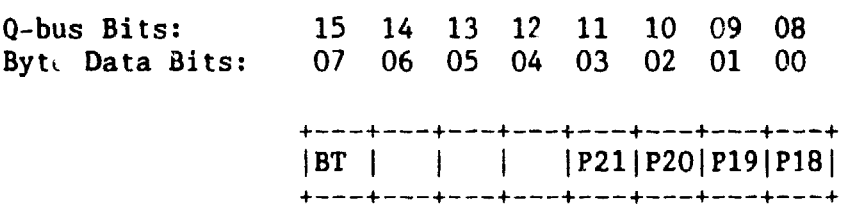


Figure 10-5 TSDBX Register Format

* M7196 only

Table 10-5 TSDBX Register Bit Definitions

Bit	Name	Definition
15	BT	Boot Command Bit — When written to "1" with SSR=1, causes the tape to be rewound to BOT, the first tape record to be skipped, and the second record (only the first 512 bytes of it) to be loaded into CPU memory space starting at location "0".
14-12	-	Reserved — Should always be written to "0".
11-08	P<21:18>	Command Pointer Bits 21-18 — When the TSDBX is written, and SSR=1, the data is loaded into bits 21-18 of the internal TSBA register. TSDBX is cleared after TSDB is written, and is also cleared by initialize.

10.2.5 Extended Status Register 0 (XST0)

XST0 appears as the fourth word in the message buffer stored by the TSV05 subsystem upon completion of a command or on an ATTN. Figure 10-6 illustrates the register format, and Table 10-6 describes each bit.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
									S						
S,2	2	2	2	3,6	3	3	3	S	1,3	S	S,3	S	S,3	S,3	S,2

Figure 10-6 XST0 Register Format

Table 10-6 XST0 Register Bit Definitions

Bit	Name	Code	Description
15	TMK	S,2	Tape Mark Detected — Set whenever a tape mark is detected during a read, space, or skip command, and also as a result of the write tape mark or write tape mark retry commands.
14	RLS	2	Record Length Short — This bit indicates that either the record length was shorter than the byte count on read operations, a space record operation encountered a tape mark or BOT before the position count was exhausted, or a skip tape marks command was terminated by encountering BOT or a double tape mark (if that operational mode is enabled, see LET) prior to exhausting the position counter.
13	LET	2	Logical End of Tape — Set only on the skip tape marks command when either two contiguous tape marks are detected, or when moving off of BOT and the first record encountered is a tape mark. The setting of this bit does not occur unless this mode of termination is enabled through use of the write characteristics command.
12	RLL	2	Record Length Long — When set, indicates that the record read on a read was longer than the byte count specified.
11	WLE	3,6	Write Lock Error — When set, indicates that a write operation was issued, but the mounted tape did not contain a write enable ring.
10	NEF	3	Nonexecutable Function — When set, indicates that a command could not be executed due to one of the following conditions: • The command specified reverse tape direction, but the tape was already at BOT. • The issuing of any motion command when the Volume Check (VCK) bit is set. • Any command, except get status or drive initialize, when the transport is off-line. • Any write command when the tape does not contain a write enable ring (also causes write lock status - WLE).
09	ILC	3	Illegal Command — Set when a command is issued, and either its command field or its command mode field contains codes that are not supported by the TSV05.

Table 10-6 XST0 Register Bit Definitions (Cont)

Bit	Name	Code	Description
08	ILA	3	Illegal Address — Set when a command specifies an address of more than 18 bits (when the extended features switch is OFF) or more than 22 bits (when the extended features switch is ON), or an odd address when an even one is required.
07	MOT	S	Motion — Tape is moving. Indicates that the transport is asserting formatter busy or rewinding status.
06	ONL	S	On-Line — When set, indicates that the TS05 tape transport is on-line and operable. A change in this bit can cause a termination class of 1 (ATTN interrupt, if ATTENTIONS are enabled). When clear and a motion command is issued, causes NEF (termination class 3).
05	IE	S	Interrupt Enable — Reflects the state of the IE bit supplied on the last command.
04	VCK	S	Volume Check — When set, indicates that the TS05 tape transport has been either powered down or turned offline. Cleared by the Clear Volume Check (CVC) bit in the command header word. This bit can cause a termination class of 3.
03	PED	S	Phase-Encoded Drive — Always set. Indicates that the TSV05 is capable of reading and writing only phase-encoded data.
02	WLK	S,3	Write Locked — When set, indicates that the mounted reel of tape does not have a write enable ring installed. The tape is, therefore, write protected.
01	BOT	S,3	Beginning of Tape — When set, indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape.
00	EOT	S,2	End of Tape — This bit is set whenever the tape is positioned at or beyond the EOT reflective strip. Does not reset until the tape passes over the strip in the reverse direction under program control. If the controller is read buffering (pre-reading records from tape automatically) and the EOT strip is seen, this bit is not set until the program actually requests the record associated with the EOT.

10.2.6 Extended Status Register 1 (XST1)

XST1 appears as the fifth word in the message buffer stored by the TSV05 subsystem upon completion of a command, or on an ATTN. Figure 10-7 illustrates the register format, and Table 10-7 describes each bit.

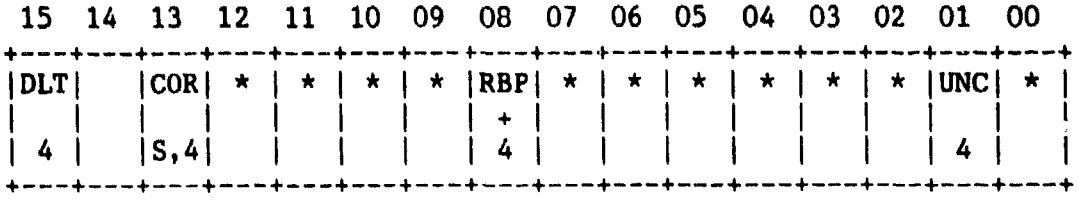


Figure 10-7 XST1 Register Format

Table 10-7 XST1 Register Bit Definitions

Bit	Name	Code	Description
15	DLT	4	Data Late — Set when the module's internal FIFO buffer is full on a read and the tape transport attempts to enter another byte, or when it is empty on a write and the tape transport requests another byte. These conditions occur whenever the Q-bus latency exceeds the required data transfer rate of the TSV05.
14	-	-	Not used.
13	COR	S,4	Correctable Data — When set, indicates that a correctable data error has been encountered while reading or writing. On a write, this bit causes a termination class of 4. On a read, the termination class is 0 (no corrective action required).
12-09 07-02, 00	-	-	Not used by the TSV05; always set to "0". In the TS11, these bits indicate Crease Detected (CRS), Trash in Gap (TIG), Deskew Buffer Fail (DBF), Speed Check (SCK), Invalid Preamble or Postamble (IPR, IPO), Sync Failure (SYN), Invalid End Data (IED), Postamble Short or Long (POS, POL), and Multitrack Error (MTE). The TSV05 tape transport reports any of these errors as hard error, causing the Uncorrectable Data (UNC) bit (bit 01) to be set.
08	RBP	4	Read Bus Parity Error — Set when the controller detects a parity error on the read data lines of the transport bus (during a read or write). If this parity error is also detected by the tape transport, the UNC bit is also set. The problem is most likely in the bus drivers in the tape transport, the bus receivers in the controller, or in the tape transport bus cable.

Table 10-7 XST1 Register Bit Definitions (Cont)

Bit	Name	Code	Description
01	UNC	4	Uncorrectable Data or Hard Error — Set, in tape response to the transport asserting Hard Error, during a read or write to indicate that one of the following has occurred: • False preamble detection. • False postamble detection. • Multichannel dropout. • Parity error without associated channel dropouts (could result from bad write data interface circuit in the controller). • Loss of data envelope prior to postamble detection. • Excessive skew.

10.2.7 Extended Status Register 2 (XST2)

XST2 appears as the sixth word in the message buffer stored by the TSV05 subsystem upon completion of a command, or on an ATTN. Figure 10-8 illustrates the register format, and Table 10-8 describes each bit. Note that the low-order eight bits of this register have special meaning for the write characteristics command. Unlike the TS11, there is no display of dead tracks, or residual capstan tick count.

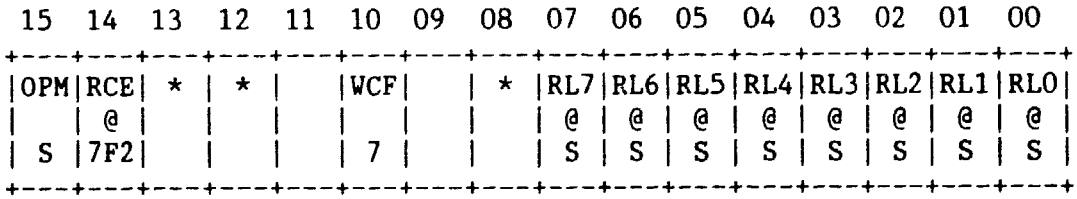


Figure 10-8 XST2 Register Format

Table 10-8 XST2 Register Bit Definitions

Bit	Name	Code	Description
15	OPM	S	Operation in Progress — (Tape moving.)
14	RCE	@	RAM Checksum Error — Set on a read or write when the checksum of a data block extracted from the module's internal RAM does not match the checksum computed when the data was entered. Causes fatal termination. This bit is Silo Parity (SIP) in the TS11.
13,12	-	*	Not used by the TSV05; always set to "0". In the TS11, bit 13 is serial 08 bus parity at drive, bit 12 is capstan acceleration fail, and bit 08 is parity dead track.
11,09	-	-	Not used.
10	WCF	7	Write Clock Failure — Set during a write to indicate that the module's internal FIFO buffer is not being emptied by the tape transport.
07-00 07-00	RL	@	Revision Level — On a write characteristics command, this field displays the settings of the extended features enable switch (bit 07), the buffering enable switch (bit 06), and the microcode revision level (bits 06-00). On all other commands, bits 02-00 show the unit number of the currently selected transport.[1]

10.2.8 Extended Status Register 3 (XST3)

XST3 appears as the seventh word in the message buffer stored by the TSV05 subsystem upon completion of a command or on an ATTN. Figure 10-9 illustrates the register format, and Table 10-9 describes each bit.

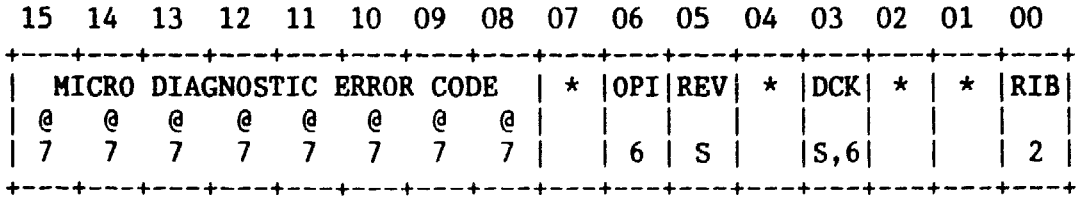


Figure 10-9 XST3 Register Format

[1] For this to be valid on M7206, bits 03,04 must both be 0, as described in Chapter 6, Table 6-18.

Table 10-9 XST3 Register Bit Definitions

Bit	Name	Code	Description
15-08	MDE	@,7	Microdiagnostic Error Code — This field is encoded by the controller to indicate various failures detected by the microprogram. Detections can occur during the running of internal on-line tests during idle periods (for example, RAM FIFO failures). Once an error occurs, an initialize must be issued to use the controller again.
07	-	*	Not used by the TSV05. In the TS11, this bit is Tension Arm Limit Exceeded (LMX).
06	OPI	6	Operation Incomplete — Set when read, space, or skip operation moves about 8 m (25 ft) of tape without detecting any data on the tape.
05	REV	S	Reverse — Set when the current operation causes reverse tape motion (includes the retry commands as well as simply reverse read, space, and so on); clear when operation is forward or rewind.
04	-	*	Not used by the TSV05. In the TS11, this bit is Capstan Response Failure (CRF).
03	DCK	S,6	Density Check — Set when a PE Identification Burst (IDB) is not detected while moving off of BOT. A read, space, or skip, however, completes (if no other errors occur) to allow tapes with the IDB wrong to be read.
02,01		*	Not used by the TSV05; always set to "0". Bit 02 is used by the TS11 to indicate that a noise bit was detected during an erase. Bit 01 is used by the TS11 to indicate that a limit switch was activated.
00	RIB	2	Reverse Into BOT — When set, indicates that a read, space, skip, or retry command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion halts at BOT.

10.2.9 Extended Status Register 4 (XST4)

XST4 appears as the eighth word in the message buffer stored by the TSV05 subsystem upon completion of a command, or on an ATTN. Figure 10-10 illustrates the register format, and Table 10-10 describes each bit. Note that for this word to be stored, the extended features option must be enabled, and the message buffer extent parameter specified in the write characteristics command must be increased by two over the normal TS11 specification.

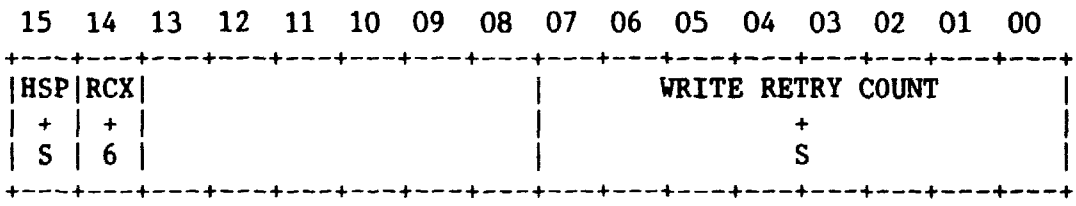


Figure 10-10 XST4 Register Format

Table 10-10 XST4 Register Bit Definitions

Bit	Name	Code	Description
15	HSP	S	High Speed — When set, indicates that the tape transport is operating in high-speed mode 254 cm/s (100 in/s). When clear, the transport is operating in low-speed mode 64 cm/s (25 in/s).
14	RCX	6	Retry Count Exceeded — When set, indicates that the controller is buffering write data, and cannot successfully output the buffered record within the specified number of retries. Causes tape position lost termination.
13-08	-	-	Reserved — Always set to "0".
07-00	WRC	S	Write Retry Count Statistic — When the controller is buffering write data records, this field indicates the total number of controller-initiated retries performed in order to write the previous buffered record. This count is cleared after it is displayed. For example, consider the situation in which: (1) buffering is in operation and record N is in RAM (the controller has given successful termination for record N), (2) the write command for record N + 1 has been issued to the controller but the controller has not yet accepted the command, and (3) the controller must perform M retries to finally write record N successfully. In this situation, M appears in the WRC field when termination of record N + 1 is finally given.

10.2.10 Summary of Registers

The formats of the hardware and remote (software-determined) registers discussed in the preceding sections are summarized in Figures 10-11 and 10-12. Figure 10-13 shows the format of the command registers implemented by the Q-bus CPU when it builds a command packet.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
TSBA (R/O)	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
	P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
TSDB (W/O)																
	SC	*	SCE	RMR	NXM	NBA	A17	A16	SSR	OFL	FC1	FC0	TC2	TC1	TC0	
TSSR (R/W)			@							S						
	S		&	S	4,5	S	S	S	S	1,3	7	7	S	S	S	
	BT				P21	P20	P19	P18								
TSDBX (W/O)									(TSDBX exists only on the TSV05)							

Legend:

* = Bit defined for TS11 but normally set to "0" by TSV05.

@ = Bit defined for TS11, but has similar (although slightly different) meaning for TSV05.

S = Status bit, not necessarily associated with a particular termination class.

1-7 = Termination class code associated with this bit.

Figure 10-11 TSV05 Hardware Device Registers

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
XST0	TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT
	S,2	2	2	2	3.6	3	3	3	S	1,3	S	S,3	S	S,3	S,3	S,2
XST1	DLT		COR	*	*	*	*	RBP	*	*	*	*	*	*	UNC	*
	4		S,4					4	+						4	
XST2	OPM	RCE	*	*		WCF		*	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	S	@ 7				7			@ S	@ S	@ S	@ S	@ S	@ S	@ S	@ S
XST3	MICRO DIAGNOSTIC ERROR CODE								*	OPI	REV	*	DCK	*	*	RIB
	@ 7	@ 7	@ 7	@ 7	@ 7	@ 7	@ 7	@ 7		6	S		S,6			2
XST4	HSP	RCX							WRITE RETRY COUNT							
	+ S	+ 6							+ S							

Legend:

* = Bit defined for TS11 but normally set to "0" by TSV05.

@ = Bit defined for TS11 but has similar (although slightly different) meaning for TSV05.

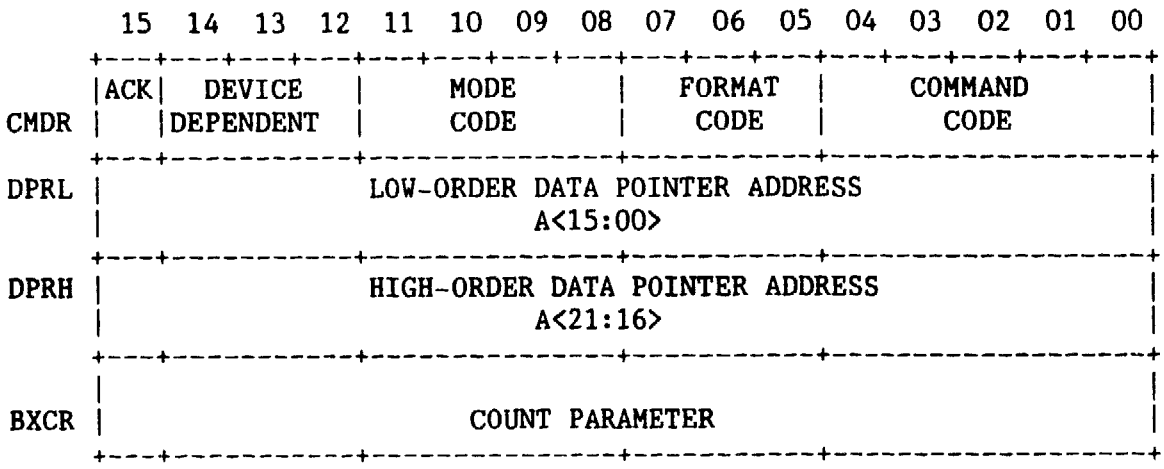
\+ = Bit not defined (unused) in TS11.

S = Status bit, not necessarily associated with a particular termination class.

1-7 = Termination class code associated with this bit.

XST4 = Extended status register 4 not defined for TS11; available in TSV05 when message buffer extent is increased.

Figure 10-12 TSV05 Extended Status Registers



NOTE
Not all words are required for all commands.

Figure 10-13 TSV05 Command Register Format

10.3 PACKET PROCESSING

The CPU passes control information to the controller by a command packet in the command buffer area (for example, a sequential series of control words) in CPU memory space. Similarly, the controller passes status information to the CPU by a message packet in the message buffer area in CPU memory space. A command is initiated by the CPU by specifying to the controller the location of the command buffer (by writing TSDBX/TSDB). The controller then becomes "busy", fetches the command and associated parameters from the command buffer, executes the command, deposits status into the message buffer, and finishes by becoming idle. The CPU then examines the TSSR hardware register and the message buffer to determine the success or failure of the command. Every command is handled in this basic manner. The following sections discuss buffer control, message buffer format, and attention handling.

The basic "packet protocol" scheme implemented by the TSV05 subsystem is identical to that implemented by the TS11/TS04 magtape system. There are, however, differences in some of the information passed between controller and CPU. These differences are in the form of extra command modes and extra or differing status fields implemented by the TSV05 subsystem when the extended features switch is set*. There is also a difference in operation of the write subsystem memory diagnostic command, whether or not extended features are enabled. These differences are discussed within the descriptions of the individual commands. The basic protocol, however, does not change.

10.3.1 Buffer Ownership and Control

To prevent the controller from updating the message buffer while the CPU is reading it, or the CPU from updating the command buffer while the controller is reading it, the concept of "ownership" is defined. Each buffer may be owned by the controller or the CPU, but not by both. Ownership of a buffer is transferred only by the current owner.

There are four different combinations of transferring the two buffers in the two directions:

1. Command Buffer: CPU to controller, by the CPU.
2. Command Buffer: Controller to CPU, by the controller.
3. Message Buffer: CPU to controller, by the CPU.
4. Message Buffer: Controller to CPU, by the controller.

Table 10-11 describes the buffer transfer operations.

An initialize aborts any current operation, and gives ownership of both the command buffer and the message buffer to the CPU.

* M7196 only. The M7206 is in extended features mode at all times.

Table 10-11 Buffer Ownership Transfers

Buffer	Direction	Transfer Method
Command Buffer	CPU to Controller	The CPU transfers ownership of the command buffer to the controller by writing the address of the command buffer into the TSDB register. This clears the SSR bit in TSSR.
Command Buffer	Controller to CPU	The controller transfers ownership of the command buffer back to the CPU by depositing a message packet (in the message buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the controller, it sets the SSR bit in TSSR to indicate that the message is in the message buffer. If the message does not contain the ACK bit set, the CPU knows that the controller did not see the last command buffer, and that the CPU still owns the command buffer. The command may be reissued by the CPU.
Message Buffer	CPU to Controller	The CPU transfers ownership of the message buffer to the controller by setting the ACK bit in the command buffer and then initiating the command by writing into TSDB. If the command buffer does not contain the ACK bit, the controller knows that the CPU did not see the last message buffer and the controller still owns it. The controller, in response to the CPU writing into TSDB, sets SSR and performs an interrupt [if the Interrupt Enable (IE) bit is set] without sending out a message, since it does not own the buffer.
Message Buffer	Controller to CPU	The controller transfers ownership of the message buffer to the CPU by writing the message buffer and setting the SSR bit. This happens at one of two times: 1. At the end of a command. 2. By outputting an ATTN message. In this case, SSR is already "1" because an ATTN only happens when the controller is inactive. Therefore, the controller clears SSR, outputs the message, and then sets SSR again (and interrupts if the IE bit was set on the message buffer release command that gave control of the message buffer to the controller). Note that for an ATTN to occur, the Enable Attention Interrupt (EAI) bit must have been set in the previous write characteristics command.

During normal command processing, the ownership of both buffers passes simultaneously: first from CPU to controller (at the start of command processing when the CPU writes a command pointer into the TSDB register), and then from controller to CPU (upon completion of the command).

10.3.2 Buffer Control on Attentions

An ATTN is enabled by the CPU by setting up the appropriate characteristics mode word on the write characteristics command. It allows the controller to flag exceptional conditions (change in transport on-line/off-line status and microdiagnostic self-test errors) when the controller is in the idle state (not executing a command).

If an ATTN condition occurs and the controller does not own the message buffer, the controller queues the ATTN internally. Then, when the CPU releases the message buffer on the next command (with the ACK bit set), the controller outputs the ATTN message with the ACK bit 00 in the message header word to indicate that the command was lost (except for the transference of ownership of the message buffer to the controller). In this case, the controller refuses to accept ownership of the command buffer. The CPU then, still owns the command buffer (because the controller did not accept the command) and also owns the message buffer now filled with an ATTN message.

If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set). Exceptions to this procedure are the write characteristics command and write subsystem memory command, which are executed regardless of a pending ATTN. These exceptions are necessary to allow the software to specify a message buffer address, control enabling of ATTNs, and perform diagnostics.

Consider the case in which the CPU wants to be notified of change in status, or a microdiagnostic error while the controller is inactive for a long period of time. To accomplish this, the controller must own the message buffer for that entire period of time. Normally, the controller gives up ownership of the message buffer at the end of a command. However, for enabling ATTN messages, ownership of the message buffer is transferred to the controller by means of the message buffer release command. This is a special command that tells the controller not to give ownership of the message buffer back to the CPU at the end of the command. The controller does not output a message at the end of this command, but just updates the TSSR register (with the SSR bit set) and interrupts (if the IE bit was set in the command and such an interrupt was enabled by the Enable Release Interrupt (ERI) bit in the previous write characteristics command). The controller then maintains ownership of the message buffer until an ATTN condition is seen, and then immediately clears SSR, outputs the ATTN message (with the ACK bit not set since the controller is not responding to a command), and then sets SSR and interrupts the CPU (if the IE bit was set on the message buffer release command). In this condition, the CPU owns the command buffer, and the controller owns the message buffer.

If the controller outputs an ATTN message, ownership of the message buffer is passed to the CPU. At that time the system is back to the state of the CPU owning both buffers. Another ATTN is not done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

If the CPU has done a message buffer release command and wants to do another command but has not received an ATTN from the controller (so that the controller still owns the message buffer from the message buffer release command), the CPU can do a command without the ACK bit set in the command buffer. At the time the command is issued, the CPU does not own the message buffer, so the CPU cannot release the message buffer.

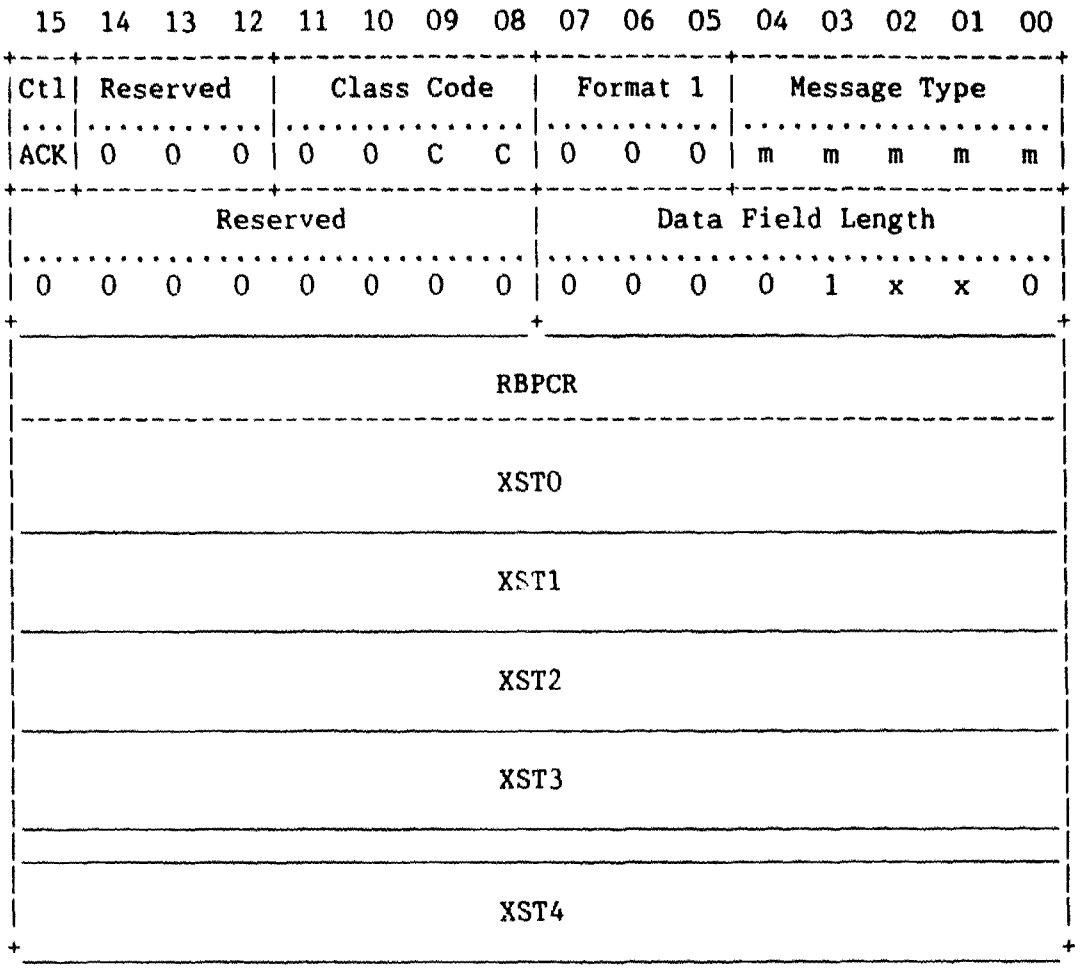
If the CPU does set the ACK bit, nothing happens except the CPU might miss an ATTN if the controller was sending out an ATTN message at the same time that the CPU was issuing the command.

It is possible that the CPU may attempt to initiate a new command at or near the same time that the controller attempts to output an ATTN message. (The command must not have the ACK bit set, since the CPU does not own the message buffer.) If the CPU writes the TSDB register while SSR is clear during an ATTN, the RMR error bit is set, and that command is ignored. The ATTN message does not have the ACK bit set, since the controller does not own the command buffer.

Note that RMR may set in this way on a bug-free system. All other settings of RMR indicate a software bug (the CPU tried to do a command before the previous command was finished). If the CPU command is lost because the controller is outputting an ATTN message, VCK and IE are not updated. If the CPU command is rejected (illegal command, and so on) and not ignored, VCK and IE are updated to the start of the rejected command.

10.3.3 Message Packet Format

Figure 10-14 illustrates the format of the message packet in the message buffer. This format is used for all messages, whether at an end of a command, or for an ATTN. The message consists of a header word, a data field length word, a residual byte/record/tape-mark count word, and either four or five extended status registers. Normally, only four extended status registers are provided. The fifth one (XST4) is available only when the extended features mode function of the controller is enabled. Table 10-12 describes the message packet.



NOTE

XST4 is not part of a TS11-compatible message buffer. It is available only when the Extended Features mode is enabled.

Figure 10-14 Message Packet Format

Table 10-12 Message Packet Field Definitions

Word	Bit	Description
1 (Header)	15	ACK (Acknowledge) – This bit is set by the TSV05 to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit is not set, since the controller does not own the command buffer.
	14-12	Reserved — These bits are reserved for future expansion. They always appear as zero.
	11-08	Class Code Field — These bits define the class of failure determined for the rest of the message buffer when the message type field is not indicating a normal END message. The codes are as follows.

Message Type	Class Code	Definition
ATTN	0000	On-line or off-line.
ATTN	0001	Microdiagnostic failure.
FAIL	0000	Not used. (On the TS11, this code indicates a bad packet due to a serial bus parity error.)
FAIL	0001	Illegal Command (ILC), Illegal Address (ILA), or NBA on a tape motion command.
FAIL	0010	Write-lock error on non-executable function.
FAIL	0011	Microdiagnostic error.

	07-05	Packet Format 1 Field — The single value supported by the TSV05 is 000, which specifies a one-word message header.
	04-00	Message Type Code — This field, together with the format field, indicates the format and length of message packets. For the TSV05 (and TS11), the message type is of the form 10xxx, which indicates that the message contains a header word, a data-Cont'd length word, and then xxx data/status words. This field indicates the general type of message contained in the buffer and is related to the termination class code appearing in the TSSR register as follows.

Termination Class Code	Message Type	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error
1,7	10011	Attention

Table 10-12 Message Packet Field Definitions (Cont)

Word	Bit	Description
2	15-08	Reserved — This field is reserved for future expansion. It always appears as "0".
(Data Length)	07-00	Data Field Length — This field specifies how many bytes of information follow this word in the message packet. Normally, with the extended features mode of the TSV05 disabled, this field contains a value of 12 (binary 00001010), indicating that the packet contains the RBPCR plus four extended status registers. With the extended features mode enabled, this field contains a value of 14 to indicate that an additional extended status register (XST4) is supplied.
3 (RBPCR)	15-00	Residual Byte/Record/File Count Register — After a read command, this word contains the difference between the number of bytes specified in the command and the number of bytes actually transferred from tape. In other words, this register indicates by how much the tape record fell short of the expected length. After a space records or skip tape marks command, this register contains the difference between the number of records or tape marks specified in the count word of the command, and the number of records or files actually skipped. Note that spacing and skipping operations can terminate before the count is exhausted for a variety of reasons (tape mark, BOT, and so on).
4 (XST0)	15-00	Extended Status Register 0 — See Section 10.2.5 for a description of this register.
5 (XST1)	15-00	Extended Status Register 1 — See Secction 10.2.6 for a description of this register.
6 (XST2)	15-00	Extended Status Register 2 — See Section 10.2.7 for a description of this register.
7 (XST3)	15-00	Extended Status Register 3 — See Section 10.2.8 for a description of this register.
8 (XST4)	15-00	Extended Status Register 4 — See Section 10.2.9 for a description of this register. Note that this register is not supplied in TS11 compatibility mode (extended features disabled).

10.3.4 General Status Handling Information

Table 10-13 summarizes the relationship between the termination class code appearing in the TSSR register, and the message type code appearing in the header word of the message buffer after a message packet has been deposited by the controller.

Table 10-13 Termination Class/Message Type Relationship

TC2-0 Value	Offset	Message Type	Meaning
0	00	END (20)	Normal Termination — The operation is completed without incident.
1	02	ATTN (23)	Attention condition — This code indicates that the drive has undergone a status change, such as going off-line or coming on-line.
2	04	END (20)	Tape Status Alert — A status condition is encountered that may have significance relating to the program. Bits of interest in the extended status registers include TMK, EOT, and RLL.
3	06	FAIL (21)	Function Reject — The specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC, and ILA.
4	10	ERROR (22)	Recoverable Error — Tape position (22) is a record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	12	ERROR (22)	Recoverable Error — Tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.
6	14	ERROR (22)	Unrecoverable Error — Tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers. Recovery is handled by the specific application program.
7	16	ATTN (23) or ERROR (22)	Fatal Subsystem Error — The subsystem is incapable of properly performing commands, or at least its integrity is seriously questionable. Refer to the fatal class code field in the TSSR register for additional information on the type of fatal error.

The following points should be noted in reference to status and error handling.

1. Error bits in the TSSR register (SC and RMR) are cleared by successfully loading a command pointer into the TSDB register, and by successfully depositing an END message.

2. All commands (even the get status command) clear the internal copy of each error bit in the extended status registers except bits 16-08 of XST3 (micro-diagnostic error code). Therefore, a Get Status command does not return the error bits as set up by a previous tape operation.

3. A read operation that encounters a TMK does not transfer any data, and gives a tape status alert termination. The TMK and RLS status bits are set, and the RBPCR word in the message buffer contains the original byte count as specified in the command.

4. A space records operation automatically terminates when a TMK is traversed, and the TMK status bit is set. Also, RLS is set if the record count is not decremented to zero.

5. A skip tape marks operation automatically terminates when two consecutive tape marks are encountered and the "Enable Skip Stop" (ESS) mode is enabled by means of the write characteristics command. RLS is set if the count is not decremented to zero. The same is also true if a tape mark is the first record off BOT, and both the ESS and ENB bits were set in the previous write characteristics data word.

6. Every write, write retry, write tape mark, write tape mark retry, and erase command that is executed at or beyond the EOT marker results in a tape status alert termination. The internal EOT status bit remains set until logically passed over in the reverse direction (rewind, reverse read, reverse space, and so on). The EOT status bit is not specifically identified with a particular record.

7. A read reverse, space reverse, reverse, or skip tape marks reverse command that encounters BOT (after the operation is underway) results in a tape status alert termination (the RIB status bit is set).

8. If a read reverse, space records reverse, or skip tape marks reverse command is issued while the tape is already at BOT, a function reject (non-executable function) status is returned.

9. When a normal rewind command is issued, the termination message and interrupt does not occur until the tape reaches BOT and has stopped. If the tape space is already at BOT when the command is issued, the transport is still commanded to rewind to make sure the tape is properly positioned.

10. When a rewind with immediate interrupt is issued, the controller commands the transport to rewind, checks for proper status, and then issues an interrupt and END message for normal termination. If a new tape motion command is issued to a rewinding unit, the controller waits until the tape is rewound to BOT before proceeding with the new command. During execution of a rewind with immediate interrupt, the MOT bit in XST0 is set if a Get Status command is performed.

11. Any write function issued at BOT (including erase, which results in the DCK bit being set) causes a termination of that command with a TSSR termination class code of 6 set to indicate an unrecoverable error. Normally, a write function causes the PE Identification (ID) burst to be written off BOT, and the controller checks for the appropriate status signal from the transport. Therefore, if DCK is set on a write off BOT, a serious transport or controller problem exists.

12. If a DCK condition is detected during a read, space, or skip function, the DCK bit is set, but the operation is not aborted. If DCK is the only error status bit set during the operation, normal termination is reported. This allows tapes with good data but bad density check (ID) areas to be read. If, in fact, a tape of the wrong density is mounted, other errors are reported and the operation stopped.

13. Note that if you begin reading a tape, get a DCK with no other errors, and then append data to the tape, the write gets a termination class code of 6, indicating that tape position is lost because DCK remains set. The whole tape should be copied over so that drives that depend on the ID burst are able to read the tape.

14. Certain failures can result in no interrupt even though the specified command had IE set. These failures include Nonexistent Memory Error (NXM), since the failure could have occurred before the IE bit was fetched from the command packet.

15. The following are notes concerning interrupts:

    a. If interrupts are enabled (the IE bit was set on the previous command accepted by the controller), interrupts may occur at any time. This is due to the possibility of diagnostic interrupts occurring immediately after normal terminations (even if ATTN interrupts are not enabled). The software must therefore defend against unexpected interrupts. The subsystem may not be usable, but the software should still not crash. Similarly, the controller could be broken in such a way that interrupts may be issued even with IE clear.

    b. With ATTN interrupts enabled (EAI bit set on the write characteristics command), a nonfatal diagnostic failure is not reported until control of the message buffer is returned to the controller. A fatal failure may interrupt at any time as long as IE is set.

    c. With ATTN interrupts disabled, a diagnostic failure is not noticeable until the next command is issued. At this time, the command is rejected.

d. When record buffering for writes is in operation, the controller issues normal termination messages and interrupts immediately after the data to be written has been stored in the controller's RAM, and before the data is actually written on tape. The possibility exists that the record cannot successfully be written on tape with the first attempt, in which case a retry algorithm is executed to attempt to successfully write the data. If the data is eventually written successfully, the CPU will not know that any problem occurred unless the extended features mode is enabled, in which case the write retry count field in XST4 is examined in the message termination the NEXT command. If retries are therefore to be logged, the software should examine the write retry count field in each message packet.

e. If record buffering for writes is in operation and the controller cannot write a stored record successfully from its RAM (retry count exhausted), the next tape motion command following the write command associated with the failed record is terminated with termination class 6 (tape position lost), and the RCX bit in XST4 is set. In addition, the Uncorrectable Error (UNC) bit in XST1 is set. The tape is positioned one record beyond the last successfully written record.

10.4 COMMANDS

The TSV05 subsystem is capable of running on programs that are, in most cases, identical to those written for the TS11/TS04 magtape subsystem. When the extended features mode of the TSV05 subsystem is disabled, the following commands and their associated command modes operate identically to those of the TS11, except for some of the extended error status bits provided for by the TS11, but not by the TSV05.

- READ
- WRITE
- POSITION
- FORMAT
- GET STATUS

With extended features enabled*, the above commands have the capability to perform 22-bit memory addressing and, in addition, some command modes (subcommands) are added that are not in the TS11 repertoire; however, basic operation of the basic TS11 command remains the same.

The following commands differ in their meanings to TSV05 and TS11 hardware.

WRITE CHARACTERISTICS	Same as TS11 except for the ability of the TSV05 subsystem to specify an extra characteristics data word to control special features (when the extended features switch is set), and also to specify a longer than normal message buffer length to accommodate an extra extended status register.
WRITE SUBSYSTEM MEMORY	The data format and function is entirely different from that of the TS11.
CONTROL	Function is the same as TS11 except for the clean tape command mode, which the TSV05 subsystem treats as a NO-OP — tape is not moved. In addition, when extended features is enabled, two new command modes are added.
INITIALIZE	Similar to TS11 in that control logic is initialized but the tape transport itself is not initialized in certain non-error states.

The following sections describe the general command format, then each command is described in detail.

* M7206 always enabled

10.4.1 Command Packet Definitions

The CPU issues a command to the TSV05 subsystem by first building a command packet in CPU memory space (on a modulo-4 address boundary), then writing the address of the packet into the TSV05 TSDB hardware register. The address written is called the command pointer. Assuming that the TSV05 subsystem is ready to accept a command, writing the command pointer initiates command processing, in which the controller fetches the command packet and executes the command encoded within the packet.

Logically, a command packet can be composed of one, two, three, or four 16-bit words, depending upon the type of command and the amount of information it needs to proceed with execution. All command packets begin with a command packet header word (Figure 10-15). The format of this word is the same for all commands; the encoding of the various fields within the word distinguishes one command from another. Table 10-14 defines the fields within the header word. Table 10-15 summarizes the command code and command mode field definitions. The following sections describe each command in detail, along with its specific command packet format. Figure 10-15 illustrates the positioning of tape data bytes in CPU memory under various conditions (forward, reverse, swap bytes, and so on) for read and write commands.

Certain bits of the header word and other words within the command packet are not defined for all commands. When building the command packet, the software sets these undefined bits to zero. If any bit is undefined or reserved with respect to a particular command and the bit is not zero, the command is not executed and is terminated with a function reject (termination class 3).

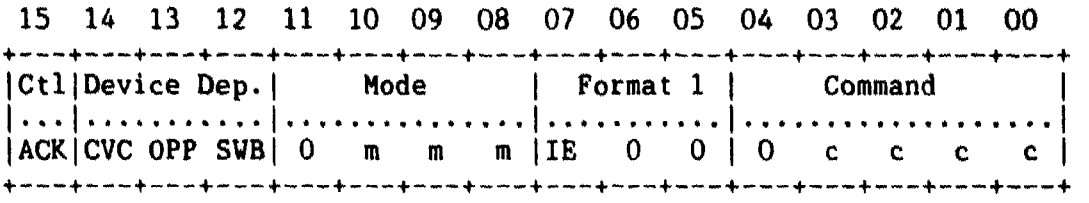


Figure 10-15 Command Packet Header Word

Table 10-14 Command Packet Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge (ACK)	This bit should be set when issuing a command when the CPU owns the message buffer. Its function is to inform the TSV05 that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the TSV05 controller. If the CPU has released ownership of the message buffer to the TSV05 for ATTNs and has not received an ATTN message yet, the ACK bit is coded as a "0".
14-12	Device Dependent Bits	These three bits perform functions applicable to particular commands. The bit definitions are as follows.
		Bit **Name** **Definition**
		14 CVC Clear Volume Check — When set, causes the volume check condition, set when the transport goes from off-line to on-line, to be cleared, thereby allowing tape operations to be executed on the transport.
		13 OPP Opposite — When set, reverses the execution sequence of reread commands (that is, reread next, previous, and so on).
		12 SWB Swap Bytes — When set, instructs the TSV05 to alter the sequence of storing and retrieving tape data bytes from the CPU memory. When SWB=0, the "first" byte in a word is the least significant byte (bits 07-00); this is the standard DIGITAL method. When SWB=1, an industry-standard method is specified, in which the first byte of a word is considered to be bits 16-08. Figure 10-16 illustrates the positions of bytes as written or read from memory.
11-08	Command Mode Field	This field acts as an extension to the command code field and allows further specification of device commands, as detailed in Table 10-15.

Table 10-14 Command Packet Header Word Bit Definitions (Cont)

Bit	Name	Function
07-05	Packet Format #1	This field defines the header type (only one type is used in the TSV05 and Field TS11) and the interrupt enable. The only two valid configurations are: **Bit Values** — **Definition** 000 — One-Word Header; Interrupt Disable 100 — One-Word Header; Interrupt Enable
04-00	Command Code	This field defines that major command category. It is used together with the command mode field to specify the command, as defined in Table 10-15.

Table 10-15 Command Code and Mode Field Definitions

Command Code	Command Name	Command Mode		Mode Name
00001	READ	0000	-	Read Next (Forward)
		0001	-	Read Previous (Reverse)
		0010	-	Reread Previous (Space Reverse, Read Forward)
		0011	-	Reread Next (Space Forward, Read Reverse)
00100	WRITE CHARACTERISTICS	0000	-	Load Message Buffer address and Set Device Characteristics
00101	WRITE	0000	-	Write Data (Next)
		0010	-	Write Data Retry (Space Reverse, Erase, Write Data)
00110	WRITE SUBSYSTEM MEMORY	0000	-	Enter Maintenance Mode and Load Test Functions (diagnostic use only)
01000	POSITION	0000	-	Space Records Forward
		0001	-	Space Records Reverse
		0010	-	Skip Tape Marks Forward
		0011	-	Skip Tape Marks Reverse
		0100	-	Rewind
01001	FORMAT	0000	-	Write Tape Mark
		0001	-	Erase
		0010	-	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
01010	CONTROL	0000	-	Message Buffer Release
		0001	-	Rewind and Unload
		0010	-	NO-OP (Performs Clean Tape function in TS11)
		0100*	-	Rewind with Immediate Interrupt
01011	INITIALIZE	0000	-	Controller/Drive Initialize
01111	GET STATUS	0000	-	Get Status (output END status message)

* Extended features function not part of the TS11 repertoire.

Swap Bytes = 0
Buffer Address = 1000
Byte Count = 10(8)
Block Size = 10(8) bytes

1000	1	0
1002	3	2
1004	5	4
1006	7	6

Swap Bytes = 1
Buffer Address = 1000
Byte Count = 10(8)
Block Size = 10(8) bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	7

Swap Bytes = 0
Buffer Address = 1001
Byte Count = 10(8)
Block Size = 10(8) bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

Swap Bytes = 1
Buffer Address = 1001
Byte Count = 10(8)
Block Size = 10(8) bytes

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

NOTE
Byte 0 indicates the byte nearest to BOT.

a. Forward Tape Direction, Read or Write; Reverse Read with Even Byte Count

Figure 10-16 Memory/Tape Data Byte Positioning (Sheet 1 of 2)

Swap Bytes = 0
Buffer Address = 1000
Byte Count = 7
Block Size = 7 bytes

1000	1	0
1002	3	2
1004	5	4
1006		6

Swap Bytes = 1
Buffer Address = 1000
Byte Count = 7
Block Size = 7 bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	

Swap Bytes = 0
Buffer Address = 1001
Byte Count = 7
Block Size = 7 bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5

Swap Bytes = 1
Buffer Address = 1001
Byte Count = 7
Block Size = 7 bytes

1000		0
1002	1	2
1004	3	4
1006	5	6

NOTE
Byte 0 indicates the byte nearest to BOT.

b. Forward or Reverse Read, Odd Byte Count

Figure 10-16 Memory/Tape Data Byte Positioning (Sheet 2 of 2)

10.4.2 Get Status Command

Figure 10-17 illustrates the Get Status command packet. This command causes a message packet to be deposited in the message buffer area in order to update the extended status registers. However, after the end of any command except message buffer release, the TSV05 hardware automatically updates the extended status registers, so this command need be used only when the TSV05 subsystem is left idle for some time, or when a status register update is desired without performing a tape motion command, or when the user desires to read the unit number of the currently selected tape transport (deposited in bits 02-00 of extended status register 2).

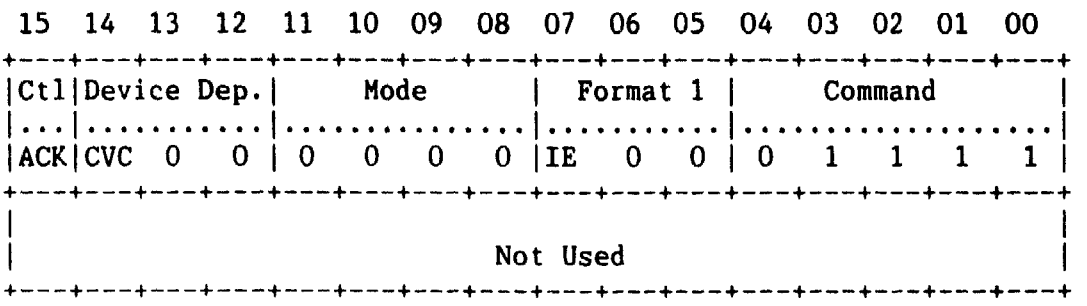


Figure 10-17 Get Status Command Packet

10.4.3 Read Command

Figure 10-18 illustrates the command packet for a read. There are four normal modes of operation: read forward, read reverse, reread previous, and reread next. Two of these modes (the rereads) are further controlled by the state of the OPP bit in the packet header word.

Mode	Function
0000	Read Next (Forward)
0001	Read Previous (Reverse)
0010	Reread Previous
	OPP = 0: Space Reverse, Read Forward
	OPP = 1: Read Reverse, Space Forward
0011	Reread Next
	OPP = 0: Space Forward, Read Reverse
	OPP = 1: Read Forward, Space Reverse

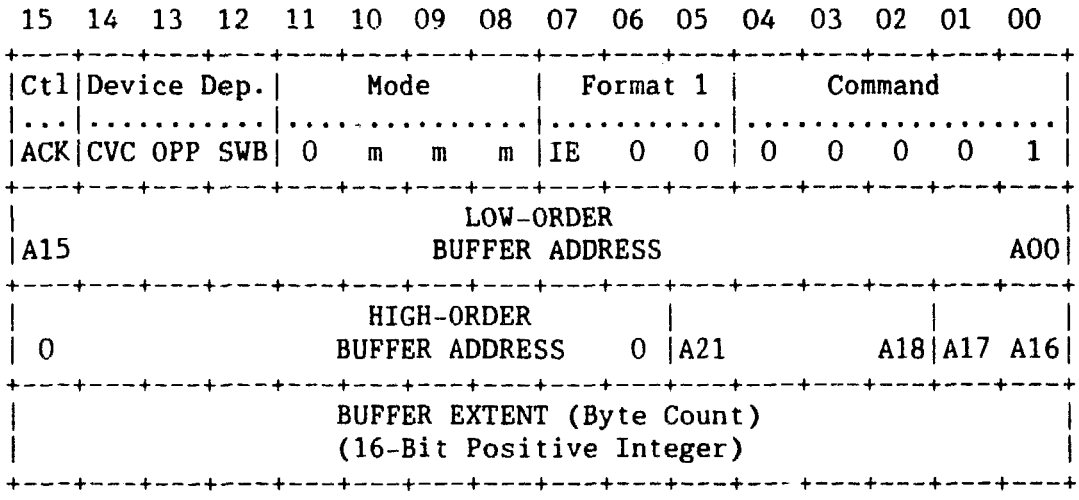


Figure 10-18 Read Command Packet

The command packet for a read contains four words: a header word, two words specifying the address of the data buffer in CPU memory space where the data read from tape is to be deposited, and a buffer extent (byte count) word specifying the number of bytes available in the data buffer and the number of bytes expected in the tape record to be read. A byte count of "0" specifies that 65,536 (64K) bytes are expected.

The third word in the packet specifies the high-order address bits of the starting address of the data buffer. When the extended features mode is disabled (that is, the TSV05 subsystem is running in TS11 compatibility mode), only the two low-order bits (A17 and A16) may be nonzero. These bits, together with the 16 bits in the second word of the packet, allow an 18-bit memory address to be specified for the start of the data buffer. In this case, if any of bits 02-15 are nonzero, the function is not performed, but terminates with a function reject with ILA error status. When the extended features mode is enabled, the low-order six bits of the third word are used to specify bits A21-A16 of a 22-bit memory address. In this mode, if any of bits 06-15 in the third word are nonzero, the command is aborted with function reject termination with ILA error status.

The read operation is assumed to be for a record of known length. Therefore, the correct record byte count (fourth word of the packet) must be known. If the byte count exactly equals the record length, normal termination occurs. If the record is shorter than the specified byte count, the RLS error bit is set in XST0, and a tape status alert termination occurs. If the record on tape is larger than the byte count, the RLL error bit is set in XST0, and tape status alert termination given. In this case, only the number of bytes specified in the byte count is transferred to the data buffer. Also, any read operation that encounters a tape mark does not transfer any data. In this case, the TMK and RLS bits are set, and a tape status alert termination given.

Reverse read operations that pass BOT cause the RIB bit in XST3 to be set, and tape status alert termination given. If the tape is already at BOT when a reverse read (that is, read previous or reread previous with the OPP bit set) is issued, there is no tape motion, and function reject termination occurs, with the NEF error bit set in XST0.

The OPP bit in the header word (bit 13) alters the execution sequence of the reread command modes as follows:

- Reread previous (space reverse, read forward) becomes read reverse, space forward.
- Reread next (space forward, read reverse) becomes read forward, space reverse.

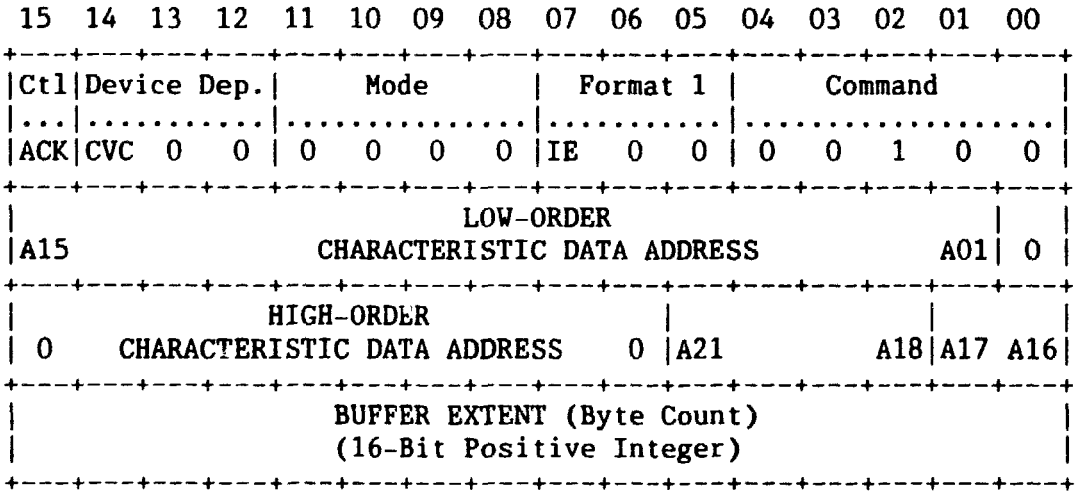
Reading data in the reverse direction with a correct byte count places data in memory correctly (as if the record were read in the forward direction), not in reverse order. This feature allows data to be placed correctly in memory on one retry (read reverse). On a reverse read, data is placed in the data buffer in the reverse order (highest address first); the starting address is calculated by adding the byte count to the address specified in the command packet and then subtracting 1. If the byte count is greater than the actual record length, the beginning of the data buffer (lowest addresses) does not contain the data from tape. Similarly, if the actual record is larger than the byte count, the first part of the record (that nearest to BOT) is not placed in the data buffer.

For any of the data transfers, the Swap Bytes (SWB) bit in the command header word controls the storing of bytes in CPU memory, as shown in Figure 10-16.

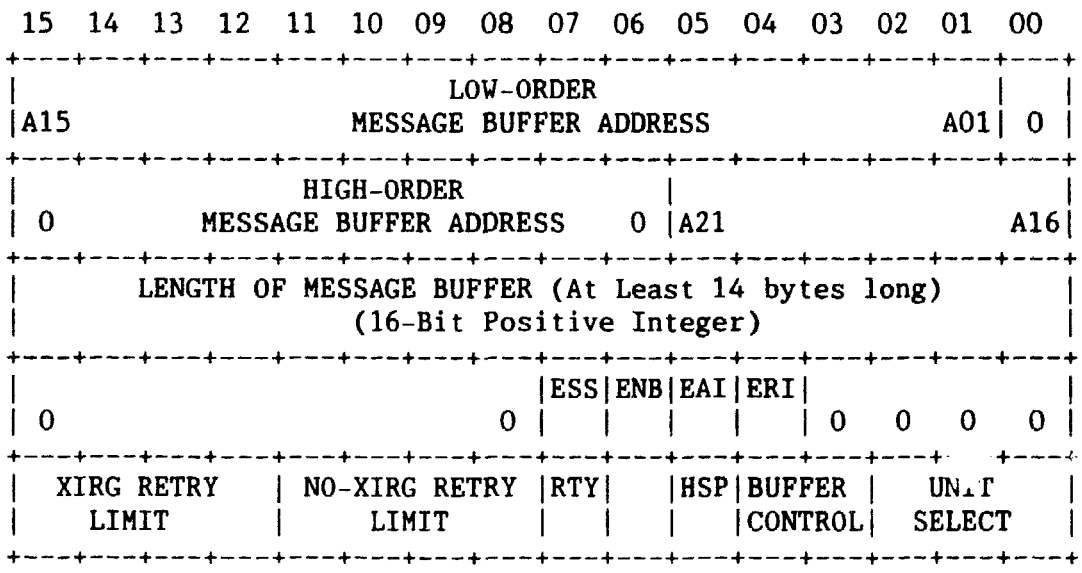
10.4.4 Write Characteristics Command

Figure 10-19 illustrates the write characteristics command packet and data format. The objective of this packet is to inform the TSV05 subsystem of the location and size of the message buffer in the CPU memory space. The message buffer must be at least seven contiguous words long (eight when the extended features mode is enabled), and located on a word boundary.

The write characteristics command also transfers a characteristics mode word to the controller and, if extended features is enabled, an additional control word. The characteristics mode word causes specific actions for certain operational modes. The bits for this word are defined in Table 3-17. Table 3-18 defines the bits in the additional control word available when extended features is enabled.



a. Command Packet



b. Characteristics Data

Figure 10-19 Write Characteristics Command Format

Table 10-16 Characteristics Mode Data Word Bit Definitions

Bit	Name	Definition
15-08 03-00	-	Not used. These bits are not checked by the TSV05 controller. Their state does not affect operation, but they should be written to 0.
07	ESS	Enable Skip Tape Marks Stop — When set, this bit instructs the controller to stop and set the LET status bit during a skip tape marks command when a double tape mark (two contiguous tape marks) is detected. Setting this bit also enables operation of the ENB bit. In the default setting of "0", the skip tape marks command terminates only on tape mark count exhausted, if it runs into BOT, or if it runs 4.6 m (15 ft) past the EOT marker.
06	ENB	Enable Tape Mark Stop Off BOT — This bit is meaningful only if the ESS bit is set. When this bit is set (and ESS = 1), the tape is at BOT, a skip tape marks forward command is issued, and the first record seen is a tape mark. Then the controller stops the operation and sets the LET status bit in XST0. If this bit is clear under these conditions, the controller merely counts the tape mark and continues.
05	EAI	Enable Attention Interrupts — When this bit is "0", attention conditions such as transitions from on-line to off-line and off-line to on-line and microdiagnostic failures do not result in interrupts to the CPU. Rather, a diagnostic failure or off-line/on-line transition is not noticeable until the next command is issued; at this time, the command is rejected. With this bit set to "1", attention conditions cause an ATTN message to be generated (and an interrupt, if the IE bit is set on the last command) as soon as the controller owns the message buffer.
04	ERI	Enable Message Buffer Release Interrupts — If this bit is "0", interrupts are not generated upon completion of a message buffer release command. Upon recognition of the command, only SSR is reasserted. If ERI is "1", an interrupt is generated (without an accompanying message packet).

Table 10-17 Extended Characteristics Data Word Bit Definitions

Bit	Name	Description
15-12	XGRL	Extended Interrecord Gap (XIRG) Retry Limit — The value in this field, taken as a 4-bit positive integer, specifies the number of times the controller attempts to write a buffered record before aborting buffered write operation. A retry with XIRG consists of a backspace over the faulty record, an erase of 8.9 cm (3.5 in) of tape, then a write of the buffered record (from RAM). An XIRG retry is attempted once after the non-XIRG retry limit is reached; then, if still not successful, another series of non-XIRG retries is attempted. The total number of retries allowed on any record is therefore the non-XIRG limit times the XIRG limit. This field has meaning only if write buffering is enabled and bit 07, Retry Algorithm Control (RTY), is set.
11-08	NXGRL	Nonextended Interrecord Gap Retry Limit — The value in this field, taken as a 4-bit positive integer, specifies the number of times the controller attempts to write a buffered record without generating an extended IRG before attempting a retry with an extended IRG. A retry without an XIRG consists of a backspace over the faulty record, then a write of the buffered record (from RAM); no special erase is performed. This field has meaning only if write buffering is enabled and bit 07, RTY, is set.
07	RTY	Retry Algorithm Control — When this bit is "0" and the controller is write buffering, the default retry algorithm (one backspace, then write with extended IRG, up to 10 times) is used when a record cannot be successfully written onto tape. When this bit is "1", the retry limits in bits 08-15 are used.
05	HSP	High-Speed Select — When this bit is "0", the transport operates at a tape speed of 64 cm/s (25 in/s) When "1", the transport operates at 254 cm/s (100 in/s).
04,03	BUF CTL	Buffering Mode Control — This 2-bit field controls the read and write buffering capabilities of the controller. The codes are defined as follows.

M7196

Bit 04	Bit 03	Function
0	0	Buffering is enabled or disabled by means of the switch setting on the module. This is the default condition.
0	1	No buffering is performed; the switch is ignored.
1	0	Enable read buffering only; the switch is ignored.
1	1	Enable both read and write buffering; the switch is ignored.

Table 10-17 Extended Characteristics Data Word Bit Definitions (Cont)

Bit	Name	Description
		M7206
		Bit 04 / **Bit 03** / **Function** 0 / 0 / Use hardware DIP switch setting 0 / 1 / No auto speed control and no PE ID burst detect 1 / 0 / Auto speed control in firmware and no ID burst detect 1 / 1 / Let driver control auto speed and detect ID burst
02-00	USEL	Unit Select — This field selects a transport for subsequent tape operations. Initialize always sets the unit selection to "0".

The four command packet words are identical to those used for the TS11, except for the third word (high-order characteristic data address). In this word, bits 02 through 05 are used to specify bits 18 through 21, respectively, of the address specifying the location of the associated characteristics data buffer.

The data buffer must reside on an even address in CPU memory space. If bit 00 of the second packet word (low-order characteristic data address), or bits 02-15 (extended features disabled), or bits 06-15 (extended features enabled) of the third packet word (high-order characteristic data address) are nonzero, the function is not executed but is terminated with a function reject. In this case, no message packet is stored, but an interrupt is generated if the IE bit is set.

When the extended features switch on the interface/controller module is OFF, the write characteristics command functions identically to that of the TS11. When the extended features switch is ON, a fifth characteristics data word can be specified to invoke special functions. In addition, a message buffer extent of 16 bytes (eight words) can be specified so that extended status register 4 (unique to the TSV05 subsystem) can be output.

Similarly, the first four words of the five-word characteristic data buffer are identical to those used for the TS11, except for the third word (high-order message buffer address). In this word, bits 02 through 05 are used to specify bits 18 through 21, respectively, of the address specifying the location of the message buffer to be used for subsequent status and attention messages.

The fifth characteristic data word is used to specify parameters for the multirecord buffering mode of operation, and is also used to select a tape unit in a multidrive system.

The write characteristics command clears the NBA bit in the TSSR register, indicating that a valid message buffer is specified, if all of the following conditions are met.

- The command was not rejected because of nonzero bits in reserved or unused fields within the first three command packet words.
- The fourth packet word (byte count) contains at least a count of six to allow the first three characteristic data words to be fetched.
- The first two data words specify a valid even address (word boundary).
- The third data word contains a value of 14 or greater (specifying the length of the message buffer).

If any of the above conditions are not met, then the NBA bit is set (even if it was already clear from a previous valid write characteristics command) and no further message packets are deposited.

Note that if the byte count word in the command packet is less than seven, the characteristic mode data word is not fetched, causing the current values of the characteristic mode bits stored in the controller to be retained. Similarly, if the byte count is less than 10, the additional extended features control word is not fetched and the current values retained.

10.4.5 Write Command

Figure 10-20 illustrates the command packet for a write. There are two normal modes of operation: write data and write data retry.

The allowable mode field codes and their functions are:

Mode	Function
0000	Write Data
0010	Write Data Retry (Space Reverse, Erase, Write Data)

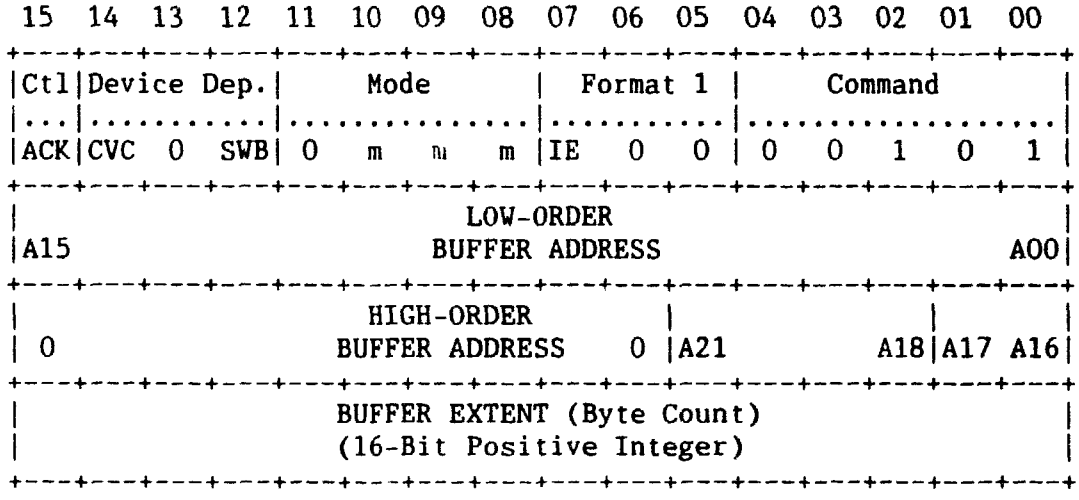


Figure 10-20 Write Command Packet

The command packet for a write contains four words: a header word, two words specifying the address of the data buffer in CPU memory space where the data to be written onto tape is stored, and a buffer extent (byte count) word specifying the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

The third word in the packet specifies the high-order address bits of the starting address of the data buffer. When the extended features mode is disabled (that is, the TSV05 subsystem is running in TS11 compatibility mode), only the two low-order bits (A17 and A16) may be nonzero. These bits, together with the 16 bits in the second word of the packet, allow an 18-bit memory address to be specified for the start of the data buffer. In this case, if any of bits 02-15 are nonzero, the function is not performed but terminates with a function reject with ILA error status. When the extended features mode is enabled, the low-order six bits of the third word are used to specify bits A21-A16 of a 22-bit memory address. In this mode, if any of bits 06-15 in the third word are nonzero, the command is aborted with function reject termination with ILA error status.

For any of the write modes, the SWB bit in the command header word controls the fetching of bytes from CPU memory, as shown in Figure 10-16.

If a write command is executed at or beyond the EOT marker, the data is written but a Tape Status Alert (TSA) termination occurs. EOT remains set until passed in the reverse direction.

If a write data command is issued while the tape is positioned at BOT, the PE IDB is written onto the tape. This should clear the DCK status bit if it was set. If DCK does not clear, the transport is faulty. If any write command is issued with the DCK bit set and the tape not positioned at BOT, no data is written and tape position lost termination occurs. If a write retry command is issued while the tape is positioned at BOT, a function reject termination occurs, with the NEF error bit set in XST0.

During writes, the controller generates a parity bit for each data byte sent to the transport; the transport then writes this bit along with the data byte onto tape. During the write, the transport also reads the written bytes from tape and checks the parity; the data is also sent to the controller, which also checks the parity. Therefore, two types of data errors can arise during a write: a correctable error or an uncorrectable error. In either case, the CPU should immediately issue a write retry command to rewrite the data correctly.

10.4.6 Position Command

Figure 10-21 illustrates the position command packet. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. The tape mark/record count is the second word of the command packet. This word is ignored for a rewind command.

The allowable mode field codes and their functions are:

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Record Count Ignored)

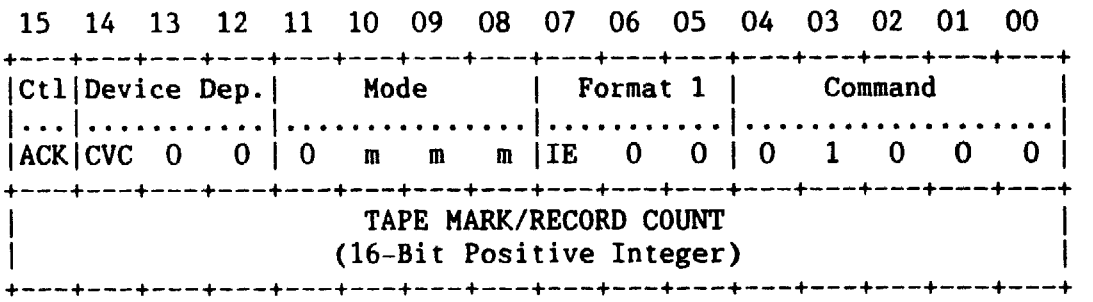


Figure 10-21 Position Command Packet

The space records operation skips over the number of records specified in the record count word of the command packet. However, the operation automatically terminates, with a TSA termination code, when a tape mark is traversed (the tape mark is included in the record count). Also, the RLS status bit in XST0 is set if the record count is not decremented to zero.

A skip tape marks command skips over the number of tape marks specified in the tape mark count word of the command packet. However, the operation automatically terminates if a double tape mark (two contiguous tape marks without intervening data) is encountered and the ESS bit is set in the characteristic mode word on the last write characteristics command. Termination also occurs if a tape mark is the first record off of BOT and ESS, and ENB bits are set in the characteristic mode word. RLS is set if the tape mark count is not decremented to zero.

A space records reverse or skip tape marks reverse, which runs into BOT, sets the Reverse Into BOT (RIB) status bit, and causes a TSA termination. If one of these reverse commands is issued while the tape is already positioned at BOT, the NEF error bit is set, and function reject termination given. In this case, the tape does not move. If the DCK error is present when a position command is issued, the DCK bit is set, but the operation is not stopped (it terminates with TSA). This allows tapes with a bad IDB area to be read.

When a rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches BOT and has stopped.

10.4.7 Format Command

Figure 10-22 illustrates the format command packet. Note that the second word is present (fetched by the controller) but is not used in the command. This command can write a tape mark, rewrite a tape mark, or erase tape

The allowable mode field codes and their functions are:

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

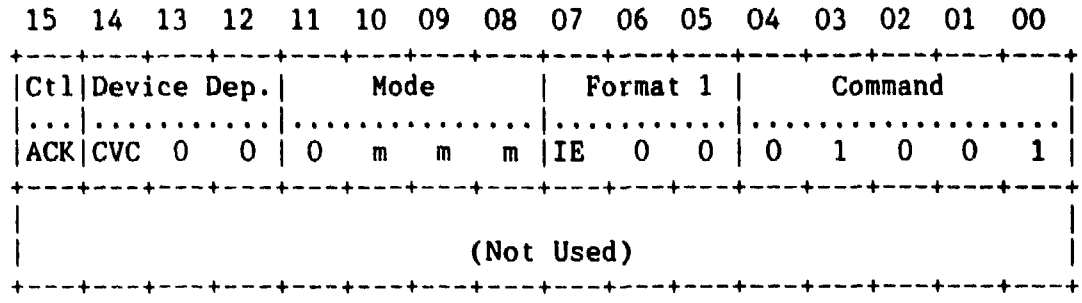


Figure 10-22 Format Command Packet

In all cases, executing a format command at or beyond EOT causes a TSA termination. The EOT bit remains set until the EOT marker is passed in the reverse direction.

A write tape mark or erase command issued at BOT automatically causes the PE IDB to be written on the tape. If, during this operation, the IDB is not received from the transport (that is, there is a transport or cable problem), DCK error is set and tape position lost termination occurs.

If the DCK bit is already set and the tape is not at BOT, a format command is aborted with tape position lost termination; the tape will not move.

The write tape mark command causes approximately 9.5 cm (3.75 in) of tape to be erased, and a file mark to be written. The erase command merely causes 9.5 cm (3.75 in) of tape to be erased. Successive erase commands are used to erase more than 9.5 cm (3.75 in) [9.5 cm (3.75 in) increments].

The write tape mark retry command causes a space reverse (over the previous record), followed by an erase of 9.5 cm (3.75 in) of tape, followed by a write tape mark [which erases 9.5 cm (3.75 in) more of tape before writing the file mark]. If the tape is positioned at BOT when the write tape mark retry command is issued, the operation is aborted with function reject termination, and the NEF error bit is set.

10.4.8 Control Command

Figure 10-23 illustrates the control command packet. There are three normal modes (message buffer release, rewind and unload, and NO-OP) and one additional mode (rewind with immediate interrupt). The control command is characterized by the fact that termination (and an interrupt if the IE bit is set) occurs immediately at the start of the command.

The allowable mode field codes and their functions are:

Mode	Function
0000	Message Buffer Release
0001	Rewind and Unload
0010	NO-OP (performs clean tape function in TS11)
0100	Rewind with Immediate Interrupt

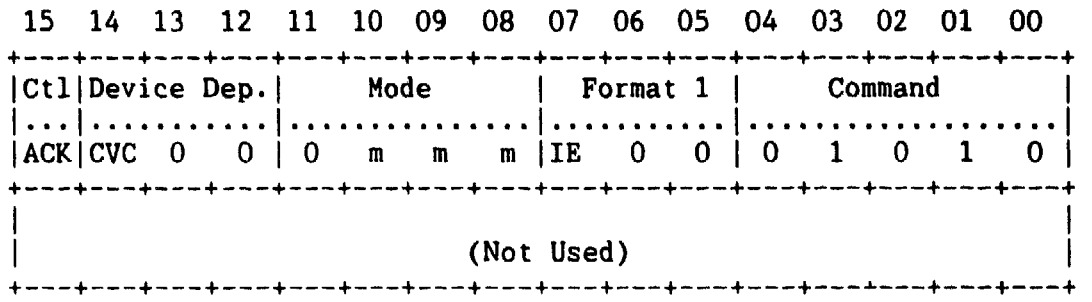


Figure 10-23 Control Command Packet

When executed with the ACK bit set, the message buffer release command allows the controller to own the message buffer so it can update the status in the message buffer area on an ATTN. This would be used when the CPU is not operating the TSV05 subsystem for a period of time, but desires to be notified of a change in status or a microdiagnostic error.

The rewind and unload command rewinds the tape completely onto the supply reel, and places the transport in the off-line state. When this command is executed, termination (and an interrupt if IE is set) occurs immediately.

When the NO-OP command is issued, normal termination occurs immediately, and no tape motion results.

The rewind with immediate interrupt command causes the tape to be rewound to BOT. This command differs from the normal rewind command, in that termination response to the CPU occurs at the start of the rewind rather than when the tape reaches BOT. This command would therefore be used in a multitransport system when it is desired to select another unit after issuing a rewind. If a transport is rewinding and another tape motion command is issued to it, the new controller waits until the tape is rewound to BOT before proceeding with the new command. During execution of a rewind with immediate interrupt, the MOT bit in XST0 is set if a get status command is performed.

10.4.9 Initialize Command

Figure 10-24 illustrates the initialize command packet. If there are no microdiagnostic errors, this command is treated as a NO-OP. If there are errors present, however, the command performs the same as a write into the TSSR register. In either case, IFEN to the tape transport is pulsed to stop runaway commands.

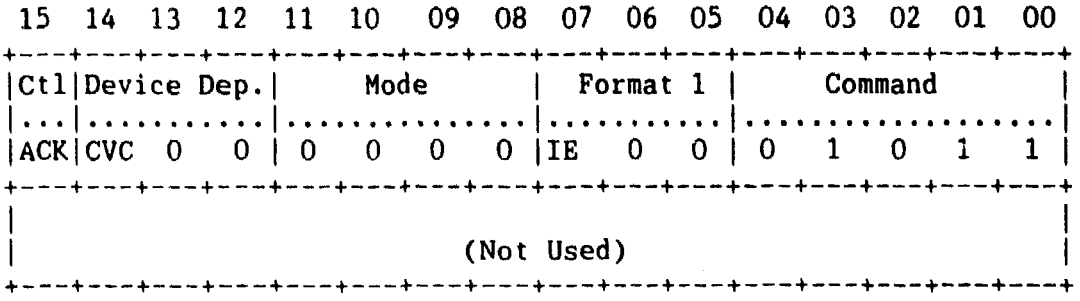


Figure 10-24 Initialize Command Packet

10.4.10 Write Subsystem Memory Command

This command is used for the diagnostic programs, and is not applicable to programming for normal operations.

10.5 RECORD BUFFERING (-A/B ONLY)

The record buffering mode of operation can be invoked to optimize system performance when performing read and write operations on a "streaming" tape transport. The technique causes tape records to be "cached" (buffered) in the controller, in order to avoid many of the long repositioning delays frequently encountered when dealing with a streaming tape transport. Repositioning occurs if the tape transport does not receive its next command before the reinstruct period expires.

On a typical system, the chances are high that, in a non-buffering mode, the software misses the reinstruct period (for example, data to be written must be transferred from a disk, or data read must be transferred to a disk, and so on) since the software cannot always keep the transport busy. Buffering is a means to decrease the number of repositionings while transferring a file of sequential records.

The effect of buffering serves to lengthen the apparent reinstruct period (as seen from the CPU), since tape data transfers can be overlapped with the CPU operations required to prepare for issuing the next command to the tape subsystem.

Read buffering causes an additional record to be read from tape in response to a program requesting just one. Typically, a program requests several records in succession, so a record stored in the controller is available for immediate transfer to the CPU, and can be transferred while another record is being read or the tape is repositioning. Only the read next command (for example, a forward read) causes the buffering algorithm to be invoked.

Write buffering allows one record to be accumulated within the controller and subsequently written to tape, allowing transfer of data from CPU memory to controller to be overlapped with tape repositioning. This also allows the CPU to prepare and issue the next write command while the previous (stored) record is being written to tape. Therefore, there can be two records ready for transfer; one in the controller, and one in CPU memory.

Record buffering is enabled either by software or hardware. If the extended features switch is set, it can be enabled or disabled by means of the "extra" (fifth) characteristics data word. If extended features is OFF, it is enabled or disabled only by the buffering enable switch. The following sections describe the operations performed for read and write buffering.

10.5.1 Read Buffering

Assuming that the transport is ready for an operation (on-line, and so on), the following occurs when a read next (forward) command is issued to the controller, and buffering is enabled.

1. When a read next command is issued, the tape is started and data is transferred from tape to CPU memory in the normal fashion.
2. When the final byte of data from the tape has been transferred to CPU memory and the transport has negated the DATA BUSY signal, the controller tests the status inputs from the transport bus and determines if any errors or special incidents occurred.
3. If an error occurred, or if a tape mark was read, or if the tape is beyond the EOT marker, the controller terminates the operation by issuing the appropriate status message, and does not automatically issue another command to the tape transport. The controller returns to its idle state (before step 1), and the tape transport is allowed to complete its sequence.
4. If the transfer completed without incident, the controller issues its normal successful termination message. The program in the CPU can then act on this message (that is, begin transfer of the data to disk, and so on).
5. If the transfer completed without incident, and if the record just read was 3.5K bytes or less in length (for example, could fit entirely within the controller's RAM), the controller issues another read forward command to the transport, reads the next record from tape, and stores the data in its internal RAM (up to 3.5K bytes of data). This operation can be termed "pre-reading".
6. When the next record has been read, or if an "incident" occurs (tape mark, EOT, or error), whichever occurs first, the tape drive is allowed to stop. In addition, if, during a pre-read, data on tape is not encountered within one second, the pre-read is aborted and the tape allowed to stop, since there may be no more data on the tape. If this is the case and a read next is eventually issued for this nonexistent record, the operation terminates with an OPI error after 7.6 meters (25 feet) of tape have been passed without encountering data.
7. While the controller is pre-reading the next record, it is monitoring the Q-bus interface for the next command from the CPU.
8. If the next command is read next, the controller immediately begins transferring the pre-read data record from RAM to CPU memory (this transfer can be performed during the pre-read of data from tape).
9. When the pre-read record has been transferred entirely to CPU memory, the controller issues another read command to the tape transport, and the cycle repeats.

10. If additional sequential read next commands are issued, data is supplied from the RAM until its contents are exhausted. The cycle then repeats from step 1 if another read next is issued.

11. If an end of file mark is encountered on tape, or if any errors occur, pre-reading of records ceases. If errors occur, the controller spaces one record reverse (only if the 7.6 meter (25 foot) timer did not abort on the pre-read). The tape is logically positioned just before the record of incident. If and when a read command is received from the CPU to read a record, normal read operation occurs. If the 7.6 meter (25 foot) timer expired from the previous pre-read, tape position lost is reported in response to this read command. If an end of file mark is encountered on tape, the controller records this, and does not move the tape. The next command handles the file mark appropriately.

12. If any command other than a read next is issued by the CPU, and if the controller RAM still contains a pre-read record, the new command is stored internally (so that action may eventually be taken) and the controller performs a recovery action as follows:

    a. If a record is currently being read from tape, the controller allows the operation to complete and the transport to negate data busy.

    b. If the new command is a space records (either forward or reverse), the current tape position is compared with the tape position assumed by the CPU program (based upon the last record transferred to CPU memory). The controller recomputes the record count required to reach the final target position, and enters the normal space forward or space reverse sequence, using the new record count.

    c. If the new command is a rewind or rewind/unload, the rewind sequence is immediately performed; no further adjustment in tape position is required.

    d. If the new command is a skip tape marks, the controller determines if it contains an outstanding pre-read file mark, and recomputes the skip count. If there is no pre-read file mark, no adjustment is necessary. If one exists, the count as supplied by the CPU is adjusted by one (plus or minus). The normal skip sequence is then entered.

    e. If the new command is other than those listed above, the controller repositions the tape by skipping one record in reverse (to space back over the pre-read record outstanding) before executing the new command.

13. If, during pre-reading, data from the current tape record does not fit into the space currently available in RAM, the tape operation is aborted and the controller directs the transport to space reverse in order to recover proper tape position. The controller does not attempt to pre-read the record that was aborted.

10.5.2 Write Buffering

Record write buffering allows the CPU to issue successive write data commands to the controller, with the controller storing one record up to 3.5K bytes in length in its RAM. When a write data command is first received, a "fetch from memory" process is started to transfer data from CPU memory to the controller RAM. Then, when at least one byte of data is available in RAM, the tape transport is directed to write and an "output to tape" process, which is started to transfer data from the RAM to the FIFO. These processes are relatively independent, with a supervisory loop overlayed to keep track of RAM buffer management and abnormal conditions.

Initially, the tape is probably at rest or in a repositioning cycle. Therefore, the "access time" (the time elapsed since the controller commanded the transport to write, and the time when the first character was strobed out of the FIFO and written onto tape), is relatively long. During this time, another write data command can be accepted from the CPU (but not given a termination response), with the associated data held in CPU memory. When in buffering mode, a successful termination status is given to the CPU as soon as a record has been transferred completely from CPU memory to RAM, thereby allowing the CPU to issue another write next command. It is therefore possible that the "output to tape" process is one record behind the "accept new command" process. The overall effect is to allow the CPU to overlap the preparation of one record with the writing to tape of the previous record, allowing the controller to command the transport to write within its reinstruct time.

If a record is specified to be greater than 3.5K bytes (the amount of RAM allocated for buffering), the record is handled in the non-buffered mode: termination status is not given to the CPU until the record has been written entirely onto the tape, or an error occurs.

When writing a record that is not associated with the current command (last issued by the CPU), the controller performs an automatic error recovery (retry) procedure (space reverse, erase, then write forward) up to 10 times. Hence the necessity for a record to reside completely within the RAM when buffering. If the extended features switch on the interface/controller module is set, the extra (fifth) characteristics data word can specify the number of retries (from 0 up to 15) and can specify that a long gap should not be generated on an automatic retry (the erase function is eliminated from the recovery sequence).

During the write buffering mode of operation, the controller reads a block of data into its RAM from CPU memory, then responds to the CPU with a normal successful completion status. As far as the CPU software is concerned, then, the record was written on tape successfully. The controller must therefore take all the steps possible to eventually write that record onto the tape. Hence the need for automatic retries. Write buffering is a more complex operation than read buffering because of these retries. Furthermore, should the worst occur and the controller cannot write a buffered record, the CPU program will not know exactly which record failed to be written (the program could conceivably believe that a record was written properly when in fact it was not). For this reason, a tape position lost error termination is given for the next tape motion command issued by the CPU if a buffered record cannot be successfully written. In addition, if a buffered record is successfully written after retries, the CPU has no way of logging the fact that some trouble was encountered.

Because of the potential difficulties previously described, the controller implements an adaptive buffering algorithm. In this algorithm, the first write data command following any type of command other than a write next or write file mark is handled in a non-buffered mode: termination status is not returned to the CPU until the actual "write to tape" operation is complete. If the record was written without error, then subsequent write data commands cause buffering of the data. If an error occurred on this first record, the CPU can take its normal error logging and recovery procedures. Buffering is not enabled again until a successful record is written without retries.

Assuming that the transport is write-enabled and ready for an operation, the following occurs when a write data command is issued by the CPU and buffering is enabled (but not currently activated by having just completed a successful write data or write tape mark).

1. When the write is received by the TSV05 subsystem, the controller issues a write command to the tape transport and begins transferring the associated data from CPU memory to RAM.
2. As soon as the first word appears in RAM, it is transferred to the FIFO.
3. The previously issued write command to the transport eventually begins emptying the FIFO and writing the data onto tape.
4. Meanwhile, the transfer from CPU memory to RAM continues as long as there is room in the RAM; the transfer from RAM to FIFO continues as long as there is room in the FIFO.
5. Since this is the first write, it is being handled in a non-buffered mode so the "memory to RAM" process is allowed to overwrite a RAM byte that has already been transferred to the FIFO. The RAM management algorithm has the capability of suspending transfers either into or out of the RAM so that bytes not already transferred to the FIFO do not get overwritten, and so that the FIFO receives only valid bytes. (The RAM is handled as a circular buffer.)
6. When the final byte of data associated with this command has been written onto the tape and the tape transport has negated DATA BUSY, the controller tests the status inputs from the transport bus and also its internal status (that is, FIFO overrun) for errors or exceptional conditions.
7. If an error occurred or EOT was seen, the controller terminates the operation by issuing the appropriate status message and does not enable itself for write buffering. The controller reverts to its idle state (before step 1) with buffering deactivated.
8. If the transfer completed without incident, a normal successful termination message is issued and the controller enables itself for buffering of future write commands.
9. If the next command is indeed a write data, operation proceeds as in steps 1 through 4 above. However, when all the required data has been transferred from CPU memory to RAM, and if the record fits entirely in RAM, and if no exceptional condition has yet occurred, the controller issues normal successful termination status to the CPU. As far as the CPU is concerned, the record has been written onto the tape, although this is not really the case.

10. The controller continues transferring data from RAM to FIFO until the record it is currently transferring has been completely written onto tape. If the transfer is successful, the record is purged from the RAM, freeing its space for another record from the CPU. In addition, if no incident has occurred with the transfer, the controller accepts another write data command from the CPU and begins transferring data into the RAM.

11. As long as no errors are encountered, another write command continues to be accepted, and the three previous steps repeated.

12. If an error occurs, the controller enters its retry algorithm to attempt to successfully write the current record (space reverse, possibly erase forward, and rewrite the record using data stored in RAM). Statistics are kept as to the number of retries completed. If, after the specified number of retries (10 is the default) the record cannot be successfully written, operation is aborted and an error message (tape position lost) is issued to the CPU (if possible) as follows.

    Tape position lost status is issued on the next motion type command received by the controller.

13. Assume an error occurs and the record can be successfully written within the retry constraints. If a write command was currently pending (termination status not yet issued to the CPU) when the recoverable error occurred, it is then allowed to complete in the normal unbuffered fashion (so the CPU can log any errors). If this record is successfully written, buffering is again enabled and waits for the next command at step 9. If the record required retries by the CPU, the controller then returns to its idle mode (before step 1), causing the next write command to be handled in the unbuffered mode.

14. If, during the normal sequence of processing sequential write commands, buffering the records, and writing them to tape, a tape motion command other than write data is encountered, the RAM is purged (a stored record written to tape) before the new command is processed. Write Buffering is disabled until a successful write command. Therefore, after this new command is processed and its termination status issued, the tape is positioned as expected by the user, and all outstanding conditions reconciled.

15. Similarly, if a write next command specifying a record larger than 3.5K bytes is processed, this command is handled in the unbuffered fashion, but allows buffering to be attempted if the very next command is write next.

NOTE

Initialization (Bus INIT or a write into TSSR) should be avoided since it purges the RAM and current status. When this is done, it is possible to lose a record that the user might assume was properly written.


APPENDIX A

APPENDIX A
SPECIFICATIONS

This appendix contains specifications for the following TSV05 components:

- TSV05 tape transport (Table A-1).
- TSV05 interface/controller module (M7196) (Table A-2).
- TSV05-S interface/controller module (M7206-PA) (Table A-3).

A.1 MECHANICAL AND ELECTRICAL SPECIFICATIONS

Tables A-1, A-2, and A-3 contain the mechanical and electrical characteristics for the TSV05 components.

Table A-1 TSV05 Tape Transport Specifications

Tape Characteristics	
Type:	Mylar™ base, iron-oxide coated
Length:	731 m (2400 ft) maximum
Width:	13 mm (0.5 in)
Thickness:	3 mil (industry compatible)
Reel Diameter:	267 mm (10.5 in) - 2400 ft length 216 mm (8.5 in) - 1200 ft length 178 mm (7.0 in) - 600 ft length
Capacity/Tape Reel:	46 million bytes (10.5 in reel, unformatted)
Tape Motion	
Handling:	Bidirectional reel-to-reel, with compliance arm
Tape Tension:	212.6 g (7.5 oz) nominal

Mylar™ is a trademark of DuPont de Nemours & Co., Inc.

Table A-1 TSV05 Tape Transport Specificatio s (Cont)

Tape Motion (Cont)

Read/Write Speed:	64 cm/sec (25 in/sec) (using TS11 software)
	64 or 254 cm/sec (25 or 100 in/sec) (program selectable using special software)
Rewind Speed:	330 to 457 cm/sec (130 to 180 in/sec) (nominal), depending on reel size
	457 cm/sec (180 in/sec) (average), using 26.7 cm (10.5 in) reel

Rewind Time:

Reel Size	Minutes (maximum)
178 mm (7.0 in)	0.9
216 mm (8.5 in)	1.6
267 mm (10.5 in)	2.8

Auto Loading

Reliability:	An average of 96% of attempted loads will be successful with automatic retries, assuming a properly maintained transport and tape library exists
Retries:	Three automatically provided
Times:	30 seconds typical with no retry
	30 seconds maximum for each additional retry

Unloading

Time:	15 seconds maximum with tape located at Beginning Of Tape (BOT)

Tape Speed Variation

Long Term:	± 1% of nominal
Instantaneous:	± 4% of long term

Data Access Times

	64 cm/sec (25 in/sec)	254 cm/sec (100 in/sec)
Tape at Rest:	40 ms	260 ms
Worst Case:	140 ms	1040 ms
Data Transfer Rate:	40K bytes/seconds at 64 cm/sec (25 in/sec)	
	60K bytes/seconds at 254 cm/sec (100 in/sec)	

Table A-1 TSV05 Tape Transport Specifications (Cont)

Data Organization

Number of Tracks:	Nine (eight data; one parity)	
Recording Density:	1600 bits/in (nonselectable)	
Interrecord Gap:	1.3 cm (0.5 in) minimum, 1.65 cm (0.65 in) typical at 64 cm/s (25 in/sec)	
Recording Method:	Phase encoded (PE)	
Error Rates:	Recoverable write:	One error in 108 bits transferred
	Recoverable read:	One error in 109 bits transferred
	Unrecoverable read:	One error in 1010 bits transferred

Q-bus Interface Characteristics

Address Space Required:	772520/772522	1st unit
	772524/772526	2nd unit
	772530/772532	3rd unit
	772534/772536	4th unit
*Vectors Required:	224	1st unit
	300	2nd unit
	310	3rd unit
	320	4th unit

Mechanical Characteristics

	Tape Transport Cabinet (TSV05-B)	**Tape Transport Rack (TSV05-A)**
Height:	1111.3 mm (43.75 in)	222.3 mm (8.75 in)
Width:	596.9 mm (23.50 in)	482.6 mm (19.00 in)
Depth:	838.2 mm (33.00 in)	616.0 mm (24.25 in)
Weight:	121 kg (265 lb)	36 kg (80 lb)
	Tape Transport Cabinet (TSV05-SE)	**Tape Transport Rack (TSV05-SA)**
Height:	1111.3 mm (43.75 in)	222.3 mm (8.75 in)
Width:	596.9 mm (23.50 in)	482.6 mm (19.00 in)
Depth:	838.2 mm (33.00 in)	616.0 mm (24.25 in)
Weight:	121 kg (265 lb)	36 kg (80 lb)

* Rank of 37 in the floating vector area starting at 300.

Table A-1 TSV05 Tape Transport Specifications (Cont)

Mechanical Characteristics (Cont)

	Tape Transport Cabinet (TSV05-SK) TBD
Height:	1111.3 mm (43.75 in)
Width:	596.9 mm (23.50 in)
Depth:	838.2 mm (33.00 in)
Weight:	121 kg (265 lb)

Electrical Requirements

	Tape Transport	**Cabinet Power Control**
Power Consumption:	220 W average 270 W maximum	16.5 W maximum

ac Voltage (+7% or -15%):

	Nominal	**Low Limit**	**High Limit**
TSV05-AA,-BA	120	102	128
TSV05-AB,-BB	240	204	256
TSV05-AC,-BC	100	85	107
TSV05-AD,-BD	220	187	235
TSV05-SA,-SE	120	102	128
TSV05-SB,-SF	240	204	256
TSV05-SC,-SH	100	85	107
TSV05-SD,-SJ	220	187	235

Frequency: ± 1 Hz

Nominal, Hz	**Low Limit, Hz**	**High Limit, Hz**
50 or 60	49	61

Frequency Rate of Change: 1.5 Hz/s maximum

Table A-2 TSV05 Interface/Controller Module (M7196) Specifications

Mechanical Specifications	
Length:	From contact fingers to handles: 228.6 mm (9.0 in)
Width:	266.7 mm (10.5 in)
Thickness:	12.7 mm (0.5 in)
Weight:	0.51 kg (1.13 lb)
Formatter Bus Cables	
Connectors:	50-pin, right-angle, flat cable header connectors at controller end; industry standard formatter connectors at tape transport end.
Length:	2.4 m (8.0 ft)
Electrical Specifications	
Power Consumption:	5 Vdc ± 5% at 6.5 A (maximum)
Q-bus Loading:	dc: One load ac: Three loads (maximum)

Table A-3 TSV05-S Interface/Controller Module (M7206-PA) Specifications

Mechanical Specifications	
Length:	From contact fingers to handles: 228.6 mm (9.0 in)
Width:	266.7 mm (10.5 in)
Thickness:	12.7 mm (0.5 in)
Weight:	0.51 kg (1.13 lb)
Formatter Bus Cables	
Connectors:	50-pin, right-angle, round cable header connectors at controller end; industry standard formatter connectors at tape transport end.
Length:	2.4 m (8.0 ft)
Electrical Specifications	
Power Consumption:	5 Vdc ± 5% at 6.5 A (maximum)
Q-bus Loading:	dc: One load ac: Three loads (maximum)

A.2 ENVIRONMENTAL CONSIDERATIONS

Specifications presented in this paragraph apply to the TSV05-BA, -BB, -BC, -BD, -SE, -SF, -SH, and -SJ models. Specifications for the TSV05-AA, -AB, -AC, -AD, -SA, -SB, -SC, -SD, -SK, -SL, -SM, and -SN may be affected by the cabinetry in which it is installed.

A.2.1 Operating Conditions

The TSV05-BA and -SE series subsystems are designed to operate under the following conditions.

Temperature

15°C to 32°C (59°F to 90°F)

Temperature Shock: 20°C (68°F) change/hr maximum

Relative Humidity: 20% to 80% noncondensing

Altitude: Sea level to 3 km (10,000 ft)

Vibration

Frequency Range:	5 to 500 Hz
Peak Acceleration:	0.25 g, 22 to 500 Hz, 0.01 in DA5-22 Hz
Application:	Each of three orthogonal axes

Shock

+10 g peak, 1/2 sine, 10 ms

Pollutants

Atmospheric Particulates:	60 mg/1000 cu ft air by weight of particle (5 micron diameter)

Electrostatic Discharge

10 kV through 100 ohms from 350 pF

A.2.2 Nonoperating Conditions

The TSV05-B and -SE series subsystem are designed to withstand the following conditions during nonoperating periods (for example, shipping).

Temperature -40°C to 66°C Relative Humidity 95% maximum, noncondensing

Altitude Sea level to 15 km (49,000 ft)

NOTE

Magtape media typically has more restricting nonoperating environmental considerations.

Vibration (in shipping container)

Frequency Range:	10 to 300 Hz
Peak Acceleration:	1.4 g rms vertical axis 0.68 g rms longitudinal and lateral axis 200 Hz maximum

Shock (in shipping container)

Peak Acceleration:	20 g
Duration:	30 ± 10 ms
Waveshape:	1/2 sine

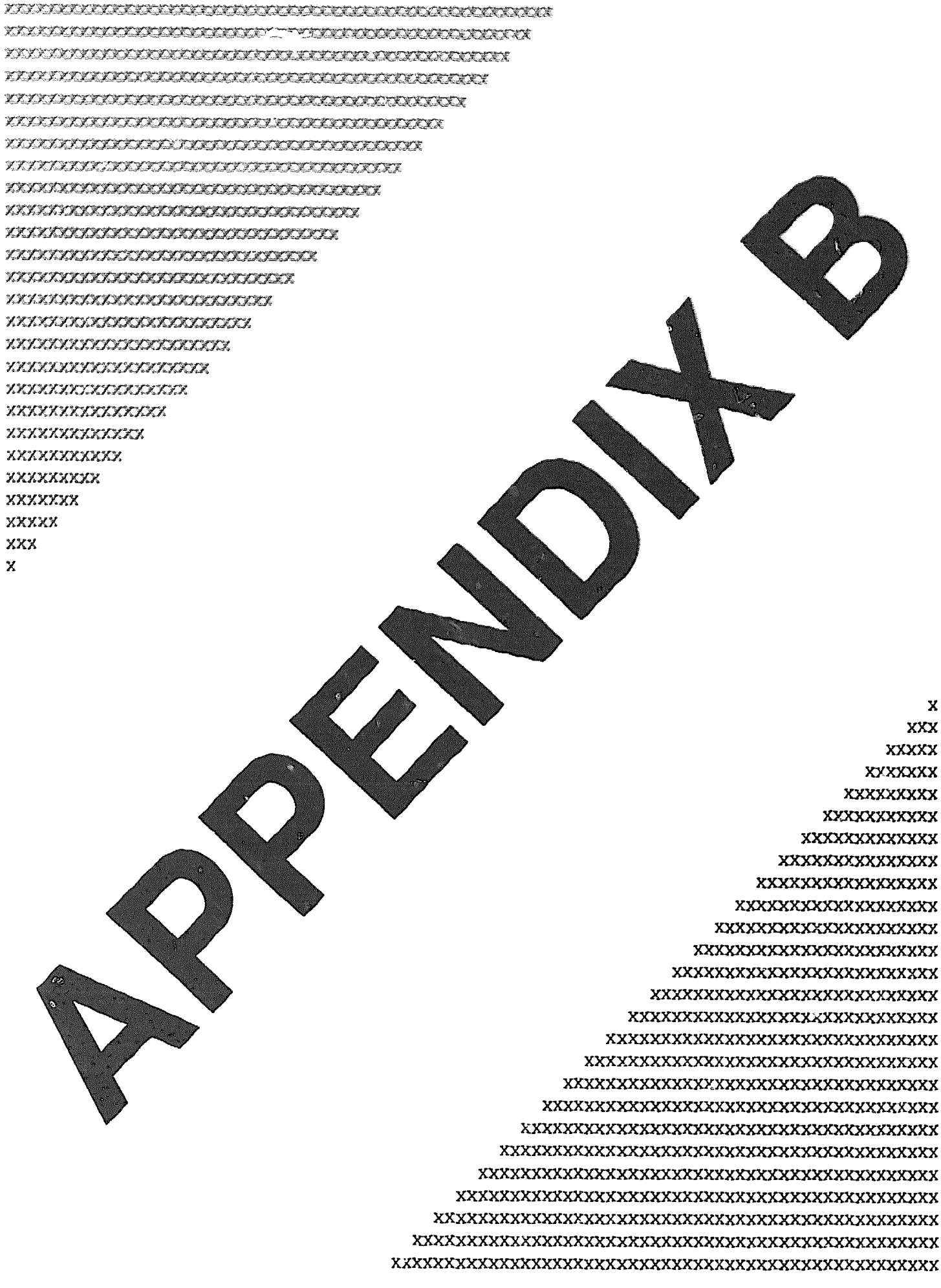
A.2.3 Emissions

During normal operation, the TSV05-B subsystem temperature is designed to emit no more than the following levels.

Heat	1100 Btu/hr maximum
Acoustic Noise Standby (blower on):	57 dB A scale
Operating Conditions:	60 dB A scale

Electromagnetic Interference (EMI)

The TSV05-B and -D comply with FCC Part 15, Subpart J, Class A, and is designed to comply with VDE 0871 B requirements.


APPENDIX B

APPENDIX B
MANUAL LOADING

If the autoloading routine does not successfully load the tape, the manual loading procedure may be used. Refer to Figure B-1 and proceed as follows.

1. Switch off the tape transport power.
2. Raise the cabinet top cover by grasping the handle on the top cover and lifting. When the top cover is raised far enough, the support arm latches to keep the cover up.
3. Raise the top cover of the tape transport unit by reaching in through the front panel door and pushing upward on the front of the top cover.
4. Ensure that there are no foreign objects in the tape path.
5. Place the reel of tape on the supply hub. Ensure that it is evenly seated on the hub, and then close the front door.
6. Thread the tape along the tape path as shown in Figure B-2. Carefully move the tachometer assembly away from the takeup hub and wrap the tape clockwise around the hub. Wrap the tape just short of one complete turn. Note that the tape should not overwind itself at this point. That is, there should be a short section of the takeup hub that has no tape on it yet.
7. Gently move the tachometer assembly back against the hub. The tape should pass beneath the tachometer assembly.
8. Check that the tape is seated correctly on the guides and threaded properly over the head assembly. Remove any excess slack by gently turning the supply reel counterclockwise.
9. Turn the takeup hub clockwise to wrap two additional turns of tape on the hub. Ensure that the tape does not ride up and extend over the top surface of the hub.
10. Close the top covers of the tape transport and the cabinet.
11. Switch on the tape transport power.
12. Press ENTER. After ENTER is pressed, press LOAD. When the LOAD indicator stops blinking, the tape is loaded and ready to be switched on-line.

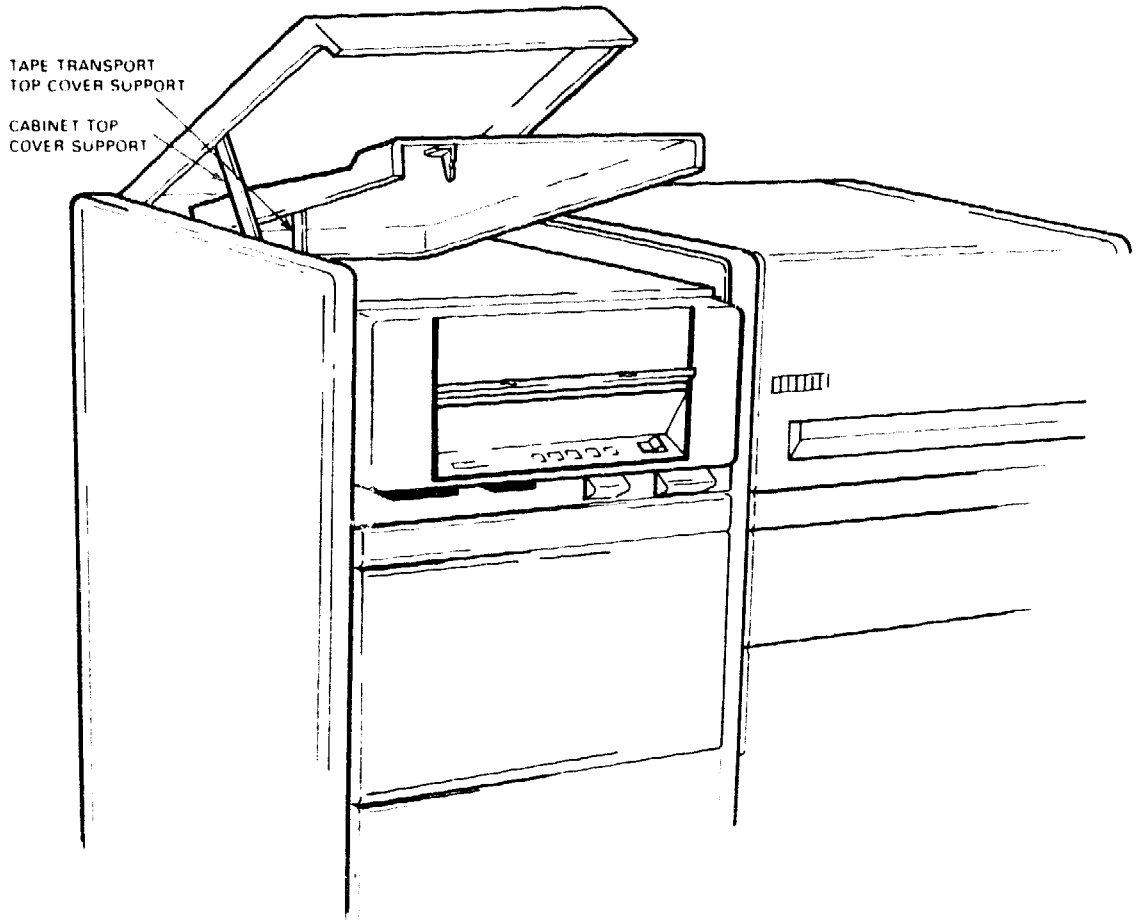


Figure B-1 Accessing the Tape Path Area

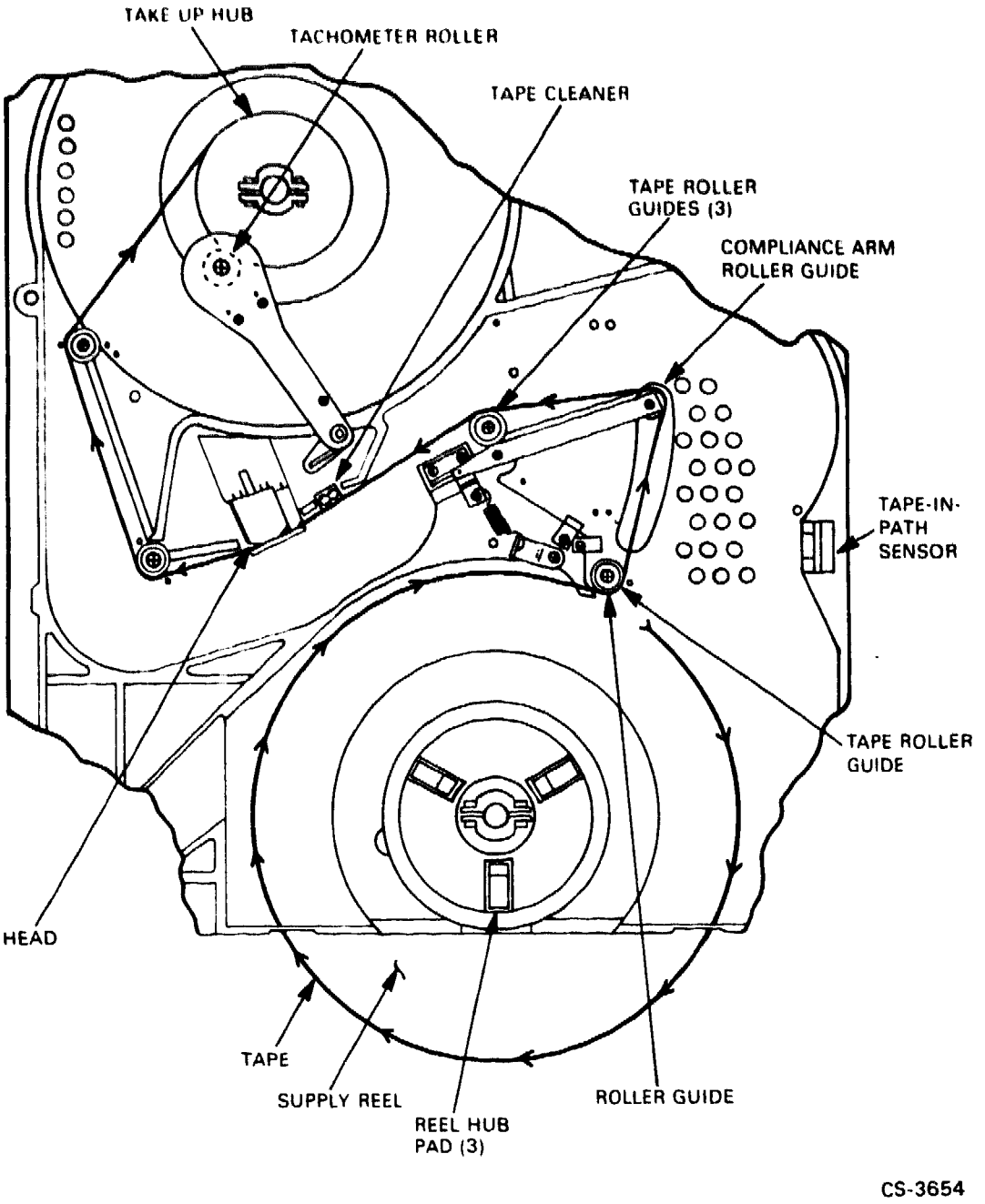
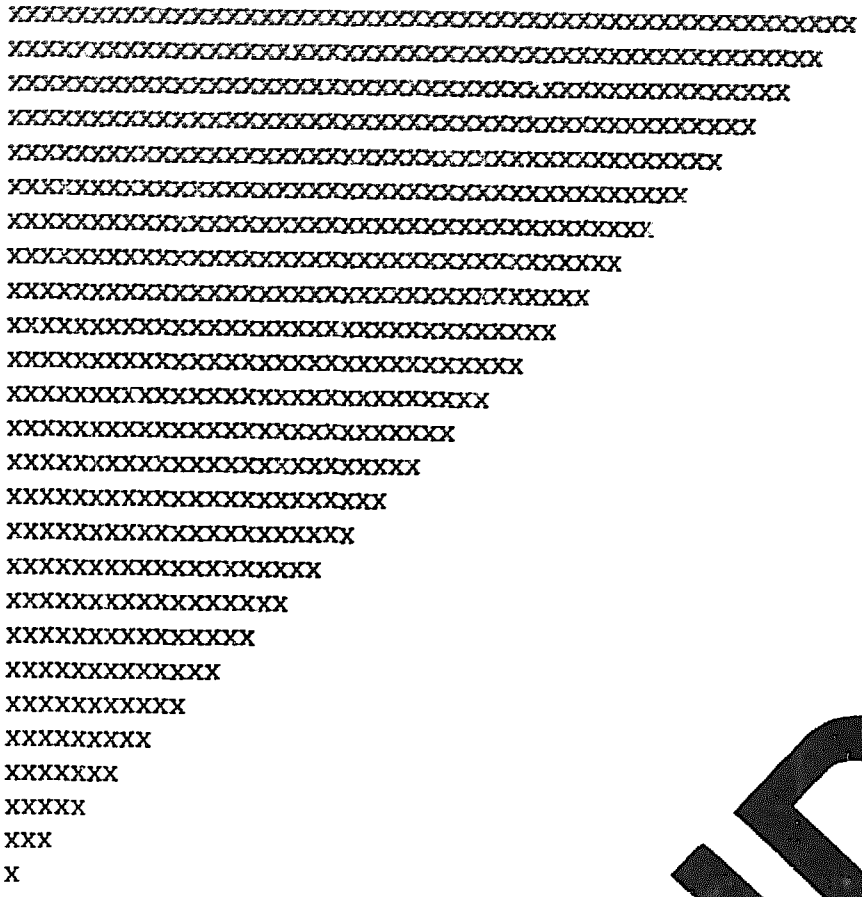
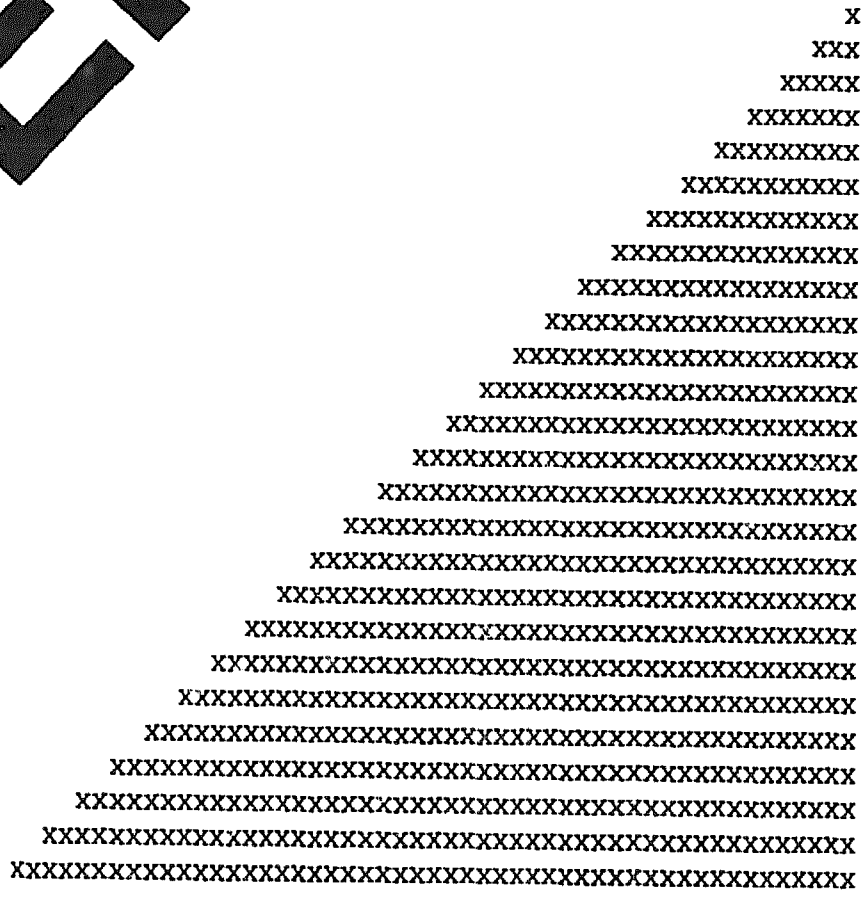


Figure B-2 Tape Threading Path



APPENDIX C



APPENDIX C
RACK MOUNTING PROCEDURES

C.1 TSV05-A AND -SA

The TSV05-A and -SA series models are designed to be mounted in an Electronic Industries Association (EIA), standard 19-inch wide equipment rack, with RETMA standard hole spacing (5/8-inch, 5/8-inch, 1/2-inch). The TSV05-A [-SA] includes mounting slides designed for 5/8-inch hole spacing. Additionally, it is shipped with a locking shipping bracket, and hardware designed to fit H9642 cabinetry. The recommended procedure for rack mounting the TSV05-A [-SA] series are as follows.

C.1.1 Cabinet Preparation

There are no additional cabinet preparations for the TSV05-A and -SA series models.

C.1.2 TS05 Installation

1. Unpack and inspect the tape transport unit (it is shipped in the largest of the cartons). Unpack, inspect, and inventory the contents of the smaller cartons as described in Chapter 2, Section 2.2.4.
2. Remove the sliding parts of the tape transport chassis mounting slides by extending them to the rear of the tape transport. This requires disengaging the safety latches.

CAUTION

The left and right mounting slides are not interchangeable. The safety latches do not engage properly if the slides are reversed.

3. Refer to Figure C-1 and to the equipment rack, and determine the desired rack elevation for mounting the slides. Items to consider when selecting the mounting location include:
   a. Power cord length is 2.4 meters (8.0 feet).
   b. Interface cable length is 2.4 meters (8.0 feet).
   c. The equipment rack must be stable when the TSV05-A [-SA] is fully extended on the slides for servicing.
   d. The TSV05-A [-SA] should not be mounted close to high heat sources.

e. A 1.75-inch trim strip can be purchased from DIGITAL (part number H9544-DA). This trim strip can be added to the tape transport to obtain a combined height of 10.5 inches. This vertical dimension is standard for many racks.

4. Using four 10-32 x 3/8 inch bolts for each slide, secure the slides to the equipment rack at both the front and rear mounting holes (Figure C-2). Note that the slides mount to the rear of the front cabinet rail.

5. Fully extend the center sections of the slides now secured to the rack. When a slide is fully extended, the latch clicks as it locks the slide in its extended position.

6. The tape transport unit should now be slid into the rack mounting slides.

WARNING

Use sufficient personnel for sliding the tape transport unit into the rack.

With one person on each side, lift the transport and insert the slides on the transport into the slides mounted in the rack. Press the spring latches located on the transport slides, and push the transport into the rack until the latches lock into place (this is approximately 8 cm (3 in)). Press the spring latches a second time, and push the transport fully into the rack. A gap of approximately 1.5 to 1.8 cm (0.6 to 0.7 in) is normally present between the rear of the transport front bezel and the mounting rail.

7. Locate the shipping bracket packed with the TSV05-A [-SA]. The bracket is designed for use on DIGITAL H9642 series cabinetry, and secures the tape transport unit to the rear cabinet rail (Figure C-1). Install the shipping bracket to protect the equipment during shipment. It is recommended that similar protection be provided by other types of cabinetry.

8. Connect the tape transport power line to the cabinet power receptacle. (Refer to Chapter 2, Section 2.1.2, for power requirements.) For the most reliable operation, the use of filtered ac line voltage is recommended. Make certain there is sufficient power cord slack for the TS05 tape transport to be placed in the service access position without damaging the power cord.

9. Remove the shipping foam from the tape transport as described in Chapter 2, Section 2.3.4.

10. Continue the checkout and installation procedures as described in Chapter 2, Sections 2.4 through 2.7.

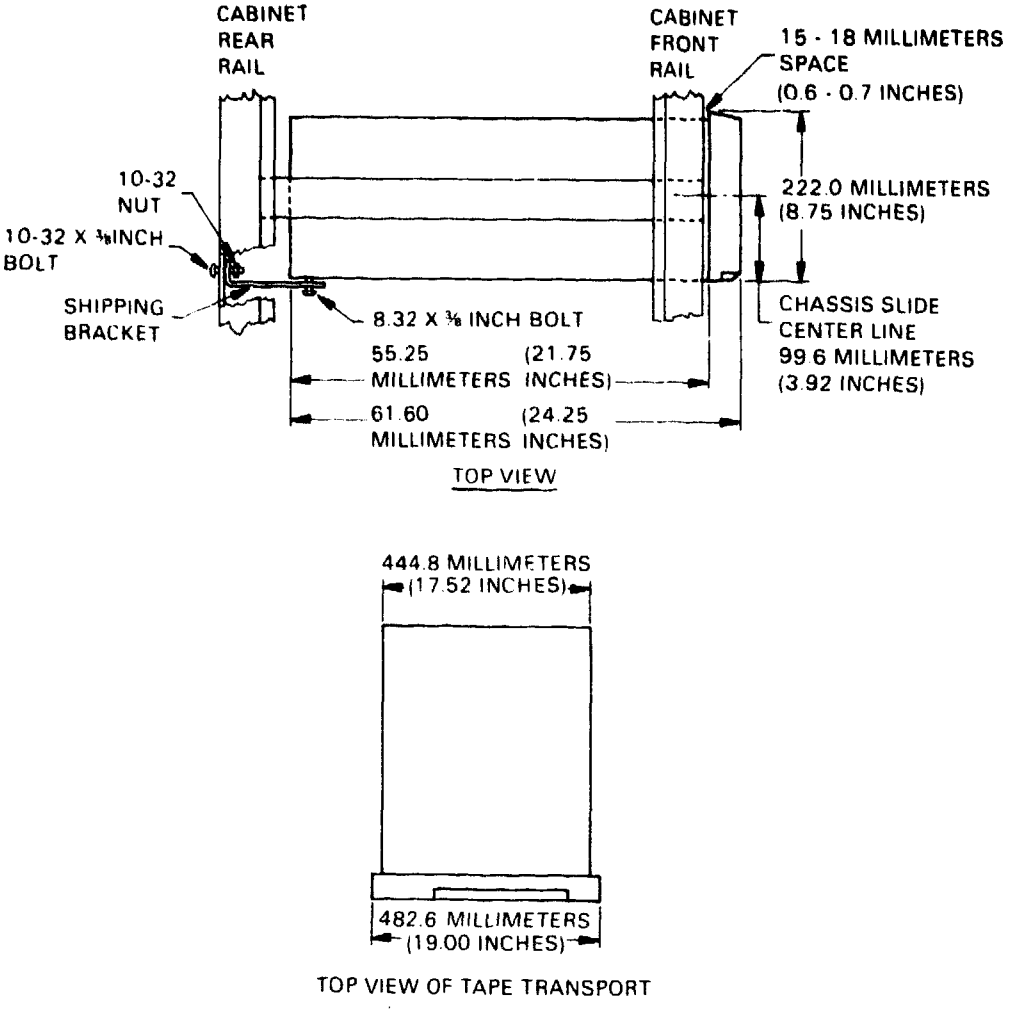


Figure C-1 TSV05-A [-SA] Mounting Requirements

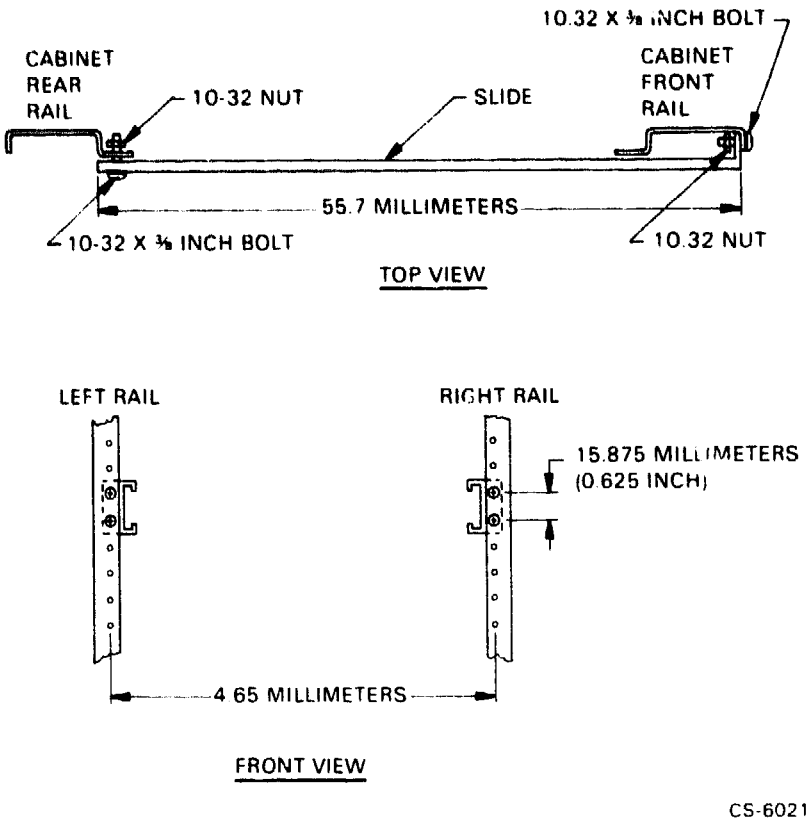


Figure C-2 Chassis Slide Mounting

C.2 TSV05-SK

The TSV05-SK, -SL, -SM, and -SN models are designed to be mounted in an H9644 cabinet. The H9644 cabinet has fixed mounting rails rather than slides. After installing the new top cover and setting the TS05 tape transport on the mounting rails, the TS05 tape transport will be placed in the maintenance position and bolted to the cabinet. Use the following procedures to install the TSV05-SK models.

C.2.1 Cabinet Preparation

This procedure assumes that you have a H9644-Ax cabinet with blank front panel, rear panel, and fixed top cover with attached rear canopy still installed. The front panel, fixed top cover, and the two piece rear canopy will be removed, and will not be replaced. The side panels and rear panel will be reinstalled as part of the TSV05 installation.

1. Open or remove the rear panel on the H9644-Ax cabinet.
2. Remove the blank front panel from the cabinet. Access the panel from the back of the cabinet and remove the four nuts, using a nutdriver.
3. Remove each side panel using the following procedure:
   a. Open the rear doors of the tape transport cabinet and computer cabinets. Typically, this requires inserting the hex key into the latch and turning it one-quarter turn counterclockwise (see Figure C-3).
   b. Remove the locking bracket located at the rear bottom, right-hand side (as viewed from the rear) of both cabinets. Each bracket is held by two bolts. Loosen but *do not remove* the bolts (see Figure C-4).
   c. Lift the side panel straight up and remove it from the cabinet. Disconnect the side panel ground wire from the cabinet frame.
4. Remove the top cover assembly and its mounting brackets using the following procedure:
   a. Remove two Phillips screws from either side of the cabinet.
   b. Remove two Phillips screws from the bottom of the rear canopy.
   c. Lift up the rear canopy to access the remaining two Phillips screws, holding the top cover assembly in place.
   d. Remove the two Phillips screws and lift the top cover assembly and the rear canopy away from the cabinet.
5. Carefully unpack the top cover assembly (70-16864-01).

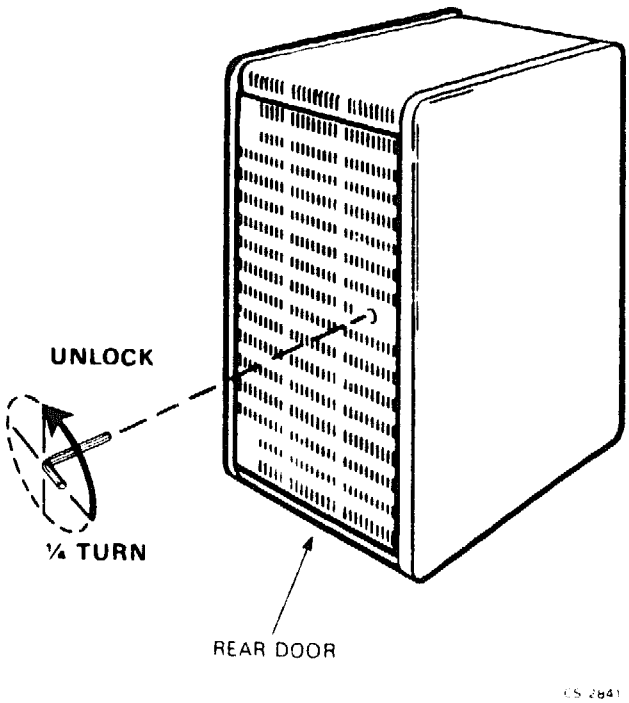


Figure C-3 Opening Cabinet Door

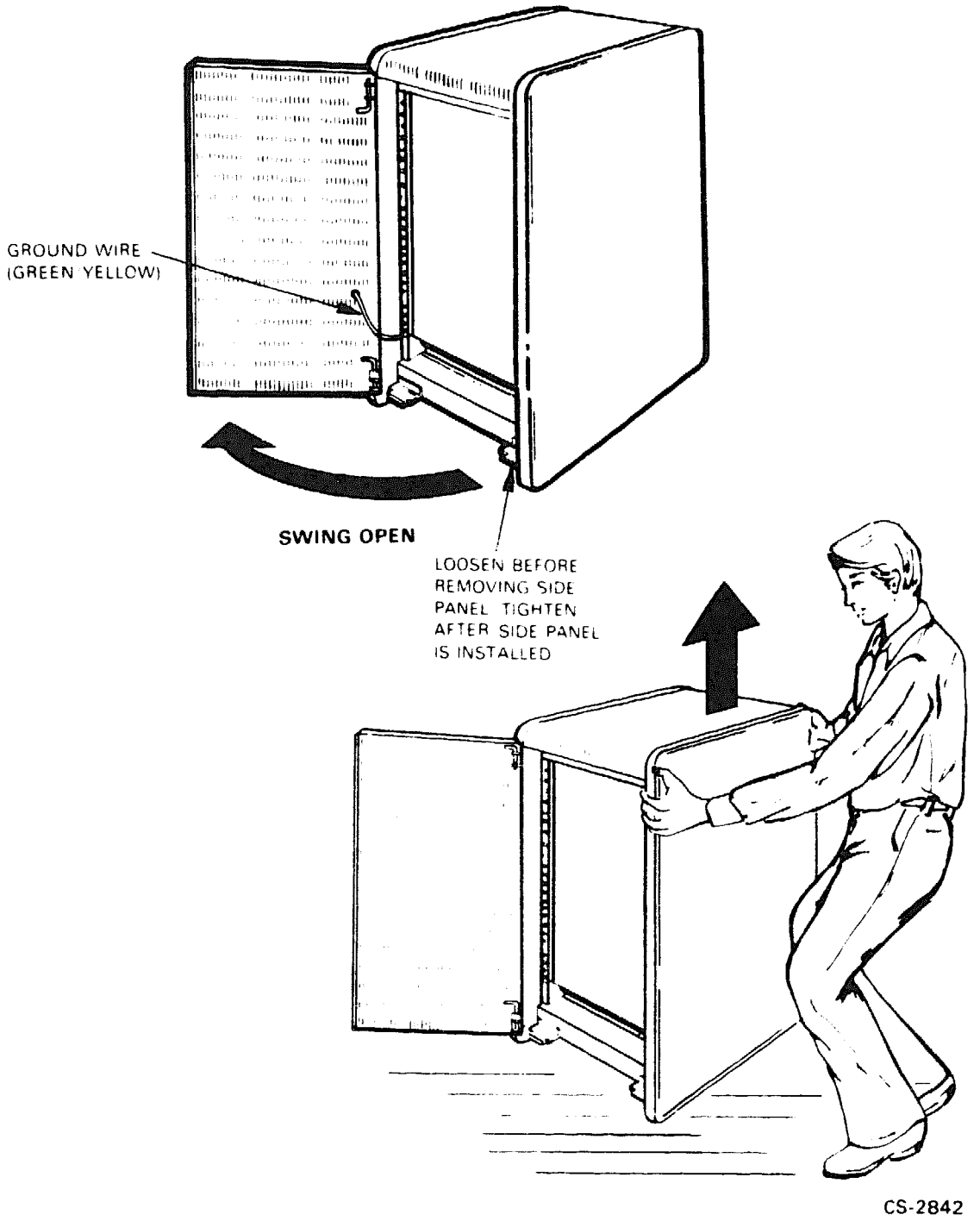


Figure C-4 Removing Side Panel

6. Mount the top cover assembly on the cabinet (Figure C-5). Extend the cabinet stabilizer leg located under the front of the cabinet.

7. Install the each of two side panels using the following procedure:

   a. Place the side panel against the tape transport cabinet. Connect the side panel ground strap to the tape transport cabinet.

   b. Position the side panel against the tape transport cabinet such that the slots align with the pins (Figure C-6). Hold the side panel a few inches above its mounted position until it is even with the front and rear of the cabinet. Slide the panel straight down such that the four pins engage the four slots.

8. Close or install the rear panel on the H9644-Ax cabinet.

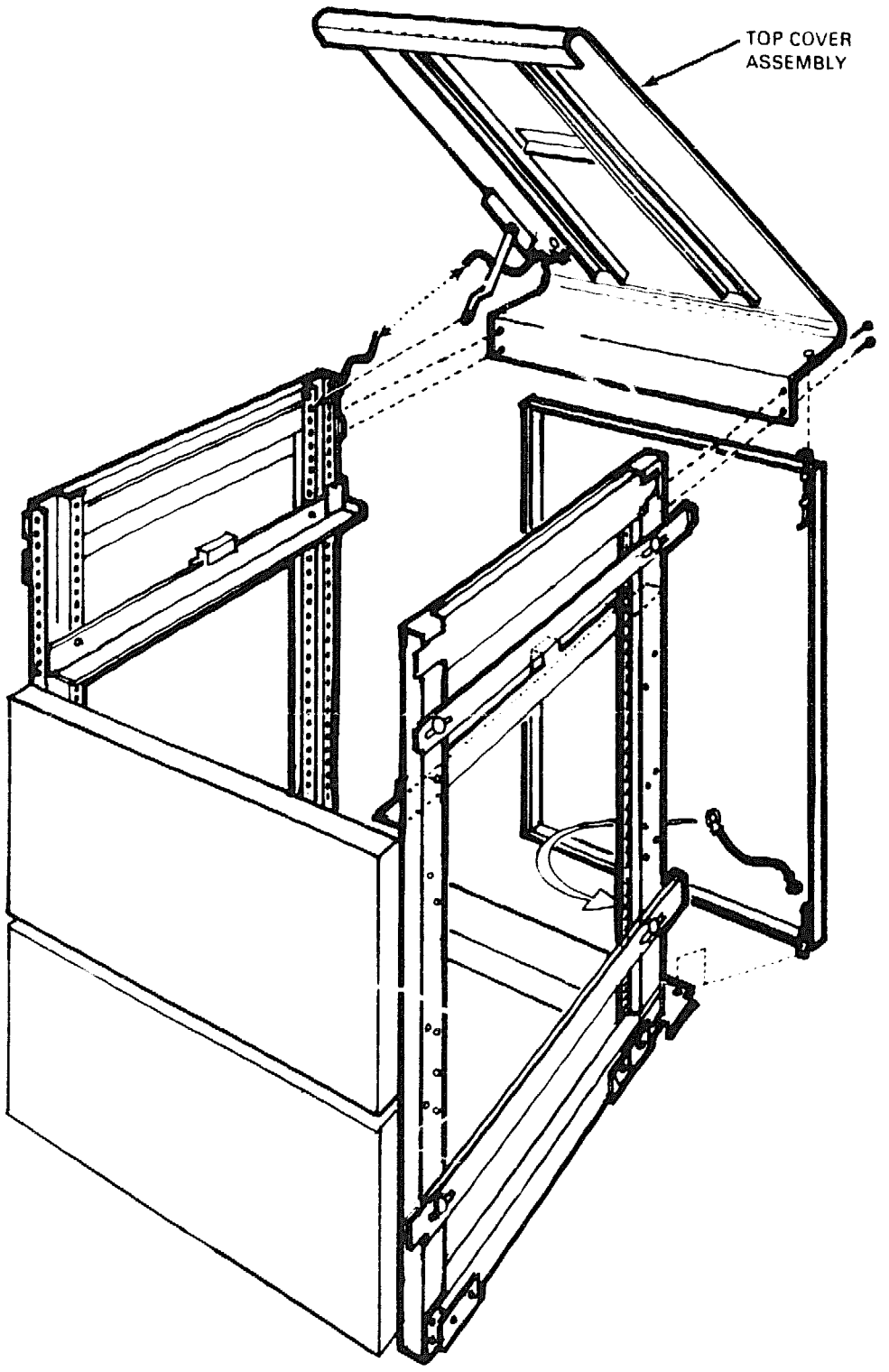


Figure C-5 Cabinet Preparation

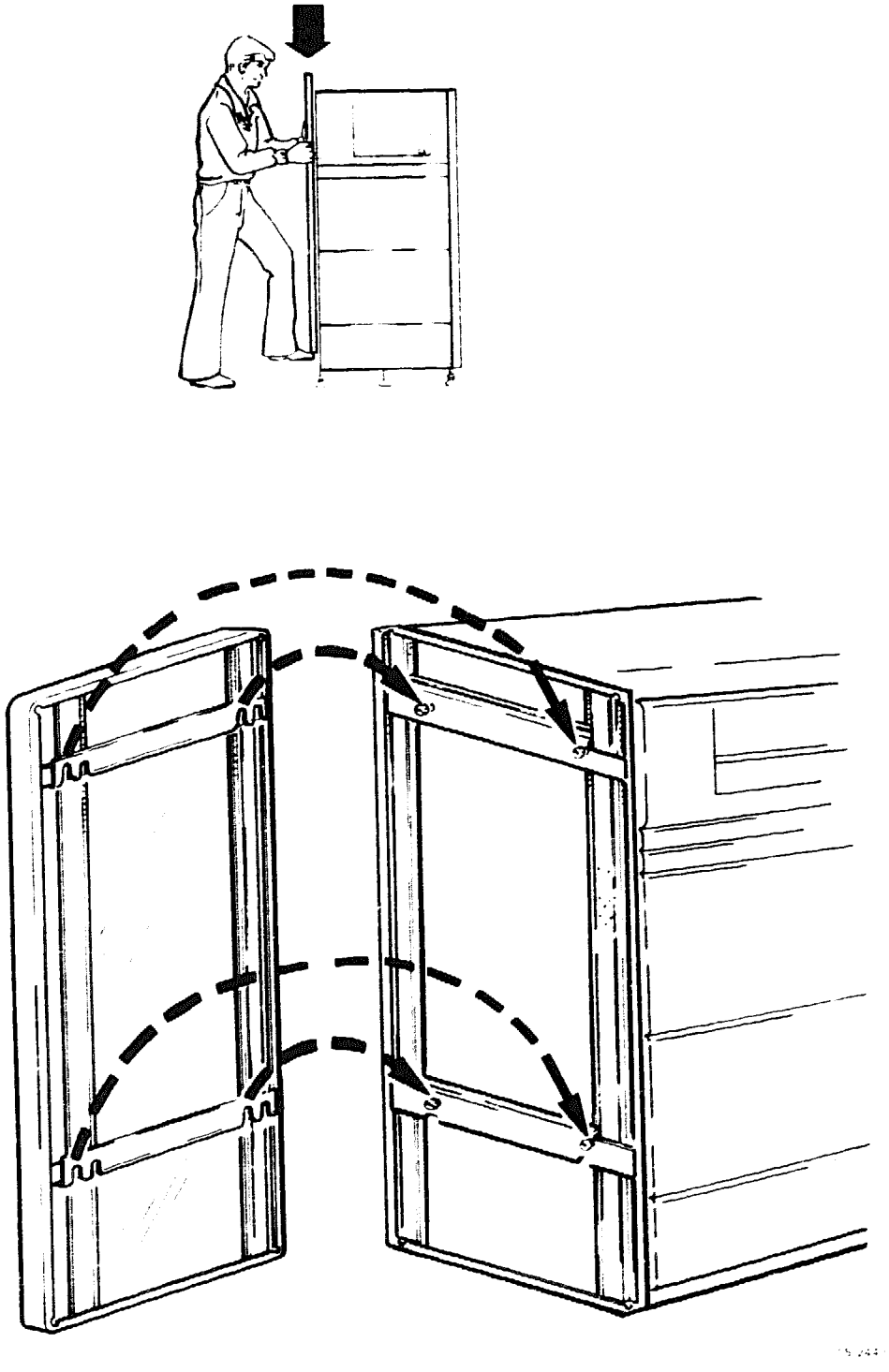


Figure C-6 Installing a Side Panel

C.2.2 TS05 Installation

1. Unpack the TS05 tape transport as described in Chapter 2, Section 2.2, of this manual.

WARNING

Use sufficient personnel for sliding the tape transport unit into the rack.

2. Using two people, carefully lift the TS05 up, and place the bottom of the TS05 onto the metal fixed runner/slides in the top of the cabinet
3. While still holding up the transport, carefully slide the transport into the cabinet until the front panel of the TS05 is approximately even with the front of the cabinet.
4. Raise the top cover assembly until it stops.
5. Raise the top lid on the transport and, with a slotted screwdriver, unlock the transport from the base.
6. Carefully lift the front of the transport up until it stops (Figure C-7). Gently let the transport down. It should stop in the raised position.
7. Install the safety pin

WARNING

Ensure that the safety pin is installed. Failure to do so can result in personnel injury if the TS05 should drop back down.

8. Gently move the transport slightly to the rear or the front of the cabinet, until the threaded holes in the runner/slides line up with the clearance holes on the inside of the transport.
9. Install one each #10 screw and lockwasher in each of the four mounting holes in the transport. These screws and lock washers are mounted from the inside of the drive.
10. Install the TSV05 cables as described in Chapter 2, Section 2.7, of this manual.

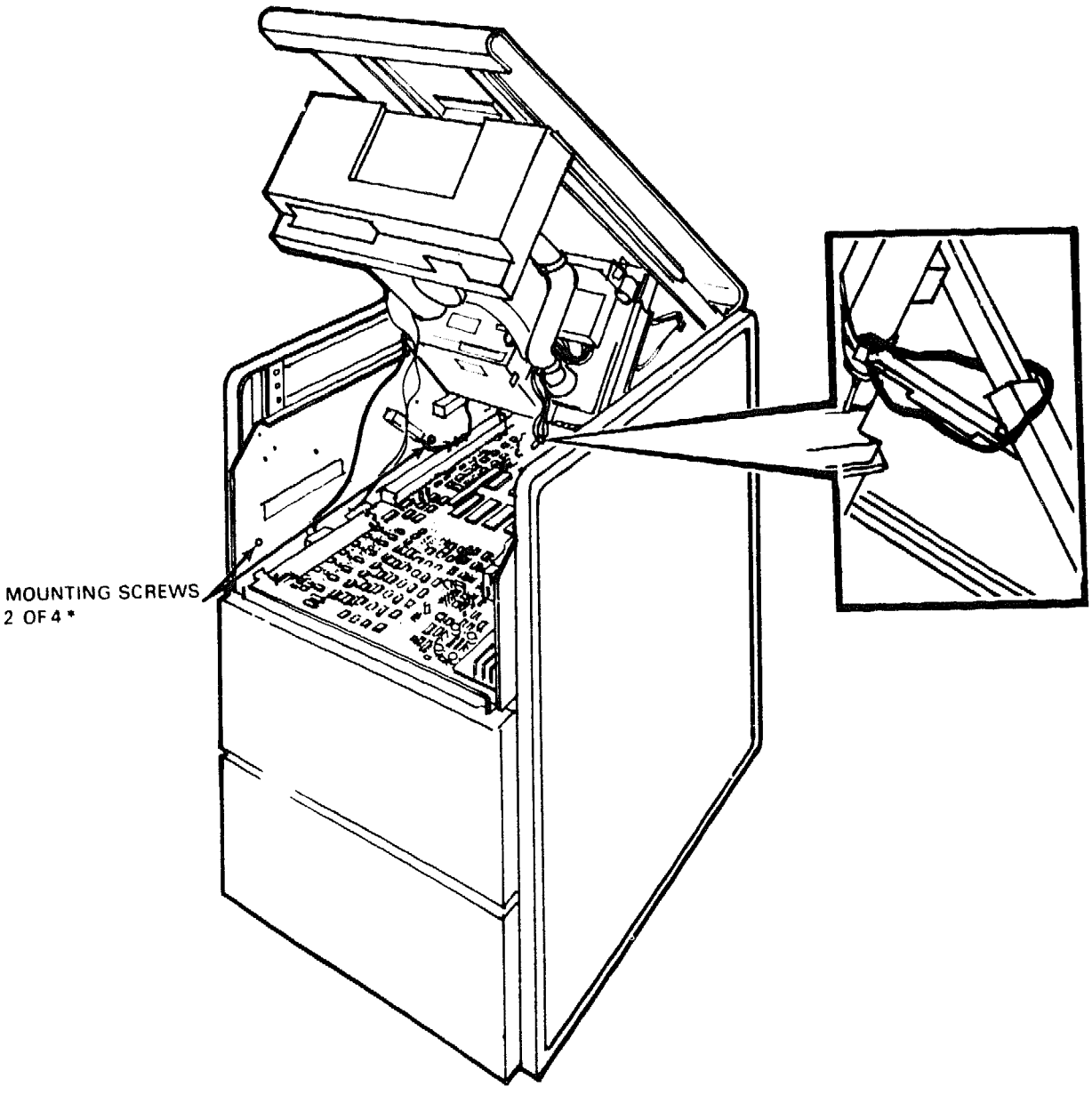


Figure C-7 TS05 Installation

C.3 TSV05-Z

C.3.1 Cabinet Preparation

This procedure assumes that you have a deep cabinet with a blank front panel, rear panel, and fixed top cover with attached rear canopy still installed. The front panel, fixed top cover, and two piece rear canopy will be removed, and will not be replaced. The side panels and rear panel will be reinstalled as part of the TSV05 installation.

1. Open or remove the rear panel on the cabinet.
2. Remove the blank front panel from the cabinet. Access the panel from the back of the cabinet and remove the four nuts, using a nutdriver.
3. Remove each side panel using the following procedure:
   a. Open the rear doors of the tape transport cabinet and computer cabinets. Typically, this requires inserting the hex key into the latch and turning it one-quarter turn counterclockwise (see Figure C-8).
   b. Remove the locking bracket located at the rear bottom, right-hand side (as viewed from the rear) of both cabinets. Each bracket is held by two bolts. Loosen but *do not remove* the bolts (see Figure C-9).
   c. Lift the side panel straight up and remove it from the cabinet. Disconnect the side panel ground wire from the cabinet frame.
4. Remove the top cover assembly and its mounting brackets, using the following procedure:
   a. Remove two Phillips screws from either side of the cabinet.
   b. Remove two Phillips screws from the bottom of the rear canopy.
   c. Lift up the rear canopy to access the remaining two Phillips screws holding the top cover assembly in place.
   d. Remove the two Phillips screws and lift the top cover assembly and the rear canopy away from the cabinet.
5. Carefully unpack the top cover assembly (70-16864-01).

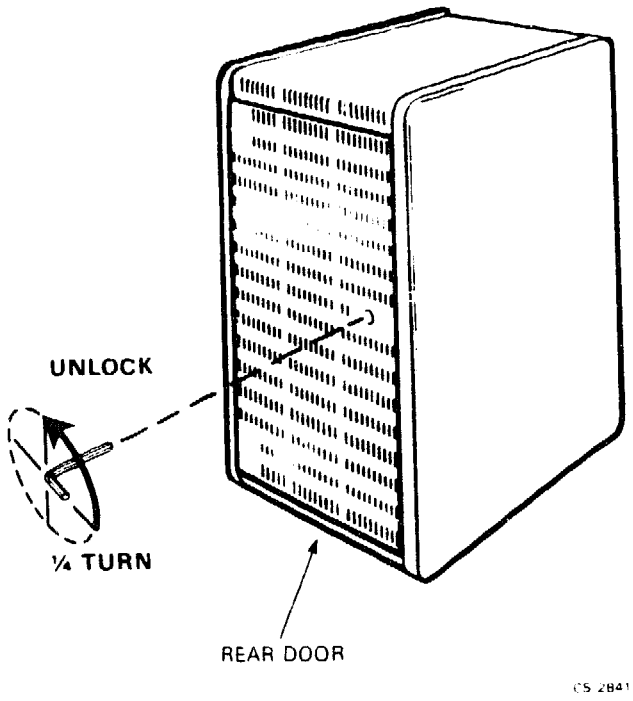


Figure C-8 Opening Cabinet Door

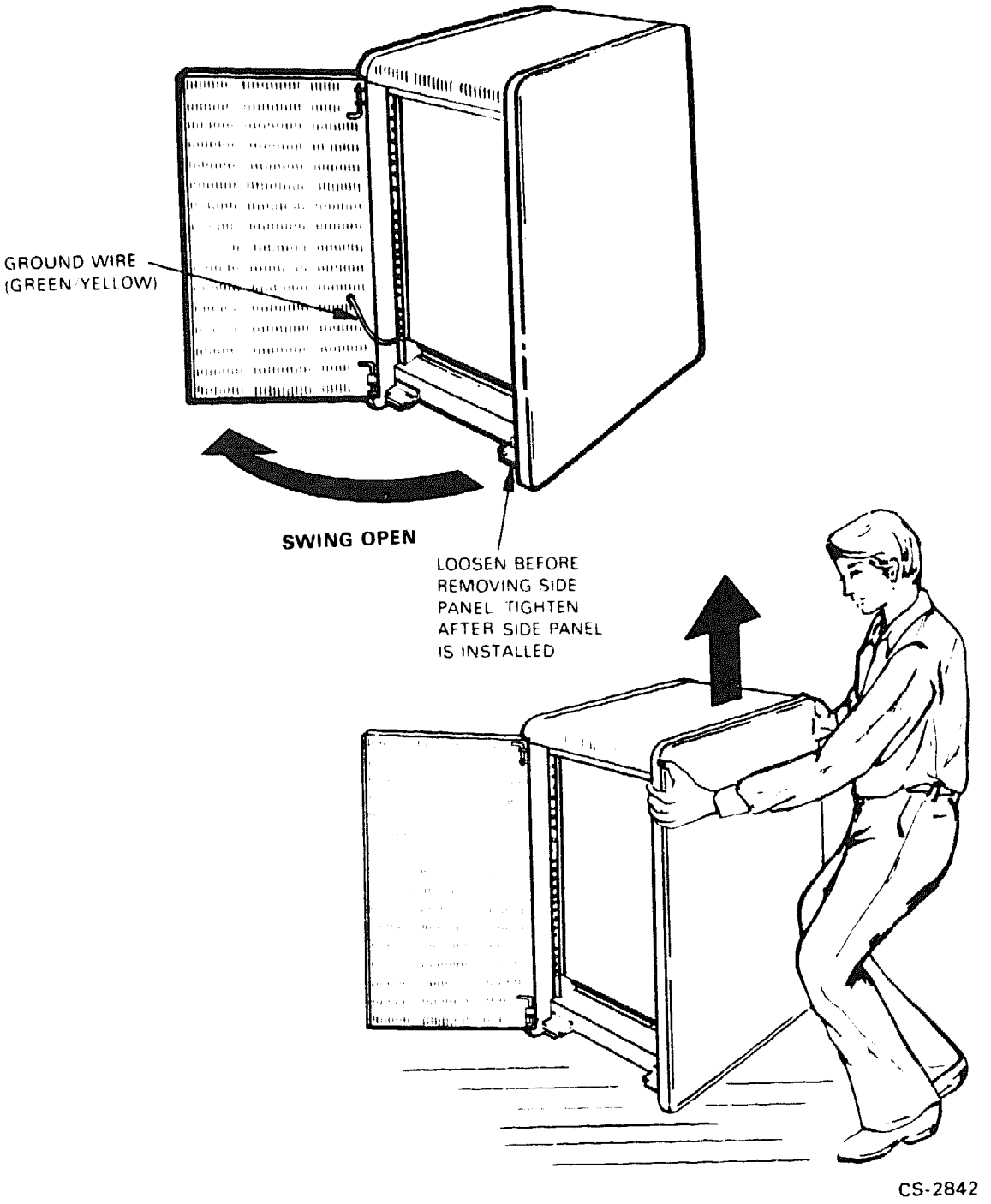


Figure C-9 Removing Side Panel

6. Mount the top cover assembly on the cabinet (Figure C-10). Extend the cabinet stabilizer leg located under the front of the cabinet.
7. Install the each of two side panels using the following procedure:
   a. Place the side panel against the tape transport cabinet. Connect the side panel ground strap to the tape transport cabinet.
   b. Position the side panel against the tape transport cabinet such that the slots align with the pins (Figure C-11). Hold the side panel a few inches above its mounted position until it is even with the front and rear of the cabinet. Slide the panel straight down such that the four pins engage the four slots.
8. Close or install the rear panel on the cabinet.

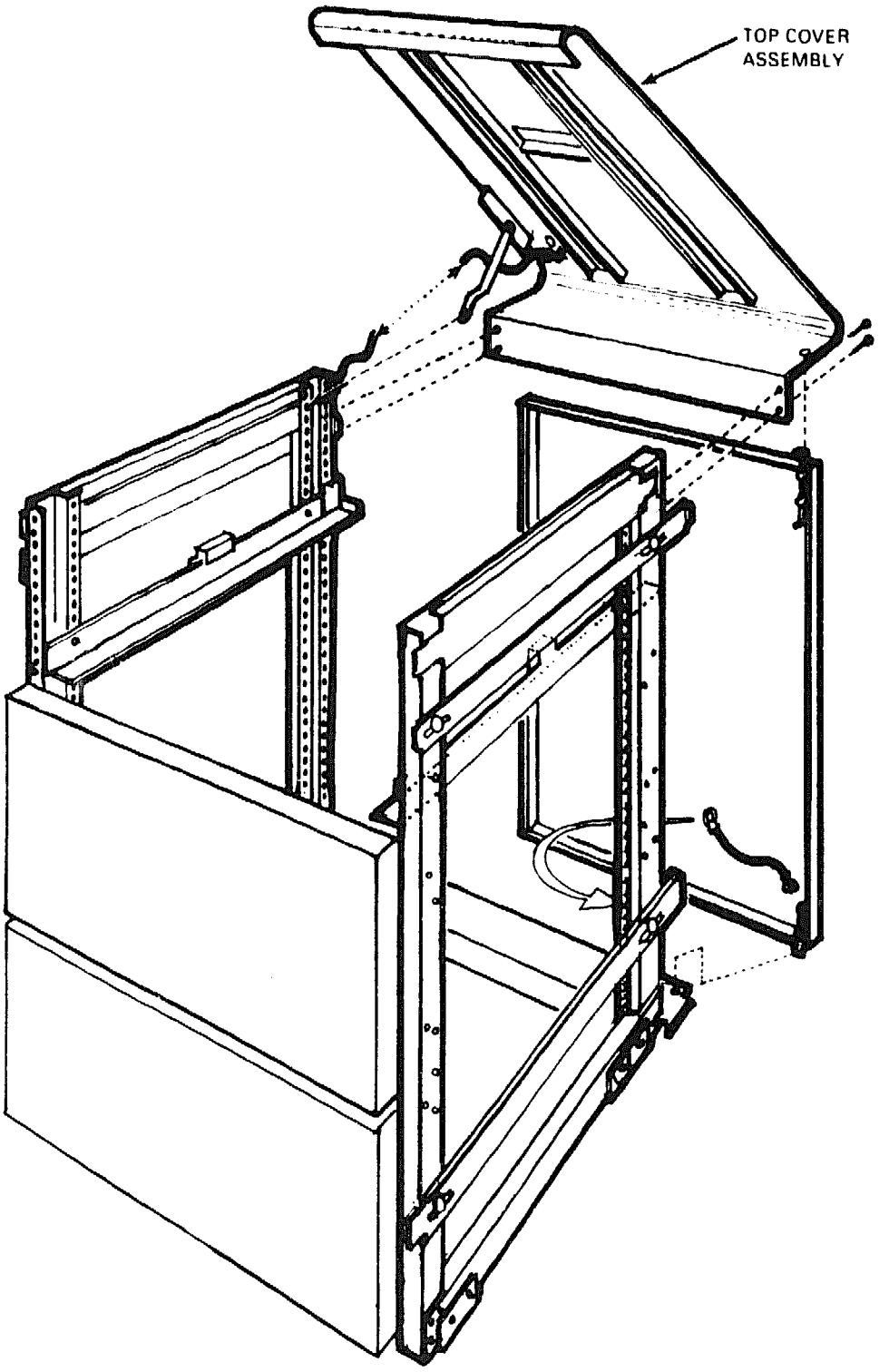


Figure C-10 Cabinet Preparation

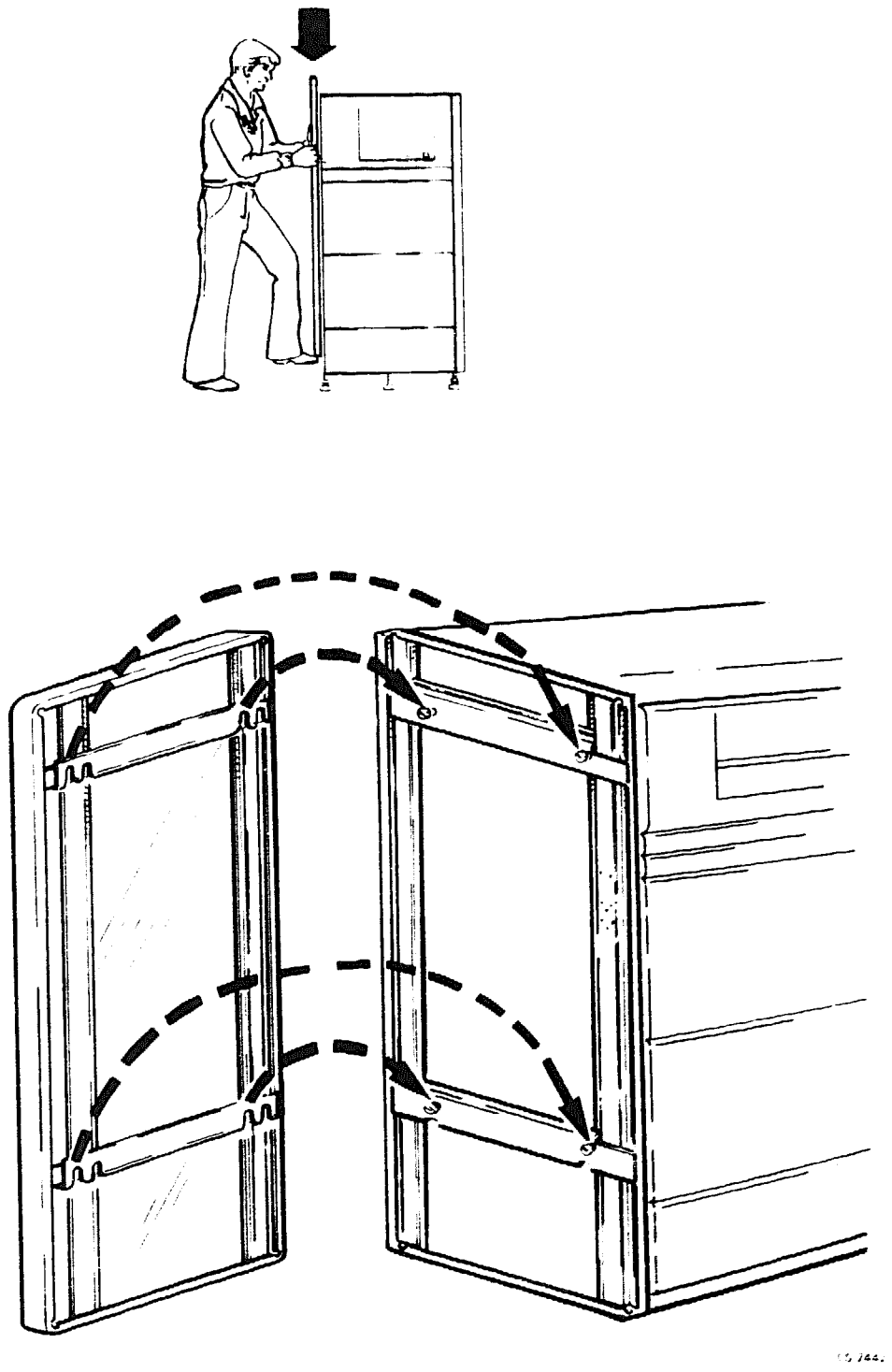


Figure C-11 Installing a Side Panel

C.3.2 TS05 Installation

1. Unpack and inspect the tape transport unit. It is shipped in the largest of the cartons. Unpack, inspect, and inventory the contents of the smaller cartons as described in Chapter 2, Section 2.2.4.

2. Remove the sliding parts of the tape transport chassis mounting slides by extending them to the rear of the tape transport. This requires disengaging the safety latches.

CAUTION

The left and right mounting slides are not interchangeable. The safety latches do not engage properly if the slides are reversed.

3. Refer to Figure C-12 and to the equipment rack, and determine the desired rack elevation for mounting the slides. Items to consider when selecting the mounting location include:

   a. Power cord length is 2.4 meters (8.0 feet).

   b. Interface cable length is 2.4 meters (8.0 feet).

   c. The equipment rack must be stable when the TSV05-Z is fully extended on the slides for servicing.

   d. The TSV05-Z should not be mounted close to high heat sources.

   e. A 1.75-inch trim strip can be purchased from DIGITAL (part number H9544-DA). This trim strip can be added to the tape transport to obtain a combined height of 10.5 inches. This vertical dimension is standard for many racks.

4. Using four 10-32 x 3/8 inch bolts for each slide, secure the slides to the equipment rack at both the front and rear mounting holes (Figure C-13). Note that the slides mount to the rear of the front cabinet rail.

5. Fully extend the center sections of the slides now secured to the rack. When a slide is fully extended, the latch clicks as it locks the slide in its extended position.

6. The tape transport unit should now be slid into the rack mounting slides.

WARNING

Use sufficient personnel for sliding the tape transport unit into the rack.

With one person on each side, lift the transport and insert the slides on the transport into the slides mounted in the rack. Press the spring latches located on the transport slides, and push the transport into the rack until the latches lock into place (this is approximately 8 cm (3 in)). Press the spring latches a second time, and push the transport fully into the rack. A gap of approximately 1.5 to 1.8 cm (0.6 to 0.7 in) is normally present between the rear of the transport front bezel and the mounting rail.

7. Locate the shipping bracket packed with the TSV05-Z. The bracket is designed for use on DIGITAL H9642 series cabinetry, and secures the tape transport unit to the rear cabinet rail (Figure C-12). Install the shipping bracket to protect the equipment during shipment. It is recommended that similar protection be provided by other types of cabinetry.

8. Connect the tape transport power line to the cabinet power receptacle. (Refer to Chapter 2, Section 2.1.2, for power requirements.) For the most reliable operation, the use of filtered ac line voltage is recommended. Make certain there is sufficient power cord slack for the TS05 tape transport to be placed in the service access position without damaging the power cord.

9. Remove the shipping foam from the tape transport as described in Chapter 2, Section 2.3.4.

10. Continue the checkout and installation procedures as described in Chapter 2, Sections 2.4 through 2.7.

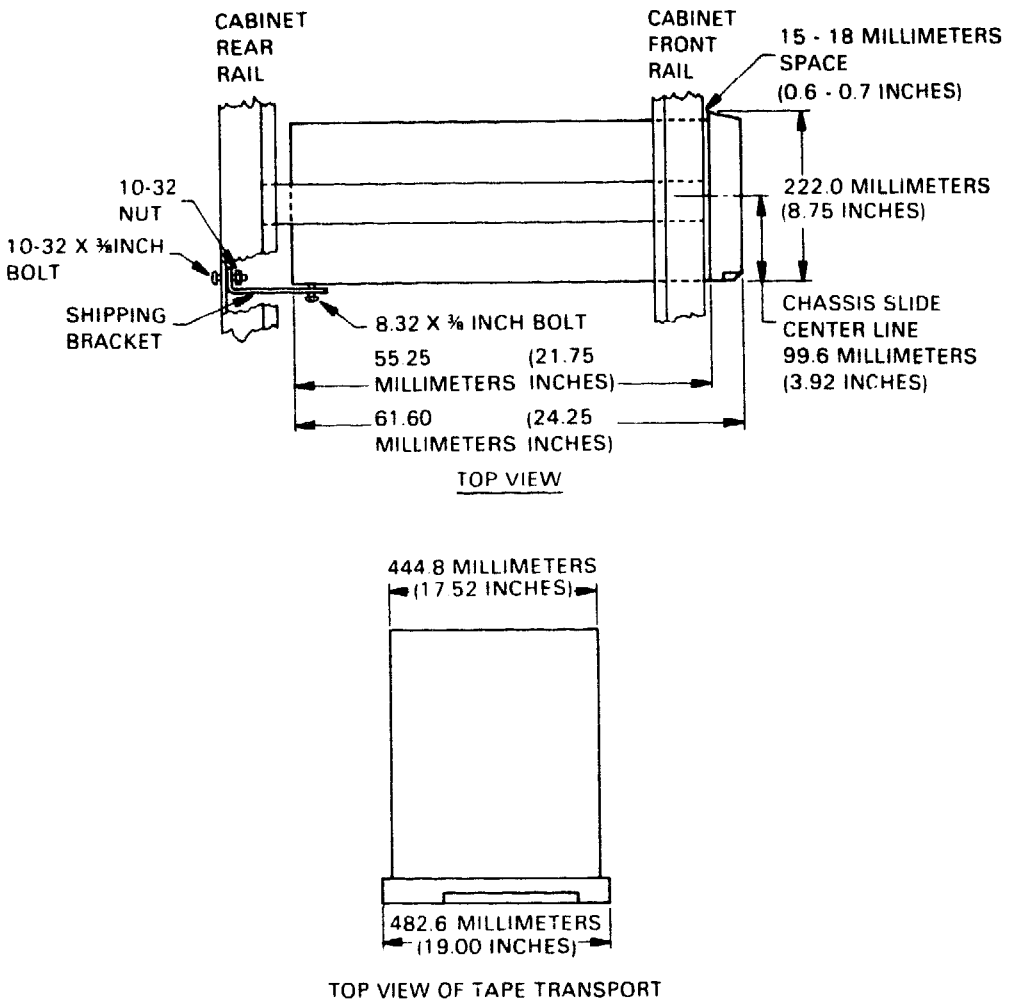


Figure C-12 TSV05-Z Mounting Requirements

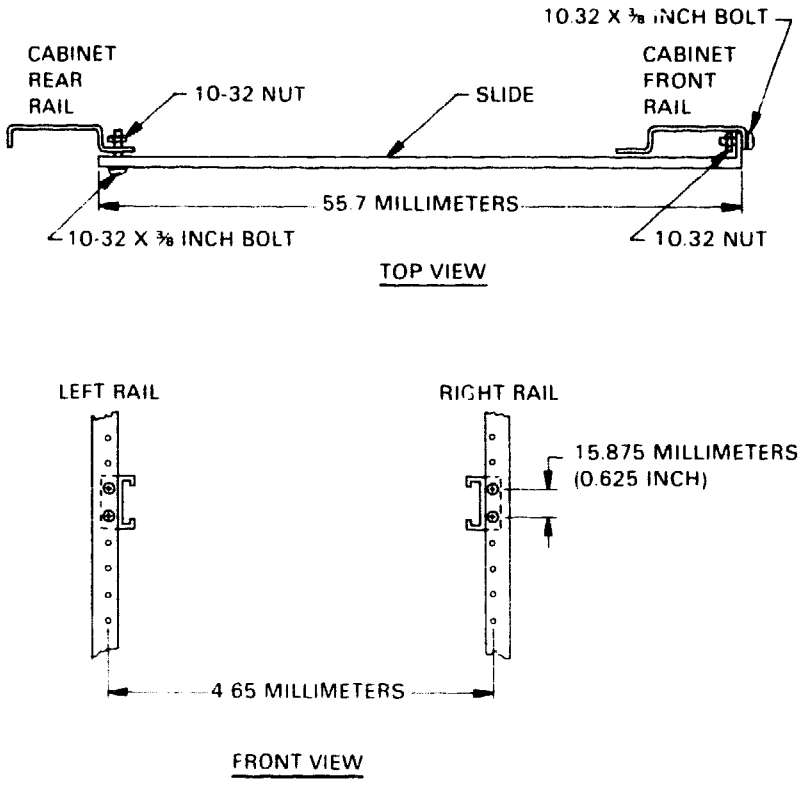


Figure C-13 Chassis Slide Mounting


APPENDIX D

APPENDIX D
CABINET INSTALLATION PROCEDURES

This appendix has been divided into the following sections:

- H9642/H9642 Cabinet Installation Procedures
- H9612/H9642 Cabinet Installation Procedures

D.1 H9642/H9642 CABINET INSTALLATION PROCEDURES

In the TSV05-BA, -BB, -BC, -BD, -SE, -SF, -SH, and -SJ models, the tape transport is shipped mounted in an H9642 cabinet that has a panel on the left side, but only has an expansion ring on the right side. This cabinet is intended to be connected to the left side of an H9642 cabinet (Figure D-1).

The TSV05-BA, -BB, -BC, -BD, -SE, -SF, -SH, and -SJ models can also be connected to earlier Q-22 computer systems that use H9612 cabinets. (Refer to Section D.2 for H9612/H9642 cabinet interconnection procedures.) Note, however, that older systems were not tested for compliance with current FCC rules. Installing the TSV05 subsystems in cabinets other than the H9642 cabinet may result in higher levels of EMI radiation.

The tape transport cabinet is installed by removing the left side panel of the computer cabinet, and then bolting the right side of the tape transport cabinet to the left side of the computer cabinet. This installation is described in the sections that follow.

D.1.1 Tools Required

NOTE

The 1/4 x 20 nuts and bolts are not required for the H9642/H9642 cabinet installation.

Cabinet installation requires the following tools:

1. 9/16- and 11/16-inch wrenches (for leveling feet)
2. 5/32-inch hex key (for door)
3. 7/16-inch wrench (for bolting cabinet together)
4. Screwdriver or nut driver (for connecting ground cable
5. Phillips screwdriver

D.1.2 Removing the Side Panel

Remove the left side panel from the computer cabinet as follows:

1. Open the rear doors of the tape transport cabinet and computer cabinets. Typically, this requires inserting the hex key into the latch, and turning it one-quarter turn counterclockwise (see Figure D-1).
2. Remove the locking bracket located at the rear bottom, right-hand side (as viewed from the rear) of both cabinets. Each bracket is held by two bolts. Loosen (but *do not remove*) the bolts (see Figure D-2).
3. Lift the side panel straight up, and remove it from the CPU cabinet left side. Disconnect the side panel ground wire from the cabinet frame.

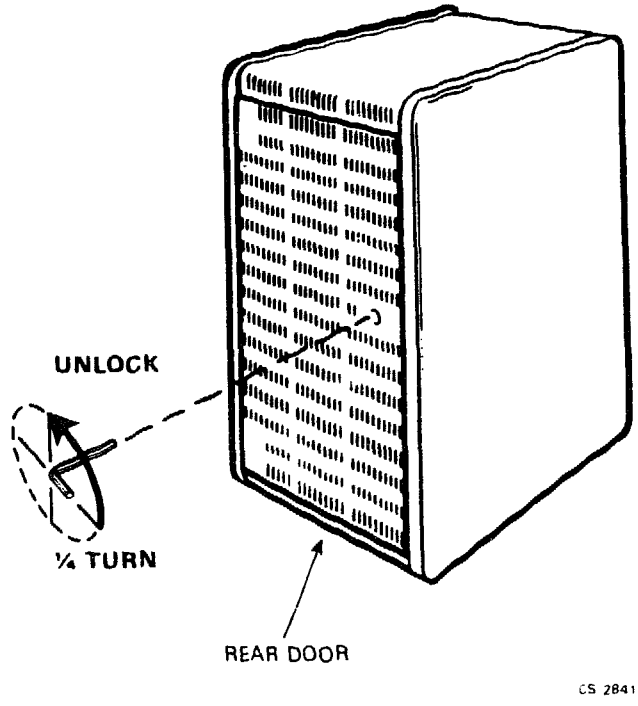


Figure D-1 Opening Cabinet Door

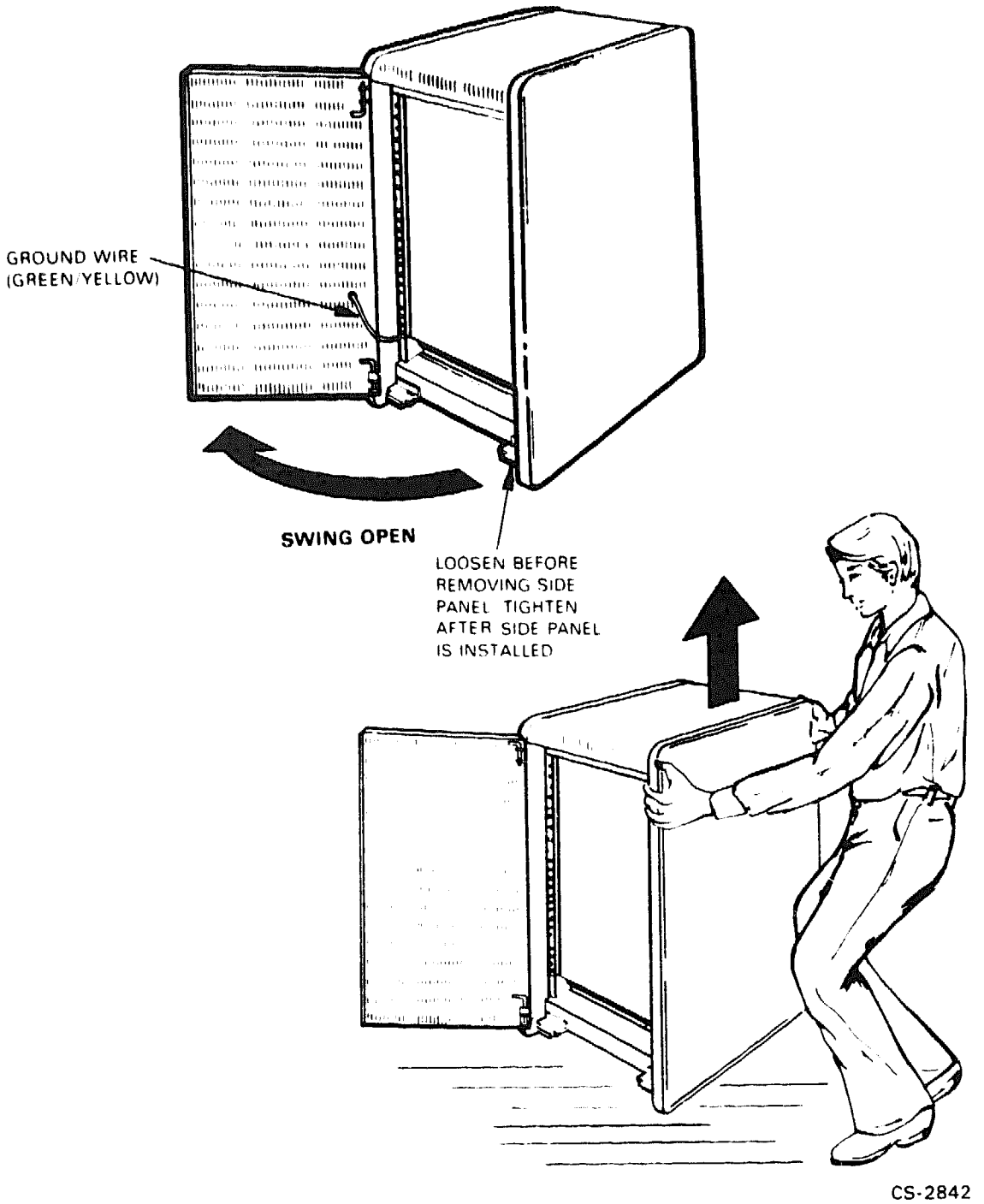


Figure D-2 Removing Side Panel

D.1.3 Connecting the H9642 Cabinets

The two cabinets must be connected together both mechanically and electrically. The mechanical connection is made as follows.

1. Roll the tape transport cabinet, next to the computer cabinet, left side. Place the tape transport cabinet 2.5 cm (1.0 in) forward of the computer cabinet such that the pins in the computer cabinet align with the cutouts in the expansion ring. To obtain this alignment, adjust the tape transport cabinet leveling feet until the top of the tape transport cabinet is level with the top of the computer cabinet.
2. Push the tape transport cabinet sideways so that it is against the computer cabinet. Push the tape transport cabinet backwards until it is even with the computer cabinet. Check that all the pins are engaged properly into the trim panel (refer to Figure D-3).
3. Reinstall the second locking bracket that was removed in Section D.1.2, step 2. Do not tighten it. This bracket is located on the computer cabinet bottom rear, right-hand side (refer to Figure D-4).
4. Loosen (but *do not remove*) the locking bracket that holds the tape transport cabinet rear door bottom pivot pin. This is easier if you partially remove the rear door by pushing down on the top pivot pin and raising the rear door out of the bottom pivot hole.
5. Install the rear intercabinet bracket. Tighten the four screws, ensuring that all brackets are fully down. Reinstall the rear door if it was removed in step 4.
6. Remove the bottom trim panels located on the tape transport and computer cabinets. Typically, these panels are held in place by two Phillips head screws.
7. Remove the four centermost bolts and two centermost trim panel brackets from the cabinetry.
8. Install the front intercabinet bracket. Reinstall the two trim panel brackets and tighten the four bolts, and then reinstall both bottom trim panels.
9. Recheck the cabinetry leveling. Adjust the leveling feet of both cabinets, if necessary, to ensure that the system is properly leveled and all leveling feet are properly supporting the system.
10. Continue with the installation by removing the foam shipping cushions, as described in Chapter 2, Section 2.3.4, and making the necessary power line connections, as described in Chapter 2, Section 2.3.5.

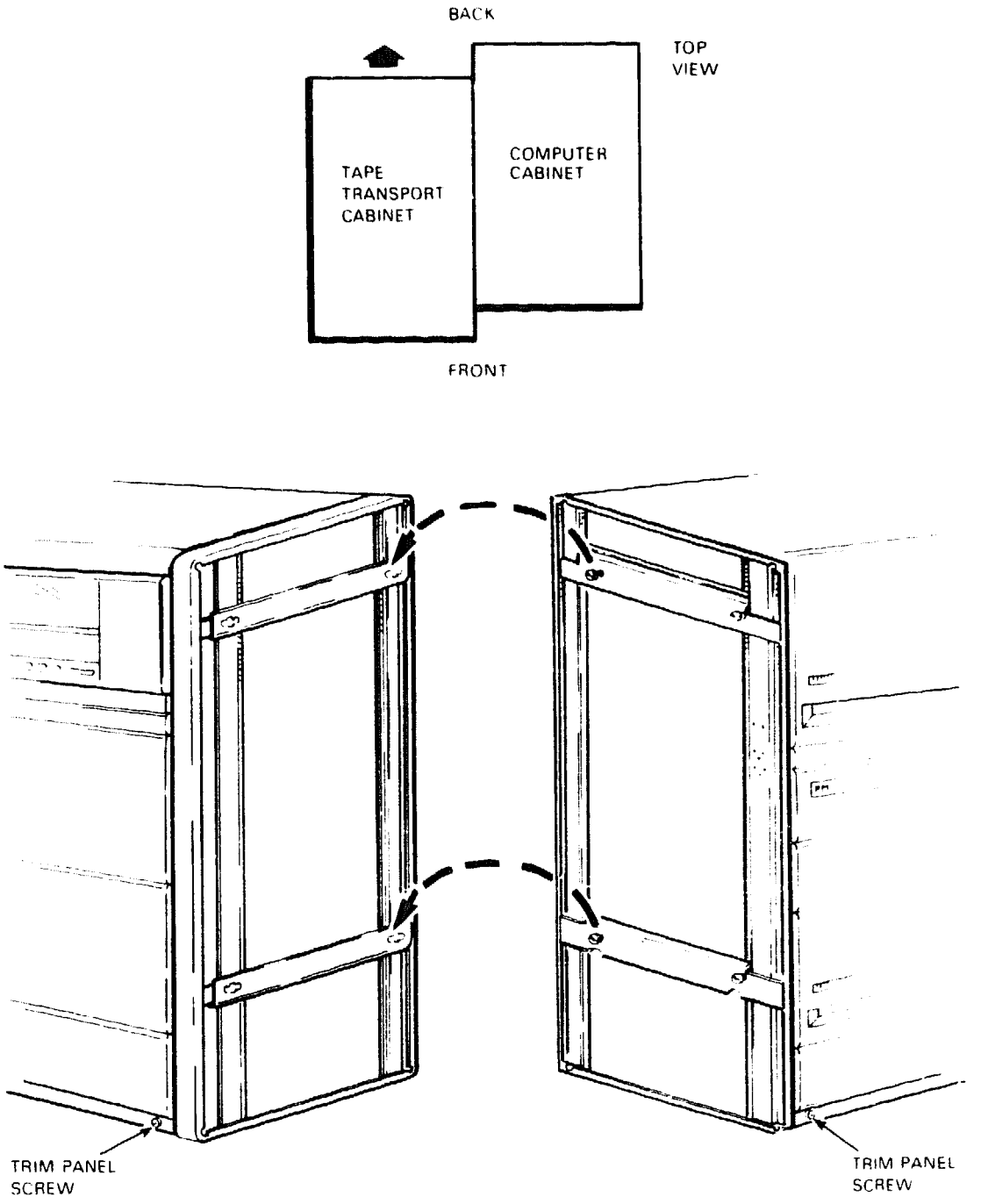


Figure D-3 Cabinet Alignment

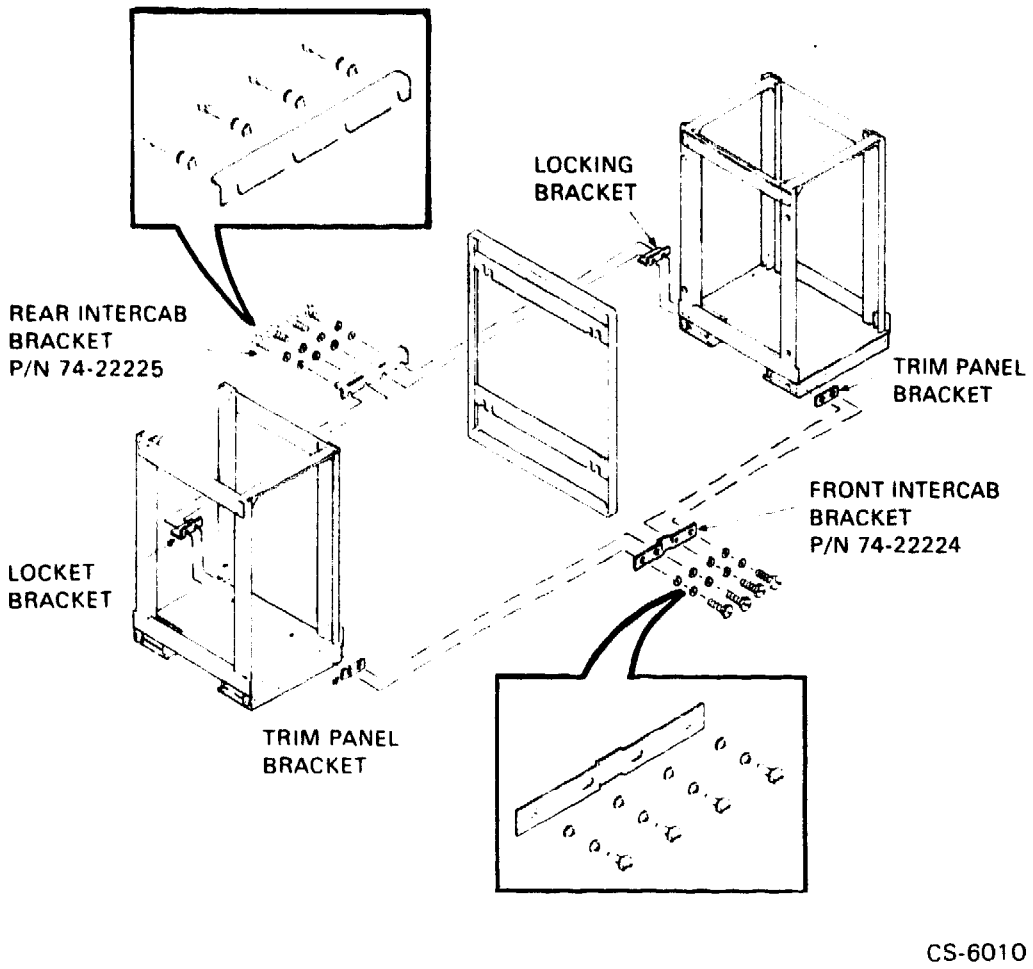


Figure D-4 H9642/H9642 Cabinet Interconnection Hardware

D.2 H9612/H9642 CABINET INSTALLATION PROCEDURES

NOTE

An assembled end panel (part number H9544-AA) can be purchased from DIGITAL.

This cabinet interconnection procedure can be used for installations that meet the following conditions:

- The system uses a PDP-11/23A computer.
- The computer cabinet is model H9612.
- The computer cabinet has pop-out type end panel inserts.
- The cabinet has four adjustable leveling feet capable of raising it 13 millimeters (1/2 inch).
- There is no external hardware connected to the cabinet that would be adversely affected by being raised 13 millimeters (1/2 inch). If these are true, then the H9642 tape transport cabinet can be connected to the H9612 computer cabinet as follows:

  1. Remove the left side pop-out end panel and ground strap from the H9612 computer cabinet. These parts are reused in step 5.
  2. Remove the expansion ring from the right side of the tape transport cabinet. Note that this requires loosening the rear bottom locking bracket. The expansion ring is reused in step 5.
  3. Place the tape transport cabinet next to the left side of the computer cabinet. Typically, the computer cabinet is approximately 13 millimeters (1/2 inch) lower than the tape transport cabinet at this point.
  4. Adjust the computer cabinet leveling feet until the top of both cabinets are even.
  5. Assemble the pop-out end panel insert (removed in step 1) with the expansion ring (removed in step 2) to make a finished end panel suitable for mounting on the tape transport cabinet. This is done as follows:

     a. Place the end panel insert into the expansion ring on the non-slotted side.

     b. Align the positioning inserts.

     c. Using a flat-blade screwdriver, pop the spring tabs into place.

  6. With both cabinets level and even, install the four bolts and 12 nuts at convenient locations to connect the two cabinets (Figure D-5). Note that the 74-22224/74-22225 intercabinet brackets are not used in this installation.
  7. Place the assembled side panel next to the left side of the tape transport cabinet. Using the supplied hardware, connect the side panel ground strap to the tape transport cabinet left rear cabinet rail.

8. Install the assembled side panel on the tape transport cabinet. Note that the rear bottom locking bracket must be loosened to perform this step

9. Recheck the cabinet leveling. If necessary, adjust the leveling feet of both cabinets to ensure that the system is level and that all leveling feet are supporting the system properly.

10. Ensure that the locking brackets loosened in steps 2 and 8 are tightened securely.

11. Continue with the installation by removing the foam shipping cushions, as described in Chapter 2, Section 2.3.4, and making the necessary power line connections as described in Chapter 2, Section 2.3.5.

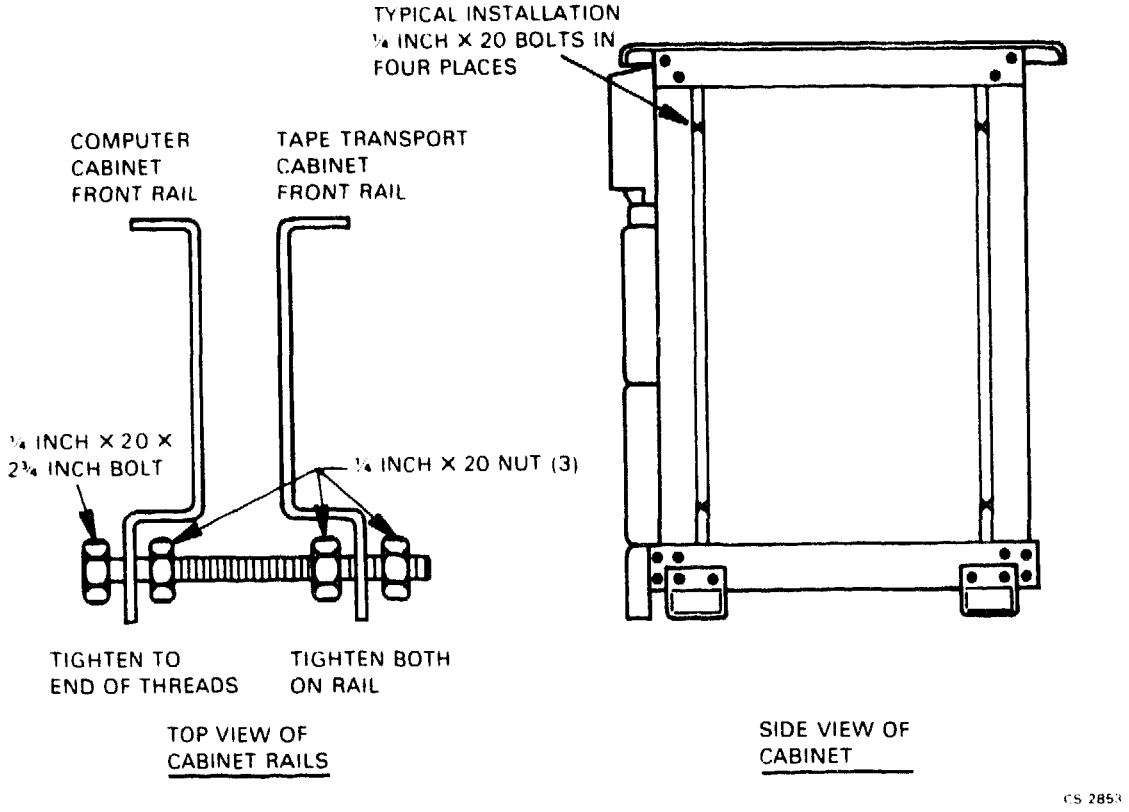


Figure D-5 Cabinet Interconnection


APPENDIX E

APPENDIX E
TAPE TRANSPORT SIGNAL DESCRIPTION

Signal Mnemonic	Print Set Sheet No.	Signal Description
A0-A15	D2	Address Bus (three-state output, active high) — Provides the address for memory data exchanges and PIO device data exchanges.
A0	D5	A Phase — One of two clocks generated by the tachometer. These clocks are used to determine tape speed, direction, and position.
B/A SEL	D2	PIO Port B or A Select (input, active high) — This pin defines which port is accessed during a data transfer between the Z80 and the PIO. A low level on this pin selects Port A, while a high level selects Port B.
BITCLK	D6	Bit Clock — Used to generate PECLK when both Channel 2 and Channel 1 are dropped. (This condition causes the hard error line to go active during data recovery.)
BLOCK	D9	Block — Term identifying a data record. Block goes active approximately 15 character times into the preamble.
B0	D5	B Phase — One of two clocks generated by the tachometer. These clocks are used to determine tape speed, direction, and position.
CS1-CS0	D2	Channel Select for CTC (input, active high) — These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O write or read (see truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

Signal Mnemonic	Print Set Sheet No.	Signal Description
CE		Chip Enable of CTC (input, active low) — A low level on this pin enables the CTC to accept control words, interrupt vectors, or time constant data words from the Z80 data bus during an I/O read cycle.
C/D SEL	D2	Control or Data Select for PIO (input, active high) — This pin defines the type of data transfer to be performed between the CPU and the PIO. A high level on this pin during a CPU write to the PIO causes the Z80 data bus to be interpreted as a command for the port selected by the B/A select line. A low level on this pin means that the Z80 data bus is being used to transfer data between the CPU and the PIO. Address bit A1 from the CPU is often used for this function.
CDATX	D9	Corrected Data Multiplexed — Data byte that is sent to the output register in serial form.
CHDROP P, 0-7	D8	Channel Drop — This signal indicates the loss of a data channel for a minimum of four character times.
CHDROPX	D9	Channel Dropped Multiplexer — This signal represents the multiplexed channel drop signals.
CHDT	D9	Channel Detect — This signal is TRUE if two or more channels are active, and assert IHER if a gap is not detected following the postamble.
CLK8M	D2	Eight Megahertz Clock — This clock is used to generate phase clock (0), 1 MHz clock (01M), RNOISE, and write clock (W2XCLK).
CTCCLK0	D2	CTC Clock Zero — This clock indicates that tape is in motion. Also indicates forward or reverse direction, depending on the tachometer quadrature.
CTCCLK1	D2	CTC Clock 1 — This clock indicates that tape is in motion. Also indicates forward or reverse direction, depending on the tachometer quadrature.
CTCZC2	D2	CTC Clock Two — This clock output from the CTC of approximately 40 Hz is used to generate a sawtooth waveform for the compliance arm transducer.
D0-D7	D2	CTC Data Bus of Z80 (three-state input/output, active high) — D0-D7 constitutes an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
DATA	D9	Recovered Data — Refers to the nine data lines clocked into the formatter.

Signal Mnemonic	Print Set Sheet No.	Signal Description
DATA P. 0-7	D7	Data — Refers to the data lines from the read logic to the formatter.
DATA0X	D9	Data Zeros Multiplexed — This signal represents the serialized data bits input into the skew buffer.
DAVL P. 0-7	D8	Data Available — Term identifying data is positioned at the read head, and is ready to be clocked into the formatter.
DAVLX	D9	Data Available Multiplexed — This signal is used to input the serialized data into the skew buffer.
DCLK	D9	Data Clock — This signal is synchronized with CDATX data to generate IRSTR.
DCLK1	D8	Data Clock 1 — Alternate input to the formatter read clock circuitry. Used in the event of data dropout in read Channel 2.
DCLK2	D8	Data Clock 2 — Primary input to the formatter read clock circuitry. Synchronizes PE clock to the data rate.
DINLOW	D6	Data In Low — Enables write data to be clocked into the formatter from the controller.
DOUT	D9	Data Out — This signal is used to enable the output from the skew buffer.
DROP1	D9	Drop One — This signal indicates that a signal channel dropout has occurred.
ENFMG	D10	Enable File Mark and Gap — Enables file mark and ID burst outputs from the formatter, as well as block detect to the Z80.
ENRD	D10	Enable Read — Enables read strobes and data output from the formatter.
FERR	D9	Format Error — This signal asserts the IHER line following a parity error or a nonzero character in the postamble.
FRC 1, 2,3	D6	Flux Reversal Control Lines — These lines determine the write formatter mode of operation. The following describes how they are used.

Command	FRC1	FRC2	FRC3
Write ID Burst	1	0	0
Write File Mark	1	0	1
Write Data	1	1	1

Signal Mnemonic	Print Set Sheet No.	Signal Description
FSEL	D3	Formatter Select — This signal indicates drive is selected by comparing the unit number of the drive to the IFAD and ITAD lines. FSEL enables drive status information (IONL, IRDY, and so on) to be sent to the controller.
FWD	D10	Forward — This signal indicates forward tape motion to the read formatter logic. When tape is moving in the reverse direction, the read data is inverted.
~HER	D9	Hard Error — This signal indicates an uncorrectable data error condition.
HIGH RATE	D9	High Rate — This signal is a phase clock used by the formatter when the drive is selected for 100 inches/second operation.
~INT	D2	Interrupt Request (input, active low generated by CTC and PIO) — ~INT is serviced by Z80 at the end of the current instruction.
~IOREQ	D2	PIO Input/Output Request from Z80-CPU (input, active low) — The ~IOREQ signal is used in conjunction with the B/A select, C/D select, ~CE, and ~RD signals to transfer commands and data between the Z80-CPU and the Z80-PIO. When ~CE, RD, and ~IORQ are active, the port addressed by B/A transfers data to the CPU (a read operation). Conversely, when ~CE and ~IORQ are active but ~RD is not active, then the port addressed by B/A accepts, from the CPU, either data or control information as specified by the C/D select signal. Also, if ~IORQ and ~MI are active simultaneously, the CPU is acknowledging an interrupt, and the interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest device requesting an interrupt.
IS	D4	Supply Servo Current — This signal represents the supply servo current.
IT	D4	Takeup Servo Current — This signal represents the takeup servo current.
~LASTW	D6	Last Word — This signal indicates that the last data character to be written is present on the interface lines. It is also used to terminate the variable length erase operation.

Signal Mnemonic	Print Set Sheet No.	Signal Description
~MREQ	D2	Memory Request (three-state output, active low) — This signal indicates that the address bus holds a valid address for a memory read or write operation.
~M1	D2	PIO Machine Cycle One Signal from CPU (input, active low) — This signal from the CPU is used as a sync pulse to control several internal PIO operations. When ~M1 is active and the RD signal is active, the Z80-CPU is fetching an instruction from memory. Conversely, when ~M1 is active and IORQ is active, the CPU is acknowledging an interrupt. In addition, the ~M1 signal has two other functions within the Z80-PIO: 1. M1 synchronizes the PIO interrupt logic. 2. When M1 occurs without an active RD or IORQ signal, the PIO logic enters a reset state.
PECLK	D9	Phase Encode Clock — Clock (22 times the data rate) that is used to synchronize the data in the formatter.
~PENAB	D9	Phase Encode Enable — This signal enables formatter to send read strobes and data information.
POSTCHR	D9	Post Character — This signal identifies detection of the postamble.
PSEL	D9	Parity Select — This signal gates parity channel from the read logic to the formatter.
PULSE 0	D3	Pulse 0 — This signal enables the I/O control register.
PULSE 1	D3	Pulse 1 — This signal sets the on-line flip-flop.
PULSE 2	D3	Pulse 2 — This signal resets the rewind flip-flop.
PULSE 3	D3	Pulse 3 — This signal sets the rewind flip-flop.
PULSE 4	D3	Pulse 4 — This signal resets the on-line flip-flop.
PULSE 5	D3	Pulse 5 — This signal is used to enable the formatter.
PULSE 6	D3	Pulse 6 — This signal trigger is used in the error routine for troubleshooting the drive.
PULSE 7	D3	Pulse 7 — This signal trigger is used in the error routine when outputting RAM to the data bus.
P0A0	D2	PIO input that represents the IREV interface line.
P0A1	D2	PIO input that represents the IWRT interface line.
P0A2	D2	PIO input that represents the IWFM interface line.

Signal Mnemonic	Print Set Sheet No.	Signal Description
P0A3	D2	PIO input that represents the IEDIT interface line.
P0A4	D2	PIO input that represents the IERASE interface line.
P0A5	D2	PIO input that represents the IHISP interface line.
P0A6	D2	Reserved for future use.
P0A7	D2	Reserved for future use.
P0B0	D2	PIO input that represents the IFEN interface line.
P0B1	D2	PIO input that represents the IGO interface line. ~POASTR strobes the command into the PIO.
P0B2	D2	PIO output that is reserved for future use.
P0B3	D2	PIO output that, when LOW, enables the erase head.
P0B4	D2	PIO output that, when LOW, enables the write head.
P0B5	D2	PIO output that, when LOW, selects the high speed [254 cm/s (100 in/s)] mode of operation, and when LOW selects the low speed [64 cm/s (25 in/s)] mode of operation.
P0B6	D2	PIO output that indicates EOF (end of file) or the completion of a write block.
P0B7	D2	PIO output that, when HIGH, selects the normal mode of write operation.
P1A0-P1A7	D2	PIO inputs that represent counter values; P1A0 (LSB), P1A7 (MSB) used by the Z80 to determine tape speed (nominal binary count of 200).
P1B0-P1B1	D2	PIO inputs that are used by the Z80 to determine the tachometer phase.
P1B2-P1B3	D3	PIO outputs that, when active, enable the Z80 to prescale the tachometer for the following speeds: 00: 254 cm/s (100 in/s) 11: 64 cm/s (25 in/s)
P1B4-P1B7	D2	PIO inputs that, when active, are used by the Z80 to calculate tape position.

Signal Mnemonic	Print Set Sheet No.	Signal Description
P2A0	D2	PIO input that, when HIGH, indicates no tape in path.
P2A1	D2	PIO input that pulses LOW to indicate the presence of a write enable ring.
P2A2	D2	PIO input that, when HIGH, indicates that the front panel door or top cover is open.
P2A3	D2	PIO output that, when LOW, enables the servos.
P2A4	D2	PIO output that, when LOW, enables the supply servo loop sense.
P2A5	D2	PIO output that, when HIGH, selects the supply servo voltage source.
P2A6	D2	PIO output that, when HIGH, selects the supply servo voltage or current drive.
P2A7	D2	PIO output that, when HIGH, selects the takeup servo voltage or current drive.
P2B0	D2	PIO output that, when HIGH, activates the door lock circuitry.
P2B1	D2	PIO output that, when HIGH, activates the hub lock circuitry.
P2B2	D2	PIO output that, when HIGH, enables +30 V to the servo circuits.
P2B3	D2	PIO output that, when LOW, enables -30 V to the servo circuits.
P2B4	D2	PIO output that, when LOW, activates the blower motor circuitry.
P2B5	D2	PIO output that, when HIGH, deactivates the system failure mechanism.
P2B8-P2B7	D2	PIO outputs that, when HIGH, select one of the following PE write modes of operation: 00: Clear 01: End of File 10: Identification Burst 11: Data Block

Signal Mnemonic	Print Set Sheet No.	Signal Description
P3A0	D2	PIO output that, when HIGH, asserts the ISPEED interface line.
P3A1	D2	Reserved for future use.
P3A2	D2	PIO input that, when HIGH, indicates gap detect.
P3A3	D2	PIO input that, when HIGH, represents the IFMK interface line.
P3A4	D2	PIO input that, when HIGH, represents the IONL interface latch.
P3A5	D2	PIO input that, when HIGH, represents the IRWD interface latch.
P3A6	D2	PIO input used to detect CHDT signal.
P3A7	D2	PIO input that, when LOW, enables the servo motor shorting relay.
P3B0-P3B4	D2	PIO outputs that enable the switch panel indicators and the PIO inputs that represent the front panel switches.
P3B5	D2	Reserved for optional use.
P3B6	D2	PIO output that, when HIGH, enables the RNOISE circuitry.
P3B7	D2	PIO output that, when LOW, enables the +5 V noise injection circuitry.
P ARDY	D2	This signal indicates that the PIO is ready to accept information.
~P ASRT	D2	This signal clocks the PIO, causing input information to be latched. When the PIO is enabled, an interrupt occurs.
~RD	D2	Memory Read (three-state, active low) — ~RD indicates that the CPU wants to read data from memory or an I/O device.
RDATA P, 0-7	D7	Read Data — These signals are the nine data lines being read off tape.
~RDROP P, 0-7	D7	Read Drop — This signal indicates the loss of data for a minimum of four character times. Used for block, file mark, and ID burst detection.
~RES	D2	Reset — Input to the Z80, active low signal that forces program counter to zero and initializes the CPU.

Signal Mnemonic	Print Set Sheet No.	Signal Description
RNOISE	D2	Read Noise — This signal injects a 500 kHz low amplitude signal into the read amplifiers, used for diagnostic firmware.
SCAN P. 0-7	D9	This signal selects which data channel is multiplexed into the formatter.
SIDR	D4	Supply Input Drive — The drive is operating on either the current or voltage mode, depending upon the feedback enable.
SMDH	D4	Supply Motor Drive High — This signal is used for the supply motor drive voltage.
SMDL	D4	Supply Motor Drive Low — This signal is used for current sense.
-STRBX	D9	This signal enables read strobes and read data from the formatter. Used to disable read strobes when the postamble has been detected.
TIDR	D4	Takeup Input Drive — The drive is operating in either the current or voltage mode, depending upon the feedback mode.
TMDH	D4	Takeup Motor Drive High — This signal is used for the takeup motor drive voltage.
TMDL	D4	Takeup Motor Drive Low — This signal is used for current sense.
VCOM	D7	Read Threshold Voltage — VOUT 0 will change the read threshold during a read or write operation.
-VHMON	D4	Voltage High Minus ON — This signal enables -30 V to the takeup and supply motors.
-VHPON	D4	Voltage High Positive ON — This signal enables +30 V to the takeup and supply motors.
VIN0	D5	Voltage Input Zero — This signal is input voltage from the EOT sensor.
VIN1	D5	Voltage Input One — This signal is input voltage from the BOT sensor.
VIN2	D5	Voltage Input Two — This signal is input voltage from the compliance arm transducer logic.
VIN3	D4	Voltage Input Three — This signal is used to determine supply servo EMF and voltage.

Signal Mnemonic	Print Set Sheet No.	Signal Description
VIN4	D4	Voltage Input Four — This signal is used to determine takeup servo EMF and voltage.
VIN5	D4	Voltage Input Five — This signal is used to determine supply servo current.
VIN6	D4	Voltage Input Six — This signal is used to determine takeup servo current.
VIN7	D4	Voltage Input Seven — This signal is used to determine the supply motor offset voltage.
VOUT0	D3	Voltage Output Zero — This signal controls the read threshold voltage.
VOUT1	D3	Voltage Output One — This signal controls the compliance arm offset voltage into the supply servo logic.
VOUT2	D3	Voltage Output Two — This signal is the supply servo voltage control.
VOUT3	D3	Voltage Output Three — This signal is the supply servo current limit control.
VOUT4	D3	Voltage Output Four — This is a takeup servo voltage control.
VOUT5	D3	Voltage Output Five — This is a takeup servo current limit control.
VRCCHR	D9	Parity — This signal indicates the calculated parity of the byte being transferred to the bus.
VS	D4	Voltage Supply — This signal represents the supply motor voltage feedback.
VT	D4	Voltage Takeup — This signal represents the takeup motor voltage feedback.
V30P	D5	Voltage 30 Positive — Positive 30 V drive voltage for the reel servo circuits (clockwise rotation).
V30M	D5	Voltage 30 Minus — Negative 30 V drive voltage for the reel servo circuits (counterclockwise rotation).
V20P	D5	Voltage 20 Positive — Positive 20 V drive voltage for the reel servo circuits (clockwise rotation).
V20M	D5	Voltage 20 Minus — Negative 20 V drive voltage for the reel servo circuits (counterclockwise rotation).

Signal Mnemonic	Print Set Sheet No.	Signal Description
V7AC	D5	Voltage 7 Alternating Current — This signal is the ac input for the +5 Vcc noise injection circuitry.
V9P	D5	Voltage 9 Positive — This signal is the positive voltage from the power supply that is used to generate the +5 V sources.
~WAIT	D3	When active (LOW), this signal causes the Z80 to go into the wait state. The wait state is only used to send or receive data from the DAC.
~WR	D2	Memory Write (three-state, active low) — This signal indicates that the CPU data bus (D0-D7) holds valid data that is to be stored in memory or an I/O device.
~WSTROBE	D6	This signal is a clock that latches the write data to the formatter.
W2XCLK	D6	Write 2 Times Clock — This signal clocks the data to the write head.
0	D2	System Phase Clock — This signal is a 2 MHz clock used for the microprocessor circuitry.
01M	D2	One Megahertz Clock — This signal is a 1 MHz clock used for the microprocessor circuitry.