DECpc 433T
Technical Reference Manual

Order Number ER-PCT1Y-AA-001

digital equipment corporation
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Contents

Introduction

This manual is written for software developers, systems integrators and others who require technical knowledge of the DECpc 433T computer system. The manual is not intended as a tutorial or tool for teaching microcomputer architecture.

The following documents provide more detailed information about the standard components used in the DECpc 433T computer system:

Intel i486 Data Book
Intel 82350 EISA Chip Set Data Book
Intel 8742AH Universal Peripheral Interface Microcontroller Data Sheet
Western Digital WD37C65 Diskette Controller Data Sheet
Western Digital WD16C452 Dual Enhanced Asynchronous Communications Element (ACE) Data Sheet
Western Digital WD7000-EX Interface Specification

We recommend you have these documents readily available when you use this manual.

About This Manual

The purpose of this manual is to provide technical information about the hardware architecture and device programming of the DECpc 433T. The manual is divided into the following sections:

Introduction	Describes the purpose of the manual and notational conventions used.
Specifications and Features	Provides a basic technical description of the system equipment.
Technology Overview	Provides a brief overview of EISA.
Theory of Operation	Describes the individual components of the system and their interaction.

System Configuration	Lists the default configuration settings. Describes modification of the standard configuration.
Device Programming	Describes the registers and programming of all programmable components in the system.
BIOS Services	Provides a detailed listing of BIOS services and error messages available to programmers.
EISA SCSI Host Adapter Reference	Describes the EISA SCSI Host adapter and its interface with the system
VGA 1024 Adapter Reference	Describes the optional VGA 1024 video adapter

Conventions

This section describes the notations, abbreviations, and special print styles that are used in this manual.

Abbreviations and Acronyms

A variety of abbreviations and acronyms are used throughout this manual. They are listed here for convenient reference.

Abbreviation or Acronym	Full Meaning
A	Amperes (amps)
b	bit(s)
B	byte(s)
Btu	British Thermal Unit
BPI	Bits per Inch
EISA	Extended Industry Standard Architecture
Hz	Hertz
IDE	Integrated Drive Electronics
in.	inch(es)
ISA	Industry Standard Architecture
SCSI	Small Computer Systems Interface
SIMM	Single In-line Memory Module
V	Volts

Abbreviations and Acronyms

Standard Prefixes

This manual uses standard prefixes to indicate multiples of fundamental units. The standard prefixes are listed in the following table:

Prefix	Symbol	Multiple
giga-	G	10^9
mega- (decimal sense)	M	10^6
Mega- (binary sense)	M	2^{20}
kilo- (decimal sense)	k	10^3
Kilo- (binary sense)	K	2^{10}
centi-	c	10^{-2}
milli-	m	10^{-3}
micro-	μ	10^{-6}
nano-	n	10^{-9}

Standard Prefixes

Special Notations

Signal names are specified in uppercase letters, such as HIGH. A signal name followed by a minus sign, as in LOW–, indicates an active low signal. A signal name without a minus sign indicates an active high signal.

Special Print Styles

The following print styles are used to differentiate various types of information:

- Words that are printed in small bold capital letters represent keys on your keyboard. For example: ENTER.
- Groups of keys are printed like this: CTRL+ALT+DEL. Press and hold the keys (CTRL, ALT, and DEL in this example) in the order shown.
- Information that you should type or that is shown on the screen is printed as in the following example:

  Type `3` at the `Select the Desired Action` prompt.

Specifications and Features

This section lists the major subassemblies and components in the DECpc 433T and provides detailed specifications for most subassemblies and components.

System Specifications

This section includes a summary of the standard configuration of the DECpc 433T. Refer to "*Device and Component Specifications*" for detailed specifications of the components in this list.

This section also summarizes the physical and electrical characteristics of the system unit and defines the environmental requirements for safe operation of the computer.

Configuration Overview

The following devices and components are included in the standard configuration of the DECpc 433T.

Devices in standard configuration

- Intel i486 microprocessor
- 4MB DRAM (70 ns)
- 1.44MB 3½-inch diskette drive
- 383-watt power supply (115/230V input, automatically sensed)
- 101/102-key enhanced keyboard
- Multi-function adapter providing diskette controller, 2 serial ports, one parallel port, and an LCD display interface
- EISA SCSI Host Adapter
- DEC two-button serial mouse

Expansion support	◦ Eight EISA 32-bit expansion slots ◦ Ten half-height 5¼-inch drive bays ◦ Sixteen SIMM sockets ◦ 128KB external cache upgrade ◦ Weitek 4167 math coprocessor socket
Software supplied with system	◦ Computer Configuration Utility (in 5 languages) diskette ◦ ISA Options Configuration diskette ◦ SCO Unix 3.2 Drivers diskette ◦ Diagnostic software package
Self-test diagnostic procedures	◦ ROM-based; perform memory tests and verify operation on power-up and reset
Clock speeds	
CPU	◦ 33 MHz
EISA Expansion bus	◦ 8.25 MHz
I/O Ports	◦ Centronics-compatible parallel port (25-pin D-shell) ◦ Dual RS-232 serial ports (9-pin D-shell) ◦ PS/2-style keyboard port (6-pin mini-DIN)

Available System Upgrades

The following lists describe some of the internal options and examples of external options that are available for the DECpc 433T.

Internal options supported	◦ Memory upgrades using 1MB x 9 or 4MB x 9 SIMMs (70ns or faster) ◦ 128KB external cache upgrade ◦ 3½- and 5¼-inch storage including diskette drives, SCSI hard drives, and tape cartridge systems ◦ Network adapter ◦ VGA graphics adapter ◦ Weitek 4167 math coprocessor ◦ CD-ROM Drives ◦ SCSI Tape cartridge systems
External options supported	◦ Printers ◦ Modems

Physical Specifications

Dimensions of system unit	Depth: 68.58 cm (27 in.) Width: 22.86 cm (9 in.) Pedestal width: 36.0 cm (14 in) Height: 64.77 cm (25.5 in.)
Weight	
Shipping weight (system unit, documentation, and packing material)	33 kg (73.5 lbs.)
Base system unit only	32 kg (70.0 lbs.)

Electrical Specifications

Nominal input voltage	
115V	Input AC voltage: 90V to 135V Frequency: 60 Hz Peak Current: 11.0 A
230V	Input AC voltage: 198V to 264V Frequency: 50/60 Hz Peak Current: 6.0 A
Power consumption	547 Watts
DC output power	383 Watts
IEC 320 AC power outlet	115 VAC; 2 A 230 VAC; 1 A

Environmental Requirements

Acceptable temperature range	
Operating:	10°C to 35°C (50°F to 95°F)
Storage:	-20°C to 66°C (-4°F to 150°F)
Humidity tolerance	
Operating:	20% to 80% (non-condensing)
Storage:	10% to 90% (non-condensing)

Operational Characteristics

Heat output	1866 Btu/hr
Operational clearance requirements	10.0 cm (4 in.) back and sides
Industry certification	UL, CSA, FCC Class A, TUV-GS, VDE Class B

Device and Component Specifications

This section provides detailed physical, electrical and operational specifications for most of the devices and components in the standard configuration.

Processor

Processor type	◦ Intel i486, 33 MHz
Data types supported	◦ Bit, byte, word, double-word
Registers	◦ 16 base architecture registers ◦ 7 systems level registers ◦ 13 floating point registers ◦ 11 debugging and test registers
Address space	◦ 4GB physical address space ◦ 64 Terabytes (i.e. 64×2^{64} bytes) virtual address space
Segment size	◦ variable length, maximum 4GB

System Memory

Standard configuration	◦ 4MB (minimum)
Memory type	◦ 1MB X 9 or 4MB X 9 DRAMs (SIMM package)
Memory speed	◦ 70 ns (or faster)
Memory upgrade support	◦ Expandable to 64 MB
Memory organization	◦ Page mode
Local bus type	◦ 32 dedicated data lines ◦ 32-bit address bus (30 address lines and 4 byte enable lines which replace the two least significant address bits)

Cache Memory

Primary cache

Controller	◦ Intel i486 (internal)
Type	◦ Unified Code/Data, write-through
Organization	◦ Four-way set associative
Size	◦ 8KB

Secondary cache

Controller	◦ Discrete logic
Type	◦ Buffered write-through SRAM
Organization	◦ Direct mapped
Size	◦ 128KB, expandable to 256KB

BIOS ROM

Source	◦ Phoenix
Type	◦ 80486/EISA ROM BIOS Plus
Version	◦ 1.00.17D

Expansion Slots

Type	◦ Eight 188-pin 32-bit EISA slots (six support bus mastering) ◦ All slots are 8/16-bit ISA (IBM PC/AT) compatible
Size	◦ Up to 34.07 cm x 12.7 cm (13.415 in. x 5 in.)

Interrupt Controller

Model	Equivalent to 2 X 8259 cascaded
Number of interrupt levels	15

DMA Controller

Model	Equivalent to 2 X 8237 cascaded
Number of channels	7

Diskette Drive

Model	Sony MP-F11W-72D or equivalent
Capacity	1.44 MB formatted
Average access time	94 ms
Transfer rate	500,000 bits per second (max.)
Mean Time Between Failure	30,000 hours

Ports

Parallel	Centronics-compatible
Serial (2)	Standard RS-232C Data length: 5-, 6-, 7-, and 8-bits Stop bits: 1, 1½, or 2 Parity: odd, even, or none Transmission rates: 50 to 56,000 baud UART: 16451 equivalent

Power Supply

Input Voltage	115V/230V AC, automatically sensed

Output Voltages and Currents (nominal)

Voltage	Current
+12 Vdc	14 A (19 A peak)
+ 5 Vdc	40 A
- 5 Vdc	0.5 A
-12 Vdc	1 A

Video Support

With the appropriate graphics adapter and monitor, the DECpc 433T can support Hercules Mono, EGA, VGA, and Super VGA modes including 132-column text, 800 x 600 graphics, and 1024 x 768 graphics.

Keyboards

Several keyboards are available as options on the DECpc. Keyboards used with the DECpc must be equipped with a 6-pin miniature DIN (PS/2-style) connector.

Industry Standard PS/2-style 101-key Keyboard

The 101-key enhanced keyboard (PCXAL-AA) provides the industry-standard PS/2-style key arrangement with American English keys.

International 102-key Industry Standard Keyboards

The international keyboards provide a standard 102-key arrangement in language-specific variations (PCXAL-xx, where xx is the country specific code). Country-specific keyboards are available for Belgium (AB), Denmark (AD), Finland (CA), France (AP), Germany (AG), Israel (AT), Italy (AI), Norway (AN), Portugal (AV), Spain (AS & AR), Sweden (CA), Switzerland (CH), and the United Kingdom (AE).

Technology Overview

This section provides a brief overview of EISA and related issues. Those needing more information than presented here are encouraged to obtain the complete EISA Specification from BCPR Services, Inc. at the following address:

BCPR Services, Inc.
1400 L Street, N.W.
Washington,D.C. 20005.

About EISA

Extended Industry Standard Architecture (EISA) is a high performance 32-bit system design. EISA is a superset of the popular Industry Standard Architecture (ISA) used in the IBM PC/AT. EISA extends ISA to take advantage of high performance 32-bit microprocessors, such as the Intel 386DX and i486.

EISA supports *intelligent bus masters*. Bus masters improve system speed by performing administrative bus duties normally performed by the CPU. This leaves the CPU free to perform its primary tasks. EISA also supports *level sensitive interrupts*. This permits interrupt sharing, a significant advantage over the ISA bus' edge-triggered interrupts that cannot be shared.

The EISA expansion bus accepts EISA and ISA expansion boards. EISA Expansion boards can have 16- or 32-bit data paths. Some 32-bit EISA boards can support data transfer rates as fast as 33MB per second. The EISA bus adds many grounding lines to the ISA bus which minimizes bus noise.

EISA systems identify hardware using a unique product identification and addressing system. A configuration utility (supplied with the system) uses the product identifiers to simplify expansion board installations.

ISA and EISA expansion boards can use the same expansion slot, even though they have different connector designs. *Keyed* EISA connectors prevent ISA boards from entering areas where they could connect to EISA signals. However, EISA expansion boards can pass these keys and connect to the EISA contacts.

EISA DMA Transfers

Some devices can transfer data directly to and from memory without help from the CPU. This ability, called DMA (direct memory access), frees the CPU for other tasks. DMA transfers are an important part of normal operation and can increase performance under the EISA bus design.

Using EISA, four types of DMA transfers are possible:

- **ISA-Compatible.** The default transfer type, compatible with the DMA devices used in ISA computers.
- **Type A.** Allows ISA-type transfers at higher performance than the ISA-Compatible type. It requires special programming and works selectively with some ISA-compatible DMA devices.
- **Type B.** Allows ISA-type transfers at higher performance than Type A. It requires special programming and works selectively with some ISA-compatible DMA devices.
- **Type C (Burst DMA).** The fastest transfer type. It is available only for EISA expansion boards designed for this type of transfer.

The following table defines the four DMA transfer types in terms of EISA bus cycles.

ISA-compatible*	Executes one transfer cycle in eight EISA bus cycles
Type A cycle	Executes one transfer cycle in six EISA bus cycles
Type B cycle	Executes one transfer cycle in four EISA bus cycles
Type C cycle	Executes one transfer cycle in one EISA bus cycle

* Most ISA-compatible DMA devices can transfer data 130% to 200% faster by programming the EISA controller to use Type A and B cycles instead of ISA-compatible cycles. Existing hardware and software can use the EISA controller without modification, so it actually improves compatibility with older systems.

The following table shows the possible bus transfer rates (often referred to as *bus bandwidth*).

DMA Transfer Type	Expansion Board Type	Transfer Rate (MB/second)	DMA Device Type
ISA Compatible	8-bit	1.0	All ISA
	16-bit	2.0	All ISA
Type A	8-bit	1.3	Most ISA
	16-bit	2.6	Most ISA
	32-bit	5.3	EISA Only
Type B	8-bit	2.0	Some ISA
	16-bit	4.0	Some ISA
	32-bit	8.0	EISA Only
Type C (Burst DMA)	8-bit	8.2	EISA Only
	16-bit	16.5	EISA Only
	32-bit	33.0	EISA Only

Automatic System Configuration

EISA systems automatically configure system devices, such as memory, serial ports, parallel ports, video, and expansion boards plugged into the expansion bus.

Expansion board manufacturers include a configuration file (also referred to as a *.cfg* file) with each EISA expansion board and with some ISA hardware. The Computer Configuration Utility (CCU) uses the information contained in the configuration files to set up a conflict-free configuration for the system. The CCU stores the information in the EISA CMOS RAM and saves a backup copy on diskette in an *.sci* file. The system uses the configuration information when you turn the computer on to configure the EISA expansion boards for operation.

The Computer Configuration Utility assists configuring ISA expansion boards that provide a *.cfg* file. The CCU uses the information from the ISA configuration file to determine the correct DIP switch settings, jumper settings, and I/O port initializations for ISA expansion boards. The CCU then indicates to the installer how the switches and jumpers on the ISA board should be set.

Configuration Filenames

EISA uses a product identifier for systems and expansion boards during the configuration and initialization sequence. The identifier of each product is selected by the product manufacturer.

The filename of an EISA or ISA configuration file consists of an exclamation point followed by the product ID and a filename extension. For example, an expansion board with a product ID of ABC1234 has a configuration file named *!abc1234.cfg*.

If the Computer Configuration Utility finds expansion boards or devices with duplicate IDs, it replaces the exclamation point in the filename with a number. The CCU numbers the configuration files sequentially. For example, if two expansion boards with the ID ABC1234 are installed in the same system, the CCU renames the files when copying them to the Configuration Diskette. It copies the first configuration file detected to *!abc1234.cfg* and the second one detected to *1abc1234.cfg*. (A third file with the same ID would be renamed to *2abc1234.cfg*.)

Device numbers

EISA supports up to 64 devices. A **physical device** resides in an actual slot in the computer. Physical devices are referenced by their slot number. An **embedded device** is a device that has been integrated on the system board. Embedded devices are addressed as additional EISA devices. The device (slot) number for embedded devices begins with the next number after the last physical device number used. All other embedded devices are numbered sequentially afterwards. A **virtual device** is generally a software driver that may need system resources, but does not actually exist as a physical entity. Virtual devices are numbered sequentially after the last embedded device, but must be addressed as slot 16 through 64.

Error Handling During Slot Initialization

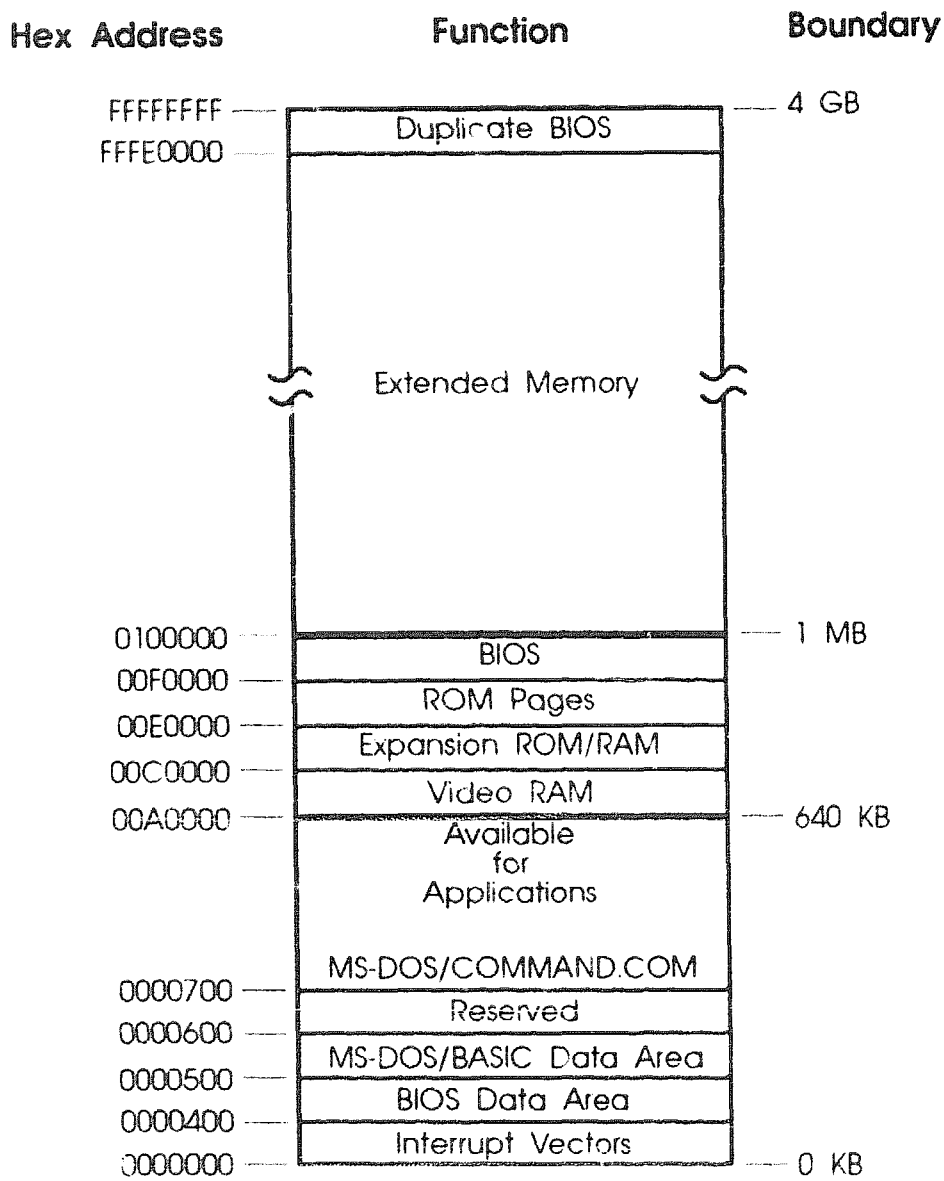
If any of the following errors occur during the startup routine, an error is displayed and initialization continues with the next slot:

- an expansion board indicates a not-ready condition when the board ID is read. The startup routine pauses and then tries again to read the ID. If the second attempt fails, an error message is displayed.
- the board ID does not match the setup contents of the CMOS RAM.
- CMOS RAM indicates the presence of an EISA board ID but no matching board is found in the system.
- a slot is tagged *not readable* in CMOS RAM but a valid ID is read from the slot.
- CMOS RAM indicates that a slot is empty but a valid ID is read from the slot.
- CMOS RAM information does not match the information read during initialization.

Theory of Operation

This section provides information about the basic operation of the components in the system and their interactions.

System Memory Map



System I/O Map

The following tables describe the I/O space of the DECpc 433T. Any addresses not listed may be considered undefined.

EISA/ISA System Board (0000-00FF)	
Hex Range	**Device**
0000-000F	DMA Controller 1
0020-0021	Interrupt Controller 1
0040-0043	Timer 1
0048-004B	Timer 2
0060	Keyboard Data Port
0061	NMI Control/Status Port
0064	Keyboard Status Port
0068	"Turbo" LED Port
0070	NMI Mask Port
0071	Real-Time Clock
0080-008F	DMA Page Registers
0092	Gate A20 Control
00A0-00A1	Interrupt Controller 2
00C0-00DF	DMA Controller 2
00F0-00FF	Numeric Processor Extension (i486 internal)

ISA Expansion Boards (0100-03FF)	
Hex Range	**Device**
0170-017F	Hard Drive Port 2
01F0-01FF	Hard Drive Port 1
0200-0207	Game I/O
0240-0241	LCD Panel
0242(bit 0)	Scroll button
0278-027F	LPT3 (Parallel Port)
02E8-02EF	COM4
02F8-02FF	COM2 (Serial Port 2)
0300-031F	Prototype Card
0350-0352	SCSI Host Adapter (ASC mode only)
0370-0377	Diskette Drive Port 2
0378-037F	LPT2 (Parallel Port)
0380-038F	SDLC, Bisynchronous 2
03A0-03AF	Bisynchronous 1
03B0-03BB	Monochrome display adapter
03BC-03BF	LPT1 (Parallel Port)
03C0-03CF	EGA adapter
03D0-03DF	CGA adapter
03E8-03EF	COM3
03F0-03F7	Diskette Drive Port 1
03F8-03FF	COM1 (Serial Port 1)

EISA System Board Controllers (0400-04FF)	
Hex Range	**Device**
0401-040F	Extended DMA ch. 0-3
0461-0462	Extended NMI and reset control
0464-0465	EISA Bus Master
0481-04CE	Extended DMA ch. 4-7
04D0	Interrupt controller 1 edge/level control
04D1	Interrupt controller 2 edge/level control
04D4-04D6	DMA controller 2 chaining mode
04E0-04EF	DMA controller 1 Stop registers
04F0-04FF	DMA controller 2 Stop registers

EISA System Board (0800-08FF,0C00-0CFF)	
Hex Range	**Device**
0800-08FF	EISA Extended CMOS RAM
0C00-0CFF	System Board
0C02	FC0000 relocation control
0C03	External cache control

Any I/O address that contains a 1 in either bit 8 or bit 9 or a 1 in both bit 8 and bit 9 is an alias for the ISA expansion address range 0100-03FF. The following table lists the aliases of 0100-03FF.

ISA expansion address
Aliases for 0100-03FF
0500-07FF 0900-0BFF 0D00-0FFF
1100-13FF 1500-17FF 1900-1BFF 1D00-1FFF
• • •
*x100-x3FF x500-x7FF x900-xBFF xD00-xFFF

* 'x' signifies any hex digit from 0 to F.

EISA expansion cards use the slot-specific addresses listed in the following table.

EISA Slot-specific addresses	
Hex Range	**Reserved for:**
1000-10FF 1400-14FF 1800-18FF 1C00-1CFF	Slot 1 Slot 1 Slot 1 Slot 1
2000-20FF 2400-24FF 2800-28FF 2C00-2CFF	Slot 2 Slot 2 Slot 2 Slot 2
• • •	• • •
*0z000-0z0FF 0z400-0z4FF 0z800-0z8FF 0zC00-0zCFF	Slot z Slot z Slot z Slot z

* 'z' can be any hex digit from 1 to F.
However, only 1 to 8 are defined for this system.

Example: The EISA SCSI host adapter occupies slot 2 on the main logic board. The I/O port for the EISA SCSI host adapter is therefore 02C80-02CFF. (Although in ASC mode it also uses addresses 0350-0352.)

Slot-specific addresses 0zC80 through 0zC83 are reserved for the product ID. Address 0zC84 is reserved for control bits. All other addresses are available to the EISA expansion board for configuration registers and general I/O.

Direct Memory Access (DMA)

The system supports seven DMA channels. The ISP contains the equivalent of two 8237A-5 DMA Controller chips, with four channels for each controller. The DMA channels are assigned as follows:

Controller 1	Controller 2
Ch 0 - Spare Ch 1 - SDLC or Spare Ch 2 - Diskette Ch 3 - Spare	Ch 4 - Cascade for Ctlr 1 Ch 5 - Spare Ch 6 - Spare Ch 7 - Spare

DMA Channels

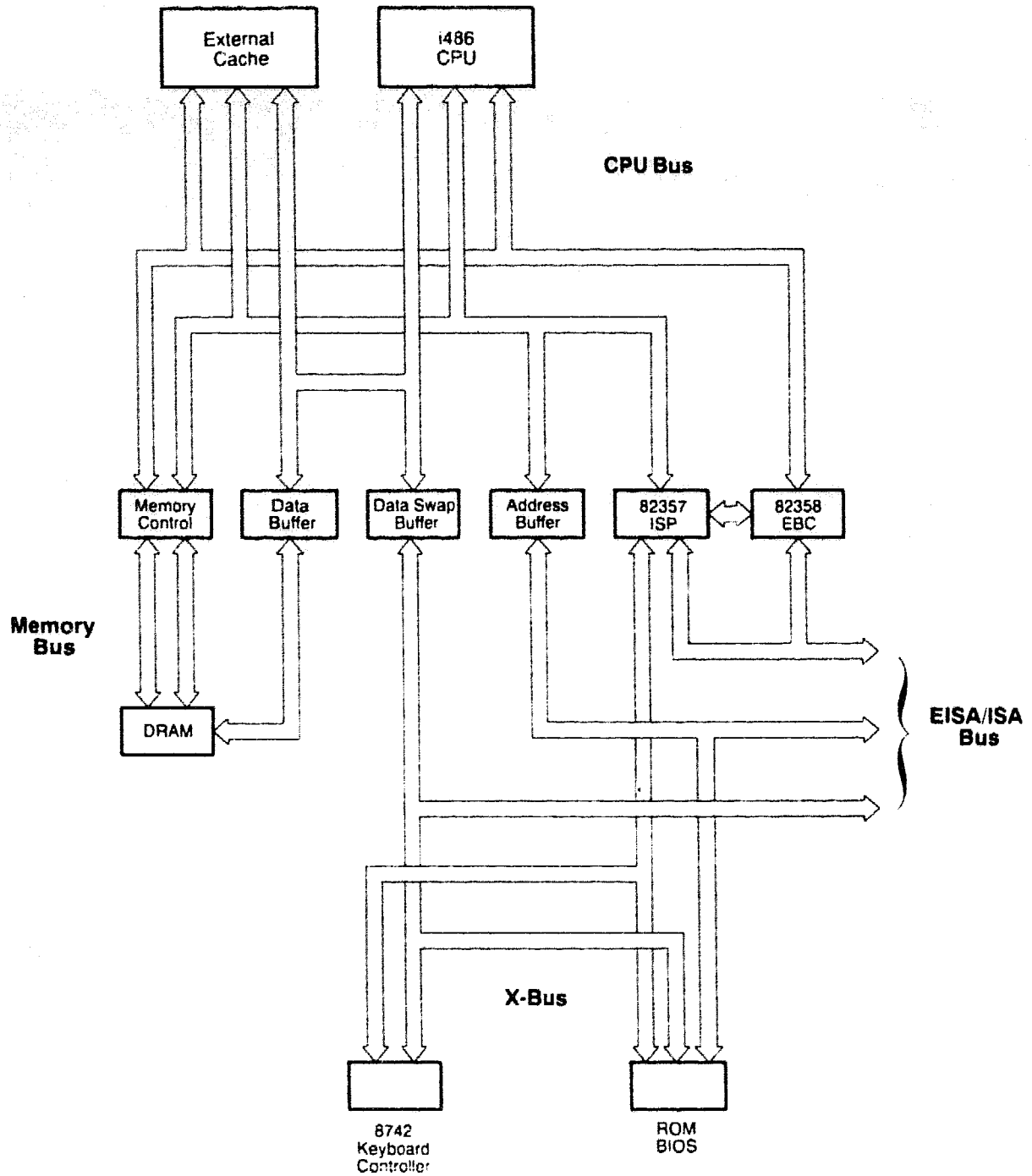
IRQ Assignments

The following table lists the default interrupt request assignments for the DECpc 433T. Interrupt requests from controller 2 are transferred to interrupt 2 on controller 1.

CTLR1	CTLR2	Function
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR2
	IRQ 8	Real-time Clock
	IRQ 9	Software redirected to IRQ 2
	IRQ 10	EISA/ISA bus
	IRQ 11	EISA/ISA bus
	IRQ 12	EISA/ISA bus
	IRQ 13	Coprocessor
	IRQ 14	EISA SCSI host adapter
	IRQ 15	EISA/ISA bus
IRQ 3		COM2
IRQ 4		COM1
IRQ 5		EISA/ISA bus
IRQ 6		Diskette Controller
IRQ 7		Parallel Port

IRQ Assignments

System Block Diagram



Components on the Main Logic Board

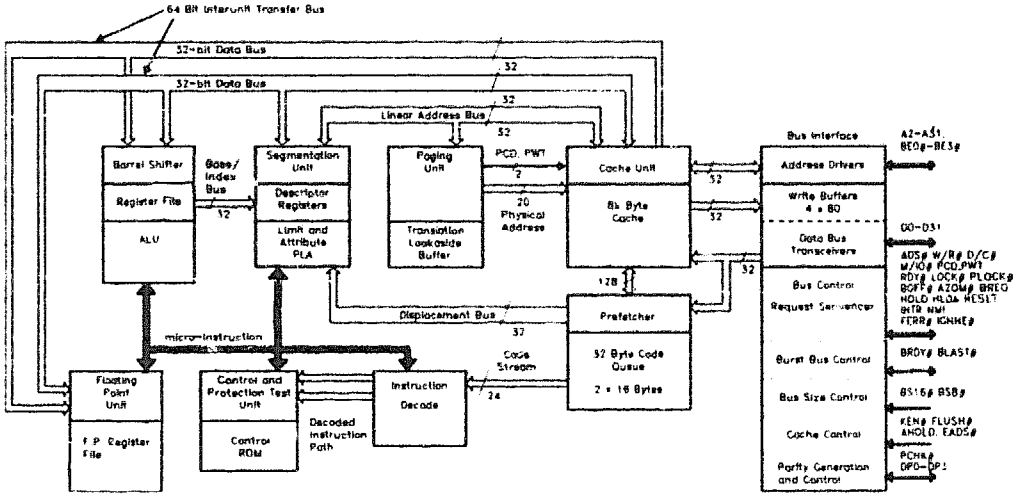
This section provides a brief description of the logical components of the DECpc 433T. If you need more information than this section supplies, refer to the documents cited at the beginning of the manual.

The following components on the main logic board are included in this section:

- Intel i486 Microprocessor
- Weitek 4167 Math Coprocessor (Optional)
- Intel 82358 EISA Bus Controller
- Intel 82357 Integrated System Peripheral (ISP)
- Memory Controller
- 8742 Keyboard Controller
- BIOS ROM

i486 Processor

The i486 processor is an advanced CPU chip that is compatible with previous members of the Intel 80x86 family of microprocessors. Designed for applications needing very high performance, the i486 features discrete 32-bit data and address busses. The i486 CPU is optimized for multi-tasking systems. Cache memory, floating point hardware, and memory management functions are built into the i486. The internal pipelined architecture of the i486 increases the effective speed of instruction execution by overlapping fetch and execution cycles.



Functional Units within the i486

The **Bus Interface Unit** is the microprocessor's link to the local CPU bus. It contains address and data drivers/ transceivers and the bus control logic.

The Prefetcher and the Code Queue allow the i486 to fetch pending instructions when the bus is idle. The **Instruction Unit** decodes the instruction opcodes. The **Control/ Protection Test Unit** verifies the privilege level of the instructions. After decoding and verification, instructions are passed to the Execution Unit.

The **Execution Unit** includes the Arithmetic Logic Unit (ALU) and the Register File. Instructions from the Instruction Decoder are executed within the ALU (or passed on to the FPU). The results are sent to the Memory Management Unit or to the Bus Interface Unit via the cache.

The **Memory Management Unit** (MMU) consists of the Segmentation Unit and the Paging Unit. The MMU handles the addressing duties of the microprocessor. The Paging Unit controls memory paging (hardware based) while the Segmentation Unit handles indexed memory addressing (software based).

The **Floating Point Unit** (FPU) extends the numeric processing power of the ALU by supporting more precise data types. In addition, the FPU adds transcendental functions to the instruction set of the i486. The FPU is, effectively, a 387DX built into the CPU chip. The FPU has the same registers and command set as the 387DX.

The **Cache Unit** is an on board 8KB unified code/data cache with complementary control logic. The cache provides a highly efficient interface between the Bus Interface Unit and other internal blocks of the i486. The cache in the i486 is 4-way set-associative and is transparent to application software.

4167 Numeric Processor (Optional)

The i486 processor in the DECpc features a floating point unit that enhances the numeric processing power of the DECpc. If additional numeric processing is required, the Weitek 4167 Abacus Math Coprocessor can be added to the DECpc.

The Weitek 4167 supplements the floating point math performance for "Weitek-aware" applications. This chip independently executes mathematical calculations, allowing the i486 to perform other tasks.

NOTE: The math coprocessor speed must match the CPU speed (33 MHz).

82358 EISA Bus Controller (EBC)

The 82358 EBC provides the state machine interface for the host CPU bus, the EISA bus, and the ISA bus. The EISA Bus Controller eliminates problems caused by the diversity in data widths and transfer types. The EBC adapts accesses from the host CPU or from a 32- or 16-bit EISA master to any slave (EISA or ISA). Through a process called *cycle translation*, the EBC translates the master protocol to the slave protocol on a cycle-by-cycle basis. The 82358 also supports the assembly/disassembly of data bytes on the busses. When the EBC encounters incompatible master/slave bus sizes, it will run multiple cycles to route bytes to the appropriate byte lane(s).

The EBC also features RESET control logic which coordinates system resets for the CPU and the ISP. Clock generation logic in the EBC synchronizes the host CPU bus (33 MHz) and the EISA bus. The clock generation logic also provides a clock for the keyboard processor. On-board I/O recovery logic inserts delays in back-to-back ISA I/O cycles. The delays allow slower ISA devices to recover before receiving another access. Finally, the EBC has slot support logic that coordinates the address latch enable signals (and timing) for the different slot connectors (ISA and EISA).

82357 Integrated System Peripheral (ISP)

The ISP works very closely with the 82358 EBC chip to provide most of the EISA-specific system functions. The two chips work in tandem to facilitate the CPU/System bus interface.

The ISP contains the DMA controller, the interrupt controller, five counter/timers, and the refresh address generation logic. The interrupt controller in the ISP provides edge- or level-triggered interrupt support on a channel-by-channel basis. The ISP also provides the arbitration logic that allows bus sharing among the CPU, EISA bus masters, and DMA devices.

8742 Keyboard Controller

The keyboard controller is a single-chip microcontroller (Intel 8742) that is programmed to be IBM PC/AT-compatible. The controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer.

BIOS ROM Subsystem

The system BIOS (Basic Input/Output System) functions as the low-level interface for hardware I/O. The BIOS provides a device independent set of routines which ensures compatibility with the EISA specification. The BIOS consists of two 32K x 8 EPROMs, with the code for even and odd addresses on separate EPROMs. Accessing the BIOS is discussed in *BIOS Services*.

Memory Control Logic

Several PAL's serve as the memory control logic that interfaces the CPU address bus and the DRAM array. These PAL's control the address to the DRAMs for memory read/writes and generate the addresses for memory refresh cycles. The memory control logic also generates the row and column address strobe signals in the read/write and refresh modes.

Components on the Multi-Function Adapter

The multi-function board contains a dual diskette drive controller, 2 serial ports, 1 parallel port and the LCD interface.

The following components on the multi-function adapter are included in this section:

- WD37C65 Diskette Drive Controller
- 16C452 Serial/Parallel Interface
- LCD control logic

WD37C65 Diskette Drive Controller

The diskette drive controller resides on the multi-function board and is tied to the ISA data bus. The Western Digital WD37C65 integrated system provides all the logic necessary for complete diskette drive control. It supports up to two diskette drives through a daisy-chained ribbon cable.

WD16C452 Serial/Parallel Interface

The Western Digital WD16C452 Dual Asynchronous Communications Element is compatible with the IBM PC/AT. The serial portion of the chip supports two EIA RS-232C standard serial ports. The serial ports are accessed though two 9-pin male D-shell connectors located under the top cover of the unit for external chassis access. The parallel port is a fully

Centronics compatible interface and is accessible via a 25-pin female D-shell connector also under the top cover of the unit.

LCD control logic

The multi-function adapter has programmed logic that decodes and generates the signals necessary to control the LCD panel.

EISA SCSI Host Adapter

The DECpc includes an EISA bus to SCSI host bus adapter. This adapter provides the interface for SCSI devices and the EISA bus. The EISA SCSI Host adapter can support up to seven SCSI devices. Refer to "*EISA/SCSI Host Adapter Reference*" at the back of this manual for more information.

System Configuration

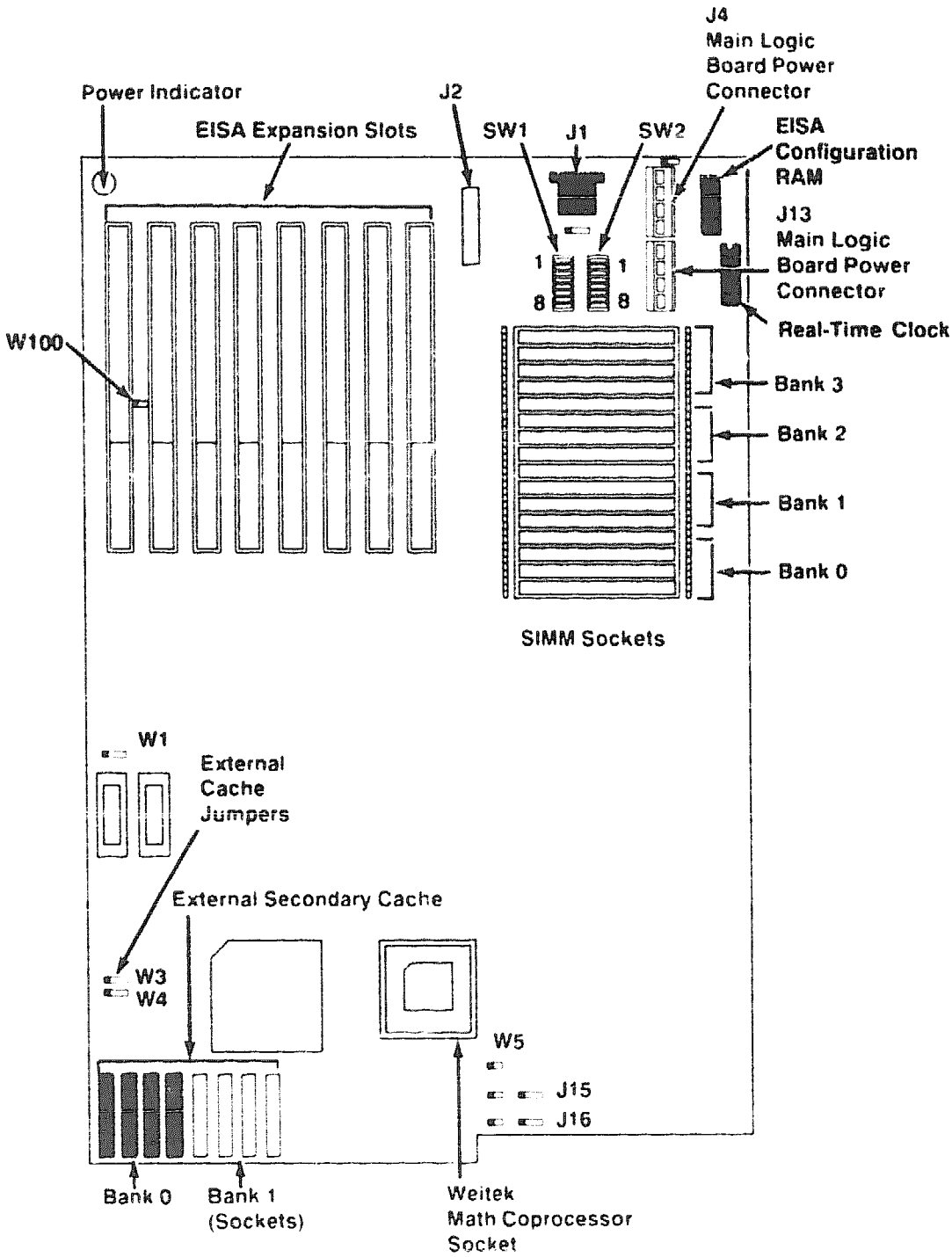
This section describes the standard configuration of the system as shipped from the factory and explains how to change configuration settings when necessary.

If you add internal or external options to the system, it may be necessary to change some of the factory default configuration settings. You may also want to change the configuration settings to suit your personal preferences or to meet certain application requirements.

Jumpers and Switches

The following pages define the jumpers and switches on the main logic board, the multi-function adapter, and the EISA SCSI Host adapter. Many of the default settings are critical to the system's operation. Exercise caution when changing any jumper or switch setting.

Main Logic Board Diagram



Main Logic Board Jumpers

Jumper	Description	Setting
W3	64KB or 128KB external cache 256KB external cache	1-2* 2-3
W4	64KB external cache 128KB or 256KB external cache	1-2 2-3*
W100	Slot 8 EISA Slot 8 ISA	1-2* 2-3
* Indicates factory default setting.		

Main Logic Board Switch Settings

DIP Switch 1 (SW1)		
Switch	**Description**	**Setting**
1	Reserved for factory use	ON*
2	Disable on-board BIOS Enable on-board BIOS	ON OFF*
3	128KB or 256KB external cache 64KB external cache	ON* OFF
4	25MHz system 33MHz system	ON OFF*
5	Reserved	OFF*
6	Reserved	OFF*
7	CGA/EGA/VGA Monochrome	ON* OFF
8	128KB external cache 64KB or 256KB external cache	ON* OFF
* Indicates factory default setting.		

Main Logic Board Switch Settings (continued)

DIP Switch 2 (SW2)		
Switch	**Description**	**Setting**
1	Memory configuration settings (see note below)	ON*
2	Memory configuration settings	ON*
3	Memory configuration settings	ON*
4	Memory configuration settings	ON*
5	Memory configuration settings	ON*
6	Video BIOS non-cacheable Video BIOS cacheable	ON OFF*
7	13MB–15MB cacheable 13MB–15MB non-cacheable	ON* OFF
8	Reserved	OFF*
* Indicates factory default setting.		
Note: Switches 1-5 are set according to the memory configuration. (4MB is default.) Refer to the following chart for the memory configuration switch settings.		

Memory Configurations

The standard configuration includes four 70 ns, 1M X 9 SIMMs in Bank 0 of the SIMM sockets on the main logic board.

When you install new memory, run the *Setup Computer* option from the Computer Configuration Utility. From the Setup Computer screen, you can verify that the system recognizes the new memory.

The following chart defines all valid system memory configurations.

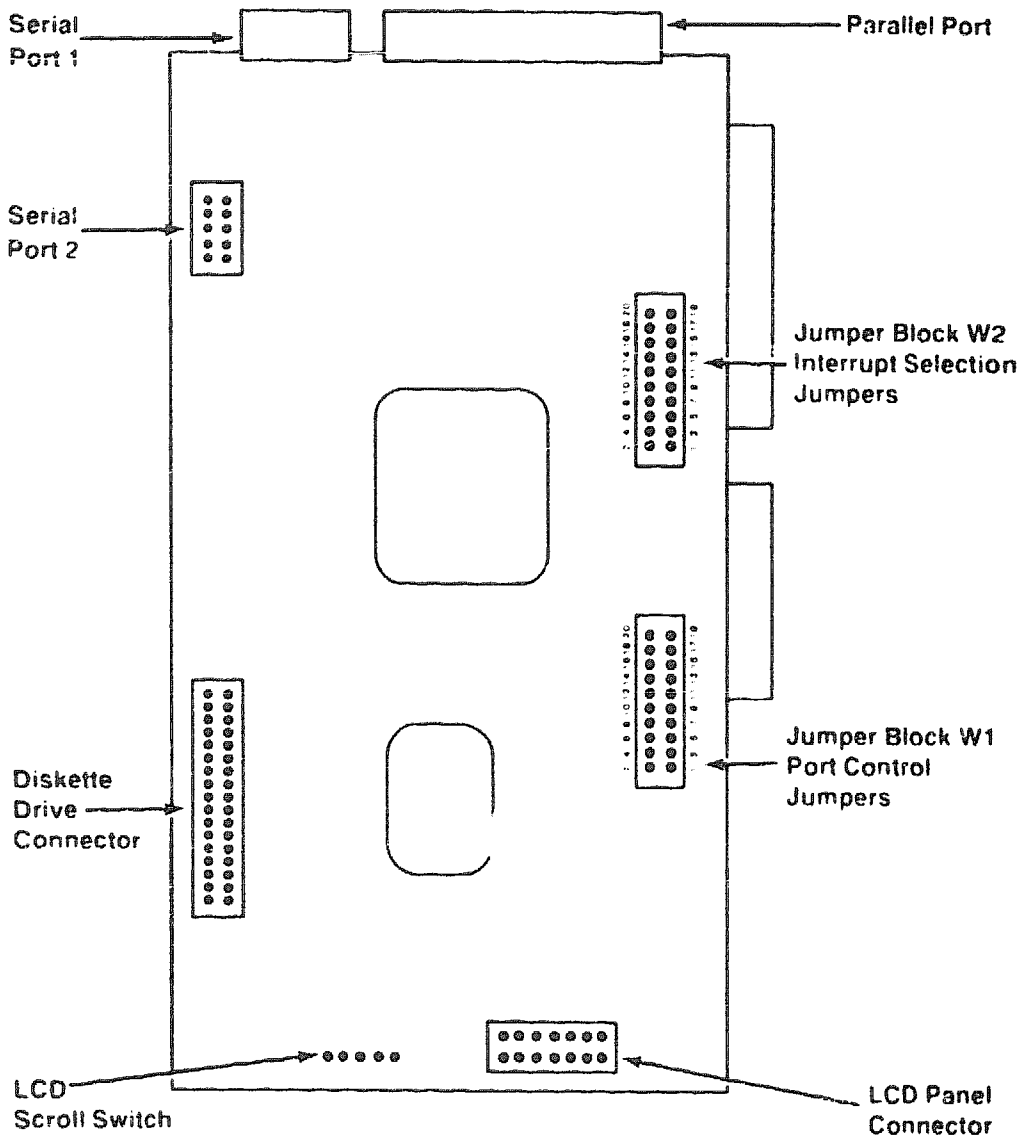
Memory Configuration Settings (SW2 switches 1-5)

	SIMM Size								
Total (MB)	Bank 0	1	2	3	Switch 1	2	3	4	5
4*	1MB	–	–	–	ON*	ON*	ON*	ON*	ON*
8	1MB	1MB	–	–	OFF	ON	ON	ON	ON
12	1MB	1MB	1MB	–	ON	OFF	ON	ON	ON
16	1MB	1MB	1MB	1MB	OFF	OFF	ON	ON	OFF
16	4MB	–	–	–	ON	ON	OFF	ON	OFF
20	1MB	4MB	–	–	ON	ON	OFF	OFF	OFF
24	1MB	1MB	4MB	–	ON	OFF	ON	OFF	OFF
28	1MB	1MB	1MB	4MB	OFF	ON	ON	OFF	OFF
32	4MB	4MB	–	–	OFF	ON	OFF	ON	OFF
36	1MB	4MB	4MB	–	ON	OFF	OFF	OFF	OFF
40	1MB	1MB	4MB	4MB	OFF	OFF	ON	OFF	OFF
48	4MB	4MB	4MB	–	ON	OFF	OFF	ON	OFF
52	1MB	4MB	4MB	4MB	OFF	OFF	OFF	OFF	OFF
64	4MB	4MB	4MB	4MB	OFF	OFF	OFF	ON	OFF

* Indicates factory default setting.

Note: The switches on DIP switch SW2 ***must*** correspond to the memory configuration on the main logic board.

Multi-Function I/O Adapter Diagram



Multi-Function I/O Adapter Jumper Settings

Port Control Jumper Block (W1)		
Function	**Pins**	**Setting**
Reserved for factory use	1,2	Not Installed*
Diskette Controller Primary Port (03F0h) Secondary Port (0370h)	3-4 3,4	Installed* Not Installed
Disable Serial Port 2	5,6 7,8	Not Installed Not Installed
Enable Serial Port 2 as COM4	5,6 7-8	Not Installed Installed
Enable Serial Port 2 as COM3	5-6 7,8	Installed Not Installed
Enable Serial Port 2 as COM2	5-6 7-8	Installed* Installed*
Disable Serial Port 1	9,10 11,12	Not Installed Not Installed
Enable Serial Port 1 as COM3	9,10 11-12	Not Installed Installed
Enable Serial Port 1 as COM2	9-10 11,12	Installed Not Installed
Enable Serial Port 1 as COM1	9-10 11-12	Installed* Installed*
* Indicates factory default setting.		

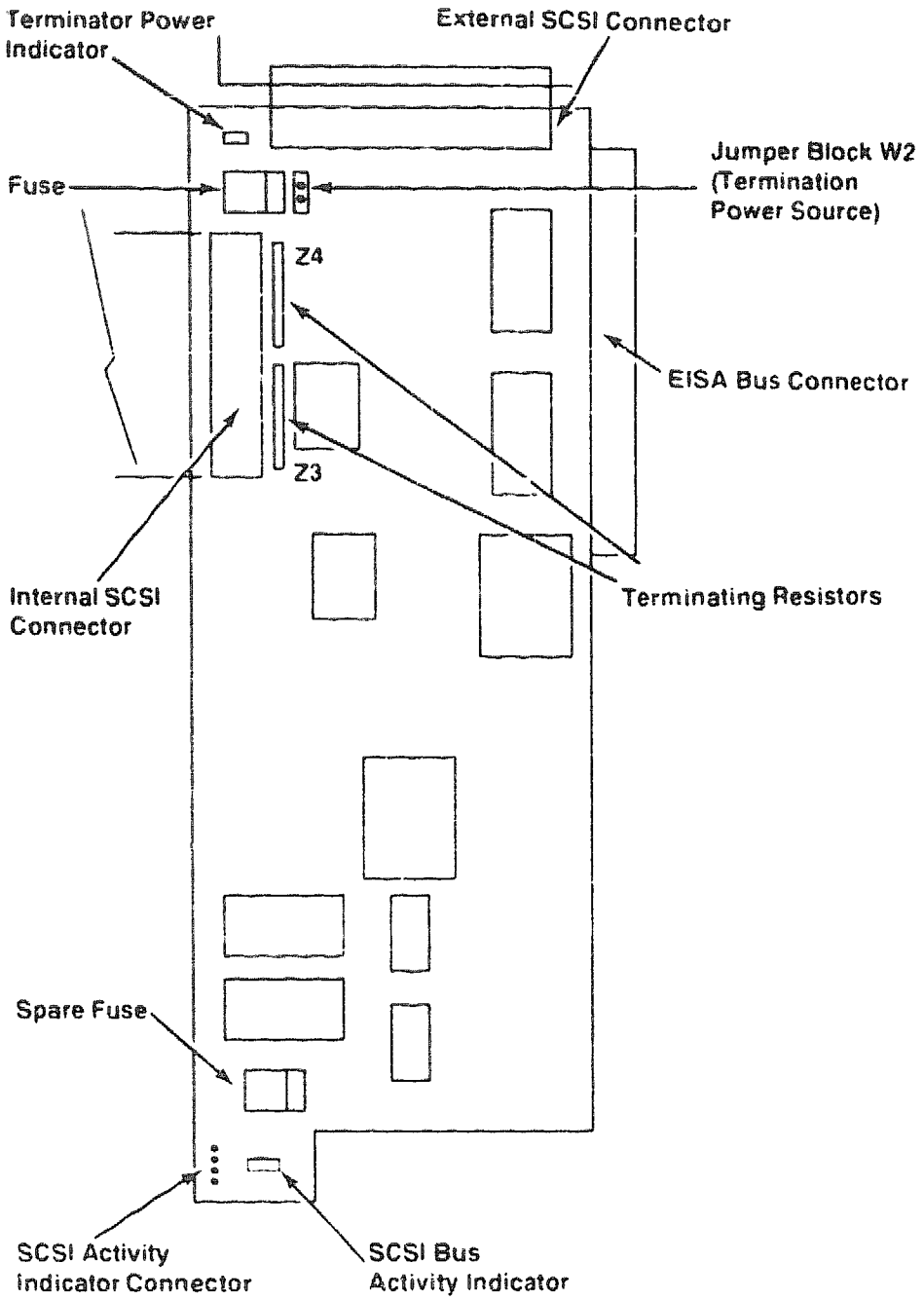
Multi-Function I/O Adapter Jumper Settings (continued)

Port Control Jumper Block (W1)		
Function	**Pins**	**Setting**
Disable Parallel Port	13,14 15,16	Not Installed Not Installed
Enable Parallel Port as LPT3	13,14 15-16	Not Installed Installed
Enable Parallel Port as LPT2	13-14 15,16	Installed Not Installed
Enable Parallel Port as LPT1	13-14 15-16	Installed* Installed*
Reserved for factory use	17,18 19,20	Not Installed Not Installed
Enable Bidirectional Parallel Port	17,18 19-20	Not Installed* Installed*
Enable Parallel Port as Output Only	17-18 19,20	Installed Not Installed
Reserved for factory use	17-18 19-20	Installed Installed
* Indicates factory default setting.		

Multi-Function I/O Adapter Jumper Settings (continued)

Interrupt Selection Jumper Block (W2)			
Port	**Interrupt**	**Pins**	**Setting**
Serial Port 1	IRQ3 IRQ4 IRQ10 IRQ11	1-2 3-4 5-6 7-8	Installed Installed* Installed Installed
Serial Port 2	IRQ3 IRQ4 IRQ10 IRQ11	9-10 11-12 13-14 15-16	Installed* Installed Installed Installed
Parallel Port	IRQ5 IRQ7	17-18 19-20	Installed Installed*
* Indicates factory default setting.			

EISA SCSI Host Adapter Diagram



EISA SCSI Host Adapter Jumper (W2)

Jumper	Description	Setting
W2	SCSI bus termination power is provided by adapter	Installed*
	SCSI bus termination power is provided by SCSI device	Not Installed
* Indicates factory default setting.		

All of the configuration settings on the EISA SCSI host adapter are software selectable using the Computer Configuration Utility. The following table lists the configurable settings and factory defaults.

Function	Valid Settings
BIOS Address (16KB window)	C0000 C4000 C8000 *CC000 D0000 D4000 D8000 DC000
Interrupt Select	IRQ10 IRQ12 *IRQ14 IRQ15
I/O Port DACB mode ASC mode	 *2C80-2CFF (2 is the slot number) 350-352
* Indicates factory default setting.	

Programmable configuration settings

The menu-driven System Configuration diskette (shipped with the system) must be used when options are added to the system. Use the System Configuration Diskette that supports the language you choose.

When the System Configuration Diskette is used as a boot disk, an option menu displays. From this menu, select the desired utility:

```
Learn about configuring your computer
Copy Diskette
Setup Computer
Configure Computer
Set power-on password
Set front panel message.
```

The Computer Configuration Utility

The CMOS RAM contains information about the system configuration that the BIOS uses at power-up. The configuration software included with the system can modify the contents of the CMOS RAM, if directed by the user. The Computer Configuration Utility permits access to the EISA system board configuration registers.

> **NOTE:** Make a copy of the System Configuration Diskette before running the Computer Configuration Utility.

The Computer Configuration Utility should be run whenever the system configuration is changed. Refer to the *DECpc 433T User's Guide* for more information on running the Computer Configuration Utility.

The Setup Computer Utility

The Setup Utility on the System Configuration diskette allows the user to:

Set the date and time (Real Time Clock)
Identify hard drive type(s) from a drive table
Identify the type of video adapter installed
Specify the number and type of diskette drive(s) installed
Specify cache options
Specify the amount of base memory and extended memory installed

Refer to the *DECpc 433T User's Guide* for more information on running the Setup Utility.

Invalid configurations

This section describes any configurations that may cause the system to function improperly or not at all.

8514/A-Compatible Video Adapter

The 8514/A-compatible video adapter ***must*** be installed in Slot 2 to function properly.

Invalid memory configurations

The DECpc 433T requires 70ns (or faster) SIMMs.

1MB and 4MB SIMMs may be used (in separate banks) on the main logic board. Refer to "***Memory Configurations***" for the supported memory configurations.

Invalid device combinations (hard disks)

SCSI drives are recommended.

Do not plug an IDE drive into a SCSI Port. Do not plug a SCSI drive into an IDE port.

IDE, ESDI, and ST-506 (MFM & RLL) drives cannot be used in the same system.

Non-supported hardware peripherals

The DECpc 433T will support any peripheral card that conforms to the EISA specification, Version 3.11. The computer will also support any DEC-certified ISA peripheral (IBM PC/AT-compatible).

Internal Interface Connectors

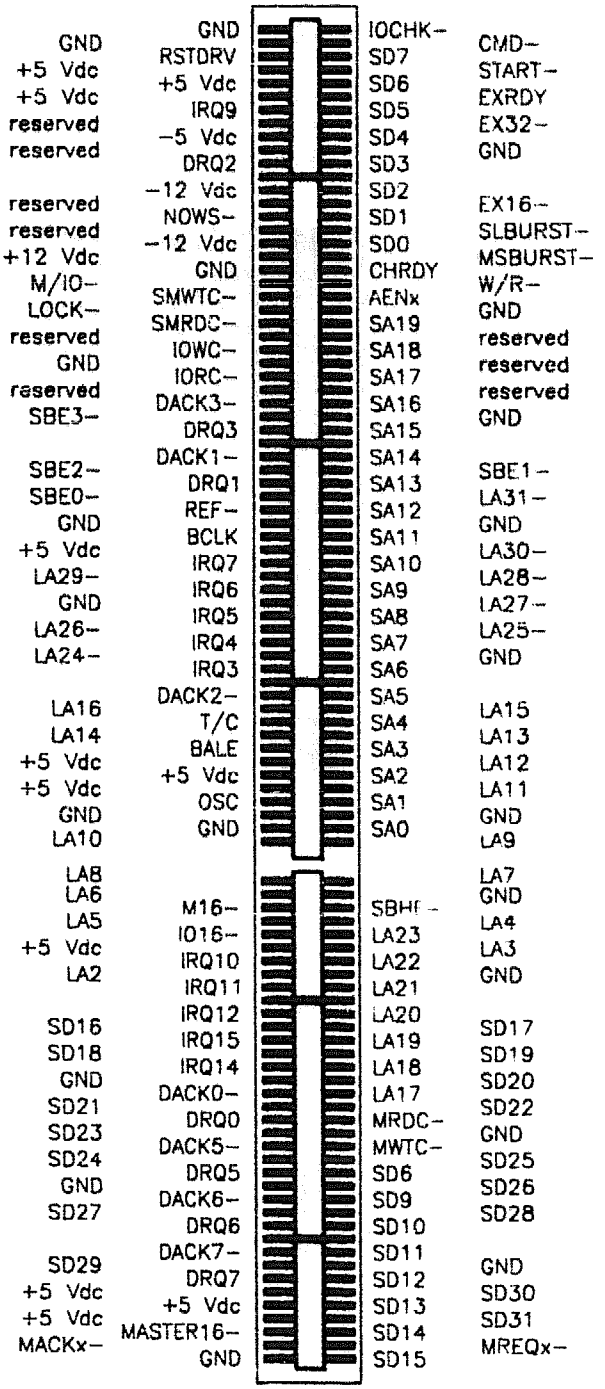
This section describes the pin assignments for the interface connectors on the system that are only accessible by opening the system case.

EISA 32-bit expansion slots

This section identifies the signals and interface requirements for the EISA expansion slots. There are eight 32-bit EISA expansion slots in the system. Six slots support bus mastering (Slots 2 through 7); two do not support bus mastering (Slots 1 and 8).

Each slot has a 188-pin connector.

The following are signal descriptions for the EISA expansion bus:



EISA connector pin assignments

Address and data signal group

BE0– through **BE3–**. BE0– through BE3– are byte enable signals that identify the specific bytes addressed in a double-word. BE0– indicates the least significant byte (D0 through D7); BE1– indicates D8 through D15; BE2– indicates D16 through D23; and BE3– indicates the most significant byte (D24 through D31). BE0– through BE3– are active low.

D24 through **D31**. These bidirectional signals are the data bits 24 through 31. These are the highest eight data bits for 32-bit memory and I/O devices.

D16 through **D23**. These bidirectional signals are the data bits 16 through 23.

D8 through **D15**. These bidirectional signals are the data bits 8 through 15. These are the highest eight data bits for 16-bit memory and I/O devices.

D0 through **D7**. These bidirectional signals are the data bits 0 through 7. These are the lowest eight data bus bits for all memory and I/O devices.

LA2 through **LA16**. These signals are used to address memory and I/O devices on the EISA bus. These signals are valid when BALE is high. Because the signals are not latched during microprocessor cycles, they do not stay valid for the entire cycle. LA2 through LA16 are active high.

LA17 through **LA23**. These signals are used to address memory and I/O devices on the EISA and ISA buses. These signals are valid when BALE is high. Because the signals are not latched during microprocessor cycles, they do not stay valid for the entire cycle. LA17 through LA23 are active high.

LA24– through **LA31–**. These signals are used to address memory and I/O devices on the EISA bus. These signals are valid when BALE is high. Because the signals are not latched during microprocessor cycles, they do not stay valid for the entire cycle. LA24– through LA31– are active low; decode logic should be inverted. A high on one of these signals must be interpreted as an address bit of 0. A low must be interpreted as a 1.

SA0 through **SA19**. These 20 address signals are used to address memory and I/O devices on the ISA bus. They are gated on the system bus when the BALE signal is high and are latched on the falling edge of the BALE signal. SA0 through SA19 are active high.

SBHE–. Byte High Enable. This signal indicates to 16-bit devices that they should drive data onto the D8 through D15 data lines. SBHE– is active low.

AENx. AENx is a slot-specific Address Enable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AENx active, the DMA controller has control of the address bus, the data bus, and the read and write command lines. AENx is also used to disable accesses to all other slots during accesses to the specified slot's I/O address range (0x000h-0x0FFh, 0x400h-0x4FFh, 0x800h-0x8FFh, or 0xC00h-0xCFFh). AENx is active high.

Data transfer control signal group

BCLK. BCLK is the bus clock. BCLK has a frequency of 8.25MHz with a normal duty cycle of 50 percent. The BCLK period is sometimes extended for synchronization with the CPU or other system board devices. BCLK should not be used for applications which require a fixed frequency.

MSBURST–. An EISA CPU or bus master asserts MSBURST– to indicate to the slave (typically main memory) that the CPU or bus master can provide burst cycles. MSBURST– is asserted with the LA31 through LA2 address lines for the second and all subsequent cycles of the burst and is sampled on the rising edge of BCLK by the slave.

SLBURST–. A slave (typically main memory) indicates its support of EISA burst cycles by asserting SLBURST–. The slave develops SLBURST– from the LA31 through LA10 address lines and M/IO– and produces SLBURST– regardless of the state of MSBURST–. SLBURST– is sampled on the rising edge of BCLK by the CPU, DMA controller, or bus master.

M/IO–. The CPU or an EISA bus master asserts M/IO– to indicate whether the cycle in progress is a memory cycle (high) or an I/O cycle (low). M/IO– is pipelined from one cycle to the next and is latched by the addressed slave if needed for the whole cycle. M/IO– should be included in all decodes by EISA slaves. M/IO– must not be used in decoding the signals M16– or IO16–.

LOCK–. The CPU or bus master asserts LOCK– to guarantee exclusive memory access during the time LOCK– is asserted. A bus master can also assert LOCK– to guarantee exclusive I/O access during the time LOCK– is asserted. Assertion of LOCK– enables bit test-and-set operations (as used for semaphores) to execute as a unit. The bus lock prevents multiple devices from simultaneously modifying the semaphore bit.

EX32–. An EISA memory or I/O slave asserts EX32– to indicate that it supports 32-bit transfers. A two BCLK cycle is executed when a slave asserts EX32– during a memory access. The slave asserts EX32– after decoding a valid address on the LA31 through LA2 address lines and M/IO–. EX32– should not be latched by the slave. Both 16-bit and 32-bit

EISA bus masters must monitor EX32– at the trailing edge of START– to determine whether the slave supports 32-bit (and 16-bit) EISA transfers (low) or whether the system is performing data size translation (high). If data size translation is being done and the master is a 32-bit master, the system asserts EX32– to indicate completion of the translation.

EX16–. An EISA memory or I/O slave asserts EX16– to indicate that it supports 16-bit transfers. A 16-bit EISA bus master samples EX16– low to confirm a 16-bit EISA slave. An EISA cycle (two BCLKs) is executed when a slave asserts EX16– during a memory access by the system or a 16-bit EISA bus master. The slave asserts EX16– after decoding a valid address on the LA31 through LA2 address lines and M/IO–. EX16– should not be latched by the slave. 16-bit EISA bus masters must monitor EX16– to determine whether the slave supports 16-bit EISA transfers (EX16– low) or whether the system is performing data size translation (EX16– high). If data translation is being done (ISA cycles) and the master is a 16-bit master (indicated by the master asserting MASTER16–), the system asserts EX16– to indicate completion of the translation.

EXRDY. EISA I/O and memory slaves negate EXRDY to request wait state timing. (Each wait state is one BCLK.) The system samples EXRDY on each falling edge of BCLK after it asserts CMD–. The system holds CMD– asserted during the entire period EXRDY is negated and at least 1/2 BCLK after sampling EXRDY asserted. EXRDY must be driven with an open-collector type buffer. (A pull-up resistor provides the asserting drive current.) The EISA slave should negate EXRDY during START– or on the rising edge of BCLK at the end of START– if wait states are to be added. The slave must allow EXRDY to float high synchronously with BCLK falling edge and must not hold EXRDY negated longer that 2.5 microseconds.

START–. The START– signal provides timing control at the start of a cycle. The CPU (or bus master) asserts START– after LA31 through LA2 and M/IO– become valid. After one BCLK cycle time, the CPU negates START– on the rising edge of BCLK. Note: BE3– through BE0– and W/R– might not be valid on the leading edge of START–.

CMD–. CMD– provides timing control within the cycle. The system asserts CMD– on the rising edge of BCLK, simultaneously with the negation of START–. The system holds CMD– asserted until the end of the cycle. The end of the cycle normally is synchronized with the rising edge of BCLK, but in certain cases is asynchronous. A bus master does not drive CMD–.

W/R–. The status signal W/R– identifies an EISA cycle as a write (high) or read (low). W/R– becomes valid after the assertion of START– and before the assertion of CMD–. W/R– remains valid as long as address lines LA31

through LA2 are valid. W/R– is driven from the same edge of BCLK that activates the START– signal.

BALE. BALE is a Buffered Address Latch Enable signal. It is used to latch valid addresses on the bus. BALE is pulled to a high state during DMA cycles, including refresh cycles. BALE is active high.

MRDC–. Memory Read Command. This signal is used to instruct 16-bit ISA memory devices to drive data onto the data bus. The address lines on the bus must be valid for at least one system clock period before MRDC– is asserted. MRDC– is active low.

MWTC–. Memory Write Command. This signal is used to instruct 16-bit ISA memory devices to store data present on the data bus. The address lines on the bus must be valid for at least one system clock period before MWTC– is asserted. MWTC– is active low.

SMWTC–. Memory Write Command. This is a write signal that instructs an ISA memory device to latch the data on the data lines D0 through D7. SMWTC– is active only when the memory address is within the first 1 megabyte range (000000h-0FFFFFh). SMWTC– is active low.

SMRDC–. Memory Read Command. This is a read signal that instructs an ISA memory device to drive its data onto the data lines D0 through D7. SMRTC– is active only when the memory address is within the first 1 megabyte range (000000h-0FFFFFh). SMRDC– is active low.

IOWC–. I/O Write Command. This is a write signal that instructs an ISA I/O device to latch the data on the data lines D0 through D7. IOWC– is active low.

IORC–. I/O Read Command. This is a read signal that instructs an ISA I/O device to drive its data onto the data lines D0 through D7. IORC– is active low.

CHRDY. This signal is used by ISA memory and I/O devices to generate wait states. Any slow device using this line should drive it low (NOT Ready) immediately upon detecting its valid address and a read or write command. This signal should not be held low more than 2.5 microseconds. CHRDY is active high (Ready condition).

NOWS–. This signal is used by 16-bit ISA I/O and memory cards to indicate 0 wait state capability. NOWS– is active low.

M16–. This ISA signal is used to tell the system that a peripheral is capable of 16-bit memory transfers. M16– is active low.

IO16–. This ISA signal is used to tell the system that a peripheral is capable of 16-bit I/O transfers. IO16– is active low.

MREQx–. MREQx is a slot-specific signal used by EISA bus masters to request bus access. The x refers to the slot number. Bus masters requiring use of the bus must assert MREQx– until the system grants bus access by asserting MAKx–. The bus master can begin driving the bus with address and other signals on the falling edge of BCLK when MAKx– is sampled low. When a master completes a transfer, it can release the bus by negating the MREQx– signal. A bus master must wait at least two BCLKs after releasing the bus before re-asserting its MREQx–.

MAKx–. MAKx– is a slot-specific signal that is asserted by the system to grant bus access to an EISA bus master. The x refers to the slot number. The system negates MAKx– after sampling MREQx– negated. The system can also negate MAKx– to indicate to an active bus master that another device has requested the bus. The bus master must negate MREQx– to release the bus within 64 BCLKs (8 microseconds) of sampling MAKx– negated.

Bus arbitration signal group

DRQ1, DRQ2, and **DRQ3**. DMA request lines 1 through 3. DRQ1 has the highest priority and DRQ3 has the lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform 8-bit transfers only. These DRQ lines are active high.

DRQ0, DRQ5 through **DRQ7**. DMA request lines 0 and 5 through 7. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ0 will perform 8-bit transfers, and DRQ5 through DRQ7 will perform 16-bit transfers. These signals are active high.

DACK1–, DACK2–, and **DACK3–**. DMA acknowledge. These lines used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. These signals are active low.

DACK0–, DACK5– through **DACK7–**. These lines are used to acknowledge DRQ0 and DRQ5 through DRQ7. These signals are active low.

T/C. Terminal Count. This signal provides a high pulse when the terminal count for any DMA channel is reached. T/C is active high.

MASTER16–. This signal is used by 16-bit ISA and EISA bus masters to gain control of the bus and by 32-bit EISA bus masters to indicate a 16-bit data size.

An ISA bus master issues a DMA request (DRQ) to a DMA channel and receives a DMA acknowledge (DACK–). In response to DACK–, the ISA bus master asserts MASTER16–, allowing the ISA bus master to control the system data, address, and control buses. The ISA bus master negates MASTER16– when the system board negates DACK–.

A 16-bit EISA bus master asserts MASTER16– in response to MAKx–. The 16-bit EISA bus master negates MASTER16– after completing the last transfer.

A 32-bit EISA bus master can assert MASTER– to disable 32-to-16-bit data size translation. This permits the 32-bit bus master to perform 16-bit Burst cycles to a 16-bit EISA slave.

REFRESH–. This signal is used to indicate a DRAM refresh cycle. REFRESH– is active low.

Utility signal group

OSC. 14.31818 MHz clock (used by some video boards). This signal is not synchronized to any other signals on the bus.

RSTDRV. RSTDRV is used to reset or initialize the expansion logic during power-up, line voltage outage, or when the Reset switch on the front panel is pressed. RSTDRV is active high.

IRQ3 through **IRQ7**, and **IRQ9**. Six maskable interrupt request lines. An interrupt request is generated when an IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IRQ10 through **IRQ12**, **IRQ14**, **IRQ15**. Five additional maskable interrupt request lines. IRQ13 is reserved for the system board.

IOCHCK–. The IOCHCK– signal alerts the system to parity and other non-recoverable errors through a non-maskable interrupt. IOCHCK– is active low.

Diskette drive interface connector

The diskette drive connector is located on the multi-function adapter. The pin assignments for the diskette drive connector are given in the following chart.

Pin	Signal	Pin	Signal
1	GND	2	NDEN–
3	GND	4	N/C
5	N/C	6	N/C
7	GND	8	IDX–
9	GND	10	MOTEN0–
11	GND	12	DS1–
13	GND	14	DS0–
15	GND	16	MOTEN1–
17	GND	18	DIR–
19	GND	20	STEP–
21	GND	22	WD–
23	GND	24	WE–
25	GND	26	TRK00–
27	GND	28	WP–
29	GND	30	RDD–
31	GND	32	HS–
33	GND	34	DCHNG

Diskette drive interface pin assignments

External Interface Connectors

This section describes the pin assignments for connectors that are accessible under the top cover of the system unit.

Keyboard connector

The keyboard connector uses a standard 6-pin miniature DIN connector. The pin assignments are listed in the following table.

Pin	Signal Name
1	Data
2	N/C
3	GND
4	+5Vdc
5	Clock
6	N/C

Keyboard connector pin assignments

Serial port connectors

The following are signal definitions for the 9-pin Serial port connectors.

Pin	Signal	Function
1	DCD	Data carrier detect
2	RD	Receive data
3	TD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal Ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator

Serial port pin assignments

Parallel port connector

The following are signal definitions for the 25-pin Parallel port connector.

Pin	Signal	Function
1	STB–	Strobe
2	PD0	Data bit 0
3	PD1	Data bit 1
4	PD2	Data bit 2
5	PD3	Data bit 3
6	PD4	Data bit 4
7	PD5	Data bit 5
8	PD6	Data bit 6
9	PD7	Data bit 7
10	PRACK–	Acknowledge
11	BUSY	Busy
12	PE	Paper End
13	SLCT	Select
14	AFD–	Auto Feed
15	ERR–	Error
16	INIT–	Initialize
17	SLIN–	Select Input
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

Parallel port pin assignments

Device programming

This section includes information about programming logic components in the DECpc 433T.

i486 Microprocessor

It is beyond the scope of this manual to describe i486 programming. Detailed information about programming the i486 is available from Intel Corporation. This section provides a brief overview of the i486 operating modes and registers.

Modes of Operation

The microprocessor operates in two modes - 8086 Real Address Mode (**Real Mode**) and Protected Virtual Address Mode (**Protected Mode**). To maintain compatibility with the 8086, the processor "wakes up" (i.e. at power-up or reset) in Real Mode. In Real Mode, the i486 functions as a high-speed 8086 microprocessor. In this mode, the processor can address only 1MB of memory, which must be linear.

Protected Mode provides access to the sophisticated memory management paging and privilege capabilities of the microprocessor. In Protected Mode, the i486 can map 64 Terabytes of virtual memory into 4 GB of physical memory. This means that programs have access to an enormous amount of memory (64 TB) by letting the microprocessor swap unused code or data to disk. Protected Mode also supports multiple task protection through four privilege levels. The task protection feature enables the i486 to perform **Virtual 8086 Mode** tasks.

In Virtual 8086 Mode, the i486 allows the simultaneous execution of 8086 operating systems, 8086 applications, a 386 Protected Mode operating system, and 80286/386/486 Protected Mode applications. In other words, the i486 can set-up multiple "virtual 8086 machines" with a shared 8086 operating system while running under a 386 Protected Mode operating system. Each virtual machine is simply a Protected Mode task.

In Virtual 8086 Mode, the paging unit of the i486 can break up the 8086 1MB contiguous linear address space into pages (up to 256) and map each page into free areas within the physical address space. In addition, each Virtual 8086 Mode task can use a different mapping scheme to map pages specific

to that task. The paging hardware also allows the sharing of 8086 operating system code between 8086 applications.

i486 Registers

The i486 provides 47 registers for data manipulation, system control and configuration, and instruction execution. These registers are described in the following sections.

Base Architecture Registers

The base architecture registers are accessible to applications programs at any privilege level. The base architecture registers consist of eight general purpose registers, six segment registers and 2 flag registers. The contents of these registers are task specific and are automatically loaded with a new context upon a task switch operation.

General Purpose Registers

Register Name	Size (in bits)
EAX (AX,AH,AL)	32 (16,8,8)
EBX (BX,BH,BL)	32 (16,8,8)
ECX (CX,CH,CL)	32 (16,8,8)
EDX (DX,DH,DL)	32 (16,8,8)
ESI (Source Index)	32 (16)
EDI (Destination Index)	32 (16)
EBP (Base Pointer)	32 (16)
ESP (Stack Pointer)	32 (16)

Segment Registers

Register Name	Size (in bits)
CS (Code Segment)	16
SS (Stack Segment)	16
DS (Data Segment)	16
ES (Extra Segment)	16
FS (Extra Segment)	16
GS (Extra Segment)	16

Flag Registers

Register Name	Size (in bits)
EFLAGS (Flags)	32 (16)
EIP (Instruction Pointer)	32 (16)

System Level Registers

The systems level registers are only accessible at privilege level 0 (the highest privilege level). The system level registers consist of three control registers and four system address registers. These registers control operation of the on-chip cache, the on-chip floating point unit, and the memory management unit.

Control Registers	
Register Name	**Size (in bits)**
CR0	32
CR2 Page Fault Linear Address	32
CR3 Page Directory Base Register	32

System Address Registers	
Register Name	
GDTR	Global Descriptor Table Register
IDTR	Interrupt Descriptor Table Register
LDTR	Local Descriptor Table Register
TR	Task State Segment Register

Floating Point Registers

The operation of the i486 microprocessor's on-chip floating point unit is exactly the same as the Intel 387DX math coprocessor. The floating point unit (FPU) is stack-oriented with an 80-bit internal architecture. There are eight data registers and five control/status registers within the FPU. The floating point registers are accessible to applications programs at any privilege level.

FPU Data Registers (General Purpose)	
Register Name	**Size (in bits)**
R0 through R7	80

Each of the eight data registers in the FPU conforms to the following format:

Bit 79	Sign bit
Bits 64-78	Exponent
Bits 0-63	Significand

FPU Control/Status Registers	
Register Name	**Size (in bits)**
Control Register	16
Status Register	16
Tag Word	16
Instruction Pointer	48
Data Pointer	48

Floating Point Registers

Debugging and Testing Registers

The debugging and test registers are for advanced applications and systems level programs. These registers are only accessible at privilege level 0.

Debugging Registers
Register Name
DR0 Linear Break Point Address 0
DR1 Linear Break Point Address 1
DR2 Linear Break Point Address 2
DR3 Linear Break Point Address 3
DR6 Break Point Status
DR7 Break Point Control

Test Registers
Register Name
TR3 Cache Data Test Register TR4 Cache Data Test Register TR5 Cache Data Test Register TR6 Command Test (Control) Register TR7 Data Test (Status) Register

82357 Integrated Systems Peripheral (ISP)

DMA Controller

The following pages describe the addressing and command scheme for the DMA controller.

DMA Channel 4 is used to cascade the two controllers and should not be programmed for any mode other than cascade mode.

The DMA subsystem of the ISP chip includes a large number of internal registers. To expedite operations involving the count register or the address register, the ISP uses an internal byte-pointer flip-flop to add an extra bit. This bit selects between the high and low bytes of these registers. The flip-flop toggles each time a read or write command that involves any of the Word Count or Address Registers in the DMA subsystem is issued. The internal flip-flop is cleared when the CPU issues either a reset or a Master Clear command.

Refer to *EISA DMA Transfers* in *Technology Overview* for more information about the EISA-specific "Extended" mode commands.

DMA Controller 1

Address	W/R	Description	Notes
0000h	W/R	Ch. 0 Base/Current Address	see 0087h and 0487h
0001h	W/R	Ch. 0 Base/Current Word Count	see 0401h
0002h	W/R	Ch. 1 Base/Current Address	see 0083h and 0483h
0003h	W/R	Ch. 1 Base/Current Word Count	see 0403h
0004h	W/R	Ch. 2 Base/Current Address	see 0081h and 0481h
0005h	W/R	Ch. 2 Base/Current Word Count	see 0405h
0006h	W/R	Ch. 3 Base/Current Address	see 0082h and 0482h
0007h	W/R	Ch. 3 Base/Current Word Count	see 0407h
0008h	W	Command	see 00D0h
0008h	R	Status	see 00D0h
0009h	W	DMA Request	see 00D2h
000Ah	W	Write Single Mask Bit	see 00D4h
000Bh	W	Mode	see 00D6h
000Ch	W	Clear Byte Pointer Flip-flop	see 00D8h
000Dh	W	Master Clear	see 00DAh
000Eh	W	Clear Mask Register Bits	see 00DCh
000Fh	W	Write All Mask Register Bits	see 00DEh
000Fh	R	Mask Status	see 00DEh

DMA Controller 2

Address	W/R	Description	Notes
00C4h	W/R	Ch. 5 Base/Current Address	see 008Bh and 048Bh
00C6h	W/R	Ch. 5 Base/Current Word Count	see 04C6h
00C8h	W/R	Ch. 6 Base/Current Address	see 0089h and 0489h
00CAh	W/R	Ch. 6 Base/Current Word Count	see 04CAh
00CCh	W/R	Ch. 7 Base/Current Address	see 008Ah and 048Ah
00CEh	W/R	Ch. 7 Base/Current Word Count	see 04CEh
00D0h	W	Command	see 0008h
00D0h	R	Status	see 0008h
00D2h	W	DMA Request	see 0009h
00D4h	W	Write Single Mask Bit	see 000Ah
00D6h	W	Mode	see 000Bh
00D8h	W	Clear Byte Pointer Flip-flop	see 000Ch
00DAh	W	Master Clear	see 000Dh
00DCh	W	Clear Mask Register Bits	see 000Eh
00DEh	W	Write All Mask Register Bits	see 000Fh
00DEh	R	Mask Status	see 000Fh

DMA Controller 1 - Extended Registers

Address	W/R	Description	Notes
0401h	W/R	Ch. 0 Extended Word Count	see 0001h
0403h	W/R	Ch. 1 Extended Word Count	see 0003h
0405h	W/R	Ch. 2 Extended Word Count	see 0005h
0407h	W/R	Ch. 3 Extended Word Count	see 0007h
040Ah	W	Set Chaining Mode	see 04D4h
040Ah	R	Channel Interrupt Status	
040Bh	W	Extended Mode	see 04D6h
040Ch	R	Chain Buffer Expiration Control	

DMA Controller 2 - Extended Registers

Address	W/R	Description	Notes
04C6h	W/R	Ch. 5 Extended Word Count	see 00C6h
04CAh	W/R	Ch. 6 Extended Word Count	see 00CAh
04CEh	W/R	Ch. 7 Extended Word Count	see 00CEh
04D4h	W	Set Chaining Mode	see 040Ah
04D4h	R	Set Chaining Mode Status	
04D6h	W	Extended Mode	see 040Bh

Low Page Registers

Address	W/R	Description	Notes
0081h	W/R	Ch. 2 Low Page Segment	see 0481h
0082h	W/R	Ch. 3 Low Page Segment	see 0482h
0083h	W/R	Ch. 1 Low Page Segment	see 0483h
0087h	W/R	Ch. 0 Low Page Segment	see 0487h
0089h	W/R	Ch. 6 Low Page Segment	see 0489h
008Ah	W/R	Ch. 7 Low Page Segment	see 048Ah
008Bh	W/R	Ch. 5 Low Page Segment	see 048Bh

High Page Registers

Address	W/R	Description	Notes
0481h	W/R	Ch. 2 High Page Segment	see 0081h
0482h	W/R	Ch. 3 High Page Segment	see 0082h
0483h	W/R	Ch. 1 High Page Segment	see 0083h
0487h	W/R	Ch. 0 High Page Segment	see 0087h
0489h	W/R	Ch. 6 High Page Segment	see 0089h
048Ah	W/R	Ch. 7 High Page Segment	see 008Ah
048Bh	W/R	Ch. 5 High Page Segment	see 008Bh

008h (0D0h) Command/Status Register

Write (Command)

Bit	Description	1/0	Notes
7	DACK sense	high/low	
6	DREQ sense	low/high	
5	Reserved	must be 0	
4	Priority	rotating/fixed	
3	Reserved	must be 0	
2	Controller	disable/enable	
1	Reserved	must be 0	
0	Reserved	must be 0	

Read (Status)

Bit	Description	1/0
7	CH 3 request status	DRQ3/DRQ3-
6	CH 2 request status	DRQ2/DRQ2-
5	CH 1 request status	DRQ1/DRQ1-
4	CH 0 request status	DRQ0/DRQ0-
3	Ch 3 terminal count	TC3/TC3-
2	Ch 2 terminal count	TC2/TC2-
1	Ch 1 terminal count	TC1/TC1-
0	Ch 0 terminal count	TC0/TC0-

009h (0D2h) DMA Request Register (Write)

Bit	Description	1/0	
7-3	Reserved	must be 0	
2	Request bit	set/reset	
1-0		bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Ah (0D4h) Write single bit DRQ Mask			
Bit	**Description**	**1/0**	
7-3	Reserved	must be 0	
2	Mask bit	set/reset	
1-0		bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Ah (0D4h) Read Command Register
refer to Command Register description (Port 008h)

00Bh (0D6h) Mode Register

Bit	Description	1/0	
7-6	Mode select	bit 7	bit 6
	Demand mode	0	0
	Single cycle	0	1
	Block mode	1	0
	Cascade mode	1	1
5	Address counter	decrement/increment	
4	Autoinitialize	enable/disable	
3-2	Transfer type	bit 3	bit 2
	Verify transfer	0	0
	Write transfer	0	1
	Read transfer	1	0
	illegal	1	1
1-0	Channel select	bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Fh (0DEh) Write All Mask Register Bits

Bit	Description	1/0
7-4	Reserved	must be 0
3	Ch. 3 mask bits	set/reset
2	Ch. 2 mask bits	set/reset
1	Ch. 1 mask bits	set/reset
0	Ch. 0 mask bits	set/reset

00Ah (0D4h) Write single bit DRQ Mask			
Bit	**Description**	**1/0**	
7-3	Reserved	must be 0	
2	Mask bit	set/reset	
1-0		bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Ah (0D4h) Read Command Register
refer to Command Register description (Port 008h)

00Bh (0D6h) Mode Register

Bit	Description	1/0	
7-6	Mode select	bit 7	bit 6
	Demand mode	0	0
	Single cycle	0	1
	Block mode	1	0
	Cascade mode	1	1
5	Address counter	decrement/increment	
4	Autoinitialize	enable/disable	
3-2	Transfer type	bit 3	bit 2
	Verify transfer	0	0
	Write transfer	0	1
	Read transfer	1	0
	illegal	1	1
1-0	Channel select	bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Fh (0DEh) Write All Mask Register Bits

Bit	Description	1/0
7-4	Reserved	must be 0
3	Ch. 3 mask bits	set/reset
2	Ch. 2 mask bits	set/reset
1	Ch. 1 mask bits	set/reset
0	Ch. 0 mask bits	set/reset

40Ah DMA1 Chaining Mode Register (Write Only)

Bit	Description	1/0
7-5	Reserved	must be 0
4	Buffer expiration	TC/IRQ13
3	set up	programming complete/ do not start chaining
2	Chaining	enable/disable
1-0	Channel select	bit 1 bit 0
	Ch 0 select	0 0
	Ch 1 select	0 1
	Ch 2 select	1 0
	Ch 3 select	1 1

40Ah Channel IRQ13 Status Register (Read Only)

Bit	Description	1/0
7	Ch. 7	IRQ13/IRQ13-
6	Ch. 6	IRQ13/IRQ13-
5	Ch. 5	IRQ13/IRQ13-
4	Reserved	
3	Ch. 3	IRQ13/IRQ13-
2	Ch. 2	IRQ13/IRQ13-
1	Ch. 1	IRQ13/IRQ13-
0	Ch. 0	IRQ13/IRQ13-

40Bh (4D6h) Extended Mode Register

Bit	Description	1/0	
7	Stop Register	enable/disable	
6	End-of-Process (EOP) signal	input/output	
5-4	Timing	bit 5	bit 4
	Compatible	0	0
	Type "A"	0	1
	Type "B"	1	0
	Burst	1	1
3-2	Data size	bit 3	bit 2
	8-bit, byte count	0	0
	16-bit, word count	0	1
	32-bit, byte count	1	0
	16-bit, byte count	1	1
1-0	Channel select	bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

40Ch Chain Buffer Expiration Control Register (Read Only)

Bit	Description	1/0
7	Ch. 7	TC/IRQ13
6	Ch. 6	TC/IRQ13
5	Ch. 5	TC/IRQ13
4	Reserved	
3	Ch. 3	TC/IRQ13
2	Ch. 2	TC/IRQ13
1	Ch. 1	TC/IRQ13
0	Ch. 0	TC/IRQ13

4D4h DMA2 Chaining Mode Register (Write Only)

Bit	Description	1/0
7-5	Reserved	must be 0
4	Buffer expiration	TC/IRQ13
3	set up	programming complete/ do not start chaining
2	Chaining	enable/disable
1-0	Channel select	bit 1 bit 0
	Reserved	0 0
	Ch 5 select	0 1
	Ch 6 select	1 0
	Ch 7 select	1 1

4D4h Chaining Mode Status Register (Read Only)

Bit	Description	1/0
7	Ch. 7 Chaining mode	enable/disable
6	Ch. 6 Chaining mode	enable/disable
5	Ch. 5 Chaining mode	enable/disable
4	Reserved	
3	Ch. 3 Chaining mode	enable/disable
2	Ch. 2 Chaining mode	enable/disable
1	Ch. 1 Chaining mode	enable/disable
0	Ch. 0 Chaining mode	enable/disable

Interrupt Controller

The interrupt controller recognizes two types of commands: initialization command words (ICWs) and operational control words (OCWs). The initialization process consists of writing a sequence of four bytes to the interrupt controller.

The initialization sequence is started by writing the first initialization command word (ICW1) to Address 020h (CTLR-1) or 0A0h (CTLR-2) with a 1 on Bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1. Resets the Edge sense circuit (low-to-high generates an interrupt)
2. Clears the Interrupt Mask Register
3. Assigns priority 7 to IRQ7
4. Sets the Slave Mode address to 7
5. Clears Special Mask Mode
6. Selects the Interrupt Request Register for status read operations

The next three I/O writes to Address 021h (or 0A1h for CTLR-2) will load ICW2-ICW4. (All four bytes must be written for the controller to be properly initialized.) The initialization sequence can be terminated at any point by writing to Address 020h (0A0h) with a 0 in Data Bit 4. Note that this will allow OCW2 or OCW3 to be written. Operational Control Words (OCWs) allow the interrupt controller to be controlled or reconfigured at any time during operation.

Initialization Command Words (ICWs)

Note: Initialization words are defined by the operating system and are generally not to be changed. Writing an initialization word might cancel pending interrupts.

Port 020h (0A0h) ICW1

Bit Description

0 = 0 ICW4 Not Needed
= 1 ICW4 Needed

1 = 0 Cascade Mode (default)
= 1 Single Mode

2 Not Used

3 = 0 Edge Triggered Mode
= 1 Level Triggered Mode

Note: EISA ignores bit 3. EISA uses the Edge/Level Control Registers (4D0h and 4D1h) to determine interrupt triggering on a channel-by-channel basis

4 = 0 Operational Control Word
= 1 Initialization Command Word 1

5-7 Not Used

Port 021h (0A1h) ICW2

Bit Description

0-2 Must be 0

3-7 V3-V7 Of Interrupt Vector Address

Port 021h ICW3 (Master Device - INTC1)

Bit Description

0-7: = 1 Indicated IR input has a slave (bit 2)
= 0 Indicated IR input does not have a slave (bits 7-3 and 1-0)

Port 0A1h ICW3 (Slave Device - INTC2)

Bit Description

0-2: Bit2 Bit1 Bit0 Slave ID #

Bit2	Bit1	Bit0	Slave ID #
0	0	0	0
0	0	1	1
0	1	0	2 (default)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

3-7 = 0 (Not Used)

Port 021h (0A1h) ICW4

Bit Description

0: Must be 1

1: = 0 Normal EOI (Auto EOI disabled)
= 1 Automatic EOI Enabled

2-3: Not Used (Must be 0)

4: = 0 Disable Special Fully Nested Mode
= 1 Enable Special Fully Nested Mode

5-7: Not Used

Operational Control Words (OCWs)

Operational Control Words (OCWs) allow the interrupt controller to be controlled or reconfigured at any time during operation.

Port 021h (0A1h) OCW1

Bit Description
0-7: Interrupt Mask For IRQ0-IRQ7 (IRQ8-IRQ15)
= 0 Mask Reset (Enable IRQn)
= 1 Mask Set (Disable IRQn)

Port 020h (0A0h) OCW2

Bit	Description								
0-2:	Interrupt Level =	0	1	2	3	4	5	6	7	(CTLR-1)
		8	9	10	11	12	13	14	15	(CTRL-2)
	Bit0 (L0):	0	1	0	1	0	1	0	1	
	Bit1 (L1):	0	0	1	1	0	0	1	1	
	Bit2 (L2):	0	0	0	0	1	1	1	1	

3 = 0

4 = 0

5-7: Rotate And End Of Interrupt Modes

7 6 5	
0 0 1	Non-Specific EOI Command
0 1 1	Specific EOI Command
1 0 1	Rotate On Non-Specific EOI
1 0 0	Rotate In Automatic EOI Mode (Set)
0 0 0	Rotate In Automatic EOI Mode (Clear)
1 1 1	*Rotate On Specific EOI Command
1 1 0	*Set Priority Command
0 1 0	No Operation

*L0-L2 (bits 2-0) are used

Port 020h (0A0h) OCW3

Bit Description

0-1:

Bit 1	Bit 0	Read Register Command
0	0	No Action
0	1	No Action
1	0	Read IRQ Register On Next IOR- Pulse
1	1	Read IS Register On Next IOR- Pulse

2 = 0: Disable Polled Mode
= 1: Enable Polled Mode

3 = 1

4 = 0

5-6

Bit6	Bit5	Special Mask Mode
0	0	No Action
0	1	No Action
1	0	Normal Mask Mode
1	1	Special Mask Mode

7 = 0

EISA Edge/Level Triggered Control Register (ELCR)

Only the interrupts that connect to the EISA bus may be programmed for level sensitivity using the ELCR.

Port 4D0h (4D1h) EISA Edge/Level Triggered Control Register

Bit	Description	
7	Int 7/15	0 = Edge sensitive 1 = Level sensitive
6	Int 6/14	0 = Edge sensitive 1 = Level sensitive
5	*Int 5	0 = Edge sensitive 1 = Level sensitive
4	Int 4/12	0 = Edge sensitive 1 = Level sensitive
3	Int 3/11	0 = Edge sensitive 1 = Level sensitive
2	*Int 10	0 = Edge sensitive 1 = Level sensitive
1	*Int 9	0 = Edge sensitive 1 = Level sensitive
0	*Must be 0	

* IRQ13, IRQ1, and IRQ0 must be programmed for edge sensitive operation.

NMI Status/Control Registers

NMI Status/Control (Port B) Register 061h

This register is located at I/O address 061h. The register is defined as follows:

061h	NMI Status/Control Register

Bits 4-7 are read only (must be 0 for writes)
Bits 0-3 are read/write

Bit	Description
7	System memory parity check status
6	IOCHCK- (I/O channel check) status
5	Timer 1, Counter 2 output status
4	Refresh status
3	I/O channel check NMI 1 = IOCHCK- NMI disabled 0 = IOCHCK- NMI enabled
2	System memory parity check 1 = Parity check disabled 0 = Parity check enabled
1	Speaker (Timer 1, Counter 2) 1 = on 0 = off
0	Gate signal for speaker timer 1 = Timer 1, Counter 2 (Speaker) enabled 0 = Timer 1, Counter 2 (Speaker) disabled

Extended NMI Status/Control Register 461h

This EISA register is located at I/O address 461h. The register is defined as follows:

461h Extended NMI Status/Control Register

Bits 4-7 are read only (must be 0 for writes)
Bits 0-3 are read/write

Bit	Description
7	NMI from fail-safe timer 1 = Fail-safe timer active and NMI pending 0 = No NMI pending
6	NMI from bus timeout 1 = NMI pending 0 = No NMI pending
5	NMI I/O port status 1 = NMI pending 0 = No NMI pending
4	Reserved
3	32-bit bus timeout 1 = with NMI enabled 0 = with NMI disabled and cleared
2	1 = Fail-safe NMI enabled 0 = Fail-safe NMI disabled and cleared
1	1 = NMI I/O port enabled 0 = NMI I/O port disabled
0	1 = Bus reset asserted (RSTDRV) 0 = Normal bus reset operation

Counters/Timers

The counters are programmed by writing a control word and then an initial count. To set the control register of a counter, write to the control word address. The control register is a write-only location. The following table shows the addresses and format of the control words and the control word register.

Address	Function
040h-043h	Timer 1
040h 041h 042h 043h	Counter 0 System Clock Counter 1 Refresh Request Counter 2 Speaker Tone Control Register (Write Only)
048h-04Bh	Timer 2
048h 049h 04Ah 04Bh	Counter 0 Fail-safe Timer Reserved * Counter 2 Control Register (Write Only)
* EISA systems do not implement Counter 1 of Timer 2	

Control Register

Bit	Description
0	1 = BCD Select 0 = Binary Select
1-3	Mode Select

Bit 3	Bit 2	Bit 1	Mode
0	0	0	Mode 0 Interrupt on terminal count
0	0	1	Mode 1 Hardware retriggerable one-shot
x	1	0	Mode 2 Rate generator
x	1	1	Mode 3 Square wave generator
1	1	0	Mode 4 Software triggered strobe
1	1	1	Mode 5 Hardware retriggerable strobe

4-7 Command

Bit 7	Bit 6	Bit 5	Bit 4	Command
0	0	0	0	Latch Counter 0
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read Back Command

Read/Write Counter Command

When writing to a counter, observe the following conventions:

- Write each counter's control word before writing the initial count.
- When writing the initial count, follow the format specified in the control word (for example, least significant byte only or least significant byte, then most significant byte).
- Providing the programming format is observed, a new initial count can be written into the counter at any time after programming without rewriting the control word.

Latch Counter Command

When a Latch Counter command is issued, the current state of the counter element is latched. The count remains latched until read by the CPU or until the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the counter element can be read directly.

Read Back Command

The Read Back command allows you to check the count value, mode, and state of the OUT signal, and the Null Count Flag of the selected counter(s). The format for the Read Back command is:

Read Back Command

Bit	Description
7	Must be set To 1
6	Must be set To 1
5	0 = Latch count of selected counter
4	0 = Latch status
3	1 = Counter 3 select
2	1 = Counter 2 select
1	1 = Counter 1 select
0	Must Be 0

Status Byte

Bit	Description
7	OUT Signal State
6	Null Count Flag
4-5	Command Status
1-3	Mode Status
0	BCD/Binary Status

DS1287 Real Time Clock with RAM (RTC)

Most of the setup information stored in the Real Time Clock with RAM (RTC) can be accessed through BIOS or operating system calls. However, the RTC can be accessed directly by issuing software I/O commands. Reading the RTC is accomplished by writing an index byte to 070h and then reading from I/O address 071h. Writing to the RTC is similar. First write the index to I/O address 070h Then write to I/O address 071h.

This section lists the index values for the storable configuration bytes and defines the bit-parameters of the configuration bytes.

RTC Index Definitions

The index bytes for the RTC are defined as follows:

Index	Function
0Eh	Diagnostic status byte
0Fh	Shutdown status byte
10h	Diskette drive type byte (Drives A and B)
11h	Reserved
12h	Hard disk type byte (Drives C and D)
13h	Reserved
14h	Equipment byte
15h	Low base memory byte
16h	High base memory byte
17h	Low expansion memory byte
18h	High expansion memory byte
19h	Disk C extended byte
1Ah	Disk D extended byte
1Bh-2Bh	Reserved
2Ch	Bit 0 = swap disk bit
2Dh	Reserved
2Eh-2Fh	2-byte CMOS checksum
30h	Low expansion memory byte
31h	High expansion memory byte
32h	Date century byte
33h	Information flags (set during power on)
34h	BIOS/Cache/CPU Speed
35h-3Fh	Reserved

RTC Byte Definitions

Diagnostic Status Byte (Index 0Eh)

Bit	Function
7	Power Loss
6	Checksum Status Indicator
5	Incorrect Configuration
4	Memory Size Compare Error
3	Fixed Disk Initialization
2	Time Status Indicator
1	Reserved
0	Reserved

Bits 0-1 - Reserved.

Bit 2 - A 0 in this bit location indicates that the time is valid. A 1 in this bit location indicates that the time is invalid.

Bit 3 - A 0 in this bit location indicates that the fixed disk and adapter are operating properly, and the system can attempt a boot up. A 1 in this bit location indicates that either the fixed disk or the adapter has failed initialization.

Bit 4 - A 0 in this bit location indicates that the power on check has determined the memory size to be the same as that stored in the configuration. A 1 in this bit location indicates that the memory size is different than that stored in the configuration.

Bit 5 - A 0 in this bit location indicates that the configuration information is correct. A 1 in this bit location indicates that the configuration information is incorrect.

Bit 6 - A 0 in this bit location indicates that the configuration checksum is good. A 1 in this bit location indicated that the configuration checksum is bad.

Bit 7 - A 0 in this bit location indicates that the Real Time Clock has not lost power. A 1 in this bit location indicates that the Real Time Clock has lost power.

Shutdown Status Byte (Index 0Fh)

The bits in this byte are defined by the power on diagnostics.

Diskette Drive Type Byte (Index 10h)

Bit	Function
4-7	Drive A Type
0-3	Drive B Type

Bits 4-7 and bits 0-3 - These bits indicate the type of diskette drive installed in the following manner:

Bit 7(3)	Bit 6(2)	Bit 5(1)	Bit 4(0)	Drive Type
0	0	0	0	No Drive Installed
0	0	0	1	Double Sided 48 TPI
0	0	1	0	High-Capacity 96 TPI
0	1	0	0	High-Density 1.44MB

Hard Disk Type Byte(Index 12h)

Bit	Function
4-7	Drive C Type
0-3	Drive D Type

Bits 4-7 - These bits define the hard disk drive type for drive C in the following manner:

Bit 7	Bit 6	Bit 5	Bit 4	Drive Type
0	0	0	0	(0h) No Drive Installed
0	0	0	1	(1h-Eh) Define type 1-14
		TO		
1	1	1	0	
1	1	1	1	(Fh) Define type 16-255 (as defined by the Extended Drive Type Byte at 019h)

Bits 0-3 - These bits define the hard disk drive type for drive D in the following manner:

Bit 3	Bit 2	Bit 1	Bit 0	Drive Type
0	0	0	0	(0h) No Drive Installed
0	0	0	1	(1h-Eh) Define type 1-14
		TO		
1	1	1	0	
1	1	1	1	(Fh) Define type 16-255 (as defined by the Extended Drive Type Byte at 01Ah)

Drive C (19h) and Drive D (1Ah) Extended Bytes

These bits define the hard disk drive type for drive C and drive D in the following manner:

Bit 7	6	5	4	3	2	1	0	Drive Type
0	0	0	0	0	0	0	0	(00h-0Fh) Reserved
				TO				
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	(10h-FFh) defines type 16-255
				TO				
1	1	1	1	1	1	1	1	

Equipment Byte (Index 14h)

Bit	Function
7	Number Of Diskette Drives
6	Number Of Diskette Drives
5	Primary Display
4	Primary Display
3	Not Used
2	Not Used
1	Coprocessor Present
0	Diskette Drive Present

Bits 6-7 - These bits define the number of diskette drives installed in the system in the following manner:

Bit 7	Bit 6	Number Of Diskette Drives
0	0	1 Drive
0	1	2 Drives
1	0	Reserved
1	1	Reserved

Bits 4-5 - These bits define the type of display connected to the system in the following manner:

Bit 5	Bit 4	Display Type
0	0	Adapter has its own BIOS (EGA or VGA)
0	1	40 Column CGA
1	0	80 Column CGA
1	1	Monochrome Display

Bits 2-3 - Not Used.

Bit 1 - A 1 in this bit location indicates that a coprocessor is installed. A 0 in this bit location indicates that a coprocessor is not installed.

Bit 0 - A 1 in this bit location indicates that a diskette drive is installed. A 0 in this bit location indicates that a diskette drive is not installed.

Low (15h) and High (16h) Base Memory Bytes

Index 15h contains the Low Base Memory Byte and index 16h contains the High Base Memory Size Byte. The Base Memory Size bytes are defined in the following manner:

Value In 15-16h	Memory Size
0100h	256 KB
0200h	512 KB
0280h	640 KB
0400h	1024 KB

Low (17h) and High (18h) Expansion Memory Bytes

Index 17h contains the Low Expansion Memory Byte and index 18h contains the High Expansion Memory Size Byte. The Expansion Memory Size bytes are defined in the following manner:

Value In 17-18h	Expansion Memory Size
0400h	1024KB
0600h-3C00h	1536KB to 15360KB

Checksum Bytes (2Eh-2Fh)

Index 2Fh contains the Low Checksum Byte and index 2Eh contains the High Checksum Byte. The Checksum is calculated on addresses 10h-2Dh.

Date Century Byte (Index 32h)

These bits are read and set by BIOS and contain the BCD value for the century.

Information Flag (Index 33h)

Bit	Function
7	Top 128KB Memory Installed
6	First User Message Enable
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Bit 7 - A 1 in this bit location indicates that the top 128KB of base memory is installed. A 0 in this bit location indicates that the top 128KB of base memory is not installed.

Bit 6 - A 1 in this bit location causes a first user message to be displayed after initial setup. A 0 in this bit location omits the first user message displayed after initial setup.

Bits 0-5 - Reserved.

Configuration Register

The DECpc 433T uses a special register (Index 34h) in the RTC to store BIOS, cache, and processor speed configuration information. This configuration register is defined as follows:

BIOS/Cache/CPU Speed (Index 34h)

Bit	Function
7	BIOS relocation 1 = BIOS relocated 0 = BIOS not relocated
6	Secondary Cache – 1 = Disabled 0 = Enabled
5	i486 Internal Cache – 1 = Disabled 0 = Enabled
4-1	Reserved
0	Processor speed 1 = Fast (33 MHz) 0 = Slow (8 MHz)

EISA Extended CMOS RAM

This area is used to store configuration information about the main logic board and EISA and ISA adapter boards. ***The Access EISA System Information BIOS function (INT 15h, AH=D8h) should be the only method used to access the extended CMOS RAM in an EISA system.*** This function is used to autoconfigure EISA controllers. For details on the data for each slot refer to the definition for INT 15h, AH=D8h in *BIOS Services*.

For more information about the extended CMOS RAM, refer to the official EISA Specification available from BCPR Services, Inc., Washington, D.C.

LCD Module

The built-in controller on the Optrex DMC40218 LCD display module is equipped with an internal character generator ROM, character generator RAM, and display data RAM. All display functions can be controlled by instructions.

Registers

The LCD controller has two registers, the Instruction Register (IR) and the Data Register (DR). The Instruction Register is used to store instruction codes for the LCD controller. The Instruction Register is also used to specify addresses for the display data RAM (DD RAM) or the character generator RAM (CG RAM). The Data Register temporarily stores data written to or read from DD RAM or CG RAM.

Data written to the Data Register from the host system is automatically written into DD RAM or CG RAM by an internal operation.

The Data Register stores data when reading data from DD RAM or CG RAM. When address information is written to the Instruction Register, data from the DD RAM or CG RAM is placed in the Data Register by an internal operation. Data is then transferred to the host system by reading the Data Register. After the Data Register is read, data in the DD RAM or CG RAM at the next address is placed in the Data Register for the next read from the host system.

The following table defines the register addresses:

System Address	Read/ Write	Operation
0240h	WR	IR write, internal operation instruction
0240h	RD	Busy Flag (D7) and Address Counter (D0-D6)
0241h	WR	DR write (DD RAM or CG RAM)
0241h	RD	DR read (DD RAM or CG RAM)

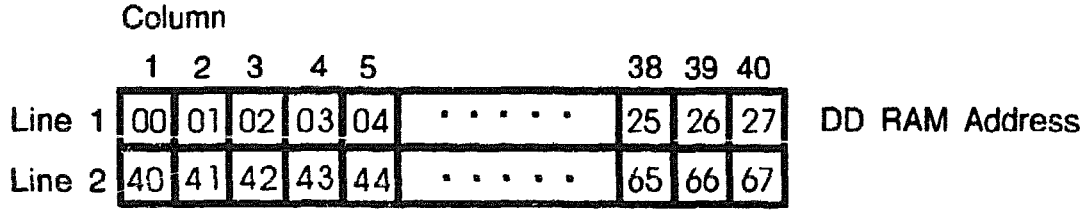
Busy Flag(BF)/Address Counter(AC)

When Busy Flag = 1, the LCD controller is performing an internal operation and the next instruction will not be accepted. The next instruction must be written after ensuring that the Busy Flag = 0. The Busy Flag value is available by reading D7 at 0240h.

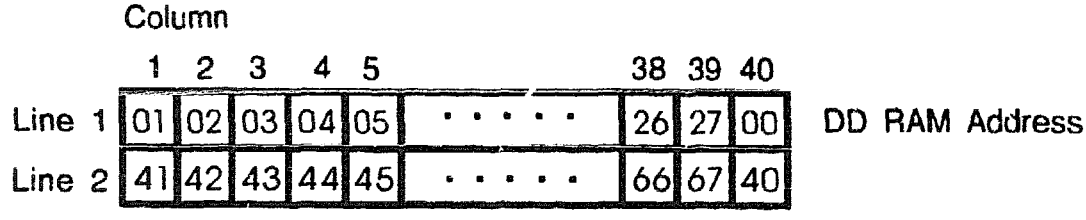
The Address Counter (AC) assigns an address to DD RAM or CG RAM. When an address instruction is written to the Instruction Register, the address is sent to the Address Counter. The instruction determines whether the address is for DD RAM or CG RAM. After data is written to or read from DD RAM or CG RAM, the Address Counter is automatically incremented or decremented by 1, depending on the Entry Mode. The current Address Counter value is available by reading D6-D0 at 0240h.

Display Data RAM (DD RAM)

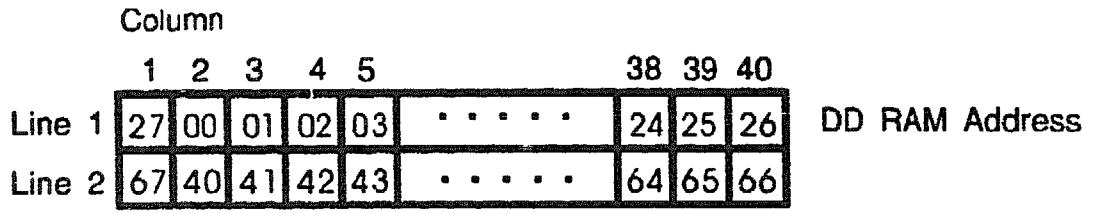
The Display Data RAM (DD RAM) is an 80 byte storage area for display data. The DD RAM Address (ADD) is set in the Address Counter and is represented in hexadecimal notation. The relationships between DD RAM Addresses and LCD positions (Line and Column) are shown in the following diagram:



Note that the last address of the first line and the first address of the second line are not consecutive. For example, when the display is shifted left, the DD RAM Address moves as follows:

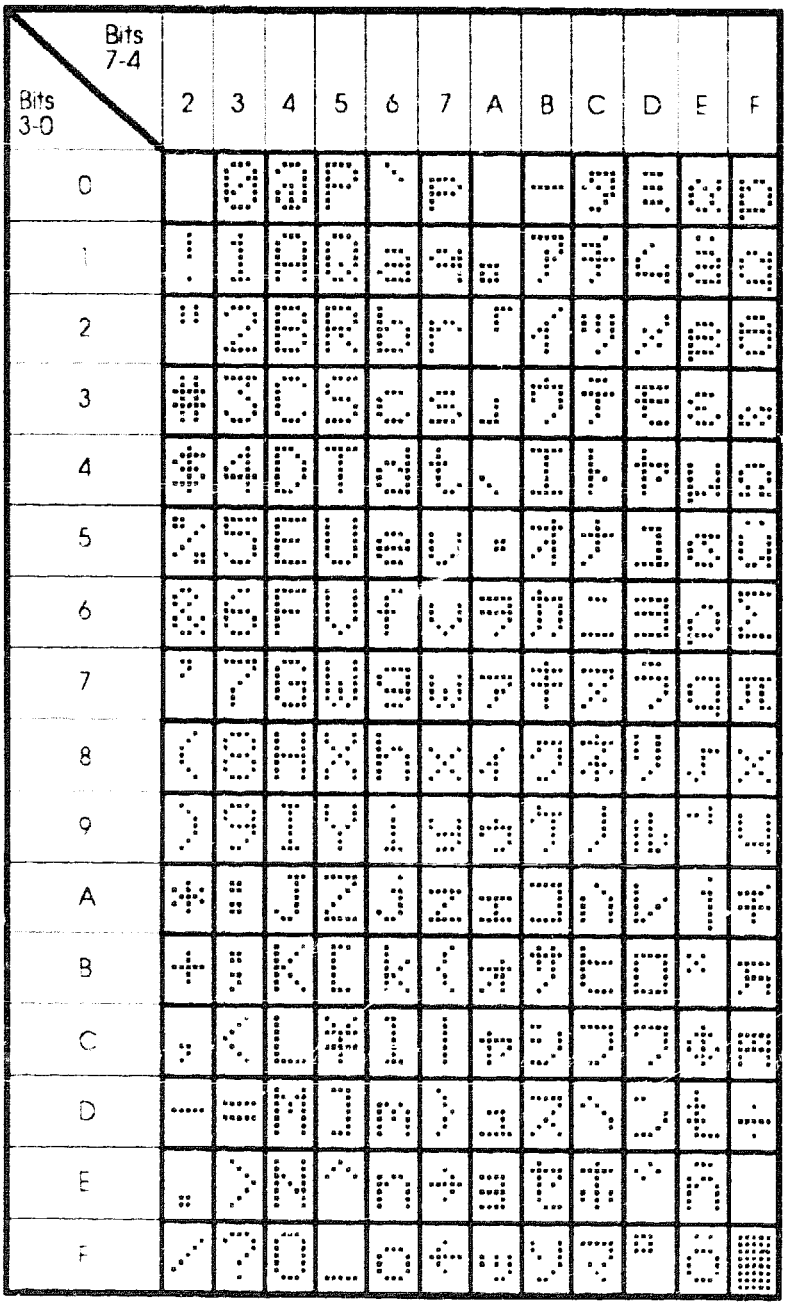


Similarly, when the display is shifted right, the DD RAM Address moves as follows:



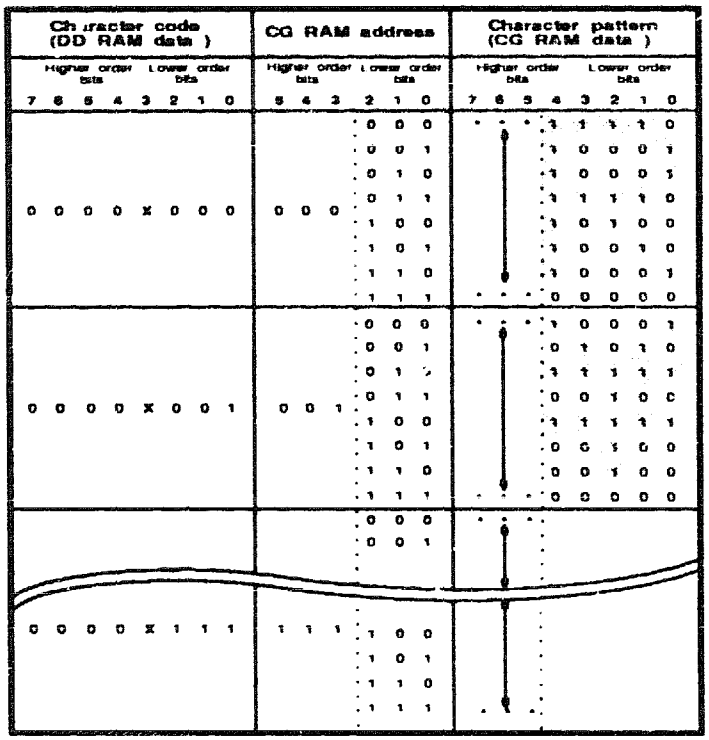
Character Generator ROM

The Character Generator ROM (CG ROM) contains the look-up table for the dot-matrix character patterns. The CG ROM holds 192 distinct 5x7 dot patterns. The following table depicts the dot patterns contained in the CG ROM, and their addresses:



Character Generator RAM

The Character Generator RAM is a storage area (look-up table) for user-defined characters. The CG RAM has space for up to eight 5x7 user-defined characters. The following table shows the relationships between the character code, the CG RAM address, and the character pattern:



Character code (DD RAM data)								CG RAM address						Character pattern (CG RAM data)							
Higher order bits				Lower order bits				Higher order bits			Lower order bits			Higher order bits			Lower order bits				
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	x	0	0	0	0	0	0	0	0	0	*	*	*	1	1	1	1	0
											0	0	1				1	0	0	0	1
											0	1	0				1	0	0	0	1
											0	1	1				1	1	1	1	0
											1	0	0				1	0	1	0	0
											1	0	1				1	0	0	1	0
											1	1	0				1	0	0	0	1
											1	1	1	*	*	*	0	0	0	0	0
0	0	0	0	x	0	0	1	0	0	1	0	0	0	*	*	*	1	0	0	0	1
											0	0	1				0	1	0	1	0
											0	1	0				1	1	1	1	1
											0	1	1				0	0	1	0	0
											1	0	0				1	1	1	1	1
											1	0	1				0	0	1	0	0
											1	1	0				0	0	1	0	0
											1	1	1				0	0	0	0	0
											0	0	0	*	*	*					
											0	0	1								
0	0	0	0	x	1	1	1	1	1	1	1	0	0	*	*	*					
											1	0	1								
											1	1	0								
											1	1	1								

Notes:

(1) Character code bits 0-2 correspond to CG RAM address bits 3-5. (3 bits 8 characters)

(2) CG RAM address bits 0-2 designate the row position of the character pattern. The 8th row is the cursor position and should be filled with 0's.

(3) The character pattern column positions correspond to data bits 0-4 of the CG RAM. CG RAM data bits 5-7 are not used for display and can be used for general data RAM.

(4) As shown in the table, CG RAM character patterns are selected when character code bits 4-7 are all "0". Bit 3 of the character code is ignored. For example, the character pattern selected by character code 00h is also selected by character code 08h.

Instructions

The LCD controller has eight instructions. Instructions are sent to the LCD controller by writing the instruction code to 0240h. The following chart is a summary of the instructions.

Instruction	Code	Notes
Clear Display	0 0 0 0 0 0 0 1	Clears entire display and sets DD RAM address 0 in the Address Counter.
Return Home	0 0 0 0 0 0 1 x	Sets DD RAM address 0 in Address Counter. Returns display to original position. DD RAM contents remain unchanged.
Entry Mode Set	0 0 0 0 0 1 I/D S	Sets cursor movement direction and specifies shift of display.
Display ON/OFF Control	0 0 0 0 1 D C B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and cursor blink ON/OFF (B).
Cursor or Display Shift	0 0 0 1 S/C R/L x x	Moves cursor and shifts display without changing DD RAM contents.
Function Set	0 0 1 DL N F x x	Sets interface data length (DL), number of display lines (L), and character font (F).
Set CG RAM Address	0 1 AGC (6 bits)	Sets CG RAM address. CG RAM is sent or received after this instruction.
Set DD RAM Address	1 ADD (7 bits)	Sets DD RAM address. DD RAM is sent or received after this instruction.

Clear Display (01h)

This command writes the space code (20h) into all addresses of DD RAM and returns the display to its original position if it was shifted. The cursor moves to the first position on the first line. The Clear Display instruction sets the Entry Mode to increment.

Return Home (02h)

This command sets the DD RAM address to 0 in the Address Counter without disturbing the contents of DD RAM. The cursor moves to the first position on the first line.

Entry Mode Set (04h - 07h)

This command sets the Entry Mode and shifts the display left or right.

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	1	I/D	S

I/D: The Increment/Decrement (I/D) bit determines whether the DD RAM (or CG RAM) Address is incremented or decremented when a character code is written into or read from DD RAM (or CG RAM). The I/D bit also determines the shift direction when S = 1.

S: The Shift (S) bit, when set (= 1), shifts the entire display either to the left or right. When S = 1 and I/D = 1, the display is shifted left; when S = 1 and I/D = 0, the display is shifted right. The cursor is not shifted with the display.

Display ON/OFF Control (08h - 0Fh)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	1	D	C	B

D: The Display (D) bit turns the display ON (D = 1), or OFF (D = 0). Display data (DD RAM) remains unchanged.

C: The Cursor (C) bit turns the cursor ON (C = 1), or OFF (C = 0). The setting of the Cursor ON or OFF does not affect the function of the Entry Mode I/D bit.

B: The Blink bit turns blinking ON (B = 1), or OFF (B = 0). When B = 1, the character at the cursor position blinks. The cursor and blink can be set simultaneously.

Display Shift

This command shifts the cursor or display without disturbing the display data.

Bit	7	6	5	4	3	2	1	0
	0	0	0	1	S/C	R/L	x	x

S/C: The Screen/Cursor bit determines whether the display or the cursor is shifted: S/C = 1 shifts the entire display; S/C = 0 shifts the cursor.

R/L: The Right/Left bit determines the direction of the shift: R/L = 1 shifts right; R/L = 0 shifts left.

When the cursor is shifted, the Address Counter (AC) is incremented (R/L = 1) or decremented (R/L = 0) by 1. The cursor moves to the second line when it passes the 40th digit of the first line.

When the entire display is shifted, the first and second lines will shift at the same time. Each line moves horizontally, but the second line display does not shift into the first line. The contents of the Address Counter are not changed when the display is shifted.

Function Set

The function set command initializes the display. The function set command is performed at the start of program code – before any instructions are executed. For the LCD controller on the DECpc 433T, the function set command ***must*** be 38h.

Bit	7	6	5	4	3	2	1	0
	0	0	1	DL	N	F	x	x

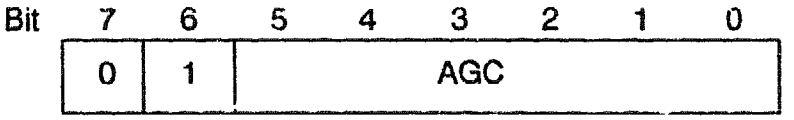
DL: The Data Length bit must be set to DL = 1 (8-bit operation).

N: The Number of lines bit must be set to N = 1 (2-line display).

F: The Font bit must be set to F = 0 (5x7 dots).

Set CG RAM Address

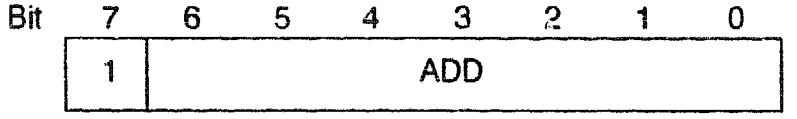
This command sets the 6-bit CG RAM Address (AGC) into the Address Counter (AC). Data is then written to or read from the CG RAM by accessing 0241h.



ACG: Binary CG RAM Address (6-bits)

Set DD RAM Address

This command sets the 7-bit DD RAM Address (ADD) into the Address Counter (AC). The DD RAM Address range is 00h-27h for the first line, and 40h-67h for the second line. Data is then written into or read from the DD RAM by accessing 0241h.



ADD: Binary DD RAM Address (7-bits)

Diskette Drive Controller

There are several registers contained in the WD37C65 Floppy Disk Controller for configuration, status information, and command execution. These registers are listed below with their I/O addresses.

Address	Register
03F2h	Operations Register (W)
03F4h	Main Status Register (R)
03F5h	Data Register (W/R)
03F7h	Control Register (W)

Operating Modes

There are two basic operating modes of the Floppy Disk Controller. They are as follows:

Non-DMA Mode

DMA Mode

These modes comprise two basic methods of data handling between the system microprocessor, in this case the CPU, and the disk controller. In the DMA mode, the command that is to be executed need only be loaded into the controller by the CPU. The controller, along with the 8237A DMA sections of the 82357 ISP, then handle all of the controls and handshaking necessary to complete the command and transfer the data. In the Non-DMA mode of operation, the 37C65 will issue an interrupt to the CPU every time a data byte is to be transferred. It is then the responsibility of the CPU, its support peripherals, and the programmer to generate the proper handshaking and control signals to transfer the data to or from the 37C65.

Registers

Operations Register (03F2h)

This register is used to control drive motors, drive selection, DMA enable, and Reset. The format of this Register is as follows:

Bit	Function
7	Mode Select
6	Reserved (not used)
5	Motor Enable 2–
4	Motor Enable 1–
3	DMA Enable
2	Controller Reset–
1	Reserved (must be 0)
0	Drive Select

Bit 7 A 0 in this bit location selects AT/EISA mode. A 1 selects Special mode. This bit should be 0.

Bit 6 This bit is not used.

Bit 5 A 0 in this bit location enables the motor for Floppy Drive 2. A 1 disables it.

Bit 4 A 0 in this bit location enables the motor for Floppy Drive 2. A 1 disables it.

Bit 3 A 1 in this bit location selects DMA operation. A 0 in this bit location selects non-DMA operation.

Bit 2 A 0 in this bit location resets the 37C65. A 1 in this bit location enables normal operation.

Bit 1 Reserved. This bit should be 0.

Bit 0 This bit is used to select the Floppy Drive.

Bit 5	Bit 4	Bit 0	Drive
0	1	0	Drive 1
1	0	1	Drive 2

Main Status Register (03F4h)

The Main Status Register is a read only register that is used to support the transfer of data between the system and the controller. This register has the following format:

Bit	Function
7	Request for Master
6	Data In/Out
5	Non-DMA Mode
4	Controller Busy
3	Drive 3 Busy (not used)
2	Drive 2 Busy (not used)
1	Drive 1 Busy
0	Drive 0 Busy

Bit 7 When this bit is a 1, the Data register is ready for transfer with the system

Bit 6 This bit determines the direction of the data transfer between the data register and the system. A 1 in this bit indicates the transfer is from the data register to the system. A 0 indicates a transfer from the system to the data register.

Bit 5 When this bit is a 1, the controller is in the non-DMA mode.

Bit 4 When this bit is set to 1, a read or write command is being executed by the controller.

Bit 3 When set to 1, this bit indicates that diskette drive 3 is in the seek mode.

Bit 2 When set to 1, this bit indicates that diskette drive 2 is in the seek mode.

Bit 1 When set to 1, this bit indicates that diskette drive 1 is in the seek mode.

Bit 0 When set to 1, this bit indicates that diskette drive 0 is in the seek mode.

Data Register (03F5h)

The Data Register is a storage area that is read from or written to one byte at a time. It is used to store data, commands, parameters, and status. Data bytes are passed through the Data Register to program the Floppy Disk Controller or to obtain status after a command has been executed.

Control Register (03F7h)

When written to, this register is used to set the data transfer rate. The format of the Data Rate Register is as follows:

Bit(s)	Function
7-3	Reserved
2	Write Precompensation
1-0	Rate Select

Bits 0-1 These bits are used to select the data transfer rate of the floppy disk drive in the following manner:

Bit 1	Bit 0	Rate
0	0	500 Kbits/sec
0	1	300 Kbits/sec
1	0	250 Kbits/sec
1	1	125 Kbits/sec

Commands

The Floppy Disk Controller is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The result after the execution of the command can also be a multibyte transfer back to the processor.

Command operation consists of three phases:

Command Phase – The Floppy Disk Controller receives all information required to perform a particular operation from the processor.

Execution Phase – The Floppy Disk Controller performs the operation as instructed.

Result Phase – After completion of the operation, status and other housekeeping information are made available to the processor.

For information on specific programming commands for the floppy disk controller, please refer to the Western Digital WD37C65 Data Sheet.

Keyboard Controller

The Keyboard Controller transfers data to and from the system via the data port located at I/O address 060h. A command/status port is provided at location 064h for issuing of commands to the keyboard, and reading of status from the keyboard. When the system reads the information at address 064h, it receives status from the keyboard. When the system writes data to address 064h, the Keyboard Controller interprets the data as a command.

Status Register

This is a register located at address 064h. The following is a description of the status bit definitions.

Bit	Status
7	Parity Error
6	General Time Out
5	Transmit Error
4	Inhibit Switch
3	Command Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Bit 7 - A 0 indicates the last byte received from the keyboard had odd parity. A 1 indicates the last byte received had even parity. The keyboard should send data with odd parity.

Bit 6 - A 1 indicates that a transmission was started by the keyboard but did not finish within the programmed time limit.

Bit 5 - A 1 in this bit indicates that a keyboard controller transmission was not properly completed.

Bit 4 - This bit is updated when data is placed in the output buffer. It reflects the state of the keyboard inhibit switch. A 0 in this bit means the keyboard is inhibited.

Bit 3 - The input buffer may be addressed as I/O address 60h or 64h. Address 60h is defined as a data port while address 64h is a command port. Writing to address 64h sets this bit to a 1, and writing to address 60h sets

this bit to 0. The controller uses this bit to determine if the byte in the input buffer is a data or command byte.

Bit 2 - This bit may be set to 0 or 1 by writing to the flag bit in the controller's command byte. It is set to 0 on power up reset.

Bit 1 - A 0 in this position means the input buffer at I/O address 60h or 64h is empty. A 1 indicates that data has been written into the buffer but the controller (8742) has not read it yet. When the data is read by the controller this bit is reset to 0.

Bit 0 - When this bit is a 0 it indicates that the output buffer is empty. A 1 indicates that there is data in the output buffer but the system has not yet read the data. When the system does read the data, this bit is reset to 0.

Keyboard Controller Command Summary

20-3F -- Read Keyboard Controller's RAM. Bits D5-D0 specify the address.

20 -- Read Keyboard Controller's Command Byte. The controller sends the current command byte to the output buffer.

60-7F -- Write Keyboard Controller's RAM. Bits D5-D0 specify the address.

60 -- Write Keyboard Controller's Command Byte. The next byte of data written to I/O address 60h is put in the controller's command byte. Bit definitions for the command byte are as follows:

Bit 7 - Reserved. Should be a 0.

Bit 6 - IBM Personal Computer Compatibility Mode. Writing a 1 to this bit causes the controller to convert the scan codes it receives to those used by the IBM Personal Computer.

Bit 5 - IBM Personal Computer Mode. Writing a 1 to this bit programs the keyboard to support the IBM Personal Computer keyboard interface. The controller will not check parity or convert scan codes.

Bit 4 - Disable Keyboard. Writing a 1 to this bit disables the keyboard interface by driving the clock line low. Data is not sent or received.

Bit 3 - Inhibit Override. A 1 in this bit disables the keyboard inhibit function.

Bit 2 - System Flag. The value written to this bit is put in the system flag bit of the status register.

Bit 1 - Reserved. Should be a 0.

Bit 0 - Enable Output Buffer Full Interrupt. Writing a 1 to this bit causes the controller to generate an interrupt when it places data into the output buffer.

A4 -- Test Password. This command checks if there is a password currently installed in the 8742. The test result is placed in the output buffer (I/O Address 060h). FAh means the password is installed. F1h means no password is installed.

A5 -- Load Security. This command starts the load password procedure. Following this command the 8742 will receive input from the data port until a null (0) is detected, which terminates the password entry.

A6 -- Enable Security. This command enables the 8742 security feature. This command is only valid when a password pattern is currently loaded into the 8742.

AA -- Self Test. Causes the controller to perform internal diagnostics. 55h is placed in the output buffer if no errors are encountered.

AB -- Interface Test. Causes the controller to test the keyboard clock and data lines. The result is placed in the output buffer as follows:

00 - No error detected

01 - keyboard clock line stuck low

02 - keyboard clock line stuck high

03 - keyboard data line stuck low

04 - keyboard data line stuck high

AC -- Diagnostic Dump. Sends 16 bytes of the controller's RAM, current state of the input port, current state of the output port, and the controller's program status word to the system. All items are sent in scan code format.

AD -- Disable Keyboard Interface. This disables keyboard interfacing by driving the clock line low. Data will not be sent or received.

AE -- Enable Keyboard Interface. This releases the keyboard interface.

C0 -- Read Input Port. Tells the controller to read the input port and place the data in the output buffer. This command should be used only if the output buffer is empty.

C1 -- Poll Input Port Low. Port 1 bits 0-3, in Status bits 4-7.

C2 -- Poll Input Port High. Port 1 bits 4-7, in Status bits 4-7.

D0 -- Read Output Port. Causes the controller to read the output port and place the contents in the output buffer. This command should only be used if the output buffer is empty.

D1 -- Write Output Port. The next byte of data written to I/O address 60h is placed in the output port. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

E0 -- Read Test Inputs. This causes the controller to read its T0 and T1 inputs. The data is placed in the output buffer with data bit 0 representing T0 and data bit 1 representing T1.

F0-FF -- Pulse Output Port. Bits 0-3 of the controller's output port may be pulsed low for approximately 6 microseconds. Bits 0-3 of this command indicate which bits are to be pulsed. A 0 causes the bit to be pulsed, and a 1 causes the bit not to be pulsed. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

Serial/Parallel Interface

This section describes the registers and programming of the WD16C452 Dual Enhanced Asynchronous Communications Element (ACE) with Parallel Port.

Serial Port Registers

The following chart lists the addresses of the Serial Port registers. They are listed in hexadecimal format. Serial Port 1 can be set as COM1, COM2, or COM3; Serial Port 2 can be set as COM2, COM3, or COM4. Refer to *Multi-Function Adapter Jumper Settings* in *System Configuration* for information on setting the serial ports.

Register	I/O Address			
	COM1	**COM2**	**COM3**	**COM4**
Receiver Buffer	3F8h	2F8h	3E8h	2E8h
Transmitter Holding	3F8h	2F8h	3E8h	2E8h
Interrupt Enable	3F9h	2F9h	3E9h	2E9h
Interrupt Identification	3FAh	2FAh	3EAh	2EAh
Line Control	3FBh	2FBh	3EBh	2EBh
Modem Control	3FCh	2FCh	3ECh	2ECh
Line Status	3FDh	2FDh	3EDh	2EDh
Modem Status	3FEh	2FEh	3EEh	2EEh
Scratch	3FFh	2FFh	3FFh	2FFh
Divisor Latch LSB	3F8h	2F8h	3E8h	2E8h
Divisor Latch MSB	3F9h	2F9h	3E9h	2E9h

The following is a table of register bit definitions for the serial ports. The first address is for COM1, and the second address is for COM2. Refer to the preceding table for the addresses for COM3 and COM4.

03F8 (02F8) Read Receiver Buffer Register (Character Received) Line Control Register bit 7=0 (DLAB=0)

Bit	Description
0	Bit 0 lsb (first bit received serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 msb (last bit received serially)

03F8 (02F8) Write Transmitter Holding Register (CTS) Line Control Register bit 7=0 (DLAB=0)

Bit	Description
0	Bit 0 lsb (first bit sent serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 msb (last bit sent serially)

03F9 (02F9) Interrupt Enable Register

Bit	Description
0	1 = Enables the Received Data Available Interrupt
1	1 = Enables the Transmitter Holding Register Empty Interrupt
2	1 = Enables Receive Line Status Interrupt
3	1 = Enables the Modem Status Interrupt
4-7	Always Logical 0

03FA (02FA) Interrupt Identification Register

Bit	Description		
0	0 = Interrupt Pending		
1-2	**Bit 2**	**Bit 1**	
	0	0	Fourth Level Priority
	0	1	Third Level Priority
	1	0	Second Level Priority
	1	1	Highest Level Priority
3-7	Always Logical 0		

03FB (02FB) Line Control Register

Bit	Description		
0-1	**Bit 1**	**Bit 0**	
	0	0	Five Bit Word Length
	0	1	Six Bit Word Length
	1	0	Seven Bit Word Length
	1	1	Eight Bit Word Length
2	0 = One Stop Bit 1 = 1 1/2 Stop Bits When Five Bit Word Length Selected. 2 Stop Bits With Six, Seven, or Eight Bit Word Length		
3	1 = Parity Enable		
4	0 = Odd Parity Select 1 = Even Parity Select		
5	Stick Parity Bit		
6	1 = Set Break Enable		
7	1 = Divisor Latch Access Bit (DLAB) Enable		

03FC (02FC) Modem Control Register

Bit	Description
0	1 = Data Terminal Ready Set (DTR) 0 = Data Terminal Ready Reset (DTR)
1	1 = Request To Send Set (RTS) 0 = Request To Send Reset (RTS)
2	(not used)
3	Interrupt Out 1 = Enables Interrupt 0 = Tri-states Interrupt
4	Loop
5-7	Always Logical 0

03FD (02FD) Line Status Register

Bit	Description
0	Data Ready (DR)
1	Overrun Error (OR)
2	1 = Detect Parity Error (PE)
3	1 = Detect Framing Error (FE)
4	1 = Break Interrupt (BI)
5	Transmitter Holding Register Empty 1 = Character Transferred From Holding To Shift Register 0 = Loading Transmitter Holding Register
6	Transmitter Shift Register Empty 1 = Shift Register and Holding Register are idle (empty) 0 = Transmitting data
7	Always Logical "0"

03FE (02FE) Modem Status Register

Bit	Description
0	Delta Clear To Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge Ring Indicator 1 = On 0 = Off
3	Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a 1 modem status interrupt is generated
4	Clear To Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Received Line Signal Detect (RLSD)

03F8 (02F8) Divisor Latch LSB
Line Control Register bit 7=1 (DLAB=1)

Bit	Description
7-0	Bits 7-0 Least Significant Byte of the Divisor Latch - refer to *Divisor Latch Table* on the following page

03F9 (02F9) Divisor Latch MSB
Line Control Register bit 7=1 (DLAB=1)

Bit	Description
7-0	Bits 7-0 Most Significant Byte of the Divisor Latch refer to *Divisor Latch Table* on the following page

Divisor Latch Table (Clock is 1.8432 MHz)		
Desired Baud Rate	**Divisor Used (decimal)**	**% Error**
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19,200	6	–
38,400	3	–
56,000	2	2.860

Parallel Interface

The following chart lists the addresses of the parallel port registers with jumper pins 13, 14, 15 and 16 (Port Control Jumper Block W1) set to LPT1 . The addresses in parentheses are for jumper pins 13, 14, 15 and 16 set to LPT2/LPT3.

Register	Address
Printer Data Latch	3BCh (378h/278h)
Printer Read Status	3BDh (379h/279h)
Printer Control Latch	3BEh (37Ah/27Ah)

Transfer direction

The parallel port allows either one-way or two-way data transfer:

- **Unidirectional (one-way).** The computer uses the port only to send output to the parallel device. It does not receive input through the port.
- **Bidirectional (two-way).** The computer uses the port both to send output to the parallel device and to receive input from the device.

In the default configuration, the parallel port is set up as a two-way port. For two-way data transfer, the port must be programmed by the following method:

To receive input through the port, enable input data by writing a 1 to bit 5 of the printer control latch (3BEh for LPT1, 37Ah for LPT2, 27Ah for LPT3).

To send output through the port, enable output data by writing a 0 to bit 5 of the printer control latch (3BEh for LPT1, 37Ah for LPT2, 27Ah for LPT3).

The parallel port can be configured as a one-way port using pins 17, 18, 19, and 20 of jumper block W1 on the Multi-function I/O adapter. Refer to "*Jumpers and Switches*" for more information.

Parallel Port Registers

The following is a table of register bit definitions for the parallel port.

3BCh (0378/0278) Printer - Data Latch	
Bit	**Description**
7-0	Data Bits 7-0

3BDh (0379/0279) Printer - Read Status Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	0 = Error
4	1 = Printer Select
5	1 = Out of Paper
6	0 = Acknowledge
7	0 = Busy

3BEh (037A/027A) Printer - Control Latch Bit	Description
0	1 = Strobe Low to high latches character High to low prints character
1	1 = Auto FD XT
2	0 = Initialize
3	1 = Select Printer
4	1 = Enable Interrupt
5	Directional Control 0 = Enable Output Data 1 = Enable Input Data
6	Not Used
7	Not Used

BIOS Services

The BIOS (Basic Input/Output System) is the lowest level interface between other software (application programs and the operating system) and the hardware. BIOS routines provide device input/output services, as well as bootstrap, print screen, and other services. Some BIOS services, such as graphics routines, are not available through the operating system.

All BIOS calls are made through software interrupts (assembly-language "INT x" instructions). Each I/O device is provided with a software interrupt, that transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Exit parameters are generally returned in CPU registers. To ensure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS routine. To execute a BIOS call, load the registers according to the entry conditions specified in the function description. (Register AH contains the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. For example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16h
```

Upon return, AL contains the ASCII character and AH contains the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Software Interrupt Summary

The following table is a quick reference list of software interrupts for all device I/O and system status services.

Service	Software Interrupts
Video Display	10 hex (16 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)
Floppy Disk	13 hex (19 dec)
Hard Disk	13 hex (19 dec)
Serial Communications	14 hex (20 dec)
System Support	15 hex (21 dec)
Joystick	15 hex (21 dec)
Microsecond Delay	15 hex (21 dec)
Extended Memory	15 hex (21 dec)
Virtual Mode	15 hex (21 dec)
Keyboard	16 hex (22 dec)
Line Printer	17 hex (23 dec)
System Clock	1A hex (26 dec)
Floppy Disk Parameter	1E hex (30 dec)
Hard Disk 0 Parameter	41 hex (65 dec)
Hard Disk 1 Parameter	46 hex (70 dec)

Software Interrupt Classes

Interrupt 10h: Video Display Functions

Software interrupt 10h (16 decimal) accesses video display functions, summarized in the following chart. Entry and exit conditions are defined later.

Note: Functions 10h-12h and 1Ah-1Ch are EGA/VGA functions and are contained within the VGA display adapter's BIOS, if present. These functions are included here for completeness.

Routine Group	AH	Function Description
Control Routines	00h	Set CRT mode
	01h	Set cursor type
	02h	Set cursor position
	03h	Get cursor position
	04h	Read light pen position
	05h	Select active page
	06h	Scroll active page up
	07h	Scroll active page down
Text Routines	08h	Read attribute/character
	09h	Write attribute/character
	0Ah	Write character only
Graphics Routines	0Bh	Set color palette
	0Ch	Write dot
	0Dh	Read dot
Other Routines	0Eh	Write TTY* to active page
	0Fh	Get current video state
	10h	Set palette registers
	11h	Character generator
	12h	Alternate select
	13h	Write string
	1Ah	Display combination code
	1Bh	Functionality/State information
	1Ch	Video state

Video Display Function Summary

* Screen width is determined by the mode previously set. Control characters 00h-1Fh ASCII perform the usual special terminal functions. These include (but are not limited to) BEL(07h), BS(08h), LF(0Ah), and CR(0Dh).

Note: AX is modified on all video calls.

Set CRT Mode (AH = 00h)

Sets the CRT video mode.

Entry Conditions:

AH = 00h

AL = mode value, as follows:

Mode	Resolution	Colors /Palette	Text Format	Char Box	Max Pgs	Buffer Addr.
0,1(T)[1]	320x200[2]	16/256K	40x25	8x8	8	B8000
0,1(T)	320x350[2]	16/256K	40x25	8x14	8	B8000
0,1(T)[3]	360x400[2]	16/256K	40x25	9x16	8	B8000
2,3(T)	640x200[2]	16/256K	80x25	8x8	8	B8000
2,3(T)	640x350[2]	16/256K	80x25	8x14	8	B8000
2,3(T)[3]	720x400[2]	16/256K	80x25	9x16	8	B8000
4,5(G)[1]	320x200	4/256K	40x25	8x8	1	B8000
6(G)	640x200	2/256K	80x25	8x8	1	B8000
7(T)	720x350[2]	MDAMono	80x25	9x14	8	B0000
7(T)[3]	720x400[2]	VGAMono	80x25	9x16	8	B0000
D(G)	320x200	16/256K	40x25	8x8	8	A0000
E(G)	640x200	16/256K	80x25	8x8	4	A0000
F(G)	640x350	Mono	80x25	8x14	2	A0000
10(G)	640x350	16/256K	80x25	8x14	2	A0000
11(G)	640x480	2/256K	80x30	8x16	1	A0000
12(G)	640x480	16/256K	80x30	8x16	1	A0000
13(G)	320x200	256/256K	40x25	8x8	1	A0000

1 (T) indicates a text mode; (G) indicates a graphics mode.
2 Alternate select (AH = 12h) video BIOS call must be called to select scan lines.
3 Default modes

Video Modes Supported

Set Cursor Type (AH = 01h)

Sets the cursor type and attribute.

Entry Conditions:
AH = 01h
CH - Bits 6-5 cause an invisible or blinking cursor
Bits 4-0 point to the start line for cursor within character cell
CL - Bits 4-0 point to the end line for cursor within character cell

Set Cursor Position (AH = 02h)

Writes (sets) cursor position.

Entry Conditions:
AH = 02h
BH = page number (see chart under AH = 0)
DH = row (0 = top row)
DL = column (0 = leftmost position)

Get Cursor Position (AH = 03h)

Reads (gets) cursor position.

Entry Conditions:
AH = 03h
BH = page number (see chart under AH = 0)

Exit Conditions:
DH = row of current cursor position (0 represents top row)
DL = column of current cursor position (0 represents left most column)
CH = cursor type currently set - Bits 4-0 point to the start line for cursor within character cell
CL = bit values: Bits 4-0 point to the end line for cursor within character cell

Select Active Page (AH = 05h)

Selects active display page (valid with color graphics adapter in alpha mode).

Entry Conditions:
AH = 05h
AL = new page value (0 based, see AH = 0 for maximum pages for each mode

Scroll Up (AH = 06h)

Scrolls active page up.

Entry Conditions:

AH = 06h
AL = number of lines to scroll; this number of lines will be blank at the bottom of the window. (0 means blank entire window)
CH = row of upper left corner of scroll window
CL = column of upper left corner of scroll window
DH = row of lower right corner of scroll window
DL = column of lower right corner of scroll window
BH = attribute (alpha modes) or color (graphics modes) to be used on blank line

Scroll Down (AH = 07h)

Scrolls active page down.

Entry Conditions:

AH = 07h
AL = number of lines to scroll; (0 means blank entire window)
CH = row of upper left corner of scroll window
CL = column of upper left corner of scroll window
DH = row of lower right corner of scroll window
DL = column of lower right corner of scroll window
BH = attribute (alpha modes) or color (graphics modes) to be used on a blank line

Read Attribute or Color/Character (AH = 08h)

Reads a character and its attribute or color at the current cursor position.

Entry Conditions:

AH = 08h
BH = display page number (0 based)

Exit Conditions:

AL = character read
AH = attribute of character (alpha modes only)

Write Attribute or Color/Character (AH = 09h)

Writes a character and its attribute or color at the current cursor position.

Entry Conditions:
AH = 09h
BH = display page number (0 based)
CX = number of characters to write
AL = character to write
BL = attribute of character (for alpha modes) or color of character (for graphics modes)

Write Character Only (AH = 0Ah)

Writes a character only (no attribute informationa) at current cursor position.

Entry Conditions:
AH=0Ah
BH=display page number (0 based)
CX=number of characters to write
AL=character to write
BL=color of character (graphics modes only)

Set Color Palette (AH = 0Bh)

Selects the color palette.

Entry Conditions:
AH = 0Bh
BH = 0 (Sets background color for video modes 4 and 5, sets border color for video modes 0, 1, 2, and 3, sets foreground color for video mode 6)
BL = color (0-31)

or

BH = 1 (Sets default palette for modes 4 and 5)
BL = 0 (green/red/brown)
= 1 (cyan/magenta/white)

Write Dot (AH = 0Ch)

Writes a pixel (dot).

Entry Conditions:
AH = 0Ch
BH = display page number
DX = row number
CX = column number

Exit Conditions:
AL = color value. When Bit 7 of AL is set, the resultant color value of the dot is the XOR (exclusive OR) of the current dot color value and the value in AL.

Read Dot (AH = 0Dh)

Reads a pixel (dot).

Entry Conditions:
AH = 0Dh
BH = display page number (0 based)
DX = row number
CX = column number

Exit Conditions:
AL = color value of dot read

Write TTY (AH = 0Eh)

Writes a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions:
AH = 0Eh
AL = character to write
BL = foreground color (graphics mode)

Get CRT Mode (AH = 0Fh)

Get the current video mode.

Entry Conditions:
AH=0Fh

Exit Conditions:

AL=current video mode. See "Set CRT Mode (AH = 0)" for values.
AH=number of columns on screen
BH=current active display page

Set Palette Registers (AH = 10h)

This class of interrupt is a group of subfunctions that set or read the palette registers. The value in AL determines the item that is set or read.

The first chart in this section summarizes the functions available when AH = 10h. Entry and exit conditions applicable to these functions are defined following the chart.

Summary of Palette Register Functions

AL	Description of function
00h	Set individual palette register
01h	Set overscan register
02h	Set all palette and overscan registers
03h	Set intensity/blink bit
07h	Read individual palette register
08h	Read overscan register
09h	Read all palette and overscan registers
10h	Set individual color register
12h	Set block of color registers
13h	Select color page (not valid for mode 13h)
15h	Read individual color register
17h	Read block of color registers
1Ah	Read color page status
1Bh	Sum color registers to gray shades

Summary of Palette Register Functions

Set Individual Palette Register (AL = 00h)

Entry conditions:

AH = 10h
AL = 00h Set individual palette
BL = palette register to set
BH = value to set

Set Overscan Register (AL = 01h)

Entry conditions:

AH = 10h
AL = 01h
BH = value to set

Set Overscan and All Palette Registers (AL = 02h)

Entry conditions:

AH = 10h
AL = 02h
ES:DX = pointer to 17-byte table:
Byte 16 = overscan value
Bytes 15-0 = palette values

Set Intensity/blink Bit (AL = 03h)

Entry conditions:

AH = 10h
AL = 03h
BL = 00h Enable background intensity
= 01h Enable foreground blinking

Read Individual Palette Register (AL = 07h)

Entry conditions:

AH = 10h
AL = 07h
BL = palette register to be read

Exit conditions:

BH = value read

Read Overscan Register (AL = 08h)

Entry conditions:
AH = 10h
AL = 08h

Exit conditions:
BH = value read

Read Overscan and all Palette Registers (AL = 09h)

Entry conditions:
AH = 10h
AL = 09h

Exit conditions:
ES:DX = pointer to buffer (17-byte) for return values:
Byte 16 = overscan value,
Bytes 15 - 0 = register color values

Set Individual Color Register (AL = 10h)

Entry conditions:
AH = 10h
AL = 10h
BX = color register to set
DH = red value to set
CH = green value to set
CL = blue value to set

Set Block of Color Registers (AL = 12h)

Entry conditions:
AH = 10h
AL = 12h
ES:DX = pointer to table of color values (table format: red, green, blue, red, green, blue)
BX = first color register to set
CX = number of color registers to set

Set Color Page
(AL = 13h, not valid for video mode 13h)

Entry conditions:

AH = 10h
AL = 13h
BL = 00h Set color paging mode
BH = 00h Set 4 blocks of 64 registers
= 01h Set 16 blocks of 16 registers
or

BL = 01h Set color page
BH = Set page number (0-based, see AH = 0 for maximum page)

For 64-block/register mode, select:

00h (First block of 64 color registers)
01h (Secnd block of 64 color registers)
02h (Third block of 64 color registers)
03h (Fourth block of 64 color registers)
04h (Fifth block of 16 color registers)
05h (Sixth block of 16 color registers)
06h (Seventh block of 16 color registers)
07h (Eighth block of 16 color registers)
08h (Ninth block of 16 color registers)
09h (Tenth block of 16 color registers)
0Ah (Eleventh block of 16 color registers)
0Bh (Twelfth block of 16 color registers)
0Ch (Thirteenth block of 16 color registers)
0Dh (Fourteenth block of 16 color registers)
0Eh (Fifteenth block of 16 color registers)
0Fh (Sixteenth block of 16 color registers)

Note: The SET mode function (INT 10h, AH = 0) defaults to the 64-register/block mode and only sets the first 64 color registers active. When page selection is used, alternate blocks of color registers must be initialized.

Read Individual Color Register (AL = 15h)

Entry conditions:

AH = 10h
AL = 15h
BX = color register to read

Exit conditions:

DH = red value read
CH = green value read
CL = blue value read

Read Block of Color Registers (AL = 17h)

Entry conditions:

AH = 10h
AL = 17h
BX = initial color register to read
CX = number of color registers to read
ES:DX = pointer to a buffer to store the color register values
(format: red, green, blue, red, green, blue)

Exit conditions:

ES:DX = pointer to values read

Read Color Page Status (AL = 1Ah)

Entry conditions:

AH = 10h
AL = 1Ah

Exit conditions:

BL = current paging mode
BH = current page

Sum Color Registers to Gray Shades (AL = 1Bh)

Entry Conditions:
AH = 10h
AL = 1Bh
BX = initial color register to sum
CX = number of registers to sum

Note: This call reads the red, green and blue values stored in the specified color registers and performs a weighted sum:

Gray shade = 30% red + 59% green + 11% blue.

The resulting red, green, and blue values are written to the specified color registers. The original contents of each register are not retained.

Character Generator Functions (AH = 11h)

This class of interrupt is a group of 14 subfunctions that, in one way or another, permit the loading and/or enabling of text mode and graphics mode character generators (fonts). For all these subfunctions, AH = 11h; the value in AL determines the specific subfunction to be performed.

The first chart in this section summarizes the character generator subfunctions. The rest of this section summarizes the entry and exit conditions applicable to these functions.

AL	Description of function
00h	Load user specified alphanumeric font
01h	Load ROM 8 x 14 font
10h	Load user font & adjust character height
11h	Load ROM 8 x 14 font & adjust height
12h	Load ROM 8 x 8 double dot font
14h	Load ROM 8 x 16 font
20h	Set user graphics font pointer at INT 1Fh
21h	Set user graphics font pointer at INT 43h
22h	Use ROM 8 x 14 font for graphics
23h	Use ROM 8 x 8 dot font for graphics
24h	Use ROM 8 x 16 font for graphics
30h	Font pointer information

Summary of Palette Register Functions

Load User Specified Alphanumeric Font (AL = 00h)

Entry Conditions:

AH = 11h
AL = 00h
BH = number of bytes per character
BL = block to load (0-7)
CX = number of characters to store
DX = character offset of first character
in ES:BP table
ES:BP = pointer to the user table

Load ROM 8x14 Font (AL = 01h)

Entry Conditions:

AH = 11h
AL = 01h
BL = block to load (0-7)

Load 8x8 Double Dot Font (AL = 02h)

Entry Conditions:

AH = 11h
AL = 03h
BL = select character generator block(s)
If Bit 3(BL)=0, Bits 1,0(BL) select a block, 0-3
If Bit 3(BL)=1, Bits 3,2(BL) select a block, 0-3

Load User Font & Adjust Character Height (AL = 10h)

Entry Conditions:

AH = 11h
AL = 10h
BH = number of bytes per character
BL = block to load (0-7)
CX = number of characters to store
DX = offset to first character in ES:BP table
ES:BP = pointer to table

Load ROM 8x14 Font (AL = 11h)

Entry Conditions:

AH = 11h
AL = 11h
BL = block to load (0-7)

Load ROM 8x8 Double Dot Font (AL = 12h)

Entry Conditions:

AH=11h
AL=12h
BL=block to load

Load ROM 8x16 Font (AL = 14h)

Entry Conditions:

AH = 11h
AL = 14h
BL = block to load

Set User Graphics Font Pointer at INT 1Fh (AL = 20h)

This subfunction sets the graphics font pointer to the vector contained in INT 1Fh. The INT 1Fh vector is specified in ES:BP.

Entry Conditions:

AH = 11h
AL = 20h
ES:BP = pointer to store at INT 1Fh vector (which points to the user graphics font table)

Set User Graphics Font Pointer at INT 43h (AL = 21h)

Entry Conditions:

AH = 11h
AL = 21h
BL = rows on screen specifier:
= 00h User supplied value (DL = rows)
= 01h 14 rows
= 02h 25 rows
= 03h 43 rows
ES:BP = pointer to user table
CX = points (bytes/character)

Use ROM 8x14 Font for Graphics (AL = 22h)

Entry Conditions:
AH = 11h
AL = 22h
BL = row specifier

Use ROM 8x8 Double Dot Font for Graphics (AL = 23h)

Entry Conditions:
AH = 11h
AL = 23h
BL = row specifier

Use ROM 8x16 Font for Graphics (AL = 24h)

Entry Conditions:
AH = 11h
AL = 24h
BL = row specifier

Font Pointer Information (AL = 30h)

Entry Conditions:
AH = 11h
AL = 30h
= font pointer
BH = 00h return current INT 1Fh pointer
= 01h return current INT 44h pointer
= 02h return ROM font 8x14 pointer
= 03h return current ROM 8x8 font pointer
= 04h return current ROM 8x8 font pointer (top)
= 05h return current ROM 9x14 font alternate
= 06h return current ROM 8x16 font pointer
= 07h return current ROM 9x16 font alternate

Exit Conditions:
CX = bytes per character
DL = maximum screen row number
ES:BP = pointer to character table

Alternate Select (AH = 12h)

Alternate select allows the user to enable or disable certain operations which are standard video mode defaults.

Return VGA Information:
BL = 10h

Entry Conditions:
AH = 12h
BL = 10h

Exit Conditions:
BL = memory available
= 00h 64K
= 01h 128K
= 02h 192K
= 03h 256K
BH = 00h color mode set
= 01h monochrome mode set
CH = adapter bits
CL = switch setting

Switch to Alternate Print Screen Routine (BL = 20h)

Entry Conditions:
AH = 12h
BL = 20h

Select Scan Lines for Alphanumeric Modes (BL = 30h)

Entry Conditions:
AH = 12h
BL = 30h
AL = 00h 200 scan lines
= 01h 350 scan lines
= 02h 400 scan lines

Exit Conditions:
AL = 12h Function supported

Default Palette Loading During Set Mode (BL = 31h)

Entry Conditions:
AH = 12h
BL = 31h
AL = 00h Enable default palette loading
= 01h Disable default palette loading

Exit Conditions:
AL = 12h Function supported

Video Enable/Disable (BL = 32h)

Entry Conditions:
AH = 12h
BL = 32h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Summing to Gray Shades (BL = 33h)

Entry Conditions:
AH = 12h
BL = 33h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Enable/Disable Cursor Scaling (BL = 34h)

Entry Conditions:
AH = 12h
BL = 34h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Display Switch (BL = 35h)

Entry Conditions:

AH = 12h
BL = 35h
AL = 00h Turn off initial video adapter (Must have 128 byte save area pointed to by ES:DX)
= 01h Turn on initial system board video
= 02h Disable active video (Must have save buffer pointer in ES:DX)
= 03h Enable inactive video (Must have ES:DX pointer to previously filled save buffer)
ES:DX= pointer to switch state save area buffer

Exit Conditions:

AL = 12h Function supported

Note: If a conflict arises between the on-board video and an external video adapter, the on-board video is initialized inactive. If no conflict arises, both video systems remain active, and this function allows switching between the two systems.

Video Screen ON/OFF (BL = 36h)

Entry Conditions:

AH = 12h
BL = 36h
AL = 01h Screen OFF
= 00h Screen ON

Exit Conditions:

AL = 12h Function supported

Write String (AH = 13h)

Writes a string of characters.

Entry Conditions:

AH = 13h
ES:BP = pointer to string of characters to write
CX = number of string characters to display
DX = starting cursor position (DH=row, DL=column)
BH = page number (for alpha modes)
BL = attribute for characters (if attributes are not in the string, see below)
AL 0 = Cursor is not moved, string is characters only, attribute is in BL
1 = Moves cursor to the next character position after the last character written, string is characters only, attribute is in BL
2 = Cursor is not moved, string has alternating characters and attributes
3 = Moves cursor to the next character position after the last character written, string has alternating characters and attributes

Read/Write Display Code (AH = 1Ah)

Read and write the display combination code for various combinations of video adapter and monitor hardware.

Display Code Chart

This chart defines the codes used by the display code functions.

Display Codes	Description
00h	No display attached
01h	Monochrome Display Adapter (MDA) with monochrome monitor
02h	Color Graphics Adapter (CGA) with color monitor
03h	Reserved
04h	Enhanced Graphics Adapter (EGA) with color monitor
05h	EGA with monochrome monitor
06h	Professional Graphics Adapter (PGA) with color monitor
07h	Video Graphics Array (VGA) with monochrome analog monitor
08h	VGA with color analog monitor
09h-0Ah	Reserved
0Bh	Multi-color Graphics Array (MCGA) with monochrome analog monitor
0Ch	MCGA with color analog monitor
0Dh-FEh	Reserved
FFh	Reserved

Read Display Combination Code (AL = 00h)

See "Display Code Chart" for definitions of code values.

Entry Conditions:
AH = 1Ah
AL = 00h

Exit Conditions:
AL = 1AhFunction supported
BL = active display code
BH = inactive display code

Write Display Code (AL = 01h)

See "Display Code Chart" for definitions of code values.

Entry Conditions:
AH = 1Ah
AL = 01h
BL = active display code
BH = alternate display code

Exit Conditions:
AL = 1Ah Function supported

Functionality/State Information (AH = 1Bh)

Returns information about the video subsystem. See the functionality/state table below.

Entry Conditions:
AH = 1Bh
BX = 0000h Implementation Type
ES:DI = Pointer to 40h byte Functionality/State Table

Exit Conditions:
Functionality/State Information in buffer
AL = 1Bh Function supported

Offset	Size	Description
DI+00h	1 word	Offset from top of Functionality /State table
DI+02h	1 word	Segment of functionality/state table
DI+04h	1 Byte	Video Mode
DI+05h	1 Word	Number of screen columns
DI+07h	1 Word	Length of display buffer in bytes
DI+09h	1 Word	Starting address of display buffer
DI+0Bh	1 Word	Cursor positions for all 8 video pages
DI+IBh	1 Word	Cursor type
DI+IDh	1 Byte	Active page
DI+IEh	1 Word	CRT controller base address
DI+20h	1 Byte	Current 3x8 register value
DI+21h	1 Byte	Current 3x9 register value
DI+22h	1 Byte	Number of screen rows
DI+23h	1 Word	Character height in scan lines
DI+25h	1 Byte	Active display combination code
DI+26h	1 Byte	Inactive display combination code
DI+27h	1 Byte	# colors available in video mode
DI+29h	1 Byte	Display pages supported for current video mode
DI+2Ah	1 Byte	Number of scan lines in current video mode: 00 = 200 01 = 350 02 = 400 03 = 480
DI+2Bh	1 Byte	Primary character block number (0-255)
DI+2Ch	1 Byte	Secondary character block number (0-255)

Funtionality/State Table

Offset	Size	Description
DI+2Dh	1 Byte	Miscellaneous state information Bits 7-6 Reserved Bit 5=0 Background intensity =1 Blinking Bit 4=1 Cursor emulation active Bit 3=1 Mode set palette loading is disabled Bit 2=1 Mono display is attached Bit 1=1 Gray scale summing active Bit 0=1 All modes on all displays active
DI+2Eh	1 Byte	Reserved
DI+2Fh	1 Byte	Reserved
DI+30h	1 Byte	Reserved
DI+31h	1 Byte	Video memory available 00 = 64K 01 = 128K 02 = 192K 03 = 256K
DI+32h	1 Byte	Save pointer state info (1=active) Bits 7-6 = Reserved Bit 5 = Display Combination Code Extension Bit 4 = Palette override Bit 3 = Graphics font override Bit 2 = Text mode font override Bit 1 = Dynamic save area Bit 0 = 512-character set
DI+33h to 3Fh	13 Bytes	Reserved
00h		Video modes supported (1=supported) Bit 7 = mode 07h Bit 6 = mode 06h Bit 5 = mode 05h Bit 4 = mode 04h Bit 3 = mode 03h Bit 2 = mode 02h Bit 1 = mode 01h Bit 0 = mode 000

Functionality/State Table (cont'd.)

Offset	Size	Description
01h		Video modes supported (1=supported) Bit 7 = mode 0Fh Bit 6 = mode 0Eh Bit 5 = mode 0Dh Bit 4 = mode 0Ch Bit 3 = mode 0Bh Bit 2 = mode 0Ah Bit 1 = mode 09h Bit 0 = mode 08h
02h		Video modes supported (1=supported) Bits 7-4 = Reserved Bit 3 = mode 13h Bit 2 = mode 12h Bit 1 = mode 11h Bit 0 = mode 10h
03h-06h		Reserved
07h		Scan line modes available for text modes (1 = supported) Bits 7-3 = Reserved Bit 2 = 400 Bit 1 = 350 Bit 0 = 200
08h		Number of character blocks available in text modes
09h		Maximum number of active character blocks available in text modes
0Ah		Miscellaneous (1 = supported) Bit 7 = Color paging Bit 6 = Color palette Bit 5 = EGA palette Bit 4 = Cursor emulation Bit 3 = Default palette loading Bit 2 = Character font loading Bit 1 = Gray scale summing Bit 0 = All modes on all displays

Funtionality/State Table (cont'd.)

0Bh		Miscellaneous (1 = supported) Bits 7-4 Reserved Bit 3 = Display combination codes Bit 2 = Background intensity/ blinking control Bit 1 = Save/restore video state Bit 0 = Light pen
0Ch-0Dh		Reserved
0Eh		Save pointer functions(1=supported) Bits 7-6 = Reserved Bit 5 = DCC extension Bit 4 = Palette override Bit 3 = Graphics font override Bit 2 = Text mode font override Bit 1 = Dynamic save area Bit 0 = 512 character set
0Fh		Reserved

Functionality/State Table (cont'd.)

Save/Restore Video State (AH = 1Ch)

These subfunctions save and restore the current video state.

Save/Restore Buffer Size (AL = 00h)

Entry Conditions:

AH =1Ch
AL =00h
CX =video state to store
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state

Exit Conditions:

AL = 1Ch Function is supported
BX = buffer size block count (1 block = 64 bytes)

Save Current Video State (AL = 01h)

Entry Conditions:

AH = 1Ch
AL = 01h
CX = video state to store
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state
ES:BX = pointer to buffer save state

Exit Conditions:

AL = 1Ch Function is supported

Restore Video State (AL = 02h)

Entry Conditions:

AH = 1Ch
AL = 02h
CX = video state to restore
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state
ES:BX = pointer to previously saved buffer

Exit Conditions:

AL = 1Ch Function is supported

Interrupt 11h: Equipment Functions

Equipment functions return the equipment flag (hardware configuration of the computer system) in the AX register. Various bits in the equipment flag indicate the presence or absence of particular devices.

Any device bit that is set (has a value of 1) indicates that the specified device is in the system. A device bit that is reset (has a value of 0) indicates the the specified device is not in the system.

The equipment flag bits have the following meanings:

Bits	Function
15,14	number of printers
13,12	not used
11,10,9	number of RS-232 cards
8	not used
7,6	number of diskette drives (only if Bit 0=1) 00 = 1 01 = 2
5,4	initial video mode 01 = 40x25 BW on color graphics adapter 10 = 80x25 BW on color graphics adapter 11 = 80x25 BW on monochrome text adapter
3	not used
2	pointing device 0,1
1	math coprocessor 0,1
0	diskette drive 0,1

Interrupt 12h: Memory Size Functions

This service returns the total number of kilobytes of RAM in the computer (contiguous starting from address 0) in AX. The maximum value returned is 640 (280h).

Software Interrupt: 12h (18 dec)

Interrupt 13h: Diskette Drive I/O Support Functions

These routines control diskette drive operation. The function performed depends on the value in Ah:

Value in AH	Description of Function
00h	Reset all disks
01h	Return status of last disk operation
02h	Read sectors from disk
03h	Write sectors to disk
04h	Verify sectors on disk
05h	Format track on disk
08h	Read drive parameters
15h	Read disk type
16h	Get diskette change line status
17h	Set diskette type for format
18h	Set media type for format

Reset All Disks

Resets the floppy diskette system, reset associated hardware, and recalibrate all drives.

Entry Conditions:
AH = 00h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Return Status of Last Diskette Operation

Return the status of the last diskette operation in AH.

Entry Conditions:
AH = 01h
DL = 80h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Read Sectors From Disk

Reads the specified sectors from disk into RAM.

Entry Conditions:

AH = 02h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to read (1-18)
ES:BX = pointer to disk buffer

Exit Conditions:

See "Exits From All Floppy Disk Calls."

Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:

AH = 03h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to write (1-18)
ES:BX = pointer to disk buffer

Exit Conditions:

See "Exits From All Floppy Disk Calls."

Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:

AH = 04h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to verify (1-18)

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Format Track On Disk

Format the specified track.

Note: Function Call 23 must be performed before using this routine.

To format 360K diskettes, change the gap length for format and end of track parameters of the Floppy Disk Parameter table (INT 1Eh). Restore these parameters when formatting is complete.

Entry Conditions:
AH = 05h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
AL = number of sectors per track (used only for DMA bound check)
ES:BX = pointer to sector format table consisting of four bytes per sector:
The first byte is the track number
The second byte is the head number
The third byte is the sector number
The fourth byte is the sector size code:
00 = 128 bytes/sector
01 = 256 bytes/sector
02 = 512 bytes/sector
03 = 1024 bytes/sector

Example: For Track 0, Head 1, on a nine-sector/track diskette formatted with an interleave of 1 (512 bytes/sector) the table would be:

00h,01h,01h,02h; 00h,01h,02h,02h; 00h,01h,03h,02h;
00h,01h,04h,02h; 00h,01h,05h,02h; 00h,01h,06h,02h;
00h,01h,07h,02h; 00h,01h,08h,02h; 00h,01h,09h,02h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Read Drive Parameters

Read parameter table for the selected drive.

Entry Conditions:
AH = 08h
DL = drive number (0-1)

Exit Conditions:
ES:DI = Floppy Disk Parameter table
CH = maximum number of tracks (low 8 bits of 10-bit value)
CL = Bits 7-6: Maximum number of tracks (high 2 bits of 10-bit value)
Bits 5-0: Maximum sectors per track
DH = maximum head number
DL = number of disk drives installed
BH = 0

BL = Bits 7-4: 0
Bits 3-0: Drive type value in CMOS:
0 Drive type known but CMOS type is invalid, CMOS is not present, CMOS battery discharged or CMOS checksum invalid
1 360KB, 5¼-inch, 40 track
2 1.2 Mb, 5¼-inch, 80 track
3 720K, 3½-inch, 80 track
4 1.44 Mb, 3½-inch, 80 track

Read Disk Type

Return the disk type.

Entry Conditions:
AH = 15h
DL = drive number (0-1)

Exit Conditions:
[C] = Error (possibly no drive installed)
[NC] = Operation successful. Status in AH
AH 0 = not present
1 = diskette with no change line
2 = diskette with change line
3 = hard disk

Get Disk Change Line Status

Test to see if diskette has changed.

Entry Conditions:
AH = 16h
DL = drive number (0-1)

Exit Conditions:
AH 00 = [NC] diskette has not changed
06 = [C] diskette has changed

Also, see "Exits From All Floppy Disk Calls."

Set Disk Type for Format

Set the diskette type for the next FORMAT command.

Entry Conditions:
AH = 17h
AL 00 = not used
01 = 360K media in a 360K drive
02 = 360K media in a 1.2M drive
03 = 1.2M media in a 1.2M drive, or 1.44M media in a 1.44M drive
04 = 720K disk in 720K drive
DL = drive number (0-1)

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Set Media Type for Format

Set the media type for the selected drive.

Entry Conditions:
AH=18h
DL=drive number (0-1)
CH=number of tracks (low 8 bits of 10-bit value)
CL = Bits 7-6: Number of tracks (high 2 bits of 10-bit value)
Bits 5-0: Sectors per track

Exit Conditions:
ES:DI=Floppy Disk Parameter table

Also, see "Exits From All Floppy Disk Calls."

Exits From All Floppy Disk Calls

[NC] = operation was successful (AH = 00h)
[C] = operation failed
AH 01h = Bad command or parameter
02h = Address mark not found
03h = Write protected
04h = Sector not found
06h = Diskette has changed
08h = DMA overrun error
09h = DMA boundary error
10h = Bad CRC on disk read
20h = Controller failed
40h = Seek failed
80h = Device timeout

Interrupt 1Eh: Diskette Drive Parameter Functions

This interrupt accesses the double word pointer to the current diskette drive parameter block. To change the way the floppy disk driver operates, build another parameter block and load the segment and offset of this parameter block into the software interrupt 1E hex vector area.

The layout of the Floppy Disk Parameter table is:

Offset	Length	Description
10	1 byte	Motor startup time (increments of 1/8 second)
9	1 byte	Head settle time (ms)
8	1 byte	Fill byte for format
7	1 byte	Gap length for format
6	1 byte	Data transfer length
5	1 byte	Gap length
4	1 byte	Sectors per track
3	1 byte	Number of bytes per sector: 0 = 128 bytes per sector 1 = 256 bytes per sector 2 = 512 bytes per sector 3 = 1024 bytes per sector
2	1 byte	Number of ticks to wait before turning disk drive motor off
1	1 byte	Second specify byte
0	1 byte	First specify byte

Interrupt 13h: Hard Disk I/O Support

The following routines provide access to hard disk operations, depending on the value in AH:

Value in AH	Description of Function
00h	Reset all disks
01h	Return status of last disk operation
02h	Read sectors from disk
03h	Write sectors to disk
04h	Verify sectors on disk
05h	Format track on disk
06h	Unused
07h	Unused
08h	Return current hard disk parameters
09h	Initialize hard disk parameters
0Ah	Read long
0Bh	Write long
0Ch	Perform seek on hard disk
0Dh	Reset hard disk
0Eh	Unused
0Fh	Unused
10h	Test for hard disk ready
11h	Recalibrate hard disk
12h	Unused
13h	Unused
14h	Controller internal diagnostic
15h	Read disk type

Reset Hard Disks

Reset the hard disk system. Reset associated hardware, and recalibrate all drives.

Entry Conditions:

AH=00h
DL=drive number (80h-81h)

Exit Conditions:

See "Exits From All Hard Disk Calls."

Return Status of Last Hard Disk Operation

Return the status of the last hard disk operation in AL.

Entry Conditions:
AH = 01h
DL = 80h

Exit Conditions:
AL = status of the last operation. See "Exits From All Hard Disk Calls," for values.

Read Sectors From Disk

Read the specified sectors from disk into RAM.

Entry Conditions:
AH = 02h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to read (1-80h)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:
AH = 03h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to write (1-80 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:
AH = 04h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to verify (1-80 hex)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Format Track On Disk

Formats the specified track.

Entry Conditions:
AH = 05h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
ES:BX = pointer to sector format table consisting of two bytes for each sector. The first byte is 00 for a good sector, and 80h for a bad sector. The second byte is the sector number.

Example: For a 17-sector track with an interleave of 2, the table is:

00h,01h; 00h,0Ah; 00h,02h; 00h,0Bh; 00h,03h; 00h,0Ch; 00h,04h; 00h,0Dh; 00h,05h; 00h,0Eh; 00h,06h; 00h,0Fh; 00h,07h; 00h,10h; 00h,08h; 00h,11h; 00h,09h

Exit Conditions:
See "Exits From All Hard Disk Calls."

Return Current Hard Disk Parameters

Returns current parameter values for the specified hard disk.

Entry Conditions:
AH = 08h
DL = drive number (80h-81h)

Exit Conditions:
DL=number of hard disk drives attached
DH=maximum usable value for head number
CH=least significant part of maximum usable value for cylinder number
CL Bits 7-6 = most significant part of maximum usable value for cylinder number
CL Bits 5-0 = maximum usable value for sector number
See also "Exits From All Hard Disk Calls."

Initialize Hard Disk Parameters

Initialize the hard disk parameters for the specified hard disk. The values are taken from the current drive parameter table pointed to by INT 41h for Drive 80h, and INT 46h for Drive 81h.

Entry Conditions:
AH= 09h
DL= drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Read Long

Read specified sectors and four ECC bytes per sector from disk to RAM.

Entry Conditions:
AH = 0Ah
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023). (See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1 -17)
AL = number of sectors to read (1-79 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Write Long

Write specified sectors plus four ECC bytes per sector from RAM to disk.

Entry Conditions:
AH = 0Bh
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023).
(See CL Bits 7, 6)
CL Bits 7-6 = most significant part of cylindernumber
CL Bits 5-0 = sector number (1 -17)
AL = number of sectors to write (1-79 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Perform Seek On Hard Disk

Seek to the specified hard disk track.

Entry Conditions:
AH = 0Ch
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023).
(See CL Bits 7, 6)
CL Bits 7-6 = most significant part of cylinder number
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Reset Hard Disk

Reset the hard disk system. Reset associated hardware, and recalibrate all hard disk drives.

Entry Conditions:
AH = 0Dh
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Test For Hard Disk Ready

Determine whether a specified hard disk is ready.

Entry Conditions:
AH = 10h
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Recalibrate Hard Disk

Recalibrate the specified hard disk drive.

Entry Conditions:
AH = 11h
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Controller Internal Diagnostic

Perform internal hard disk controller diagnostics.

Entry Conditions:
AH= 14h
DL= drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Read Disk Type

Return the disk type and the number of sectors available on the hard disk.

Entry Conditions:
AH = 15h
DL = drive number (80h-81h)

Exit Conditions:
AH 0 = Not present
3 = Hard disk drive
CX:DX = Number of sectors available on the hard disk.
(Assumes 512 byte sectors)

Exits From All Hard Disk Calls

[NC] = operation was successful (AH = 00h)
[C] = operation failed
AH 01h = Bad command or parameter
02h = Address mark not found
03h = Write protect error
04h = Sector not found
05h = Reset failed
07h = Drive parameter command failed
08h = DMA overrun
09h = DMA boundary error
0Ah = Bad sector flag detected
0Bh = Bad cylinder detected
0Dh = Invalid number of sectors on format
0Eh = Control data address mark detected
0Fh = DMA arbitration level out of range
10h = Bad ECC on disk read
11h = Data corrected during read
20h = Controller failed
40h = Seek failed
80h = Device timeout
AAh = Drive not ready
BBh = Undefined error occurred
CCh = Write error

Interrupts 41h and 46h: Hard Disk Parameter Functions

Characteristics of the hard disk are stored in the Hard Disk Parameter table. To read the values, load the segment and offset stored at the appropriate software interrupt vector area. Interrupt 41h applies to hard disk 0; interrupt 46h applies to hard disk 1.

The layout of the Hard Disk Parameter table is:

Offset	Length	Description
15	1 byte	Reserved
14	2 bytes	Sectors per track
12	2 bytes	Landing zone
11	1 byte	Not used
10	1 byte	Not used
9	1 byte	Not used
8	1 byte	Control byte: Bit 7: Disable retries -or- Bit 6: Disable retries Bit 5: Defect Map Present at Maximum Cylinders+1 Bit 3: More than 8 heads
7	1 byte	Not used
5	2 bytes	Starting Write Precompensation cylinder
3	2 bytes	Not used
2	1 byte	Maximum number of heads
0	2 bytes	Maximum number of cylinders

Interrupt 14h: Serial Communications Functions

These routines provide asynchronous byte-stream I/O to and from the RS-232C serial communications port. The function performed depends on the value in AH, and the port affected depends on the value in DX:

Register and Value	Meaning
AH = 00h	Initialize comm port
AH = 01h	Transmit character
AH = 02h	Receive character
AH = 03h	Get current comm status
DX=0 or 1	Port number

Initialize Comm Port

Initialize the communication port according to the parameters in AL and DX.

Entry Conditions:

DX = Communications port number (0 or 1)
AL = RS-232C parameters, as follows:
AH = 00h

Baud Rate (Bits 7 6 5)	Parity (Bits 4 3)	Stop Bits (Bit 2)	Word Length (Bits 1 0)
000 = 110 baud 001 = 150 baud 010 = 300 baud 011 = 600 baud 100 = 1200 baud 101 = 2400 baud 110 = 4800 baud 111 = 9600 baud	x0 = none 01 = odd 11 = even	0 = 1 bit 1 = 2 bits	10 = 7 bits 11 = 8 bits

Exit Conditions:

AX = RS-232 status; see "Get Current Comm Status" (AH = 03h)

Transmit Character

Transmit (output) the character in AL

Entry Conditions:

AH=01h
AL=character to transmit
DX=port number (0 or 1)

Exit Conditions:

AH=RS-232 status; see "Get Current Comm Status (AH = 03h). If Bit 7 is set, the routine is unable to transmit the character because of a timeout error.
AL is preserved.

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH contains the RS-232 status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout Bit (7), if set, indicates that data set ready was not received. Thus, AH is non zero only when an error occurs. If Bit 7 is set, the other bit values are not meaningful.

Entry Conditions:

AH=02h
DX=port number (0 or 1)

Exit Conditions:

AL=character received
AH=RS-232 status; see "Get Current Comm Status" (AH = 03h)

Get Current Communications Port Status

Read the communication port status in AX.

Entry Conditions:

AH=03h
DX=port number (0 or 1)

Exit Conditions:

AH = RS-232 status, as follows (set = true):
- Bit 7 = timeout occurred
- Bit 6 = transmitter shift register empty
- Bit 5 = transmitter holding register empty
- Bit 4 = break detect
- Bit 3 = framing error
- Bit 2 = parity error
- Bit 1 = overrun error
- Bit 0 = data ready

AL = modem status, as follows (set = true):
- Bit 7 = receive line signal detect
- Bit 6 = ring indicator
- Bit 5 = data set ready
- Bit 4 = clear to send
- Bit 3 = delta receive line signal detect
- Bit 2 = trailing edge ring detector
- Bit 1 = delta data set ready
- Bit 0 = delta clear to send

Interrupt 15h: System Support Functions

The functions in this group control hooks, joystick support, microsecond delay, virtual mode support, extended memory support, and EISA system information. The function performed depends on the value in AH.

Value in AH	Function
80h	Device Open
81h	Device Close
82h	Program Terminate
83h	Event Wait
84h	Joystick Support
85h	System Request Key Support
86h	Wait
87h	Move Block of Memory
88h	Extended Memory Size
89h	Processor to Virtual Mode
90h	Device Busy Wait Loop
91h	Interrupt Complete
C0h	System Configuration Parameters
C1h	Return extended BIOS data area segment address
C2h	Pointing device interface
C3h	Fail Safe Timer
D8h	Access EISA system information

Device Open

Entry Conditions:

AH = 80h
BX = Device ID
CX = Process ID

Exit Conditions:

None

Device Close

Entry Conditions:
AH = 81h
BX = Device ID
CX = Process ID

Exit Conditions:
None

Program Terminate

Entry Conditions:
AH = 82h
BX = Device ID

Exit Conditions:
None

Event Wait

Entry Conditions:

AH = 83h
AL = 0 Set interval
ES:BX = Pointer to a byte in caller's memory that has the sign bit set after the time interval expires
CX,DX = The number of microseconds to elapse before the high order byte in the caller's memory pointed to by ES:BX is set. Granularity is 976 microseconds
AL = 1 Cancel event wait

Exit Conditions:
None

Joystick Support

Entry Conditions:

AH = 84h
DX = 0 Read the current joystick button setting. On return, AL (Bits 4-7) contains the button settings:
Bit 4: Joystick A, Button 1
Bit 5: Joystick A, Button 2
Bit 6: Joystick A, Button 1
Bit 7: Joystick B, Button 2
DX = 1 Read the resistive inputs of the game adapter. The following values are returned:
AX = Joystick A x value
BX = Joystick A y value
CX = Joystick B x value
DX = Joystick B y value

System Request Key Support

Entry Conditions:
AH = 85h

Exit Conditions:
AL = 0 Sys Req key pressed
AL = 1 Sys Req key released

Wait

Wait indicated number of microseconds.

Entry Conditions:
AH = 86h Wait indicated number of microseconds
CX,DX = Number of microseconds to wait before returning. Granularity is 976 microseconds

Exit Conditions:
[C] = Successful wait
[NC] = Wait function already in progress

Move Block of Memory

Transfers the contents of a block of memory from memory addressed above 1024K to memory addressed below 1024K. This uses the 80286 processor "protected" mode.

Entry Conditions:

AH = 87h
ES:SI = A pointer to a Global Descriptor Table (GDT) as defined in the following table. The calling program must have previously set up this table.
CX = Number of 16-bit words to be transferred. (Max count=8000h) The source and destination global descriptors must contain a length field of at least (2 * CX - 1)

Exit Conditions:

AH = 00h Operation successful
AH = 01h RAM parity error
AH = 02h Exception interrupt occurred
AH = 03h Gating of address line 20h failed
Carry flag set if error
Zero flag set if successful

GDT Descriptor	Usage (each entry is 8 bytes)
0	Dummy
1	Segment address of this GDT
2	Pointer to area from which to move data
3	Pointer to segment to receive the data
4	BIOS code segment descriptor
5	BIOS stack segment descriptor

Extended Memory Size

Returns the amount of extended memory starting at address 1024K.

Entry Conditions:

AH = 88h

Exit Conditions:

AX = Amount of contiguous available memory in kilobytes starting at address 1024K

Processor to Virtual Mode

Set the 80286 in protected virtual memory mode.

Entry Conditions:

AH = 89h
ES:SI = Pointer to a Global Descriptor Table (GDT) set up by the calling program as defined in the following table
BH = Offset within the Interrupt Descriptor Table (IDT) that contains the first eight interrupts
BL = Offset within the Interrupt Descriptor Table that contains the second eight hardware interrupts

Exit Conditions:

AH = 00h Operation successful

Note: All segment registers are changed, AX and BP registers modified.

GDT Descriptor	Usage (each entry is 8 bytes)
0	Dummy
1	Segment address of this GDT
2	Pointer to the IDT
3	Pointer to user's data segment
4	Pointer to user's extra segment
5	Pointer to user's stack segment
6	Pointer to user's code segment
7	Pointer to BIOS code segment

Device Busy Wait Loop

Entry Conditions:

AH=90h
AL=Type code groups
00h - 7Fh = Non re-entrant devices
80h - BFh = Re-entrant devices. ES:BX points to data block
C0h - FFh = Wait only

Exit Conditions:

None

Interrupt Complete

Entry Conditions:
AH = 91h
AL = Type code (See function AH = 90h)
00h = Disk (time-out)
01h = Diskette (time-out)
02h = Keyboard (no time-out)
03h = Pointing Device (time-out)
80h = Network (no time-out)
FDh = Diskette Drive Motor Start (time-out)
FEh = Printer (time-out)

Exit Conditions:
None

System Configuration Parameters

Returns pointer to system description vector in ROM.

Entry Conditions:
AH = C0h

Exit Conditions:
AH = 00h
ES:BX = Pointer to system descriptor vector

Offset	Length	Description
0	2 bytes	Byte count of data that follows; minimum length 8
2	1 byte	Model byte
3	1 byte	Sub-Model byte
4	1 byte	BIOS revision level (00 is first release)
5	1 byte	Feature information byte 1: Bit 7: Hard Disk BIOS uses DMA channel 3 Bit 6: 2nd interrupt chip present Bit 5: Real-time clock present Bit 4: Keyboard intercept sequence (INT 15h) called in keyboard interrupt (INT 09h) Bit 3: Wait for external event supported Bit 2: Extended BIOS area is allocated Bit 1: Micro Channel implemented Bit 0: Reserved
6	4 bytes	Feature information byte Bits 2-5 - reserved

Return Extended BIOS Data Area Segment Address (AH = C1h)

Returns the address of the data segment of the extended BIOS DATA AREA.

Entry Conditions:

AH = C1h

Exit Conditions:

ES = extended BIOS data area segment address
CF = 0 No error
= 1 Error

Enable/Disable Pointing Device Interface (AH =C2h)

Entry Conditions:

AH = C2h
AL = 00h
BH = 00h Disable
= 01h Enable

Exit Conditions:

AH = 00h No error
= 01h Invalid function call
= 02h Invalid input error
= 03h Interface error
= 04h Resend
= 05h No far call installed
CF = 00h Operation succesfully completed
= 01h Operation unsuccessful

Reset Pointing Device

Entry Conditions:

AH = C2h
AL = 01h

Exit Conditions:

AH = See return for AL = 00
BH = 00h Device ID
BL = Modified
CF = 0 Operation successful
= 1 Operation unsuccessful

Set Sample Rate

Entry Conditions:

AH = C2h
AL = 02h
BH = sample rate value (00h to 06h) where:
00 = 10 reports/second
01 = 20 reports/second
02 = 40 reports/second
03 = 60 reports/second
04 = 80 reports/second
05 = 100 reports/second
06 = 200 reports/second

Exit Conditions:

See return for AL = 00h

Set Resolution

Entry Conditions:

AH = C2h
AL = 03h
BH = resolution value
00h = 1 count/millimeter
01h = 2 counts/millimeter
02h = 4 counts/millimeter
03h = 8 counts/millimeter

Exit Conditions:

AH = 0 See return for AL = 00
CF = 0 Operation successful
= 1 Operation unsuccessful

Read Device Type

Entry Conditions:

AH = C2h
AL =04h

Exit Conditions:

AH = See return for AL = 00
BH = Device ID
= 00h

Pointing Device Interface Initialization

Entry Conditions:

AH = C2h
AL = 05h
BH = data package size (01h-08h, in bytes)

Exit conditions:

AH = See return for AL = 00h
CF = 0 Operation successful
= 1 Operation unsuccessful

Extended Commands

Entry Conditions:

AH = C2h
AL = 06h
BH = 00h Return status
= 01h Set scaling factor to 1:1
= 02h Set scaling factor 2:1

Exit Conditions:

AH = See return for AL = 00h
CF = 0 Operation successful
= 1 Operation unsuccessful

For return status (BH = 0) subfunction only:
BL = Status Byte 1, where:
Bit 7 = 0 Reserved
Bit 6 = 0 Stream mode
= 1 Remote mode
Bit 5 = 1 Enable
= 0 Disable
Bit 4 = 0 1:1 scaling
= 1 2:1 scaling
Bit 3 = 0 Reserved
Bit 2 = 1 Left button pressed
Bit 1 = 0 Reserved
Bit 0 = 1 Right button pressed
CL = Status Byte 2, where:
00h = 1 count/millimeter
01h = 2 counts/millimeter
02h = 4 counts/millimeter
03h = 8 counts/millimeter
DL = Status Byte 3, where:
0Ah = 10 reports/second
14h = 20 reports/second
28h = 40 reports/second
3Ch = 60 reports/second
50h = 80 reports/second
64h = 100 reports/second
C8h = 200 reports/second

Device Driver Far Call Initialization

Entry Conditions:

AH = C2h
AL = 07h
ES:BX = device driver segment and offset address

Exit Conditions:

See returns for AL = 00h

Subsequent to this call, whenever pointing device data is available, the device driver address is called with the following arguments on the stack:

Word	Byte	Bit	Description
1	Low	7	1 Y data overflow
		6	1 X data overflow
		5	1 Negative Y data sign
		4	1 Negative X data sign
		3	1 Reserved (must be 1)
		2	0 Reserved (must be 0)
		1	1 Right button pressed
		0	1 Left button pressed
1	High	7-0	0 Reserved
2	Low	7	X data - MSB
		0	X data - LSB
2	High	7-0	0 Reserved
3	Low	7	Y data - MSB
		0	Y data - LSB
3	High	7-0	0 Reserved
4	Low	7-0	0 Reserved
	High	7-0	0 Reserved

Fail Safe Timer Control

This subfunction enables the fail-safe timer and establishes the timer count value with the value in BX. It puts the fail-safe timer in Mode 0 operation, enables the fail-safe timer NMI, and places the value in BX into WDTIC in the extended BIOS data area. It sets the Carry Flag if there is invalid input.

The fail-safe timer decrements and, at the end of the period stored in WDTIC, a fail-safe timer NMI is generated.

Entry Conditions:

AH = C3h
AL = 01h
BX = Fail-safe timer

Exit Conditions:

CF = 0 No error
= 1 Invalid input

Access EISA System Information (AH = D8h)

This function is used to autoconfigure EISA controllers. This should be the only method used to access the extended CMOS RAM in an EISA system.

Device numbers

EISA supports up to 64 devices. A ***physical device*** resides in an actual slot in the computer. Physical devices are referenced by their slot number. An ***embedded device*** is a device that has been integrated on the system board. Embedded devices are addressed as additional EISA devices. The device (slot) number for embedded devices begins with the next number after the last physical device number used. All other embedded devices are numbered sequentially afterwards. A ***virtual device*** is generally a software driver that may need system resources, but does not actually exist as a physical entity. Virtual devices are numbered sequentially after the last embedded device, but must be addressed as slot 16 through 64.

Read device (slot) information

Returns data about the specified EISA device. Determines the number of EISA functions supported in the system and the types of functions supported by the specified device.

Entry Conditions:

AH = D8h
AL = 00h (if CS specifies 16-bit addressing)
AL = 80h (if CS specifies 32-bit addressing)
CL = Device (slot) number (0-63)

Exit Conditions:

AH = 00h No error
= 80h Invalid device (slot) number
= 82h Extended CMOS RAM corrupted
= 83h Empty slot specified
= 86h Invalid BIOS routine call
= 87h Invalid system configuration
AL = Miscellaneous vendor information byte
bit 7 = Duplicate IDs exist
bit 6 = Product ID
bits 5-4 = Slot type
00 = expansion slot
01 = embedded device
10 = virtual device
11 = reserved
bits 3-0 = Duplicate ID number
BH = Major revision number of the configuration utility
BL = Minor revision number of the configuration utility
CH = MSB of checksum for configuration file
CL = LSB of checksum for configuration file
DH = Number of device functions
DL = Combined function information
SI:DI = four-byte compressed vendor ID

Error Conditions:

CF = 1
AH = nonzero

Read function information

Returns 320 bytes of data about the specific EISA function in the specified slot. Refer to "*Function Information Table*" for a description of the 320 byte data block.

Entry Conditions:

AH = D8h
AL = 01h (if CS specifies 16-bit addressing)
AL = 81h (if CS specifies 32-bit addressing)
CH = Function number (0-*n*-1)
CL = Device (slot) number (0-63)
DS:SI = Address pointer for output data

Exit Conditions:

AH = 00h No error
= 80h Invalid device (slot) number
= 81h Invalid function number
= 82h Extended CMOS RAM corrupted
= 83h Empty slot specified
= 86h Invalid BIOS routine call
= 87h Invalid system configuration
DS = Segment for return data buffer
SI = Offset to return data buffer (16-bit call)
ESI = Offset to return data buffer (32-bit call)

Error Conditions:

CF = 1
AH = nonzero

Clear configuration storage

Places zeros in all extended CMOS RAM data areas

Entry Conditions:

AH = D8h
AL = 02h (if CS specifies 16-bit addressing)
AL = 82h (if CS specifies 32-bit addressing)
BH = Configuration utility major revision level
BL = Configuration utility minor revision level

Exit Conditions:

AH = 00h No error
= 84h Error writing to extended CMOS RAM
= 86h Invalid BIOS routine call
= 87h Configuration utility not supported

Error Conditions:

CF = 1
AH = nonzero

Write configuration storage

Writes configuration data from a caller-defined table pointed to by the value in DS:SI to extended CMOS RAM. Refer to "*Function Information Table*" for a description of the configuration data block pointed to by the value in DS:SI. Updates all internal variables and generates and stores a new checksum value for extended CMOS RAM.

This function must be called sequentially for each device. It must be called once for each slot, in sequence, even for empty slots. To write configuration information for an empty slot, the caller must call this function with a pointer to a data table filled with zeros.

Note: The two-byte checksum data entry of the configuration file is a part of the input data structure, even though this subfunction recalculates the checksum before returning to the caller.

Entry Conditions:

AH = D8h
AL = 03h
CX = Length of data structure (in bytes)
DS = Segment of data buffer
SI = Offset of data buffer (16-bit call)
ESI = Offset of data buffer (32-bit call)

Exit Conditions:

AH = 00h No error
= 84h Error writing to extended CMOS RAM
= 85h CMOS RAM is full
= 86h Invalid BIOS routine call

Error Conditions:

CF = 1
AH = nonzero

Function information table

Offset	Size	Description
000h	2 Words	Compressed ID Byte 0 Bit 7 = Reserved Bits 6-2 = Character 1 Bits 1-0 = Character 2 Byte 1 Bits 7-5 = Character 2 Bits 4-0 = Character 3 Byte 2 Bits 7-4 = Second digit of product number Bits 3-0 = First digit of product number Byte 3 Bits 7-4 = Third digit of product number Bits 3-0 = Product revision number
004h	1 Word	ID and slot information Byte 0 Bit 7 = 0 No Duplicate ID present = 1 Duplicate ID is present Bit 6 = 0 ID is readable = 1 ID is not readable Bits 5-4 Slot type 00 expansion slot 01 embedded slot 10 virtual slot 11 reserved Bit 3-0 Duplicate configuration filenames (IDs) 0000 No duplicate filename 0001 First duplicate filename 1111 Fifteenth duplicate filename Byte 1 Bit 7 = 0 Configuration complete = 1 Configuration incomplete Bits 6-2 Reserved Bit 1 = 0 EISA IOCHKERR not supported = 1 EISA IOCHKERR supported Bit 0 = 0 EISA ENABLE not supported = 1 EISA ENABLE supported

Function information table (cont'd)

Offset	Size	Description
006h	1 Word	Configuration file extension revision level Byte 0 Minor revision level Byte 0 Major revision level
	1 Word	Function Length (Write only) Length does not include the length of this ("Function length") field, or the checksum at the end of nonvolatile memory. The function length of the last configuration data function entry equals zero.
008h	13 Words (1-13)	Selections Byte 0 First selection . . . Byte 25 Twenty-sixth selection
022h	1 Byte	Function information Bit 7 = 0 Function is enabled = 1 Function is disabled Bit 6 Configuration extension free-form data Bit 5 Port initialization entries follow Bit 4 Port range entries follow Bit 3 DMA entries follow Bit 2 Interrupt entries follow Bit 1 Memory entries follow Bit 0 Type/subtype entries follows
023h	80 Bytes (2-81)	Type and subtype ASCII string (strings less than 80 characters are zero-filled) Byte 0 First character of ASCII string . . . Byte 79 Eightieth character of ASCII string

Function information table (cont'd)

Offset	Size	Description
073h	63 Bytes (7-63)	Memory configuration information (if function information bit 6 is not set) Byte 0 Bit 7 = 0 Last entry = 1 More entries follow Bit 6 Reserved Bit 5 = 0 Unshared memory = 1 Shared memory Bit 4-3 Memory type 00 SYS (base and extended) 01 EXP (expanded) 10 VIR (virtual) 11 OTH (other) Bit 2 Reserved Bit 1 = 0 Not cached = 1 Cached Bit 0 = 0 Read only (ROM) = 1 Read/Write (RAM) Byte 1 Bits 7-4 Reserved Bits 3-2 Decode size 00 20 01 24 10 32 11 reserved Bits 1-0 Data size (access size) 00 Byte 01 Word 10 Doubleword 11 reserved Bytes 2-4 Memory start address divided by 100h Bytes 5-6 Memory size divided by 400h Up to eight more 7-byte entries may follow
0B2h	14 Bytes (2-14)	Interrupt configuration (if function information bit 6 is not set) Byte 0 Bit 7 = 0 Last entry = 1 More entries follow Bit 6 = 0 Not shared = 1 Shared Bit 5 = 0 Edge triggered = 1 Level triggered Bit 4 Reserved Bit 3-0 Interrupt (0-F) Byte 1 Reserved Up to six more 2-byte entries may follow

Function information table (cont'd)

Offset	Size	Description
0C0h	4 Words (1-4)	DMA channel description (if function information bit 6 is not set) Byte 0 Bit 7 = 0 Last entry = 1 More entries follow Bit 6 = 0 Not shared = 1 Shared Bit 5-3 Reserved Bit 2-0 DMA channel number (0-7) Byte 1 Bits 7-6 Reserved Bits 5-4 Data timing 00 Default (ISA compatible) 01 Type A 10 Type B 11 Type C (Burst) Bits 3-2 Transfer size 00 8-bit transfer 01 16-bit transfer 10 32-bit transfer 11 reserved Bits 1-0 Reserved Up to three more 2-byte entries may follow
0C8h	60 Bytes (5-60)	Port I/O information Byte 0 Bit 7 = 0 Last entry = 1 More entries follow Bit 6 = 0 Not shared = 1 Shared Bit 5 Reserved Bit 4-0 Number of sequential ports (minus 1) Bytes 1-2 I/O port address Up to nineteen more 3-byte entries may follow

Function information table (cont'd)

Offset	Size	Description
104h	60 Bytes (4-60)	Initialization data (if function information bit 6 is not set) Byte 0 Initialization type Bit 7 = 0 Last entry = 1 More entries follow Bits 6-3 Reserved Bit 2 = 0 Write to port without mask = 1 Write to port using mask Bit 1-0 Type of access 00 Byte addressable 01 Word addressable 10 Doubleword addressable 11 reserved Bytes 1-2 I/O port address Bytes 3-10 The values of bytes 3-10 in each initialization data entry depend on the value of byte 0, bit 2 If byte 0, bit 2 equals 0 (no mask), bytes 3-6 will have the following values based on the access type specified by byte 0, bits 1-0: Byte 0, bits 1-0 00 Byte 3 = port value 01 Bytes 3-4 = port value 10 Bytes 3-6 = port value 11 reserved If byte 0, bit 2 equals 1 (use mask), bytes 3-10 will have the following values based on the access type specified by byte 0, bits 1-0: Byte 0, bits 1-0 00 Byte 3 = port value Byte 4 = port mask 01 Bytes 3-4 = port value Bytes 5-6 = port mask 10 Bytes 3-6 = port value Bytes 7-10 = port mask 11 reserved Up to seven more 4-, 5-, 7-, or 11-byte entries may follow
	1 Word	Configuration file checksum (Write only)
When bit 6 is set in the function information byte, the 320-byte data block has a free-form format beginning at offset 073h.		

Function Information table (cont'd)

Offset	Size	Description
073h	205 Bytes (2-205)	Free-form data Byte 0 Length of free-form data Byte 1 First byte of free-form data . . . Byte 204 Two hundred and fourth byte of free-form data

Interrupt 16h: Keyboard Functions

The following routines provide access to keyboard functions. The specific function performed depends on the value in AH.

Value in AH	Function Performed
00h	Read Keyboard Input
01h	Read Keyboard Status
02h	Read Shift Status
03h	Set Typematic Rate
05h	Stuff Keyboard Buffer
10h	Read Extended Keyboard Input
11h	Read Extended Keyboard Status
12h	Read Extended Shift Status

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read). Control returns when a keystroke is available.

Entry Conditions:
AH = 00h

Exit Conditions:
AL = ASCII value of character
AH = keyboard scan code

Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to be read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (non-destructive read).

Entry Conditions:
AH = 01h

Exit Conditions:
Z = 1 no character is available
Z = 0 a character is available, in which case:
AL = ASCII value of character
AH = keyboard scan code

Get Shift Status

Return the current shift status.

Entry Conditions:
AH = 02h

Exit Conditions:
AL = current shift status
bit settings: set = true, reset = false
Bit 0 = RIGHT SHIFT key pressed
Bit 1 = LEFT SHIFT key pressed
Bit 2 = CTRL (control) key pressed
Bit 3 = ALT (alternate mode) key pressed
Bit 4 = SCROLL state active
Bit 5 = NUMBER lock engaged
Bit 6 = CAPS lock engaged
Bit 7 = INSERT state active

Set Typematic Rate

Entry Conditions:
AH = 03h
AL = 05h
BL = Typematic rate (00 - 1F hex)
BH = Typematic delay (00 - 3 hex)

Exit Conditions:
None

Stuff Keyboard Buffer

Entry Conditions:
AH = 05h
CH = Scan Code to Place in Keyboard Buffer
CL = ASCII Character to Place in Keyboard Buffer

Exit Conditions:
AL = 0 Store is Successful
AL = 1 Store is Unsuccessful
CY = 1 Error

Read Extended Keyboard Input

Control is returned when a keystroke is available. The keystroke is removed from the buffer.

Entry Conditions:
AH = 10h

Exit Conditions:
AL = ASCII Character
AH = Scan Code

Read Extended Keyboard Status

Includes extended read interface for extended keyboard.

Entry Conditions:
AH = 11h

Exit Conditions:
Z = 1 No Character Available
Z = 0 Character Available, in which case:
AL = ASCII Character
AH = Scan Code

Note: The keystroke is not removed from the buffer.

Read Extended Shift Status

Entry Conditions:
AH = 12

Exit Conditions:
AL = Shift Status Byte:
Bit = 1, on (key depressed); Bit = 0, off
Bit 7 = Ins(ert)
Bit 6 = Caps Lock
Bit 5 = Num Lock
Bit 4 = Scroll Lock
Bit 3 = Alt (alternate mode) key
Bit 2 = Ctrl (control) key
Bit 1 = Left Shift key
Bit 0 = Right Shift key

AH = Extended Shift Status:
Bit = 1, currently depressed; Bit = 0, not depressed
Bit 7 = SysRq key
Bit 6 = Caps Lock key
Bit 5 = Num Lock key
Bit 4 = Scroll Lock key
Bit 3 = Right Alt key
Bit 2 = Right Ctrl key
Bit 1 = Left Alt key
Bit 0 = Left Ctrl key

Interrupt 17h: Line Printer Functions

These routines provide an interface to the parallel line printer. The specific function performed depends on the value in AH:

Value in AH	Description of Function
00h	Print character
01h	Initialize printer port
02h	Get current printer status

Print Character

Print a character.

Entry Conditions:
AH = 00h
AL = character to be printed
DX = printer to be used (0-2)

Exit Conditions:
AH = printer status;
See "Get Current Printer Status (AH = 02h)."
If Bit 0 is set, the character could not be printed because of a timeout error

Initialize Printer Port

Initialize the printer port.

Entry Conditions:
AH = 01h
DX = printer to be used (0-2)

Exit Conditions:
AH = printer status; See "Get Current Printer Status" (AH = 02h)

Get Current Printer Status

Read the printer status in AH.

Entry Conditions:
AH = 02h

Exit Conditions:
AH = printer status, as follows (set = true = 1):
Bit 7 = not busy
Bit 6 = acknowledge
Bit 5 = out of paper
Bit 4 = selected
Bit 3 = I/O error
Bit 2 = [unused]
Bit 1 = [unused]
Bit 0 = timeout occurred

Note: If printer port specified by DX does not exist, the status value is not meaningful.

Interrupt 1Ah: System Clock Functions

These routines provide the means of reading and setting the system clock tick counter, the CMOS real-time clock, and the system alarm function. The specific function performed depends on the value of AH:

Value in AH	Function Description
01h	Set system clock
02h	Read CMOS time of day
03h	Set CMOS time of day
04h	Read CMOS date
05h	Set CMOS date
06h	Set the alarm
07h	Reset the alarm
08h	Set up sound multiplexer

Read System Clock

Read the system clock value kept in RAM.

Note: The clock runs at a rate of 1,193,180/65,536 per second, or about 18.2 ticks per second. 24 hours equals 1800B0h ticks.

Entry Conditions:
AH = 00h

Exit Conditions:
AL = 0 (zero) if the timer has not exceeded 24 hours since the last time this function was called; otherwise AL contains a non-zero value
CX = high (most significant) portion of clock count
DX = low (least significant) portion of clock count

Set System Clock

Set the system clock value kept in RAM.

Entry Conditions:
AH = 01h
CX = high (most significant) portion of clock count
DX = low (least significant) portion of clock count

Read CMOS Time Of Day

Read the time of day kept in CMOS.

Entry Conditions:
AH = 02h

Exit Conditions:
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD
DL = daylight savings time (1 = yes, 0 = no)

Set CMOS Time Of Day

Set the time of day kept in CMOS.

Entry Conditions:
AH = 03h
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD
DL = 1 if daylight savings time, 0 if not.

Read CMOS Date

Read the date kept in CMOS

Entry Conditions:
AH = 04h

Exit Conditions:
CH = century in BCD
CL = year in BCD
DH = month in BCD
DL = day in BCD

Set CMOS Date

Set the date kept in CMOS

Entry Conditions:
AH = 05h
CH = century in BCD
CL = year in BCD

DH = month in BCD
DL = day in BCD

Set the Alarm

Set the alarm function to generate an INT 4Ah at the specified time. The user must provide an alarm routine and initialize the vector for interrupt 4Ah to point to this routine.

Entry Conditions:
AH = 06h
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD

Exit Conditions:
[NC] = CMOS clock operating correctly, and no other alarm is currently in process
[C] = An alarm is currently in progress, or the CMOS clock is not operating correctly

Reset the Alarm

Reset the alarm function set by Function 6.

Entry Conditions:
AH = 07h

Exit Conditions:
None

I. ELECTRICAL

A. POWER

5V ± 10% , 300 mA MAX

B. LOGIC LEVELS

LOGIC "0" - 0.7V MAX @ 8mA MAX TOTAL SINK, 5.7 mA EXTERNAL.
LOGIC "1" - 2.4V MIN @ 0.8 mA MAX.

II. POWER ON ROUTINE

UPON SYSTEM POWER UP THE FOLLOWING ACTIVITIES OCCUR:

A. POWER ON RESET (POR)

THE KEYBOARD WILL PERFORM A POWER ON RESET (POR) WITHIN A MINIMUM OF 150 MSEC AND A MAXIMUM OF 2.0 SECONDS.

B. BASIC ASSURANCE TEST (BAT)

THE KEYBOARD WILL CONDUCT A BASIC ASSURANCE TEST (BAT) OF THE PROCESSOR.

1. TURN THE LEDs (IF SO EQUIPPED) ON AT THE BEGINNING OF THE TEST AND OFF AT THE END OF THE TEST.

2. TRANSMIT THE COMPLETION CODE; AAH IF THE TEST WAS SUCCESSFUL.

THE BAT TAKES A MAXIMUM OF 500 MSEC. DURING THIS TIME ALL ACTIVITY ON THE "CLOCK" AND "DATA" LINES WILL BE IGNORED.

THE COMPLETION CODE WILL BE TRANSMITTED WITHIN 450 MSECONDS AND NOT MORE THAN 2.5 SECONDS AFTER POR, AND WITHIN 500 MSECONDS AFTER A RESET COMMAND IS ACKNOWLEDGED.

C. AUTOSELECT

THE KEYBOARD DETERMINES WHAT KIND OF SYSTEM IT IS CONNECTED TO AS FOLLOWS:

1. TRANSMIT "AAH" IN 11-BIT (MODE 2) FORMAT AND CHECK FOR AN INHIBIT AFTER THE 10TH BIT. IF NO INHIBIT IS RECEIVED (DATA LINE AT LOGIC "0") THE FORMAT WILL REMAIN IN MODE 2 AND SCAN CODE SET 2 IS SELECTED. IF THE SYSTEM RESPONDS WITH AN INHIBIT THEN THE 9-BIT (MODE 1) FORMAT AND SCAN CODE SET 1 ARE SELECTED.

III. DATA TRANSMISSION

A. CLOCK AND DATA LINES

THE "CLOCK" AND "DATA" LINES ARE USED FOR COMMUNICATION IN BOTH DIRECTIONS BETWEEN THE SYSTEM AND THE KEYBOARD. THESE LINES ARE DRIVEN BY AN OPEN COLLECTOR DEVICE WHICH ALLOWS EITHER THE SYSTEM OR THE KEYBOARD TO FORCE THE LINE TO AN INACTIVE (LOW) LEVEL. WHEN NO COMMUNICATION IS OCCURRING BOTH LINES ARE ACTIVE (HIGH). AN INACTIVE SIGNAL (LOGIC 0) IS GREATER THAN 0 BUT LESS THAN +0.7 VOLTS. AN ACTIVE SIGNAL (LOGIC 1) HAS A VALUE OF AT LEAST +2.4 BUT NO GREATER THAN +5.5 VOLTS.

THE KEYBOARD PROVIDES THE CLOCKING SIGNALS USED TO CLOCK SERIAL DATA TO AND FROM THE KEYBOARD. THE HOST SYSTEM CAN INHIBIT THE KEYBOARD BY FORCING THE "CLOCK" LINE TO THE INACTIVE LEVEL. WHEN THE KEYBOARD IS INHIBITED THE STATE OF THE "CLOCK" LINE IS IGNORED.

THE "DATA" LINE IS USED FOR TRANSMISSION OF DATA BY BOTH THE SYSTEM AND THE KEYBOARD. THE SYSTEM ISSUES A "REQUEST TO SEND" (RTS) BY PULLING THE DATA LINE TO THE INACTIVE LEVEL (LOW).

B. DATA FORMAT

TWO MODES ARE USED FOR DATA TRANSMISSION:

1. MODE 1 IS A 10-BIT DATA STREAM THAT CONSISTS OF A LOGIC "0" TEST BIT, A LOGIC "1" START BIT, AND 8 DATA BITS (NO PARITY OR STOP BITS). SCAN CODE SET 1 IS USED WITH MODE 1.

2. MODE 2 IS AN 11-BIT DATA STREAM THAT CONSISTS OF 1 START BIT (ALWAYS LOGIC "0"), 8 DATA BITS (LEAST SIGNIFICANT BIT TO MOST SIGNIFICANT BIT RESPECTIVELY), 1 ODD PARITY BIT, AND ONE STOP BIT (ALWAYS LOGIC 1). MODE 2 IS USED WITH SCAN CODE SETS 2 AND 3.

SEE FIGURE 1, 2, AND 3 FOR GRAPHIC REPRESENTATION OF THESE SIGNALS.

C. KEYBOARD TO SYSTEM LINE PROTOCOL

1. KEYBOARD CHECKS "CLOCK" LINE FOR "CTS" - IF LOGIC "1" CONTINUE, IF LOGIC "0" STORE KEYSTROKES IN BUFFER.

2. KEYBOARD CHECKS "DATA" LINE FOR "RTS" FROM SYSTEM - IF LOGIC "1" CONTINUE, IF LOGIC "0" STORE KEYSTROKES IN BUFFER AND PREPARE TO RECEIVE DATA FROM SYSTEM.

3. KEYBOARD TRANSMITS DATA. DURING TRANSMISSION THE KEYBOARD CHECKS THE "CLOCK" LINE FOR LOGIC LEVEL "1" AT LEAST EVERY 60 MICROSECONDS. (SEE LINE CONTENTION BELOW)

LINE CONTENTION - THE SYSTEM MAY INTERRUPT KEYBOARD DATA TRANSMISSION AT ANY TIME UP TO THE 10th CLOCK BY PULLING THE "CLOCK" LINE TO A LOGIC LEVEL "0". AFTER THE 10th CLOCK THE SYSTEM MUST RECEIVE THE KEYBOARD DATA.

D. SYSTEM TO KEYBOARD LINE PROTOCOL

1. SYSTEM INHIBITS KEYBOARD BY LOWERING THE "CLOCK" LINE TO LOGIC "0" FOR A MINIMUM OF 60 MICROSECONDS.

2. SYSTEM REQUESTS TRANSMISSION BY LOWERING THE "DATA" LINE TO LOGIC LEVEL "0" (RTS) AND ALLOWS THE "CLOCK" LINE TO GO ACTIVE.

3. KEYBOARD MONITORS THE "CLOCK" LINE (10 mSEC INTERVALS) AND DETECTS THE ACTIVE LEVEL.

4. KEYBOARD DETECTS "RTS" ON THE "DATA" LINE AND CLOCKS IT IN AS THE LOGIC "0" START BIT.

5. KEYBOARD CLOCKS IN THE 8 DATA BITS AND THE ODD PARITY BIT.

6. KEYBOARD LOOKS FOR A LOGIC LEVEL "1" ON THE "DATA" LINE THEN FORCES IT LOW (WITHIN 20 mSEC) AND CLOCKS ONE MORE BIT. THIS ACTION SIGNALS THE SYSTEM THAT THE KEYBOARD HAS RECEIVED THE DATA. IF THE "DATA" IS NOT AT A LOGIC LEVEL "0" FOLLOWING THE 10th BIT THE KEYBOARD WILL CONTINUE TO CLOCK BITS INDEFINITELY UNTIL THE LINE BECOMES ACTIVE. THE KEYBOARD THEN PULLS THE "DATA" LINE LOW AND TRANSMITS A "RESEND".

IV. FIFO

THE KEYBOARD CONTAINS AT LEAST A 16-BYTE FIRST-IN-FIRST-OUT (FIFO) BUFFER WHICH STORES THE SCAN CODES UNTIL THE SYSTEM IS READY TO RECEIVE THEM.

A BUFFER-OVERRUN CONDITION OCCURS WHEN THE KEYBOARD TRIES TO PLACE MORE CHARACTERS THAN THE KEYBOARD BUFFER CAN HOLD. WHEN THIS OCCURS, AN OVERRUN CODE (FFH FOR SCAN CODE SET 1, AND 00H FOR SCAN CODE SETS 2 & 3) REPLACES THE LAST BYTE. IF MORE KEYS ARE PRESSED BEFORE THE SYSTEM ALLOWS KEYBOARD OUTPUT, THE ADDITIONAL DATA IS LOST.

WHEN THE KEYBOARD IS ALLOWED TO SEND DATA, THE BYTES IN THE BUFFER WILL BE SENT AS IN NORMAL OPERATION, AND NEW DATA ENTERED IS DETECTED AND SENT. RESPONSE CODES DO NOT OCCUPY A BUFFER POSITION.

IF KEYSTROKES GENERATE A MULTIPLE-BYTE SEQUENCE, THE ENTIRE SEQUENCE MUST FIT INTO THE AVAILABLE BUFFER SPACE OR THE KEYSTROKE IS DISCARDED AND A BUFFER-OVERRUN CONDITION OCCURS.

V. KEYS

ALL THE KEYS ON THE KEYBOARD ARE MAKE/BREAK EXCEPT THE PAUSE KEY. THE MAKE SCAN CODE IS SENT TO THE SYSTEM WHEN THE KEY IS DEPRESSED AND THE BREAK CODE IS SENT WHEN THE KEY IS RELEASED.

ALL KEYS ARE ALSO AUTOREPEAT EXCEPT FOR THE PAUSE KEY. THE KEY WILL AUTOREPEAT AFTER THE INITIAL DELAY HAS EXPIRED. ROLLOVER TO ANOTHER AUTOREPEAT KEY WILL STOP REPEATING OPERATION AND PRODUCE THE SCAN CODE FOR THE SECOND KEY. AFTER AN INITIAL DELAY, THE KEYBOARD WILL REPEAT THE SECOND CODE. ROLLOVER TO A NON-AUTOREPEAT KEY WILL NOT AFFECT THE AUTOREPEAT OPERATION. THE INITIAL DELAY AND REPEAT RATES ARE MODIFIABLE. (SEE MODIFY AUTOREPEAT RATE/DELAY (F3H) COMMAND BELOW.)

VI. SYSTEM COMMANDS

THESE COMMANDS MAY BE SENT TO THE KEYBOARD AT ANY TIME. THE KEYBOARD WILL RESPOND WITHIN 20 mSEC, EXCEPT WHEN PERFORMING THE BASIC ASSURANCE TEST (BAT), OR EXECUTING A RESET.

NOTE: MODE 1 WILL ACCEPT ONLY THE RESET COMMAND. THIS IS ACCOMPLISHED BY PULLING THE CLOCK LINE LOW FOR A MINIMUM OF 12.5 mSEC.

THE COMMANDS ARE DESCRIBED IN ALPHABETICAL ORDER AND HAVE DIFFERENT MEANINGS WHEN ISSUED BY THE KEYBOARD. (SEE KEYBOARD COMMANDS)

COMMANDS (SYSTEM TO KEYBOARD)

COMMAND	HEX VALUE
DEFAULT DISABLE	F5
ECHO	EE
ENABLE	F4
INVALID COMMAND	EF OR F1
READ ID	F2
RESEND	FE
RESET	FF
SET ALT SCAN CODES	F0
SET ALL KEYS (AR)	F7
SET ALL KEYS (M/B)	F8
SET ALL KEYS (M)	F9
SET ALL KEYS (AR, M, M/B)	FA
SET DEFAULT	F6
SET KEY TYPE (AR)	FB
SET KEY TYPE (M/B)	FC
SET KEY TYPE (M)	FD
SET/RESET STATUS IND	ED
SET AR RATE/DELAY	F3

A. DEFAULT DISABLE (F5H)

THIS COMMAND RESETS ALL CONDITIONS TO THE POWER-ON STATE. THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS THE DEFAULT KEY TYPES (SCAN CODE SET 3 OPERATION ONLY) AND AUTOREPEAT RATE/DELAY, AND CLEARS THE LAST AUTOREPEAT KEY. THE KEYBOARD STOPS SCANNING, AND AWAITS FURTHER INSTRUCTIONS.

B. ECHO (EEH)

WHEN THE KEYBOARD RECEIVES THIS COMMAND, IT ISSUES AN ECHO (EEH) RESPONSE AND CONTINUES SCANNING, IF PREVIOUSLY ENABLED.

C. ENABLE (F4H)

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, CLEARS THE LAST AUTOREPEAT KEY, AND STARTS SCANNING.

D. INVALID COMMAND (EFH & F1H)

THESE ARE INVALID COMMANDS AND ARE NOT SUPPORTED. IF ONE OF THESE IS RECEIVED, THE KEYBOARD WILL NOT ACKNOWLEDGE THE COMMAND, BUT RETURNS A "RESEND" AND CONTINUES SCANNING, IF PREVIOUSLY ENABLED. NO OTHER ACTIVITIES OCCUR.

E. READ ID (F2H)

THE KEYBOARD RESPONDS WITH "ACK", DISCONTINUES SCANNING, AND SENDS THE TWO KEYBOARD ID BYTES 83H AND ABH.

THE SECOND BYTE IS TRANSMITTED FOLLOWING THE FIRST WITHIN 500 uSEC. AFTER THE OUTPUT OF THE SECOND ID BYTE, THE KEYBOARD RESUMES SCANNING EVEN IF PREVIOUSLY DISABLED.

F. RESEND (FEH)

THIS COMMAND SHOULD BE SENT FOLLOWING THE OUTPUT OF A CODE AND BEFORE THE SYSTEM ENABLES THE INTERFACE ALLOWING THE NEXT KEYBOARD OUTPUT. THE KEYBOARD WILL RETRANSMIT THE PREVIOUS CODE UNLESS IT WAS A "RESEND" COMMAND, IN THIS CASE THE KEYBOARD WILL RESEND THE LAST BYTE PRIOR TO THE "RESEND" COMMAND.

G. RESET (FFH)

SEE SECTION ON RESET

H. SELECT ALTERNATE SCAN CODES (F0H)

THIS COMMAND INSTRUCTS THE KEYBOARD TO SELECT ONE OF THREE SETS OF SCAN CODES. THE KEYBOARD ACKNOWLEDGES RECEIPT OF THIS COMMAND WITH "ACK", CLEARS BOTH THE OUTPUT BUFFER AND THE AUTOMATIC REPEAT KEY (IF ONE IS ACTIVE). THE SYSTEM THEN SENDS THE OPTION BYTE AND THE KEYBOARD RESPONDS WITH ANOTHER "ACK". AN OPTION BYTE VALUE OF 01H SELECTS SCAN CODE SET 1, 02H SELECTS SET 2, AND 03H SELECTS SET 3.

AN OPTION BYTE VALUE OF 00H CAUSES THE KEYBOARD TO ACKNOWLEDGE WITH AN "ACK" AND SEND A BYTE TELLING THE SYSTEM WHICH SCAN CODE IS CURRENTLY IN USE. AFTER ESTABLISHING THE NEW SCAN CODE SET, THE KEYBOARD RETURNS TO THE SCANNING STATE IT WAS IN BEFORE RECEIVING THE "SELECT ALTERNATE SCAN CODES" COMMAND.

J. SET ALL KEYS (F7H, F8H, F9H, FAH)

THESE COMMANDS INSTRUCT THE KEYBOARD TO SET ALL KEYS TO THE TYPE LISTED BELOW:

F7H = SET ALL KEYS - AUTOREPEAT
F8H = SET ALL KEYS - MAKE/BREAK
F9H = SET ALL KEYS - MAKE
FAH = SET ALL KEYS - AUTOREPEAT/MAKE/BREAK

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS ALL KEYS TO THE TYPE INDICATED BY THE COMMAND, AND CONTINUES SCANNING (IF PREVIOUSLY ENABLED). ALTHOUGH THESE COMMANDS CAN BE SENT USING ANY SCAN CODE SET, THEY AFFECT ONLY SCAN CODE SET 3 OPERATION.

K. SET DEFAULT (F6H)

THIS COMMAND RESETS ALL CONDITIONS TO THE POWER-ON DEFAULT STATE. THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS THE DEFAULT KEY TYPES (SCAN CODE SET 3 OPERATION ONLY) AND AUTOREPEAT RATE/DELAY, CLEARS THE LAST AUTOREPEAT KEY, AND CONTINUES SCANNING.

L. SET KEY TYPE (FBH, FCH, FDH)

THESE COMMANDS INSTRUCT THE KEYBOARD TO SET INDIVIDUAL KEYS TO THE TYPE LISTED BELOW:

FBH = SET KEY TYPE - AUTOREPEAT
FCH = SET KEY TYPE - MAKE/BREAK
FDH = SET KEY TYPE - MAKE

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, AND PREPARES TO RECEIVE KEY IDENTIFICATION. THE SYSTEM IDENTIFIES EACH KEY BY ITS SCAN CODE VALUE AS DEFINED IN SCAN CODE SET 3. ONLY SCAN CODE SET 3 VALUES ARE VALID FOR KEY IDENTIFICATION. THE TYPE OF EACH KEY IS SET TO THE VALUE INDICATED BY THE COMMAND.

EACH SCAN CODE RECEIVED IS ACKNOWLEDGED BY THE KEYBOARD AND THE IDENTIFIED KEY IS SET TO THE TYPE DEFINED BY THE COMMAND. THE KEYBOARD WILL REMAIN IN A PARTICULAR SET TYPE COMMAND MODE UNTIL IT RECEIVES THE COMMAND FOR A NEW TYPE.

THE COMMAND IS TERMINATED BY THE ENABLE COMMAND (F4H).

M. SET RESET STATUS INDICATORS (EDH)

THE KEYBOARD ACTIVATES AND DEACTIVATES THESE INDICATORS WHEN IT RECEIVES A VALID COMMAND CODE SEQUENCE FROM THE SYSTEM. WHEN THE KEYBOARD RECEIVES THE COMMAND BYTE (EDH) IT RESPONDS WITH "ACK", DISCONTINUES SCANNING, AND WAITS OR THE OPTION BYTE AS FOLLOWS:

BIT	INDICATOR
0	SCROLL LOCK INDICATOR
1	NUM LOCK INDICATOR
2	CAPS LOCK INDICATOR
3-4	RESERVED (MUST BE 0's)

A BIT SET TO "1" TURNS THE INDICATOR "ON", A "0" TURNS IT "OFF".

THE KEYBOARD RESPONDS TO THE OPTION BYTE WITH "ACK", SETS THE INDICATORS AND, IF THE KEYBOARD WAS PREVIOUSLY ENABLED, CONTINUES SCANNING.

IF ANOTHER COMMAND IS RECEIVED IN PLACE OF THE OPTION BYTE, EXECUTION OF THE "SET/RESET INDICATORS MODE" IS STOPPED, WITH NO CHANGE TO THE INDICATORS, AND THE NEW COMMAND IS PROCESSED.

THE INDICATORS DEFAULT TO THE "OFF" STATE AT "POWER-ON" AND ARE NOT AFFECTED BY THE "SET DEFAULT" AND "DEFAULT DISABLE" COMMANDS.

N. SET AUTOREPEAT RATE/DELAY (F3H)

THE KEYBOARD RESPONDS TO THE COMMAND WITH "ACK", STOPS SCANNING, AND WAITS FOR THE RATE/DELAY VALUE BYTE. BITS 6 AND 5 OF THIS BYTE INDICATE THE DELAY, AND BITS 4, 3, 2, 1, AND 0 (THE LEAST SIGNIFICANT BIT) INDICATE THE RATE. BIT 7 (THE MOST SIGNIFICANT BIT) IS ALWAYS "0". THE DELAY IS EQUAL TO 1 PLUS THE BINARY VALUE OF BITS 6 & 5, MULTIPLIED BY 250 mSEC $\pm$ 20%. THE PERIOD (INTERVAL FROM ONE AUTOREPEAT OUTPUT TO THE NEXT) IS DETERMINED BY THE FOLLOWING EQUATION:

PERIOD = (8 + A) X (2^B) X 0.00417 SECONDS.

WHERE:

A - BINARY VALUE OF BITS 2, 1, AND 0
B - BINARY VALUE OF BITS 4 AND 3.

THE AUTOREPEAT RATE (MAKE CODES PER SECOND) IS : FOR EACH PERIOD AND ARE LISTED IN THE FOLLOWING TABLE.

BIT	AUTOREPEAT RATE	BIT	AUTOREPEAT RATE
00000	30.0	10000	7.5
00001	26.7	10001	6.7
00010	24.0	10010	6.0
00011	21.8	10011	5.5
00100	20.0	10100	5.0
00101	18.5	10101	4.6
00110	17.1	10110	4.3
00111	16.0	10111	4.0
01000	15.0	11000	3.7
01001	13.3	11001	3.3
01010	12.0	11010	3.0
01011	10.9	11011	2.7
01100	10.0	11100	2.5
01101	9.2	11101	2.3
01110	8.6	11110	2.1
01111	8.0	11111	2.0

THE DEFAULT VALUES AT POWER ON FOR THE SYSTEM KEYBOARD ARE AS FOLLOWS:

AUTOREPEAT RATE = 10.9 CHARACTERS PER SECOND ± 20%.

DELAY = 500 mSEC ± 20%.

THE KEYBOARD RESPONDS TO THE VALUE BYTE WITH "ACK", SETS THE RATE AND DELAY TO THE VALUES INDICATED, AND CONTINUES SCANNING, IF ENABLED.

THE EXECUTION OF THIS COMMAND STOPS WITHOUT CHANGE TO THE EXISTING RATE IF ANOTHER COMMAND IS RECEIVED INSTEAD OF THE RATE/DELAY VALUE BYTE AND THE NEW COMMAND IS PROCESSED.

VII. KEYBOARD COMMANDS

THESE COMMANDS MAY BE SENT TO THE SYSTEM ANY TIME THE KEYBOARD IS ENABLED. THEY ARE LISTED IN ALPHABETICAL ORDER AND HAVE A DIFFERENT MEANING WHEN SENT BY THE SYSTEM (SEE SYSTEM COMMANDS).

COMMANDS (KEYBOARD TO SYSTEM)

COMMAND	HEX CODE
ACK	FA
BAT COMPLETION	AA
BREAK CODE PREFIX	F0
ECHO	EE
KBD ID	SEE DESC. BELOW
KEY DETECTION ERROR	00 OR FF
OVERRUN	00 OR FF
RESEND	FE

A. ACKNOWLEDGE (FAH)

THE KEYBOARD SENDS "ACK" IN RESPONSE TOO ANY VALID COMMAND FROM THE SYSTEM EXCEPT "ECHO" AND "RESEND".

B. BAT COMPLETION CODE (AAH)

INDICATES TO THE SYSTEM THAT THE KEYBOARD BASIC ASSURANCE TEST (BAT) WAS SUCCESSFULLY COMPLETED. ANY OTHER CODE INDICATES A FAILURE OF THE KEYBOARD.

C. ECHO (EEH)

THE KEYBOARD SENDS THIS CODE IN RESPONSE TO AN ECHO COMMAND.

D. KEYBOARD ID

THE KEYBOARD ID CONSISTS OF 2 BYTES (SEE READ ID COMMAND UNDER SYSTEM COMMANDS). THE KEYBOARD RESPONDS TO THE READ ID WITH "ACK", DISCONTINUES SCANNING, AND SENDS THE TWO ID BYTES. THE LOW BYTE IS SENT FIRST FOLLOWED BY THE HIGH BYTE. FOLLOWING OUTPUT OF THE KEYBOARD ID, THE KEYBOARD BEGINS SCANNING.

E. KEY CODE

UNIQUE OUTPUT CODE GENERATED FOR EACH KEY POSITION OF THE SWITCH ARRAY. REFER TO "KEYBOARD SCAN CODES" FOR THE DEFINITION OF OUTPUT CODE PER POSITION.

F. KEY DETECTION ERROR (00H or FFH)

THE KEYBOARD SENDS A KEY DETECTION ERROR CHARACTER IF CONDITIONS IN THE KEYBOARD MAKE IT IMPOSSIBLE TO IDENTIFY A SWITCH CLOSURE. IF THE KEYBOARD IS USING SCAN CODE SET 1, THE CODE IS FFH. FOR SETS 2 AND 3, THE CODE IS 00H.

G. OVERRUN (00H or FFH)

THIS CODE REPLACES THE LAST CODE IN THE KEYBOARD BUFFER WHEN ITS CAPACITY HAS BEEN EXCEEDED. THE CODE IS SENT WHEN IT REACHES THE TOP OF THE BUFFER QUEUE. IF THE KEYBOARD IS USING SCAN CODE SET 1, THE CODE IS FFH, FOR SETS 2 AND 3, THE CODE IS 00H.

H. RESEND (FEH)

THE KEYBOARD ISSUES A "RESEND" COMMAND FOLLOWING RECEIPT OF AN INVALID INPUT OR ANY INPUT WITH INCORRECT PARITY.

I. DEFAULT CONDITIONS AFTER RESET (BOTH MODES)

THE FOLLOWING ARE THE DEFAULT CONDITIONS AFTER A HARDWARE & SOFTWARE RESET:

1. AUTO REPEAT 10 CPS @ 500 mSEC INITIAL DELAY, CLICK DISABLED AND LEDs OFF.

2. CLICK (OPTIONAL ANNUNCIATOR IS NOT INSTALLED)

3. TWO KEY LOCKOUT - EXCEPT FOR KEYS 60, 81, 94, 100, 101, 103, AND 104, IF TWO KEYS ARE DEPRESSED, A THIRD KEY WILL NOT BE ACCEPTED UNTIL ONE OF THE TWO KEYS ARE RELEASED.

4. IF MORE THAN TWO KEYS ARE HELD DEPRESSED AFTER A VALID RESET, A PHANTOM KEY MAY BE DETECTED.

FIG 1. KEYBOARD INPUT (11-bit)

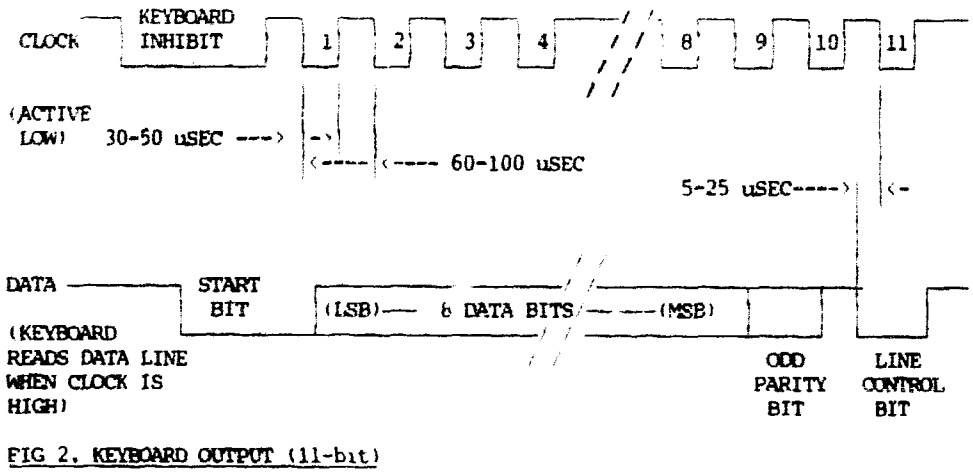


FIG 2. KEYBOARD OUTPUT (11-bit)

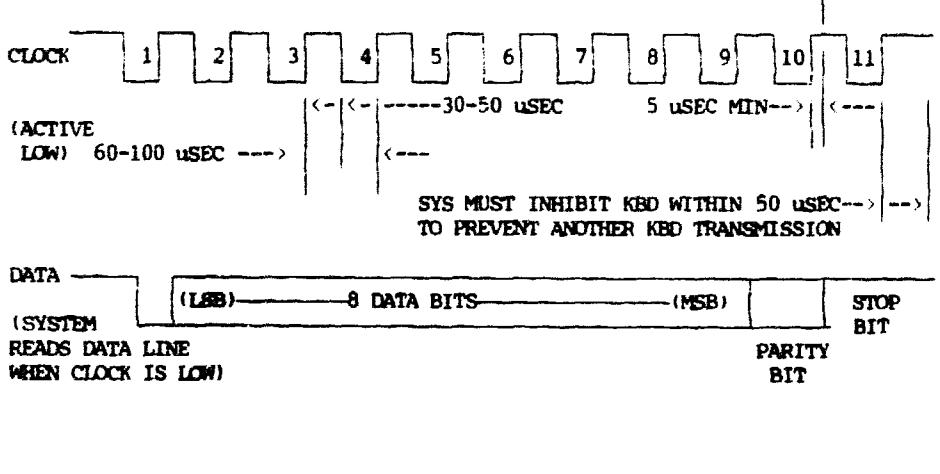
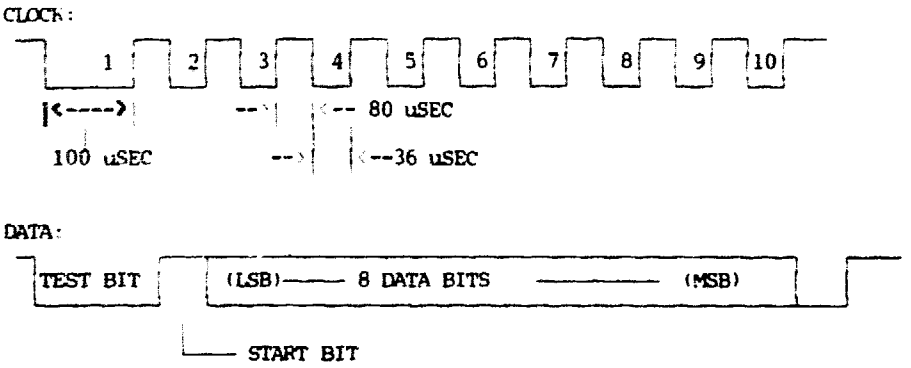


FIG 3. KEYBOARD OUTPUT (9-bit)



NOTE: ALL BIT TIMES ARE NOMINAL. TOLERANCES ARE +/- 5 uSEC.

IV. THE KEYBOARD USES THREE SETS OF SCAN CODES. THE FOLLOWING TABLE LISTS THESE CODES:

	CODE SETS			
Key No.	Set 1	Set 2	Set 3	MODE
1	01	76	08	M
2	3B	05	07	M
3	3C	06	0F	M
4	3D	04	17	M
5	3E	0C	1F	M
6	3F	03	27	M
7	40	0B	2F	M
8	41	83	37	M
9	42	0A	3F	M
10	43	01	47	M
11	44	09	4F	M
12	57	78	56	M
13	58	07	5E	M
14	(1) *	(2) *	57	M
15	46	7E	5F	M
16	(1) *	(2) *	62	M
17	29	0E	0E	AR
18	02	16	16	AR
19	03	1E	1E	AR
20	04	26	26	AR
21	05	25	25	AR
22	06	2E	2E	AR
23	07	36	36	AR
24	08	3D	3D	AR
25	09	3E	3E	AR
26	0A	46	46	AR
27	0B	45	45	AR
28	0C	4E	4E	AR
29	0D	55	55	AR
30	58	5D	5C	AR
31	0E	66	66	AR
32	(1) *	(2) *	67	M
33	(1) *	(2) *	6E	M
34	(1) *	(2) *	6F	M
35	45	77	76	M

Key No.	Set 1	Set 2	Set 3	MODE
36	(1) *	(2) *	77	M
37	37	7C	7E	M
38	4A	7B	84	M
39	0F	0D	0D	AR
40	10	15	15	AR
41	11	1D	1D	AR
42	12	24	24	AR
43	13	2D	2D	AR
44	14	2C	2C	AR
45	15	35	35	AR
46	16	3C	3C	AR
47	17	43	43	AR
48	18	44	44	AR
49	19	4D	4D	AR
50	1A	54	54	AR
51	1B	5B	5B	AR
52	2B	5D	5C	AR
53	(1) *	(2) *	64	AR
54	(1) *	(2) *	65	M
55	(1) *	(2) *	6D	M
56	47	6C	6C	M
57	48	75	75	M
58	49	7D	7D	M
59	4E	79	7C	AR
60	3A	58	14	M B
61	1E	1C	1C	AR
62	1F	1B	1B	AR
63	20	23	23	AR
64	21	2B	2B	AR
65	22	34	34	AR
66	23	33	33	AR
67	24	3B	3B	AR
68	25	42	42	AR
69	26	4B	4B	AR
70	27	4C	4C	AR
71	28	52	52	AR
72	2B	5D	53	AR
73	1C	5A	5A	AR
74	59	67	09	M
75	5A	6E	0A	M

Key No.	Set 1	Set 2	Set 3	MODE
76	5B	6A	0B	M
77	4B	6B	6B	M
78	4C	73	73	M
79	4D	74	74	M
80	5D	65	7B	AR
81	2A	12	12	M/B
82	56	61	13	AR
83	2C	1A	1A	AR
84	2D	22	22	AR
85	2E	21	21	AR
86	2F	2A	2A	AR
87	30	32	32	AR
88	31	31	31	AR
89	32	3A	3A	AR
90	33	41	41	AR
91	34	49	49	AR
92	35	4A	4A	AR
93	57	62	51	AR
94	36	59	59	M/B
95	(1) *	(2) *	63	AR
96	4F	69	69	M
97	50	72	72	M
98	51	7A	7A	M
99	E01C	E05A	79	M
100	1D	14	11	M/B
101	38	11	19	M/B
102	39	29	29	AR
103	E038	E011	39	M
104	E01D	E014	58	M
105	(1) *	(2) *	61	AR
106	(1) *	(2) *	60	AR
107	(1) *	(2) *	6A	AR
108	5E	6D	02	M
109	52	70	70	M
110	53	71	71	M
111	5C	64	78	M

SET 1 BREAK CODE = MAKE CODE + 80H
SET 2 & SET 3 BREAK CODE = F0H PREFIX THEN MAKE CODE

* = (1) (2) SEE KEYS AFFECTED BY SHIFT, ALT & CTRL BELOW:

(1) Keys Affected by Shift, Alt & Ctrl (Set 1)

Key No.	Base Case or Shft + Num Lk (Make/Break)	Shift Case (See Note 1) (Make/Break)	Num Lock on (Make/Break)
32	E052/E0D2	E0AAE052/E0D2E02A	E02AE052/E0D2E0AA
53	E053/E0D3	E0AAE053/E0D3E02A	E02AE053/E0D3E0AA
105	E04B/E0CB	E0AAE04B/E0CBE02A	E02AE04B/E0CBE0AA
33	E047/E0C7	E0AAE047/E0C7E02A	E02AE047/E0C7E0AA
54	E04F/E0CF	E0AAE04F/E0CFE02A	E02AE04F/E0CFE0AA
95	E048/E0C8	E0AAE048/E0C8E02A	E02AE048/E0C8E0AA
106	E050/E0D0	E0AAE050/E0D0E02A	E02AE050/E0D0E0AA
34	E049/E0C9	E0AAE049/E0C9E02A	E02AE049/E0C9E0AA
55	E051/E0D1	E0AAE051/E0D1E02A	E02AE051/E0D1E0AA
107	E04D/E0CD	E0AAE04D/E0CDE02A	E02AE04D/E0CDE0AA
36	E035/E0B5	E0AAE035/E0B5E02A	

Note 1: If the left shift key is held down, the AA/2A shift make and break is sent with the other scan codes. If the right shift key is held down, B6/36 is sent. If both shift keys are down, both sets of codes are sent with the other scan code.

Key No.	Base Case (Make/Break)	Ctrl Case Shift Case (Make/Break)	Alt Case (Make/Break)
14	E02AE037/E0B7E0AA	E037/E0B7	54/D4

Key No.	Base Case (Make)	Ctrl Case (Make)
16	E11D45E19DC5	E046E0C6

Note: This key is not auto-repeat. All associated scan codes occur on the make of the key.

(1) Keys Affected by Shift, Alt & Ctrl (Set 2)

Key No.	Base Case or Shft + Num Lk (Make/Break)	Shift Case (See Note 1) (Make/Break)	Num Lock on (Make/Break)
32	E070/E0F070	E0F012E070/E0F070E012	E012E070/E0F070E0F012
53	E071/E0F071	E0F012E071/E0F071E012	E012E071/E0F071E0F012
105	E06B/E0F06B	E0F012E06B/E0F06BE012	E012E06B/E0F06BE0F012
33	E06C/E0F06C	E0F012E06C/E0F06CE012	E012E06C/E0F06CE0F012
54	E069/E0F069	E0F012E069/E0F069E012	E012E069/E0F069E0F012
95	E075/E0F075	E0F012E075/E0F075E012	E012E075/E0F075E0F012
106	E072/E0F072	E0F012E072/E0F072E012	E012E072/E0F072E0F012
34	E07D/E0F07D	E0F012E07D/E0F07DE012	E012E07D/E0F07DE0F012
55	E07A/E0F07A	E0F012E07A/E0F07AE012	E012E07A/E0F07AE0F012
107	E074/E0F074	E0F012E074/E0F074E012	E012E074/E0F074E0F012
36	E04A/E0F04A	E0F012E04A/E0F04AE012	

Note 1: If the left shift key is held down, the F0 12/12 shift make and break is sent with the other scan codes. If the right shift key is held down, F0 59/59 is sent. If both shift keys are down, both sets of codes are sent with the other scan code.

Key No.	Base Case (Make/Break)	Ctrl Case Shift Case (Make/Break)	Alt Case (Make/Break)
14	E012E07C/E0F07CE0F012	E07C/E0F07C	84/F084

Key No.	Base Case (Make)	Ctrl Case (Make)
16	E11477E1F014F077	

Note: This key is not auto-repeat. All associated scan codes occur on the make of the key.

EISA/SCSI Host Adapter Reference

This section describes the design and performance of the EISA/SCSI Host Adapter that interfaces a SCSI bus (multiple target or initiator) to the EISA bus. The SCSI/EISA Host Bus Adapter (WD7000-EX) contains an on-board 80C196 LCPU to control all of the data transfer between these two buses.

It is assumed that the reader is familiar with the ANSI SCSI specification, the SBIC data sheet, the ISA and EISA bus specifications, and has a working knowledge of a multi-user environment.

Throughout this specification the host bus adapter (WD7000-EX) will be referred to as the EX.

Reference Documents

The following documents provide more detailed information about the EISA/SCSI Host Adapter:

Western Digital WD7000-EX Interface Specification
Western Digital WD33C93A/B SBIC Engineering Specification
Intel 82355TM Data Sheet
Intel 80C196TM User Manual
ANSI X3T9.2 SCSI Specification Revision 8

We recommend you have these documents readily available when you use this manual.

Product Features

- 32-bit first party EISA DMA (type C DMA) up to 33 MB/s
- Supports an 8-bit wide SCSI channel (external/internal SCSI connectors)
- SCSI synchronous data transfer rates up to 10.0 MB/s
- SCSI asynchronous data transfer rates of 2.5 MB/s
- Dual EISA DMA channels for concurrent command/data processing (Intel 82355 BMIC)

- Supports two host interface protocol modes

  DACB protocol (32-bit addressing)
  ASC driver compatible mode (24-bit addressing)

- On-board 16-bit wide BIOS support for INT 13
- Supports EISA Auto Configuration Registers with the following selectable options

  Protocol Mode (ASC/DACB)
  BIOS Base Address
  Interrupt Request Level
  Bus Preempt Time
  Adapter SCSI ID
  SCSI parity enable/disable

- On-board 16-bit wide 2K high speed FIFO for continuous SCSI bus transfers
- 16-bit 80C196 Microprocessor for high performance (Intel 80C196)
- Multiple logical thread connection (up to 56)
- Host Scatter/Gather commands (up to 32 Scatter/Gather block entries)
- Support of the following SCSI features

  SCSI bus arbitration including disconnect and reselection
  SCSI link commands
  Support for Save Data Pointers, Restore Data Pointers, Abort, Reset messages
  Support for Synchronous Negotiation messages
  Zero latency reads (Modify Data Pointers message, Non-Scatter/Gather commands only)
  Terminator power supplied via on-board jumper
  Terminator power LED indicator
  1A fuse on terminator power

- On-board Power-On Self-Tests
- Connector for external drive LED

EX Architecture

The EX is an interface channel between two multi-user worlds: the EISA bus and the SCSI bus. All necessary driver/receivers are included, permitting direct cable connections to the SCSI bus through an internal and/or external 50 pin connector.

Configurable options such as 32/24-bit addressing modes, BIOS address space, interrupt request levels and adapter SCSI ID, and SCSI parity enable/disable can be selected to suit the user's application through the EISA auto configuration registers.

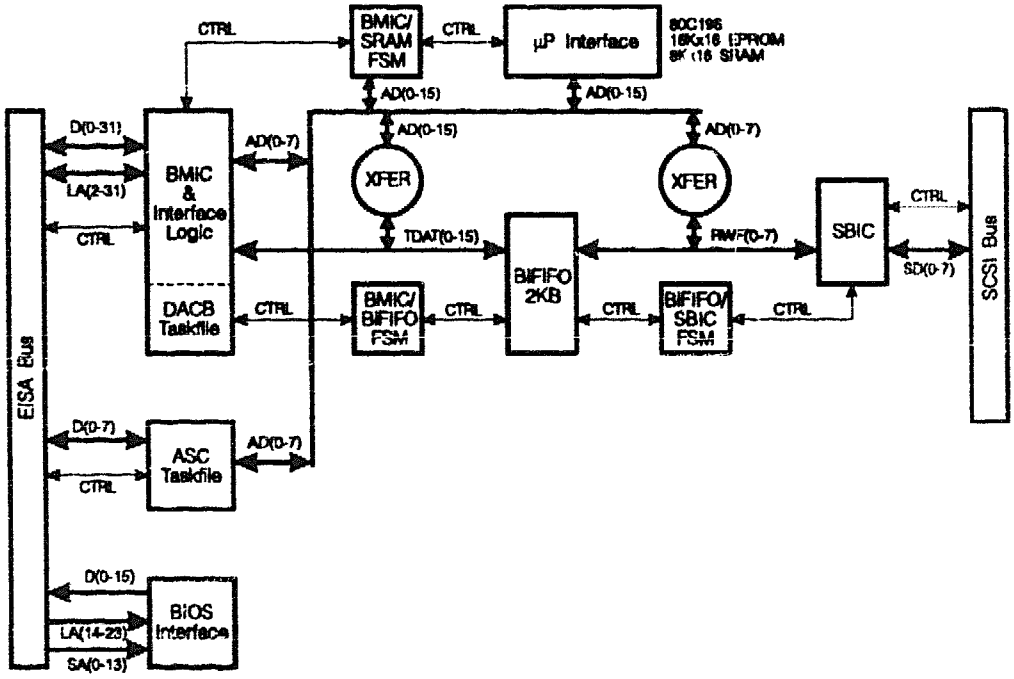
To facilitate data transfers between these 2 buses, EX contains an on-board 80C196 microprocessor (CPU), an intelligent SCSI bus controller, a 2K byte word wide DMA FIFO and a high integration EISA bus controller to maintain efficient bus utilization. First party DMA is employed to handle most of the command, data, and status information via the host interface protocol (DACB or ASC) so that several logical units can be connected simultaneously. to and from the host system memory. All other control required to transfer the data is done by the local CPU.

The SCSI interface consists of the WD33C93A/B SCSI Bus Interface Controller (SBIC) device that handles all of the arbitration, selection, disconnection, and reselection functions on the SCSI bus, leaving the CPU to manage data transfers and interrupts more efficiently. The SBIC on the EX is configured to operate as an initiator; target mode emulation is not supported on the EX. SCSI bus parity is fully supported on the board.

BIOS ROMs are provided on the EX for DOS INT 13H support, allowing the host system to boot from a SCSI drive.

Hardware Block Diagram

The following figure is a simplified hardware block diagram of the EX, with each major block displayed. The EX logic is fully described in the reference documentation or in subsequent sections of this specification.



WD7000-EX Hardware Block Diagram

EISA Host Interface Chip

The BMIC is a master mode DMA (first party DMA) controller chip designed to interface to the EISA bus. It contains three interface ports. The first port, the EISA interface port, connects directly to the host computer's EISA bus. This port provides 8 bytes of I/O decoding (zC80H to zC87H) for board ID, control, and EISA auto configuration information as well as for all the control and data lines for EISA DMA communication.

The second port, the local microprocessor port, connects to the lower byte of the local CPU's (80C196) data bus along with the associated RD-, WR- strobes and CS- with address bits LA[0:1] for register level decode. This port is used by the local CPU to communicate to the host through BMIC mailbox registers, to access EISA configuration information and manage DMA channels.

The third port, the peripheral interface port, interfaces to the 16-bit wide FIFO.

During DMA, the BMIC arbitrates for the host bus, and after it has been acknowledged, controls the address bus, data bus, and memory read/write control signals. It can transfer data to the host using word or long word data widths. The EX uses the two internal FIFOs in the BMIC for Burst DMA data transfers to/from the Host and the 16-bit wide 2K byte FIFO.

BIOS Interface

The BIOS interface is made up of two 64Kx8 EPROMs. (The EPROMs use only 16K bytes of host memory address space.) The BIOS is accessed in 16-bit mode and has associated decode and control logic. This word-wide memory interface to the host allows for increased performance.

ASC Taskfile Interface

The ASC Taskfile required for the host command protocol is implemented using a Xilinx 3030 PLD. It consists of command, control and status registers mapped into the I/O space of the host processor. The ASC 24-bit addressing protocol registers are accessed from both the host processor and the local CPU. Host course address decode is done using the IOSEL signals from the BMIC.

DACB Taskfile Interface

The DACB Taskfile required for host command protocol is mainly implemented in the BMIC. The protocol uses

- 8 of the BMIC mailbox registers as the command/response mailboxes
- the BMIC doorbell interrupt registers as command/response registers
- the BMIC doorbell enable register as the response interrupt mask
- the BMIC system interrupt enable as the system interrupt enable register

The control register is implemented in the Xilinx 3030 PLD. The DACB 32-bit addressing protocol registers are mapped into the EISA slot-specific I/O space and are accessed by both the host processor and the local CPU.

Microprocessor Interface

The microprocessor interface is made up of an 80C196 microcontroller, two 64Kx8 EPROMs for 64K of 16-bit-wide ROM, two 8Kx8 SRAMs for 16K of 16-bit-wide RAM, a 2K byte Bi-FIFO (IDT72520), the BMIC, the SBIC and the ASC Taskfile implemented using the Xilinx PLD. The 80C196 is used to control the devices which interface to the host and SCSI bus, and to aid in data transfers to/from the SCSI bus from/to the Host bus.

Bi-FIFO

The IDT72520 is a high-integration 2K byte FIFO with two bidirectional ports, A and B. Port A of the FIFO is 16 bits wide and interfaces to the 80196 LCPU for configuration and control and to the BMIC for data transfers. Port B of the FIFO is 8 bits wide and interfaces to the WD33C93A/B SBIC chip for data transfers. The FIFO offers programmable interfaces and flags, and provides the necessary 8-bit to 16-bit data conversion between the SBIC and the BMIC interfaces.

DMA State Machine Interface Logic

A DMA state machine (implemented using 16V8A and 20V8A GALs) controls the interface between the BMIC and RAM, between the BMIC and the Bi-FIFO, and between the Bi-FIFO and the SBIC.

The **BMIC to RAM** interface logic transfers command and status information to and from the local RAM to the BMIC's internal 28 byte FIFO. The state machine puts the CPU on hold and controls the BMIC's transfer buffer and the RAM while transferring bytes between these two devices.

The **BMIC to Bi-FIFO** interface logic controls the BMIC's transfer buffer and the Bi-FIFO while transferring bytes between these two devices. For SCSI read/EISA host memory write operations, the interface logic also monitors Bi-FIFO thresholds and enables or disables data transfers to the host accordingly.

The **Bi-FIFO to SBIC** interface logic controls the SBIC DMA interface and the Bi-FIFO while transferring bytes between these two devices. For SCSI read/EISA host memory write operations, the interface logic also monitors END OF SCSI DATA TRANSFER phase and loads dummy bytes into the Bi-FIFO to solve BMIC overreads and to handle odd byte transfers to the host.

SCSI Bus Interface Chip

The SBIC is a high-integration SCSI Bus Interface Chip which connects directly to and controls the SCSI bus. The SBIC is controlled via high level commands by the on-board microcontroller. The internal micro engine of the SBIC allows it to step through the various SCSI bus phases with minimal CPU interaction. This allows the local CPU to parse and queue up other commands while the SBIC processes the current command. The SBIC is programmed to use Burst-DMA mode for data transfers between itself and the Bi-FIFO.

For more details on the SBIC please refer to the WD33C93A/B Data sheet.

Host Interface

The EX host bus adapter interfaces to the EISA bus at three levels, 32-bit bus master DMA mode for command, data and status transfers, 8-bit I/O slave mode for host configuration and control access and a 16-bit memory slave mode for BIOS access. The EISA bus control signals interface directly to the BMIC while the address and data busses are buffered through latches and transceivers.

In 32-bit bus master DMA mode, the BMIC requests control of the EISA bus by asserting slot-specific signal MREQx- and waiting for bus acknowledge MAKx-. Once the BMIC gets bus grant, it takes control of the EISA bus, driving the address, data and host memory access control signals. The BMIC retains control of the bus until there are no more transfers pending inside the BMIC or until it is preempted by another bus master device on the bus.

The 8-bit I/O slave mode is used by the host to

- read board ID and status information
- load configuration information
- issue board reset and SCSI bus reset commands
- enable interrupt request lines
- pass CCB related information such as mailbox number or address pointer to the LCPU

The Taskfile required to run ASC host protocol in 24-bit addressing mode and EISA auto-configuration registers are implemented using an Xilinx XC3030 (68 pin PLCC) PLD. The I/O base addresses for the Taskfile and configuration registers are decoded by the BMIC through the BMIC's two general purpose programmable I/O decode registers.

The 16-bit memory slave mode is used for BIOS support of DOS INT13H functions. The BIOS resides in the high-memory address space anywhere from C0000 through DFFFF (programmable through EISA auto-configuration registers). The BIOS uses 16K of the host memory address space.

Hardware

The EX controller has three on-board connectors. These connectors consist of 1 host interface (EISA) edge connectors, an internal 50 pin shrouded header and 50 pin standard external SCSI interface connector. Power for the EX is supplied by the host interface.

EISA Edge Connectors

The EISA edge connectors provide interface signals that are used for communication with the EISA bus. For a complete description of signals on the EISA bus, refer to *EISA 32-bit expansion slots* in *System Configuration*. For more information about master mode DMA, 8-bit I/O slave mode and 16-bit memory slave mode, refer to the EISA bus specification 3.10 and the Intel 82355 BMIC device specification.

SCSI Interface Connectors

The EX contains two (2) SCSI connectors. The connectors include an internal 50-pin shrouded header consisting of 2 rows of 25 male pins and a 50-pin external D shaped female connector. The SCSI interface is completely defined by the ANSI X3T9.2 SCSI Specification Rev 8.

Firmware

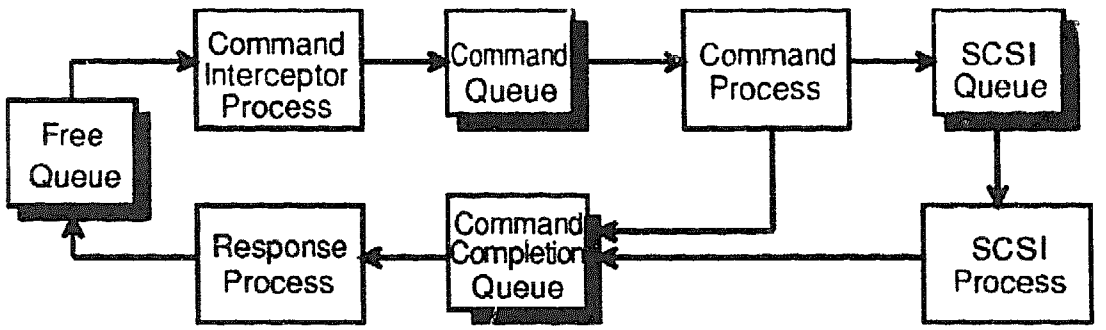
The EX firmware design segregates the SCSI firmware from the host protocol firmware. An internal interface between the SCSI and host firmware accommodates this segregation.

The host firmware is responsible for handling all functions associated with the EISA interface protocol. Such functions include inputting all command information, performing all command pre-processing, outputing all response information, and processing all internal host bus adapter commands. In this case, the host firmware is responsible for emulating two distinct protocols, the DACB 32-bit addressing protocol and the ASC 24-bit addressing protocol.

The SCSI firmware is responsible for handling all SCSI functions associated with the SCSI protocol as well as handling the initiation of all data DMA functions (host data DMA and SCSI bus DMA). The major task of the SCSI firmware is to control the SCSI interface chip and handles all its needs.

Firmware Process Map

The following figure is a simplified process map of the EX firmware. The figure displays the major processes of the firmware and depicts the normal flow of EX command processing.



Firmware Process Map

Command Interceptor Process

The command interceptor process is the first process executed when processing a command on the EX. This process is interrupt driven, responding to a host interrupt informing the adapter that a command is available. The command interceptor is responsible for handling the command interrupt protocol, inputting the necessary command information from the host I/O registers and storing that information in a buffer packet available from the free queue. The process will acknowledge the host interrupt and place the buffer packet on the command queue.

Command Process

The command process begins its execution when a command becomes available on the command queue. This process is responsible for DMAing all pertinent command information into the buffer packet and making the decision if the command is a SCSI command or internal adapter command.

If the command is an internal adapter command, the process will handle all transactions associated with the command. Upon completion of any required transactions, the command process will place the buffer packet on the command completion queue.

If the command is a SCSI command, the process will perform all the pre-processing required on the buffer packet before the command is executed on the SCSI bus. Upon completion of all pre-processing, the buffer packet is placed on the SCSI queue.

SCSI Process

The SCSI process begins its execution when a command becomes available on the SCSI queue. This process is responsible for executing the command on the SCSI bus. The process will handle all data transfer transactions between the EISA and the SCSI bus and handle all SCSI exception conditions to ensure the command gets processed properly on the SCSI bus. Upon SCSI command completion, the process will report all the appropriate completion status in the buffer packet and place the buffer packet on the command completion queue.

Response Process

The response process begins its execution when a command becomes available on the command completion queue. The process is responsible for handling all command completion interrupt protocol and DMAing all completion status to host memory. The process waits for host

acknowledgement of the command completion interrupts and returns the complete command buffer packet onto the free queue.

Host Interfaces

The EX supports two host protocols in the firmware, the DACB protocol (32-bit addressing) and the ASC protocol (24-bit addressing).

DACB Protocol

The DACB (Direct Access Control Block) protocol allows 32-bit host memory access on the EISA bus. The protocol is a simplified version of the mailbox protocol where only a single mailbox exists. This mailbox is embedded on the adapter allowing quicker access to the command information.

ASC Protocol

The ASC protocol allows 24-bit host memory access on the EISA bus. The protocol supported on the EX is a condensed version of the protocol available on the WD7000-ASC host bus adapter. This condensed version of the protocol supports the commands necessary to be compatible with the ASC software drivers.

SCSI Interface

The SCSI channel has the capability of supporting either 5.0 MB/s or 10.0 MB/s synchronous transfers (this is accomplished through board build options) and 2.5 MB/s asynchronous transfers. The SCSI channel conforms to the ANSI SCSI specification.

BIOS

The EISA/SCSI Host Adapter BIOS is used to support various disk I/O functions and to allow EISA style PCs to boot from SCSI drives. We will call this adapter BIOS, the "SCSI BIOS".

The SCSI BIOS intercepts MS-DOS system requests invoked via the INT13H handler, performs translation to SCSI type commands, dispatches commands to the adapter and returns status to the caller. The INT13H requests that are supported are Read, Write, Verify, etc.

In a DOS environment, the SCSI BIOS will be used for booting and supporting disk I/O functions The EX is user configurable to support the 32-bit Direct Access (DACB) protocol or 24-bit mailbox (ASC) protocol. The BIOS queries the configuration information stored in the system's non-volatile RAM and configures itself in one of the two modes.

BIOS Installation

The SCSI BIOS's specific address is selectable through the EISA auto-configuration registers. It may be located anywhere within the system address range C0000h to EE000h. The adapter BIOS is an extension of the motherboard BIOS and is installed during power-up and self-test (POST).

The system BIOS scans for an extension BIOS located in the above address range. If it sees a signature pattern '55AA', it assumes the next byte is the length of this BIOS (in blocks of 512 bytes) and that the entry point for the initialization of this BIOS follows the length byte. Having found a BIOS extension, the system BIOS performs a checksum of the BIOS extension and if that passes it performs a FAR JUMP to the SCSI BIOS entry point.

After the SCSI BIOS performs its installation, it returns control to the system BIOS. The system BIOS then executes INT19H interrupt to initiate boot. INT19H tries to read boot sector from the floppy drive 0 and if that fails it resets the disk subsystem and reads the boot sector from the hard disk.

Adapter BIOS Installation

At POST time, when control is passed to the SCSI BIOS, it resets the adapter. If adapter reset fails then the BIOS aborts its initialization. If adapter reset is successful, the BIOS reads the adapter configuration information which was previously stored in the system's non-volatile RAM. This information consists of the adapter's SCSI ID, 24-bit or 32-bit protocol indicator, and the adapter's base port addresses (if 24-bit mode).

The INT13H BIOS has a limitation of supporting only two fixed disk drives as logical drive 80 and logical drive 81. The SCSI BIOS determines the number of fixed drives that are installed by reading the system memory location 0:475. If no drives are already installed, then up to two SCSI disks can be supported by the BIOS. If one drive is already installed, only one SCSI disk can be supported by the BIOS. If two drives are installed, then no SCSI disks can be supported by the BIOS and it aborts installation. Any SCSI disks not supported by the BIOS will need an installable device driver.

The SCSI BIOS scans the SCSI bus and maps the logical drives 80 and 81 to a SCSI target and Logical Unit Number (LUN). It saves this information for later use when an INT13H request arrives for a particular device. Finally the BIOS installs itself by saving the original INT13H vector and loading the new INT13H vector into the SCSI BIOS.

Interface Conventions

An INT13H request is accompanied by a number of parameters passed in the processor registers. The input parameters are listed below:

AH = Function code.
AL = Number of sectors transferred. (512 bytes per sector)
DH = Head number.
DL = Drive number. (80 or 81 for hard disk; 00 or 01 for floppy disk)
CH = Low 8-bits of 10-bit cylinder number.
CL = bits 7 & 6 are high 2 bits of 10-bit cyl number and bits 0-5 are sector number.
AL = number of sectors to read.
ES:BX = address of buffer for reading to/from.

Upon exit, the carry flag (CF) will be set in case an error is encountered and cleared if no error is encountered. The actual status code for the operation is stored in register AH.

INT13H Functions

A DOS application or system service performs a disk I/O by loading the processor register AH with a function code and calling the INT13 routine. The INT13H functions as supported by the SCSI BIOS are listed below.

AH	Function	SCSI command
00h	Reset disk subsystem	Bus Device Reset
01h	Read status of last oper.	Request sense command
02h	Read data	10 byte read data.
03h	Write data	10 byte write data
04h	Verify	10 byte verify command
08h	Read drive params	Read capacity command
09h	Initialize drive character	No operation
0Ch	Seek	Seek command
0Dh	Alternate disk reset	Bus device reset to Target/LUN
10h	Test unit ready	Test unit ready command
11h	Recalibrate	Rezero unit command
15h	Read DASD Type	Read capacity command
1Ah	Format unit	Format unit command

Status Returned By BIOS

After a command is completed a status code is returned by the SCSI BIOS in the AH register. A carry is also set in case of an error.

Status (AH)	Sense Key	Additional Sense Key	Description
0 No error code	NA	NA	
1 Invalid function request	NA	NA	Unsupported function or bad parameter
2 Address mark not found	3H	1200H 2100H 2101H	No address mark found Illegal LBA Invalid Address
3 Write protect error	7H		Data protect error
4 Sector not found	8H	1400H,1401H	No record found
5 Reset failed	NA		
7 Drive parameter fail	NA		
10 Uncorrectable ECC or CRC error	3H	10H 11H	Medium error Unrecovered read
11 ECC Corrected data	1H	1700H 1800H	Recovered w/o ECC Recovered w/ ECC
20 General controller failure	2H,4H		Adapter command timeout
40 Seek operation failed	NA	02H 15H	No seek performed Seek position error
80 Timeout	NA		Adapter timeout / selection timeout
AA Drive not ready	2H	0400H-0404H	LUN not ready
BB Undefined error	NA		

INT13H Requests

The SCSI BIOS provides an extension to the system BIOS when requests are made for disk services. When a request for disk service is made via a software INT 13H, the request arrives at the SCSI BIOS. If the request is not for the SCSI drives, it is passed along to the original system BIOS INT13H handler. If the device number is below 80H (DL = 0 or DL = 1), it is passed on to the original INT13H handler which is saved in the diskette re-vector location INT40H. If the device number is larger than 80H and less than the first SCSI device, then the request is sent to the old INT13H handler.

For instance logical drive 0 (DL = 80) may be mapped to an ESDI drive and logical drive 1 (DL = 81) may be mapped to SCSI drive at Target# 1 and LUN# 0. If a request arrives for drive 0, then it is passed along to the old INT13H handler. If a request arrives for drive 1, the SCSI BIOS must handle it by building a SCSI command block for Target# 1 and LUN# 0.

If the request is determined for the SCSI drive, it is tested to be in range. Next, the function number in AH is used to access a jump table to call the appropriate function routine. Throughout these operations, the stack is used for storing temporary data and the stack is restored upon exit.

The INT13H routines handle the I/O command initiation and command completion. The typical commands that it handles are Read, Write, Format and Verify etc. As noted previously, the function to be performed and the associated parameters are loaded into the processor registers. These registers contain the function code, the number of sectors to be transferred, the head number, the drive number, the cylinder number, the sector number and a pointer to the host memory data area for reading from or writing to.

The BIOS has to convert the head, cylinder and sector number into the logical block address that SCSI devices understand. The BIOS assumes 32 sectors per track per head, 64 heads and 512 bytes per sector for a 1MByte logical cylinder size. The mapping from a cylinder number, head number and sector number to a logical block address is:

LBA = (cylinder#) * (SPT) * (# of heads) + (head#) * (SPT) + sector#

Note: Cylinders and heads are 0-based and sectors are 1-based.

A SCSI command descriptor block is built from these parameters and issued to the host bus adapter. The BIOS polls the interrupt status register in the adapter for command completion.

INT4BH Functions

When the adapter is running in a virtual mode environment such as Windows or Quarterdecks QEMM, the linear memory addresses are different from physical addresses. This presents a problem for adapters which perform first party DMA (Bus Masters) and hence requires knowledge of true physical addresses. Fortunately, virtual memory environments such as Windows and QEMM v5.0 provide services which allow for linear to physical address translation. These services are called INT4BH function 80H DMA services. The INT13H BIOS checks for the presence of these services and if they are available, it makes a request to translate all addresses to true 32-bit physical addresses. In addition INT13H also locks those areas of memory under use so that they do not get swapped out of memory. These addresses are then used in building SCSI Control Blocks which are presented to the adapter. This guarantees that the INT13H will work in virtual mode environments. If the DMA services are not available, then INT13H assumes that the linear addresses are indeed the same as physical and no translation is performed. In real mode environments the linear addresses are obtained from logical addresses by shifting left the segment component and adding to it the offset component. Refer to the DECpc 433T Applications Bulletin for more information about the INT4BH compatible driver for MS-DOS.

Microprocessor I/O Map

The following table shows the CPU memory map.

Address (Hex)	Bytes	Description
0000 - 7FFF	32K (16K x 16)	EPROM
8000 - BFFF	16K (8K x 16)	RAM
C000 - C0FF	256 (256 x 8)	BMIC
C100 - C1FF	256 (256 x 8)	ASC Taskfile
C200 - C2FF	256 (128 x 16)	Bi-FIFO
C300 - C3FF	256 (256 x 8)	SBIC
C400 - C4FF	256 (256 x 8)	Configuration Register
C500 - C5FF	256 (256 x 8)	XILINX Programming

EISA I/O Registers

The following table shows the EISA I/O registers accessible to the host.

Address (Hex)	Description
zC80	EX ASCII Board ID
zC81	EX ASCII Board ID
zC82	EX ASCII Board ID
zC83	EX ASCII Board ID
zC85	EISA Config. Register 1
zC86	EISA Config. Register 2
zC87	EISA Config. Register 3

DACB I/O Registers

The following table shows the DACB I/O registers accessible from the host.

EISA Address (Hex)	Register
zC90 - zC93H	Command Mailbox (4 bytes)
zC94 - zC97	Response Mailbox (4 bytes)
zC8D	Command Register (1 byte)
zC8F	Response Register (1 byte)
zC8E	Response Interrupt Mask (1 byte)
zC89	System Interrupt Enable (1 byte)
zCB2	Control Register (1 byte)

ASC I/O Registers

The following table shows the ASC I/O registers accessible to the host. The I/O base address for these registers is selectable through the EISA Auto Configuration Register 3 (refer to WD7000-EX Interface Specification for details).

Register	I/O Address Offset (Hex)
Command	00
Status	00
Interrupt Acknowledge	01
Interrupt Status	01
Control	02

Specifications

Performance

Host Transfer Rate:	33 Mbytes/sec burst
SCSI Transfer Rate:	10.0 Mbytes/sec Synchronous 2.5 Mbytes/sec Asynchronous
80196 Clock:	12 MHz
Intel 82355 (BMIC Clocks)	
Bus Clock (BCLK)	8.25 MHz
Transfer Buffer Interface Clock (TCLK)	12.5 MHz
WD33C93A/B Clock:	20 MHz
IDT72520 Clock:	20 MHz
Selection Timeout:	Programmable
Logical Threads:	56

Power Requirements

Voltage:	+5 V_{DC} ±5%
Ripple:	100m$V_{p\text{-}p}$ (max)
Current:	
Typical	1.9 A
Max.	2.5 A

Mechanical

Form Factor:	EISA

Length:	13.395 in
Width:	5.000 in
Height:	0.500 in
Host Interface:	32-bit EISA Bus
	118 pin Card Edge Connector
	68 pin Card Edge Connector
SCSI:	8-bit SCSI bus
SCSI Cable Length:	6 meters @ 5MB transfer rate
SCSI Connector:	50 pin Internal 50 pin External

Environmental

Temperature	
Operating	10°C to 50°C (50°F to 122°F)
Non-operating	-40°C to 60°C (-40°F to 140°F)
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20 ms square wave maximum
Vibration	1G/0-600 Hz, dwell not to exceed
Altitude	
Operating	0 to 3000 meters (max)
Non-operating	0 to 5000 meters (max)

Regulatory

FCC Class B

Reliability

MTBF 100170 Hours

Timing

Host Timing

EISA Timing as per EISA Specification 3.10

SCSI Timing

SCSI as per ANSI SCSI Specification

Also refer to the WD33C93A/B Specification

Specifications and Features

Features

The features of the VGA 1024 adapter include:

- compatibility with software written for the Hercules Graphics Card and the IBM video standards preceding VGA: Monochrome Display Adapter (MDA), Color/Graphics Adapter (CGA), Multi-Color Graphics Adapter (MCGA), and Enhanced Graphics Adapter (EGA)
- support for 80- and 132-column text modes
- a palette of over 262,000 possible colors
- 512 kilobytes (KB) of video memory to support the 640 x 480, 256-color and 1024 x 768, 16-color Super VGA modes
- support for both monochrome and color, fixed or multi-frequency VGA analog monitors
- a high-speed, 16-bit video BIOS with AutoSense, which enables use in 8-bit as well as 16-bit bus computers

Supported Video Modes

In addition to the default mode, the VGA 1024 adapter supports the following classes of video modes:

- Standard VGA modes, EGA modes, and MCGA modes which provide resolutions of up to 640 x 480.
- Super VGA modes which provide even higher resolutions and the ability to display more colors simultaneously. Super VGA can also display text 132 columns wide and 25 or 43 lines deep.
- CGA, Hercules, and MDA modes which may be required by applications designed to run under the pre-EGA/VGA video standards (CGA, Hercules, and MDA). For example, to run Hercules-compatible software and some CGA-compatible games, you must use a Hercules or a CGA mode. When in a CGA, a Hercules, or an MDA mode, the adapter emulates the earlier video standard.

Standard VGA Modes

Mode (Hex)	Video Standard	Type	Colors	Resolution	Columns Rows	Buffer	Char Size	Monitor	Notes
	Hercules	graphics	mono	720x348	80x25	B0000	9x14	A-C	
0,1	CGA	text	16	320x200	40x25	B8000	8x8	A-C	1
0,1	EGA	text	16	320x350	40x25	B8000	8x14	A-C	
0,1	VGA	text	16	360x400	40x25	B8000	9x16	A-C	
2,3	CGA	text	16	640x200	80x25	B8000	8x8	A-C	1
2,3	EGA	text	16	640x350	80x25	B8000	8x14	A-C	
2,3	VGA	text	16	720x400	80x25	B8000	9x16	A-C	2
4,5	CGA	graphics	4	320x200	40x25	B8000	8x8	A-C	1
6	CGA	graphics	mono	640x200	80x25	B8000	8x8	A-C	1
7	MDA	text	4	720x350	80x25	B0000	9x14	A-C	
7	VGA	text	4	720x400	80x25	B0000	9x16	A-C	3
D	EGA	graphics	16	320x200	40x25	A0000	8x8	A-C	1
E	EGA	graphics	16	640x200	80x25	A0000	8x8	A-C	1
F	EGA	graphics	4	640x350	80x25	A0000	8x14	A-C	
10	EGA	graphics	16	640x350	80x25	A0000	8x14	A-C	
11	VGA	graphics	mono	640x480	80x30	A0000	8x16	A-C	
12	VGA	graphics	16	640x480	80x30	A0000	8x16	A-C	
13	VGA	graphics	256	320x200	40x25	A0000	8x8	A-C	1

Monitors

A: Fixed-frequency analog
B: Multi-frequency analog (horizontal freq = 35.2 KHz)
C: Multi-frequency analog (horizontal freq = 35.5 KHz)

Notes

1: All 200-line modes are double scanned to display 400 lines
2: Default mode for color monitors.
3: Default mode for monochrome monitors.

Super VGA Modes

Mode (Hex)	VESA Mode (Hex)	Type	Resolution	Colors	Columns Rows	Buffer	Char Size	Monitor	Notes
54		text	924x387	16	132x43	B8000	7x9	A-C	
54		text	1056x387	16	132x43	B8000	8x9	A-C	1
55		text	924x400	16	132x25	B8000	7x16	A-C	
55		text	1056x400	16	132x25	B8000	8x16	A-C	1
56		text	924x387	4	132x43	B0000	7x9	A-C	
56		text	1056x387	4	132x43	B0000	8x9	A-C	1
57		text	924x400	4	132x25	B0000	7x16	A-C	
57		text	1056x400	4	132x25	B0000	8x16	A-C	1
58	6A	graphics	800x600	16	100x75	A0000	8x8	B	
58	102*	graphics	800x600	16	100x75	A0000	8x8	B	
59	6B	graphics	800x600	mono	100x75	A0000	8x8	B	
5A		graphics	1024x768	mono	128x48	A0000	8x16	C	2
5B		graphics	1024x768	4	128x48	A0000	8x16	C	2
5D	104*	graphics	1024x768	16	128x48	A0000	8x16	C	2,3
5E	100*	graphics	640x400	256	80x25	A0000	8x16	A-C	
5F	101*	graphics	640x480	256	80x30	A0000	8x16	A-C	3

*Requires use of VESA EXE terminate-and-stay-resident file. Refer to README.TXT.

Monitors

A: Fixed-frequency analog
B: Multi frequency analog (horizontal freq = 35.2 KHz)
C: Multi-frequency analog (horizontal freq = 35.5 KHz)

Notes

1: Multi-frequency monitor setting.
2: Interlaced mode.
3: Requires 512KB of video memory. Other modes require 256KB.

Specifications

Size	15.6 cm x 8.4 cm (7.25 in. x 3.9 in.) (The adapter fits in a full-sized expansion slot.)

Video Signals

Black level	0V
Full-intensity level	+0.7V

Sync Signals

Fixed-Frequency Monitor (DIP Switch 1 OFF)

Video Mode	Horizontal Sync Frequency (Polarity)	Vertical Sync Frequency (Polarity)
350 lines	31.5 kHz (+)	70.1 Hz (−)
200 lines	31.5 kHz (−)	70.1 Hz (+)
400 lines	31.5 kHz (−)	70.1 Hz (+)
480 lines	31.5 kHz (−)	59.9 Hz (−)
132 columns	31.5 kHz (−)	70.0 Hz (+)

Multi-Frequency Monitor (DIP Switch 1 ON)

Video Mode	Horizontal Sync Frequency (Polarity)	Vertical Sync Frequency (Polarity)
350 lines	31.5 kHz (+)	62.3 Hz (−)
200 lines	31.5 kHz (−)	62.3 Hz (+)
400 lines	28.0 kHz (−)	62.3 Hz (+)
480 lines	31.5 kHz (−)	59.9 Hz (−)
132 columns	27.6 kHz (−)	61.5 Hz (+)
600 lines	35.2 kHz (−)	56.2 Hz (−)
* 768 lines	35.5 kHz (+)	86.9 Hz (+)

* 1024 x 768 requires an interlaced monitor

Configuration

System Requirements

The adapter can be installed in either an 8-bit XT slot, an 8/16-bit ISA slot, or a 32-bit EISA expansion slot. If the computer has on-board VGA circuitry, you must disable the on-board VGA circuitry before installing the VGA 1024 adapter.

The adapter can be used with any interlaced multi-frequency monitor. Available video modes will depend on the monitor frequency. Refer to *Sync Signals* in *Features and Specifications*.

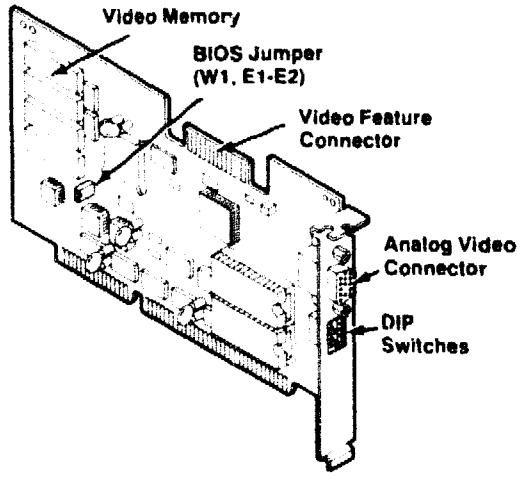
Caution: Static electricity can destroy integrated circuits. Be sure to discharge any built-up static electricity by touching a grounded, metal object before handling the adapter or touching any of the computer's logic boards.

If You Have an EMS Adapter

The VGA adapter uses memory locations A0000h-C7FFFh (the same memory locations as a standard EGA card) plus an additional 16KB for the extended video BIOS ROM. If you have an EMS (Expanded Memory Specification) adapter, that adapter **must not** conflict with these memory locations. Check with the manufacturer of your EMS adapter for information about configuring it for use with a VGA-compatible video board. You might need to exclude locations A0000-C7FFF from use by your EMS driver. Usually, you can designate these exclusions when starting your EMS driver.

Adapter Layout

The following illustration shows the locations of the jumper block and the DIP switches:



Analog Video Connector: The monitor connects to this 15-pin connector. The adapter supports monochrome and color analog PS/2 fixed-frequency monitors as well as compatible analog multi-frequency and dual-frequency monitors.

DIP Switches: These four switches enable you to define the video configuration of the computer. Refer to *DIP Switch Settings* later in this section for information on using these switches.

Video Feature Connector: This connector enables the connection of a high-resolution specialty video expansion adapter. It is provided to maintain complete compatibility with the IBM VGA standard.

Video Memory: 512KB of video memory enables support of all the Super VGA modes. The 256-color, 640 x 480 graphics mode and the 16-color, 1024 x 768 graphics mode require 512KB of video memory.

Manual 16-Bit Video BIOS Jumper (W1): Do not remove this jumper. It is used to manually override the AutoSense circuit and enable the 16-bit video BIOS to be used in systems that do not support AutoSense. This jumper should be set over both pins for normal operation using AutoSense.

Slot Connectors: These connectors plug into the expansion slot inside the computer.

Jumper and DIP Switches

The jumper and the DIP switches on the adapter are set at the factory for proper operation. Normally, you do not need to change the jumper or the DIP switches from the factory settings.

Caution: Removing the BIOS jumper might cause improper operation of the adapter.

Factory default settings

Explanations of the factory settings are listed in the following table:

Jumper/ Switch	Factory Setting	Explanation
W1	Jumper installed	Enables normal operation using AutoSense
Switch 1	OFF	Enables standard PS/2-compatible fixed-frequency display timing
Switch 2	ON	Selects PS/2-style as the manner of mode switching; makes all VGA modes available on any monitor
Switch 3	OFF	Not used
Switch 4	ON	Enables 16-bit video memory data path and uses AutoSense for 16-bit BIOS

Manual 16-Bit Video BIOS Jumper (W1)

Jumper W1 can be used to manually override the AutoSense circuit and enable the 16-bit video BIOS to be used in computers that do not support AutoSense. This jumper should be set over both pins for normal operation using AutoSense. Do not remove this jumper.

W1	BIOS Jumper
ON *	Normal AutoSense operation
OFF	Forced 16-bit BIOS path

* indicates factory setting

Caution: Removing the BIOS jumper might cause improper operation of the adapter.

DIP Switch Settings

The four DIP switches are located below the video connector on the adapter. Some switch settings are sensed only when you turn on the computer, so always turn off the computer before changing switch settings.

Monitor Timing Select (SW1)

Switch 1 enables the adapter to use special timing for multi-frequency monitors or standard VGA timing for fixed-frequency PS/2 monitors. The multi-frequency setting allows video to be displayed on some multi-frequency monitors using a larger screen area than standard PS/2 monitors. Some newer multi-frequency monitors will work better using the PS/2 monitor timing.

You might want to experiment with the two settings to determine the best results for your particular brand of multi-frequency display.

Note: If you are using an IBM PS/2 display or equivalent fixed-frequency display, select PS/2-compatible display timing (Switch 1 OFF).

Switch 1	Monitor Type
ON	Special multi-frequency display timing
OFF *	Standard PS/2-compatible fixed-frequency display timing

* indicates factory setting

VGA Mode Switching Implementation Type (SW2)

Switch 2 selects the manner in which the VGA adapter handles switching between color and monochrome VGA modes. Set Switch 2 to the ON position to select PS/2-style VGA implementation. If Switch 2 is set to ON and a monochrome monitor is connected, the adapter defaults to color text mode with 16 shades of gray.

Switch 2	Implementation Type	VGA Mode Switching
ON *	PS/2 style	all VGA modes available on any monitor
OFF	PC/AT style	color modes on color monitors, monochrome modes on monochrome monitors

* indicates factory setting

Note: Switch 3 (SW3) is reserved and should be set to OFF.

16-Bit/8-Bit BIOS Select (SW4)

In the ON position, Switch 4 selects 16-bit operation and enables full 16-bit operation whenever possible. The OFF position forces the VGA adapter to operate in 8-bit mode (even if it is installed in a 16-bit expansion slot), disables AutoSense and specifies an 8-bit BIOS and video memory data path. This switch is ignored in any 8-bit expansion slot because the adapter must operate in 8-bit mode with an 8-bit BIOS.

Switch 4	8-Bit or 16-Bit and AutoSense
ON *	Enable 16-bit video memory data path and use AutoSense for 16-bit BIOS
OFF	Force 8-bit video memory data path and 8-bit BIOS

* indicates factory setting

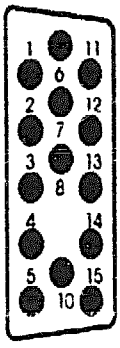
Note: The 16-bit video memory data path is possible only if the VGA 1024 adapter is the only video adapter installed.

Connector Pinouts

The following tables indicate the pin functions of the VGA adapter connectors.

Video Port Connector Pinout

Pin	Function
1	Red Video
2	Green Video
3	Blue Video
4	Monitor ID Bit 2 (not used)
5	Ground
6	Red Return (ground)
7	Green Return (ground)
8	Blue Return (ground)
9	Key (no pin)
10	Sync Return (ground)
11	Monitor ID Bit 0 (ground)
12	Monitor ID Bit 1 (ground)
13	Horizontal Sync
14	Vertical Sync
15	Not Used



Monochrome-type monitors use Green Video for all video input and ignore Red Video and Blue Video.

Monitor ID Bits are not used in the VGA 1024. Monitor type is determined by an automatic sensing circuit when your system is turned on.

Video Feature Edge Connector Pinout

Front (Component) Side of the Adapter

Pin	Function
Y1	C0 (Color Bit 0)
Y2	C1 (Color Bit 1)
Y3	C2 (Color Bit 2)
Y4	C3 (Color Bit 3
Y5	C4 (Color Bit 4)
Y6	C5 (Color Bit 5)
Y7	C6 (Color Bit 6)
Y8	C7 (Color Bit 7)
Y9	DAC Clock
Y10	DAC Blanking
Y11	Ext. Horizontal Sync
Y12	Ext. Vertical Sync
Y13	Ground

Back (Solder) Side of the Adapter

Pin	Function
Z1	Ground
Z2	Ground
Z3	Ground
Z4	Select Internal Video
Z5	Select Internal Syncs
Z6	Select Internal DAC Clock
Z7	Not Used
Z8	Ground
Z9	Ground
Z10	Ground
Z11	Ground
Z12	Not Used
Z13	Not Used

Theory of Operation

Introduction

The VGA 1024 is a mid-size card that provides enhanced VGA capability for IBM PC/XT/AT, IBM PS/2 model 25 / model 30 and compatible computers. It is completely hardware and software compatible with the IBM PS/2 VGA Display Adapter. In addition to basic VGA modes, it provides extended modes for 132-column text, 1024 x 768 x 16 color graphics, 800 x 600 x 16 color graphics, and extended 256 color modes with 640 x 480 pixel resolution. The 1024 x 768 graphics mode is only supported on interlaced multi-frequency monitors. The 800 x 600 graphics mode is only supported on multi-frequency monitors. All other modes are supported on the PS/2 monitor types 8503, 8512, 8513, and compatibles. The board is built around the WD90C00 Enhanced VGA Controller and has an 8- or 16-bit interface to the system bus.

When enabled, a special "AutoSense" circuit can detect if the board will reliably operate in the host system with a 16-bit data path to the BIOS ROM. If not, it will automatically switch to 8-bit operation.

The video output signals are analog RGB and digital syncs, available on a PS/2 compatible 15-pin D-shell connector. The VGA 1024 board's AutoMonitor feature automatically detects whether a color or monochrome analog monitor is connected and it defaults at power-up to VGA quality text in a VGA mode appropriate to the type of monitor connected.

Special features of the VGA 1024 include the AutoSense and AutoMonitor circuitry mentioned above, and 512KB of video memory.

The VGA 1024 interfaces to the system bus address, data, and control signals providing word-wide data transfers. No hardware interrupts are generated by the VGA 1024 card.

Overview

The VGA 1024 board's hardware consists of the WD90C00 chip, four 8-bit memory maps capable of addressing 128KB for each map, the BIOS subsystem, a RAM Digital-to-Analog Converter (RAMDAC), and associated support and I/O logic.

There are six main sections to the VGA 1024 board's hardware:

1. I/O bus circuitry
2. WD90C00 Enhanced VGA Controller
3. Display memory
4. BIOS subsystem
5. RAMDAC
6. Support logic

I/O bus

The VGA 1024 board interfaces to the system bus. It can support bus speeds from 4.77 MHz to 12 MHz. Both 8- and 16-bit operations are supported when accessing either the video BIOS ROM or the display memory.

The VGA 1024 board has the hardware and software required to automatically detect if a 16-bit interface between the video BIOS and the system bus will operate reliably in a particular host system - this function is called AutoSense. AutoSense is necessary because the tight timing requirements imposed on 16-bit operation and the necessity to use the latched address lines to fully decode (down to 32K) BIOS accesses. Full decoding with latched address is necessary to avoid triggering an erroneous 16-bit transfer attempt to an 8-bit device in the same unlatched address space (only 128K resolution). If AutoSense detects unreliable 16-bit operation it will switch the board to 8-bit operation. AutoSense is controlled by DIP switch 4. If DIP switch 4 is OFF at power-up the VGA 1024 will operate using an 8-bit BIOS and not perform the AutoSense tests. If DIP switch 4 is ON, the AutoSense test will be performed and, based on the results of this test, will enable either an 8- or 16-bit BIOS data path. A summary of jumper W1's operation is below:

W1	Removed	Manual 16-bit BIOS data path selection. If it is known that no other devices are resident in the 128K address space from C0000h to DFFFFh, then removal of this jumper will enable a 16-bit BIOS data path using unlatched addresses. The AutoSense test is not performed.
W1	Installed	Allows AutoSense to select 8- or 16-bit BIOS data path width if DIP switch 4 is ON.

A 16-bit video memory data path is enabled whenever the VGA 1024 board is installed in an AT type (16-bit) expansion slot. Note that a 16-bit video memory data path is only operative for single video card systems. If another video card is installed in the system the video memory data path will be set to 8-bit operation.

WD90C00 Enhanced VGA Controller

The WD90C00 internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller, and the Attribute Controller. The WD90C00 has four major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAMDAC interface.

Since the WD90C00 arbitrates video memory accesses, between the system microprocessor and the CRT Controller contained within the WD90C00, all data passes through the WD90C00 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using standard DRAMs.

The **CRT Controller** section within the WD90C00 maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware from a program of its registers. The WD90C00 CRT Controller also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking for the display monitor and RAMDAC.

The **Sequencer** functions as a timing generator for the AT bus interface, in I/O or memory cycles. It also provides the character clock, and the dot clock for the CRT, Graphics and Attribute Controllers.

The **Graphics Controller** manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using time slots defined by the Sequencer.

The **Attribute Controller** modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, pixel panning, reverse video, and background or foreground video.

Display Memory

The VGA 1024 board provides 512KB of display memory (100ns DRAM) as loaded at manufacture time.

Display memory write operations

When the CPU writes to video memory, the maps are enabled by the decoding of the memory address and, depending on the video mode, the Map Mask register.

Display memory read operations

Two methods are available for video memory reads:

1. When a Read type 0 is selected by the Graphics Mode register, CPU Reads from the video memory return an 8-bit value that is determined by the logical decode of the memory address and the Read Map Select register, if applicable.

2. When a Read type 1 is selected by the Graphics Mode register, an 8-bit value is returned that is the result of the color compare operation, which is controlled by the Color Compare and Color Don't Care registers.

BIOS Subsystem

The BIOS program is provided in two 16KB 200ns PROMs. The same PROMs are used in both 8- and 16-bit operation. A 2K address space from C6000h to C67FFh is mapped out by the address decoder in the WD90C00 due to an address conflict with the IBM PGC board and to maintain compatibility with the IBM design.

A special register located at I/O address 46E8h (2:0) has been implemented with a PAL on the VGA 1024 card in order to control the upper 3 address lines of the BIOS ROM. These lines define eight 4KB pages. The addressing has been modified such that the system address for page 6 always points to

physical address page 7 and the system address for page 7 can point to any of the 8 pages by writing the desired page number to the lowest 3-bits of 46E8h. The default setting for this register is for page 7 to point to page 6.

RAMDAC

The RAM digital-to-analog converter (DAC) integrates the function of a color look-up table with three internal DACs for driving an analog display.

The color look-up table is 256 x 18 bits allowing the display of 256 colors from a palette of 256K possible colors. Each output (Red, Green, or Blue) is driven by a 6-bit DAC. Each register in the look-up table contains 6 bits each for the Red, Blue, or Green DACs.

For normal operation, the PEL address inputs point to one of the 256 internal registers of the color look-up table. Three color DACs then convert the value of the look-up table to an analog value (red, green, and blue). The blanking input can also force all three analog outputs to 0 volts, which is independent of the PEL address inputs.

The 'sync' signals to the monitor are TTL. The analog video signals are 0 to 0.7 volts peak-to-peak.

The maximum number of colors displayed is 16 out of 256K except modes hex 13, 5E, and 5F which can display 256 out of 256K. The maximum number of shades of gray is 16 out of 64, except modes hex 13, 5E, and 5F which can display 64 out of 64 shades of gray.

The video DAC on the VGA 1024 board does not provide TTL signals to drive TTL monitors.

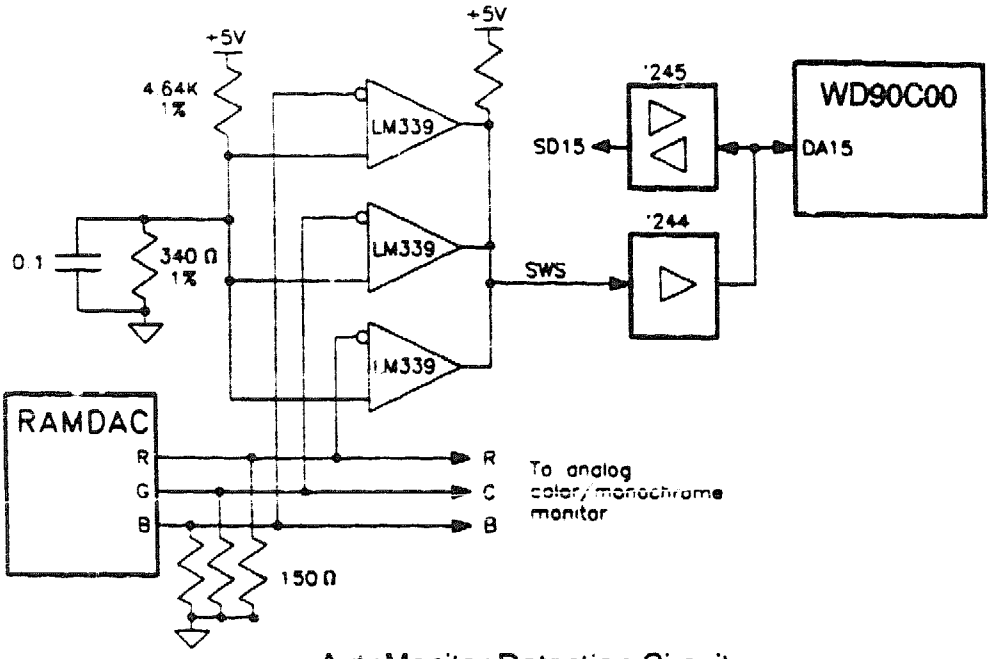
Support logic

Three on-board clock rates can be selected as required for the video dot clock. The on-board clocks are 25.175, 28.322, and 36.000 MHz. The proper video clock is chosen by the BIOS (via Port 3C2, bits 3,2 = 10 binary) when a video mode is set up.

The power-on default configuration of the VGA 1024 card is set with a DIP switch. These settings are latched into registers at power-on self-test time by the WD90C00 Enhanced VGA chip.

AutoMonitor detection

The AutoMonitor detect circuit senses the presence of a color or monochrome monitor in a system and configures the VGA 1024's RAMDAC output appropriately. According to the monitor specifications, at least 0.6 Vp-p must be presented to the input impedance of 75Ω at the R, G, and B inputs of the analog monitor. The comparitor input threshold voltage is designed to be 0.33 Volts. During power-on, the BIOS software will set one at a time, each of the three outputs (R, G, or B) of the RAMDAC for a monochrome display - if a monitor is present on that output, signal SWS goes "Low" and the WD90C00 chip directs a monochrome signal to that output. If all three outputs cause SWS to be "Low", then a color display is generated for the three (R, G, and B) outputs.



AutoMonitor Detection Circuit

Feature connector

The feature connector is a 26-pin edge connector located on the top edge of the board. It can be used by an external source to provide pixel data, sync, and blanking signals to the VGA 1024 board. This connector is functionally compatible with those signals available on the IBM VGA Adapter Card. Video cannot be passed in both directions at the same time.