DECpc™ 400ST Series

Technical Reference Manual

Order Number ER-PCT15-TR-002

Digital Equipment Corporation
Maynard, Massachusetts

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DECpc 400ST Series Technical Reference Manual

Printed in U.S.A.

The FCC wants you to know...

This equipment has been tested and found to comply with the limits for a Class B digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, can cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the computer with respect to the receiver.
- Move the computer away from the receiver.
- Connect the computer into an outlet on a circuit different from that to which the receiver is connected.
- Move the cables connected to the computer to minimize the interference.
- Tighten all screws on cables and the computer housing.
- Install blank panels, originally supplied with the computer, in all unused card slots.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: *How to Identify and Resolve Radio-TV Interference Problems*.

This booklet is available from the U.S. Government Printing Office, Washington, D.C., 20402. Stock No. 004-00398-5.

CAUTION

Any changes or modifications not expressly approved by the grantee of this device can void the user's authority to operate the equipment.

NOTE

If a Class A device is installed within this computer, then the computer is to be considered a Class A computer.

NOTE

To maintain the Class B limit on this computer product, only peripherals (computer input/output devices, terminals, printers) that comply with the Class B limits may be attached. Operation with non-compliant peripherals is likely to result in interference to radio and TV reception.

This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This digital apparatus does not exceed the Class B limits for radio noise emissions set out in the radio interference regulations of the Canadian Department of Communications.

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しかし、本装置をラジオ、テレビジョン受信機に近接してご使用になると、受信障害の原因となることがあります。

取扱説明書に従って正しい取り扱いをして下さい。

This equipment is in the 2nd Class category (information equipment to be used in a residential area or an adjacent area thereto) and conforms to the standards set by the Voluntary Control Council For Interference by Data Processing Equipment and Electronic Office Machines aimed at preventing radio interference in such residential area.

When used near a radio or TV receiver, it may become the cause of radio interference. Read the instructions for correct handling.

This equipment meets or exceeds requirements for safety in the U.S. (UL 1950), Canada (CSA C22.2 No. 950), and Europe (EN 60950/IEC 950) with Nordic requirements.

This equipment meets or exceeds the ergonomic requirements of ZH1/618 and is certified to bear the GS mark by TUV Rheinland of N.A.

This equipment has been tested for radio frequency emissions and has been verified to meet VDE 0871 Class B

Declaration of the Manufacturer or Importer

We hereby certify that the DECpc 400ST Series computer is in compliance with vfg 1046/1984 and is RFI suppressed.

The marketing and sale of the equipment was reported to the German Postal Service.

The right to retest this equipment to verify compliance with the regulation was given to the German Postal Service.

Digital Equipment Corporation

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About This Manual

Purpose

The purpose of this manual is to provide a comprehensive hardware description of the major components in a typical DECpc 400ST Series computer. Descriptions include:

- System architecture
- Buses
- Interfaces
- System specifications
- Basic input/output system (BIOS) specifications
- Configuration options

Audience

This manual is written specifically for a system engineer or hardware designer familiar with the fundamental concepts of microprocessor based computers. The information in this manual assumes a familiarity with the general terminology used in the field of microprocessor and computer design. In addition, this manual contains information for engineers who design computer accessories and for programmers who require hardware and firmware specifications.

Organization of This Manual

The following briefly describes the 11 chapters and six appendices found in this manual:

Chapter 1	System Board Overview — describes the major features of the DECpc 400ST Series system board.
Chapter 2	CPU Module Technology — describes the technology used by Intel486™ microprocessors and associated external caches.
Chapter 3	82358 EISA Bus Controller — describes the EISA bus controller and provides a signal cross reference listing.
Chapter 4	82357 Integrated System Peripheral — describes the integrated system peripheral and lists programming information about its internal registers.
Chapter 5	WD16C552 or TL16C552 Asynchronous Communication Element — provides programming information for the serial and parallel ports implemented by this integrated circuit.
Chapter 6	82077 Diskette Drive Controller — describes the diskette drive controller and lists programming information about its internal registers.
Chapter 7	8742 Keyboard and Mouse Controller — describes the keyboard and mouse controller and lists programming information about its internal registers.
Chapter 8	CLASIC — describes the Common Local I/O ASIC (CLASIC) and lists programming information about its internal registers.

Chapter 9	MECA — describes the MEM Bus EISA Control ASIC (MECA) and provides programming information about its internal registers.
Chapter 10	DPP, EBB, and RCA — describes the data path parity (DPP) and RAS CAS Address (RCA) ASICs. It also describes the 82352 EISA bus buffer (EBB).
Chapter 11	DS1287 Real-Time Clock — describes the real time clock and lists programming information about its internal registers.
Appendix A	Specifications — lists general specifications for the computer, and environmental and dimensional specifications for the system box. It also includes system board jumper information.
Appendix B	BIOS Interrupt Routines — describes the interrupt service routines available in the system's BIOS.
Appendix C	Device Mapping — provides tables that list the computer's memory map, I/O address map, interrupt map, and DMA map.
Appendix D	Configuring the Computer—describes how to use the system configuration utility and its three advance features.
Appendix E	System Board Jumpers—describes the system board jumpers.
Appendix F	Updating the System BIOS—describes how to update the system BIOS and how to recover the system BIOS if it becomes corrupt during an update.
Appendix G	CPU Modules—describe the CPU module features and jumper positions.
Index	Index — includes important terms arranged in alphabetical order for quick reference.

Notational Conventions

Notational conventions used throughout this manual include:

*	In connector pinout listings, the asterisk (*) indicates an active low signal. For example, IOCHCK*
h	An h suffix to a numerical value denotes hexadecimal numbers. For example, 0F8h equals 0F8 (hexadecimal).
Kb	A Kb suffix to a numerical value indicates size in kilobits. For example, 512 Kb. A kilobit equals 1024 bits.
KB	A KB suffix to a numerical value indicates size in kilobytes. For example, 640 KB, 7168 KB, etc. A kilobyte equals 1024 bytes.
Mb	A Mb suffix to a numerical value indicates size in megabits. For example, 4 Mb. A megabit equals 1,048,576 bits.
MB	An MB suffix to a numerical value indicates size in megabytes. For example, 1 MB, 256 MB, etc. A megabyte equals 1,048,576 bytes.
GB	A GB suffix to a numerical value indicates size in gigabytes. For example, 1 GB, 256 GB, etc. A gigabyte equals 1,073,741,824 bytes.

An italicized word or phrase represents a variable or to lend emphasis in textual descriptions. Italic also specifies file names, path names, and directories.

Special Notices

Three kinds of special notices emphasize specific information throughout this manual:

WARNING

Warnings indicate the presence of a hazard that can cause personal injury if the hazard is not avoided.

CAUTION

Cautions indicate the presence of a hazard that might cause damage to hardware or that might corrupt software.

NOTE

Notes provide important or explanatory information.

Related Documentation

The following related documents are available as supplements to the information provided in this manual.

Document	Part Number
DECpc 400ST Series User's Guide (Multilingual)	ER-PCT15-UM
DECpc 400ST Series User's Guide (English)	ER-PCT15-UA
DECpc 400ST Series Installation Guide (Multilingual)	ER-PCT15-IM
DECpc 400ST Series Installation Guide (English)	ER-PCT15-IA
DECpc 400ST Series Service Guide	ER-PCT15-SV
DECpc 400ST Series 25 MHz, 33 MHz, 50 MHz CPU Upgrade Kit Installation Guide (Multilingual)	ER-T16AA-IG
DECpc 400ST Series Intel486 DX2 50 MHz and 66 MHz CPU Upgrade Kit Installation Guide (Multilingual)	ER-T31AA-IM
DECpc 400ST Series Intel486 DX2 50 MHz and 66 MHz CPU Upgrade Kit Installation Guide (English)	ER-T31AA-IA

1

System Board Overview

Introduction

This chapter provides an overview of the DECpc 400ST Series system board (see Figure 1-1). The system board supports:

- High performance CPU modules that use Intel486 microprocessors (including external caches)
- Extended Industry Standard Architecture (EISA)
- Intel 82358 EISA Bus Controller (EBC)
- Intel 82357 Integrated System Peripheral (ISP)
- Intel CLASIC, MECA, DPP, and RCA Application Specific Integrated Circuits (ASICs)
- Intel 82352 EISA Bus Buffer
- Onboard 82077 diskette drive controller
- Integrated Disk Electronics (IDE) support
- Up to 64 MB (using 16 MB SIMMs) of onboard DRAM
- Up to 128 MB (using 16 MB SIMMs) of additional DRAM using an optional memory module
- Supports up to 384 MB of DRAM (using 32 MB SIMMs, when available)

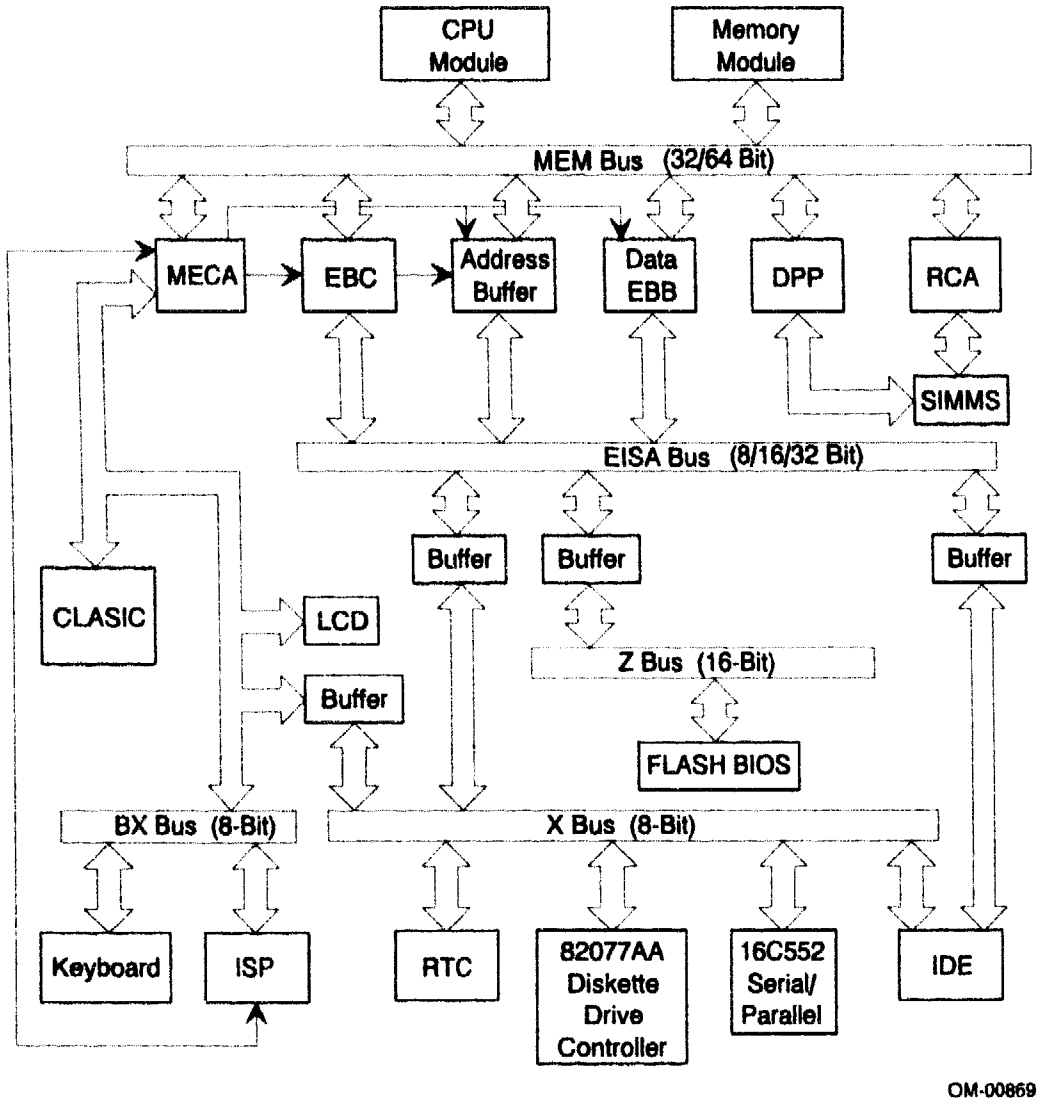


Figure 1-1. DECpc 400ST Series System Board Block Diagram

In addition, the system board supports:

- Six EISA bus master slots
- Two 9-pin serial ports
- One 25-pin parallel port
- 6-pin (mini-DIN) keyboard and 6-pin (mini-DIN) mouse connectors
- One 254 Watt power supply
- One CPU module connector
- One memory module connector

The remainder of this chapter provides descriptions of the system board, CPU module, and memory module. It also includes a brief memory description (including memory expansion board) and a brief description of the system board busses.

DECpc 400ST System Board Features

The performance features of the system board include:

- Six Extended Industry Standard Architecture (EISA) master slots
- 82357 Integrated System Peripheral (ISP)
- 82358 EISA Bus Controller (EBC)
- Two programmable ASICs (CLASIC and MECA)
- Two non-programmable ASICs (DPP and RCA)
- IDE interface that supports two hard disk drives
- Diskette drive controller that supports two diskette drives
- Two RS-232C 9-pin serial communication ports
- One Centronics™ compatible 25-pin parallel port
- Keyboard and mouse controller
- One PS/2-style keyboard port
- One PS/2-style mouse port
- One piezo speaker
- Non-volatile storage in FLASH memory
- Phoenix Technologies™ BIOS, based in FLASH memory
- CPU module connector
- Memory module connector
- Up to 64 MB of DRAM using 16 MB SIMMs
- EISA System Configuration Utility (SCU)

EISA Slots

The six EISA bus master slots provide for system expansion and performance enhancement. The EISA bus is an extension to the Industry Standard Architecture (ISA) bus. It extends the capability of the ISA bus while maintaining compatibility so ISA expansion boards also work. In addition, a bus snooping algorithm optimizes for maximum EISA bus performance, even when write-back cache mode CPU modules are in use. EISA bus clock speed is 8.33 MHz. The EISA bus provides:

- 32-bit memory addressing
- Type A transfers at 5.33 MB per second
- Type B transfers at 8.00 MB per second
- Burst transfers at 33 MB per second
- 8-bit, 16-bit, or 32-bit data transfers
- Automatic translation of bus cycles between EISA and ISA masters and slaves
- Interrupt sharing

82357 Integrated System Peripheral

The 82357 Integrated System Peripheral (ISP) integrates key EISA I/O commands by providing:

- 8237A-compatible Direct Memory Access (DMA) support
- 8254-compatible Programmable Interrupt Timers (PIT) support
- 8259-compatible Programmable Interrupt Controllers (PIC) support

82358DT EISA Bus Controller

The 82358DT EISA Bus Controller (EBC) monitors cycles initiated on either the EISA or MEMbus and provides control for the data buffers between the two buses.

Programmable ASIC Devices

Four programmable application specific integrated circuit (ASIC) devices improve reliability and reduce system board costs. The MEM bus EISA control (MECA) ASIC controls optional EISA expansion boards. The common local I/O (CLASIC) ASIC controls local system board I/O. The RAS/CAS address (RCA) ASIC and data parity path (DPP) ASIC implement DRAM control logic.

IDE Hard Drive Interface

The IDE hard drive interface interfaces IDE hard disk drives with the Intel486 microprocessor. The interface supports up to two hard disk drives and can be disabled using the System Configuration Utility (SCU). When disabled, the IDE interface interrupt (IRQ 14) is available for other EISA expansion boards.

Diskette Drive Controller

A single 82077 diskette drive controller supports both double and high density media in 3 1/2-inch and 5 1/4-inch diskette drives. The diskette drive controller can be disabled with the System Configuration Utility (SCU). When disabled, the diskette controller interrupt (IRQ 6) is available for other EISA expansion boards. The diskette controller also supports fast floppy streaming tape; however, the system BIOS does not support this feature.

Asynchronous Communications Element (ACE)

A single Western Digital™ 16C552 or Texas Instruments™ TL16C552 Asynchronous Communications Element (ACE) provides the interface for two serial ports and one parallel port.

Serial Ports

Each serial port uses a 9-pin D-sub connector and the ports can be configured as logical COM1, COM2, COM3 or COM4. The System Configuration Utility (SCU) enables and disables the serial ports. Each serial port can be separately disabled to allow any EISA bus resource access to its interrupt. The ports connect to the EISA bus with a 16-byte FIFO interface. This interface supports 16-bit software and provides baud rates of 300, 1200, 2400, 9600, 19200, 38400, and 56000 bytes per second. The system BIOS supports baud rates up to 9600 bytes per second. The higher baud rates can be used if the application driver does not use the system BIOS for serial port control. Tranzorbs protect the serial ports from surges caused by external electrical transients. RS-232C cable lengths should not exceed 50 feet (15.24 meters).

Parallel Port

The parallel port uses a 25-pin DB25 connector. The System Configuration Utility (SCU) enables, disables, or configures the parallel port. It also configures the parallel port as LPT1 or LPT2. It also can be set to either standard (Centronics compatible) or bidirectional (PS/2 compatible) using the BIOS setup utility. Disabling the parallel port allows any EISA bus resource access to its interrupts.

Keyboard and Mouse Controller

A single 8742 Universal Peripheral Interface Microcontroller (also known as the keyboard and mouse controller) supports PS/2 compatible keyboards and the PS/2 style mouse. This microcontroller supports the following HOT key sequences:

Ctrl-Alt-Del

This key sequence does a software reset of the system by jumping to the beginning of the BIOS code and running the power-on self test (POST) operation (excluding the memory tests).

Ctrl-Alt-1

Ctrl-Alt-2

These two key sequences switch between slow and fast modes. **Ctrl-Alt-1** selects slow mode that emulates an 8 MHz 80286 microprocessor by placing the CPU in hold for a period of time and disabling all caching circuitry. **Ctrl-Alt-2** selects fast mode that enables full-speed operation of the Intel486 microprocessor and enables all cache memory logic at its full speed. The key sequences are valid only on the numeric keypad.

PS/2 Keyboard Port and PS/2 Mouse Port

A PS/2 keyboard port and a PS/2 mouse port use a dual stacked 6-pin mini DIN connector. An Intel 8742 Universal Peripheral Interface Microcontroller that incorporates Phoenix Technologies keyboard controller firmware controls these ports. The PS/2 mouse port interrupt can be disabled using the SCU, allowing any EISA bus resource to use interrupt (IRQ 12).

Speaker

The speaker provides audible tones under software control.

System BIOS

System BIOS is from Phoenix Technologies. It is stored in two 32-pin 8-bit FLASH memories and can occupy up to 192 KB.

Non-Volatile Memory

Non-volatile memory consists of 8 KB and located in the user area of FLASH memory. In addition, 50 bytes of CMOS are available in the real-time clock.

CMOS Battery Backup/Real-Time Clock

The system board uses a Dallas Semiconductor™ DS1287 CMOS Real-time Clock. The DS1287 contains 64 bytes of general purpose RAM that stores system BIOS configuration information, clock registers, and general purpose control registers. The DS1287 provides an accuracy of ±1 minute per month. An integral lithium battery powers the clock for up to 10 years in the absence of power.

Direct Memory Access (DMA)

The system board provides seven ISA-compatible DMA channels through the computer's EISA bus implementation. An EISA DMA controller also supports demand and block mode DMA transfers. These modes enable multiple continuous transfers and high speed bus cycles and can achieve data transfer rates up to 33 MB per second. You can program each DMA channel for 8, 16 or 32-bit DMA device size. Also, all channels support ISA compatible, Type A (5.33 MB per second), Type B (8 MB per second), or Burst DMA (33 MB per second) timing modes. The DMA memory mapper supports the full 4 GB memory range using up to a 16 MHz clock rate. When enabled, the onboard diskette drive controller and IDE hard disk interface use DMA channels 2 and 3, respectively.

System Memory

System memory, located on the system board, consists of the RAS/CAS Address (RCA) ASIC and four SIMM sockets that support up to 64 MB of (70ns or 80ns) DRAM using 16 MB SIMMs. The RCA ASIC provides DRAM control functions RAS, CAS, WE, and address multiplexing addresses, and generates MEM bus response signals. Table 1-1 shows the system memory allocation.

The DECpc 400ST Series computers do not support use of the 000E 0000 to 000E FFFF address ranges for DEC EtherWORKS (DEPCA) controllers. DEC EtherWORKS controllers should be configured for the 000D 0000 to 000D FFFF address range to run in the 64 KB mode or for 00C 8000 to 00C FFFF to run in the 32 KB mode.

Table 1-1. System Memory Allocation

Address Range (In hex)	Function	Size	Shadow	Cache
0010 0000 to 01FF FFFF	Extended memory(1)	192 MB	No	Yes
000F 0000 to 000F FFFF	System BIOS	64 KB	Yes	Yes
000E 8000 to 000E FFFF	EISA configuration information(2)	32 KB	No	No
000E 0000 to 000E 7FFF	Adapter BIOS extension	32 KB	Yes(3)	Yes
000D 0000 to 000D FFFF	Adapter BIOS extension	64 KB	No	No
000C 8000 to 000C FFFF	Adapter BIOS extension	32 KB	Yes(3)	Yes
000C 0000 to 000C 7FFF	Video BIOS or adapter BIOS extension	32 KB	Yes(3)	Yes
000A 0000 to 000B FFFF	Video RAM	128 KB	No	No
0000 0000 to 0009 FFFF	Base memory	640 KB	No	Yes

(1) The SCU provides an option for creating a 1 MB open space between 15 MB and 16 MB to which you can map expansion board BIOS
(2) Not available for mapping expansion board memory or BIOS
(3) User configurable

Buses

The system board supports five buses (see Figure 1-1):

- BX
- EISA
- MEM
- X
- Z

BX Bus

The BX bus is an 8-bit bus that provides an interface among the keyboard, 82357 ISP, CLASIC , MECA ASIC, and LCD.

EISA Bus

The EISA bus provides computer feature expansion by allowing installation of EISA or ISA expansion boards. The EISA slot connectors implement the Extended Industry Standard Architecture and maintain compatibility with the earlier Industry Standard Architecture (ISA).

MEM Bus

The MEM bus is an Intel proprietary bus that connects the CPU module and optional memory module with the EISA bus.

X Bus

The X bus is an 8-bit bus that provides the interface between DMA and non-memory non-DMA devices.

Z Bus

The Z bus is a 16-bit bus that provides the interface between FLASH memory and the EISA bus.

System Configuration Utility

The SCU is on language-specific diskettes and sets up and configures the computer using menu driven utilities. The installed hardware and the required level of computer security determines which part of the SCU to access. Access these computer functions with the SCU:

- Select a specific keyboard type
- Copy the System Configuration Diskette
- Learn about configuring the computer
- Set the computer date and time
- Configure the computer
- Maintain the System Configuration Diskette
- Access the password utility

CPU Module Features

The CPU module supports the Intel486 microprocessor and external cache logic. Communication between the CPU module and the system board is by a proprietary bus called the MEM bus. The CPU modules have identical functionality. The only difference is CPU clock speed and cache technique (write-through or write-back) type.

Memory Module Features

The memory module expands system memory and plugs into a proprietary slot (MEM bus) next to the CPU module, where it directly interfaces with the asynchronous CPU bus. This enables the CPU module and memory control logic to synchronize with the memory module, allowing the bus to run at the highest possible transfer speed.

Eight 36-bit SIMM sockets on the memory module provide up to 128 MB of additional system memory (using 16 MB SIMM modules). The SIMMs have a minimum access time of 80ns. The SIMM DRAMs are surface mounted on a SIMM connector.

There are four banks of two SIMMs each on a memory module. The interleaved memory scheme requires memory upgrades by bank. SIMMs installed in each bank must be of the same size, type, and speed.

2

CPU Module Technology

Introduction

This chapter briefly describes the technology used by DECpc 400ST Series CPU modules. For detailed information about the CPU modules available when this manual was published refer to Appendix G. For current CPU module information, contact Digital Equipment Corporation. A CPU module provides the major system processing resources and includes the following major functional blocks:

- Intel486 microprocessor
- External cache

Intel486 Microprocessor

The Intel486 microprocessor is a high-performance 32-bit microprocessor with an on-chip memory management unit, numeric coprocessor unit (except Intel486SX), and cache memory unit. The Intel486 microprocessor supports multi-user and multi-tasking operating systems, memory management, virtual memory, and task or memory isolation. The following paragraphs describe the Intel486 microprocessor's basic architecture and its two modes of operation.

Basic Architecture

The Intel486 microprocessor has four major sections:

- Central processing unit
- Memory management unit
- Numeric coprocessor unit
- Cache memory unit

Central Processing Unit

The Central Processing Unit (CPU) consists of the execution unit and instruction unit. The execution unit contains the eight 32-bit general purpose registers used for both address calculation and data operations. The execution unit also contains a 64-bit barrel shifter that speeds up shift, rotate, multiply, and divide operations. The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

Memory Management Unit

The Memory Management Unit (MMU) consists of a segmentation unit and a paging unit. Segmentation manages the logical address space by providing an extra addressing component that allows the relocation and sharing of code and data. The paging unit operates beneath, and is transparent to, the segmentation process to allow physical address space management. Paging is optional and is under system software control.

Numeric Coprocessor Unit

The on-chip numeric coprocessor unit conforms to the ANSI/IEEE standard 754-1985 specification, operates in parallel with the arithmetic and logic unit, and provides arithmetic instructions for a variety of numeric data types. The numeric coprocessor unit executes built-in tangent, sine, cosine, and log functions and is compatible with software written for 287, 387DX, and 487SX numeric coprocessors.

Cache Memory Unit

The 8 KB on-chip cache memory unit is four-way set-associative and follows a write-through policy. It can designate individual pages as cacheable or non-cacheable by hardware or software.

Modes of Operation

The Intel486 microprocessor has two modes of operation: real address mode (real mode) and protected mode. In real mode, the Intel486 microprocessor operates as a fast 8086 and sets up the CPU for protected mode operation. Protected mode provides access to the sophisticated memory management paging and privilege capabilities of the CPU.

In protected mode, software can execute a task switch and enter into a virtual 8086 mode. In virtual mode, 8086 semantics are used and the application program or operating system executes as if running on an 8086 CPU.

External Caches

An external cache enhances the capabilities of the Intel486 microprocessor internal cache by providing zero wait-states for DRAM read cycles each time an external cache hit occurs. It physically connects to the Intel486 microprocessor address bus and acts as a bus watcher.

There are two types of external caches: write-through and write-back. Both cache types use snooping (bus watching) and non-cacheable memory designation to ensure cache consistency. Cache consistency cycles occur when one microprocessor updates DRAM but the cache data, maintained by another processor, is not updated. In snooping, the cache controller monitors the bus lines and invalidates or writes-back any shared locations that are accessed by another microprocessor. Non-cacheable memory designation prohibits copying the designated memory locations to the cache.

Write-Through Cache

In a write-through cache, the microprocessor writes data into the DRAM immediately after or at the same time data is written into the cache. This method ensures that data in DRAM is always valid. The trade-off is the high memory bus traffic, especially in systems with multiple bus masters because every write cycle requires a memory bus cycle.

Write-Back Cache

In a write-back cache, the microprocessor writes data into the cache and sets a tag bit. The tag bit indicates that a word has been written into the cache but not to DRAM. The word gets written into DRAM only if the microprocessor must remap the cache location, or if another bus master requests the word which is current only in the cache. When the cache data is written to DRAM, the tag bit is cleared. This method reduces memory bus traffic because the number of times main memory must be updated with altered cache locations is usually lower than the number of write accesses.

Base Architecture

The external cache has a 16-byte line size and is two-way set-associative. The write-through external cache contains a 82485DX cache controller and nine SRAM's. The write-back external cache contains a 82495DX cache controller and nine SRAM's. Figure 2-1 shows a block diagram of both cache types. The following paragraphs contain detailed descriptions of the cache controllers and SRAMs.

82485DX Cache Controller

The 82485DX cache controller contains two sections. Each section has 2 KB tags with 17 bits per tag so it can store the full 4 GB real address space of the Intel486 microprocessor. These tags also reference two valid bits and a write-protect bit and are forced to reference two consecutive 16-byte lines (two sectors per tag).

The control units of the 82485DX are responsible for controlling the data SRAMs, controlling the tag RAM structure, and interfacing to the Intel486 microprocessor. Because the units are independent, the 82485DX is capable of updating its tag RAM while data is burst into SRAM or it can become invalid during a line fill to a different address.

The 82485DX uses the Least Recently Used (LRU) algorithm to determine which tag to invalidated on cache misses. A single LRU bit per tag points to the tag to replace.

82495DX Cache Controller

The 82495DX cache controller is an enhanced version of the 82395 cache controller. The 82495DX also has a 16-byte line size; however, its sections have 4 KB tags and 15 bits per tag. The tags do not reference two validity bits and a write-protect bit. In addition, the 82495DX uses most-recent-used (MRU) algorithm to predict which way the next cycle occurs.

SRAMs

The external cache SRAMs operate at a speed of 24 ns and are capable of zero wait-state reads and writes, single clock bursting, and have minimized capacitive loading on the Intel486 microprocessor clock and data lines.

The SRAMs for the 50 MHz CPU module (using the 82495DX cache controller) run at 20 ns.

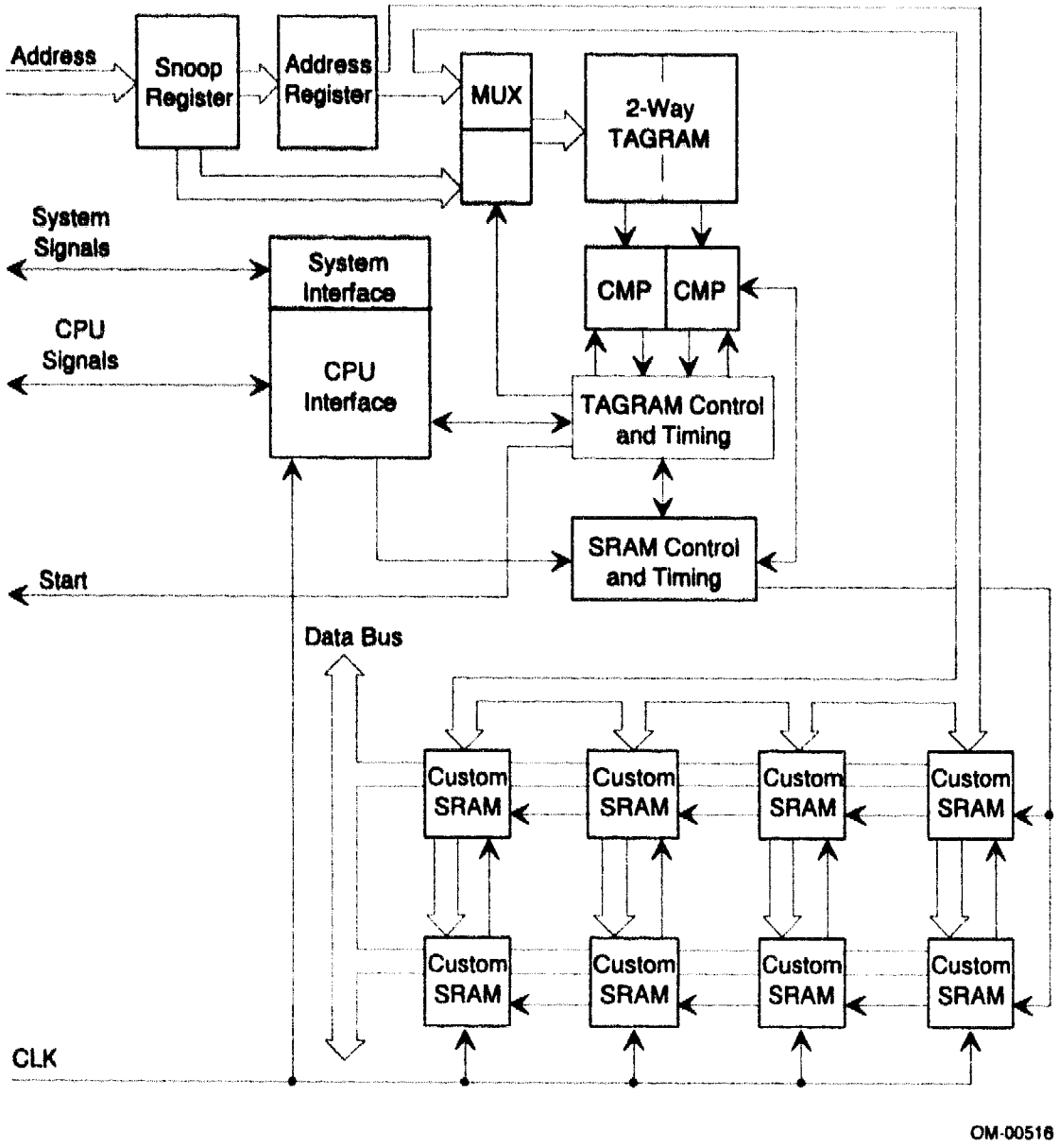


Figure 2-1. External Cache Functional Block Diagram

3

82358 EISA Bus Controller

Introduction

The DECpc 400ST Series system board uses an 82358 EISA Bus Controller (EBC) to control data transfers between the MEM bus and the EISA bus. The EBC generates data conversion and alignment control signals required by devices with different data widths. It also provides control logic for the 82352 EISA Bus Buffer (EBB). The EBC contains the following functional blocks (see Figure 3-1):

- CPU bus interface
- EISA bus interface
- ISA bus interface
- ISP interface
- Address buffer control
- Data buffer control
- Cache support
- Reset control
- I/O recovery
- Slot support
- Clock generation

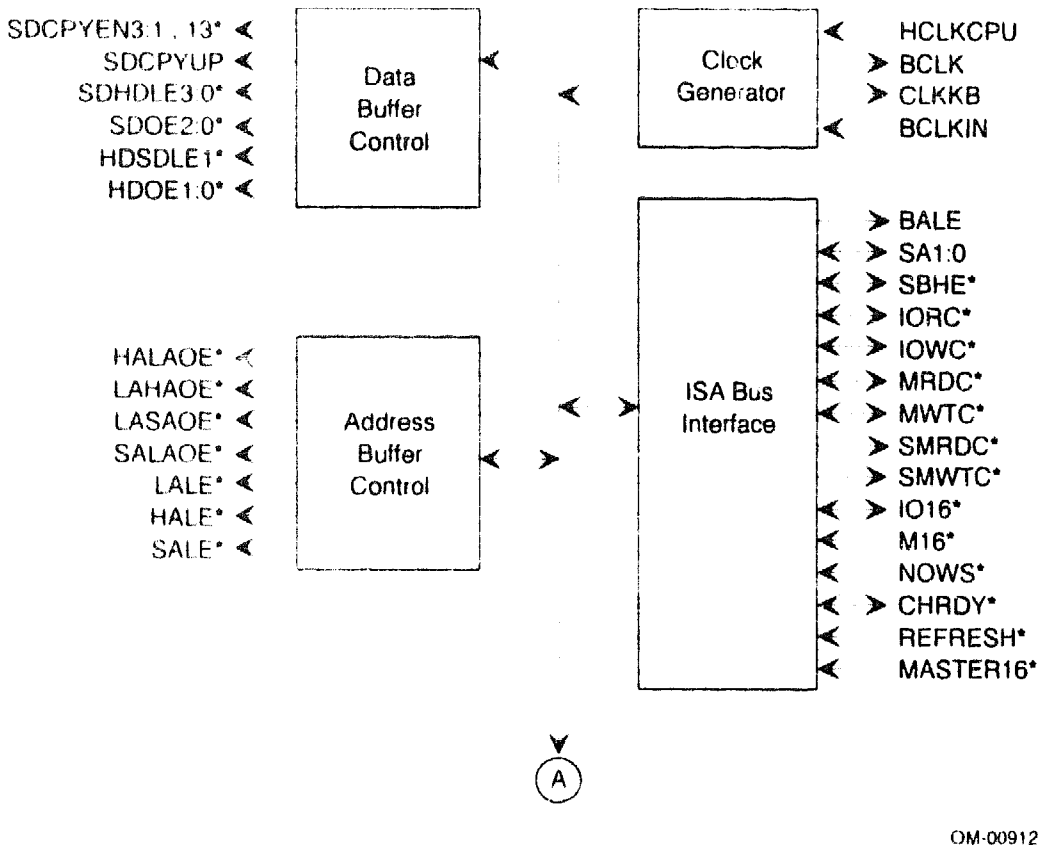


Figure 3-1. 82358 EISA Bus Controller Block Diagram (Sheet 1 of 2)

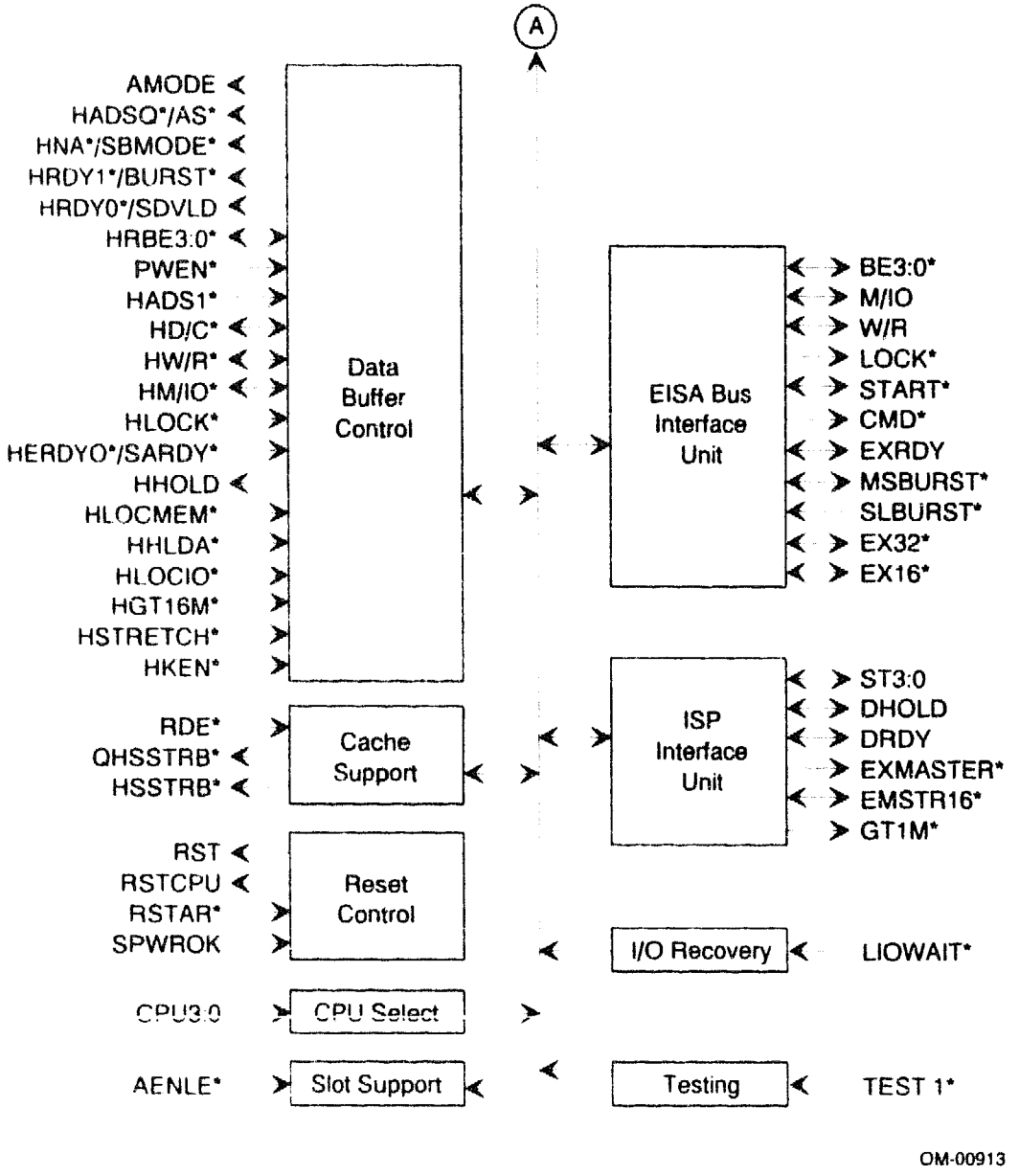


Figure 3-1. 82358 EISA Bus Controller Block Diagram (Sheet 2 of 2)

Host Bus Interface

The host bus interface monitors MEM bus cycles when the host CPU is the bus master on the MEM bus. If the host CPU does not have control of the bus, the host bus interface instructs the EISA or ISA bus interface to run a bus cycle. After the EISA or ISA bus interface completes the bus cycle, the host bus interface terminates the cycle on the MEM bus.

EISA and ISA Bus Interfaces

The EISA and ISA bus interfaces are state machines that interface with the EISA and ISA buses. Both interfaces operate at the EISA bus clock (BCLK) frequency of 8.33 MHz.

The EISA bus interface executes bus cycles for EISA devices, the CPU module, or the 82357 Integrated System Peripheral (ISP) when either controls the EISA bus. Similarly, the ISA bus interface executes bus cycles for ISA devices, the CPU module, or the ISP when either subsystem controls the ISA bus.

The EISA and ISA bus interfaces monitor cycles initiated by EISA or ISA bus masters and monitors their corresponding buses to detect a slave response. When a slave response is detected, the correct cycle is initiated to the responding slave's bus (EISA or ISA).

The EISA and ISA bus interface accepts cycles from the CPU bus interface and executes them on the EISA/ISA bus. It also performs multiple cycles (assembly/disassembly) for each CPU cycle. After performing multiple cycles, the EISA and ISA bus interface unit instructs the CPU bus interface unit to terminate the cycle on the CPU bus. In addition, the EISA and ISA bus interface instructs the CPU bus interface to notify the CPU to change the address for the next cycle.

Integrated System Peripheral Interface

The Integrated System Peripheral (ISP) interface accepts requests from the ISP for DMA or refresh cycles, and then directs the EISA or ISA bus interface to execute the appropriate cycle

- Compatible
- Type A
- Type B
- Type C (burst)

If a memory slave width does not match the I/O slave width, the EISA and ISA bus interface performs data byte assembly or disassembly (as required) through multiple EISA/ISA cycles.

Address Buffer Control

The address buffer control controls the external bidirectional address buffers between the CPU and the EISA/ISA bus. It also provides the latching clocks and output enables for the address buffers.

Data Buffer Control

The data buffer control provides the latching clock and output enables that control the data buffers between the CPU and the EISA/ISA bus. The data buffer control interfaces with CPU, EISA, and ISA interfaces to provide buffer control during assembly/disassembly of data.

Cache Support

The cache support logic signals the cache controller when to monitor the system bus using the EADS* signal. EADS* is a synchronized strobe indicating a valid address during EISA/ISA device or CPU-to-memory write cycles.

Reset Control

Reset control logic generates the following:

- A reset for the CPU (RSTCPU)
- A reset for the ISP (RST)

Three conditions cause a CPU reset (RSTCPU): power-on, shut-down from a CPU bus master, and asserting SWRST*.

The ISP reset is generated at power-on, after BCLK becomes stable.

I/O Recovery

The I/O recovery logic forces a delay between back-to-back 8-bit and 16-bit ISA I/O cycles originating on the MEM bus. No delay is inserted for EISA, ISA, or DMA bus master cycles, EISA cycles originating on the MEM bus, or back-to-back I/O sub-cycles generated as a result of byte assembly or disassembly.

Slot Support

The slot support logic generates address latch enable (AENLE*) when the LA address becomes valid.

Clock Generation

The clock generation logic generates two clocks:

- HCLKCPU
- BCLK

HCLKCPU is a divide-by-one internal clock operating at the same frequency as CLK1CPU.

Dividing HCLKCPU by four generates BCLK, the 8.33 MHz EISA clock. The clock generating can also stretch the high or low time of BCLK for synchronization purposes.

Pinouts

Table 3-1 lists the differences between the standard EBC signal pinouts and the DECpc 400ST signal pinouts.

Table 3-1. EBC Signal Cross Reference

Pin No.	EBC Signal Name	DECpc 400ST Signal Name
2	TEST1*	EBCP2
3	LIOWAIT*	LIOWAIT*
4	SDCPYEN01*	CPYEN01*
5	SDCPYEN02*	CPYEN02*
6	SDCPYEN03*	CPYEN03*
7	SDCPYEN13*	CPYEN13*
8	SDCPYUP	SDCPYUP
10	SDHDLE3*	SDHDLE3*
11	SDHDLE2*	SDHDLE2*
12	SDHDLE1*	SDHDLE1*
13	SDHDLE0*	SDHDLE0*
14	SDOE2*	SDOE2*
16	SDOE1*	SDOE1*
17	SDOE0*	SDOE0*
18	HDSDLE1*	Not used
19	Reserved	Not used
20	HDOE1*	HDOE1*
22	HDOE0*	HDOE0*
23	HALAOE*	HALAOE*
24	HALE*	Not used
25	LASAOE*	LASAOE*

Table 3-1. EBC Signal Cross Reference *(continued)*

Pin No.	EBC Signal Name	DECpc 400ST Signal Name
26	LAHAOE*	LAHAOE*
28	LALE*	Not used
29	SALAOE*	SALAOE*
30	SALE*	SALE*
31	START*	START*
32	NOWS*	NOWS*
33	REFRESH*	REFRESH*
36	LOCK*	EXLOCK*
37	SMWTC*	SMWTC*
41	CMD*	CMD*
42	SBHE*	SBHE*
43	SA0	SA0
44	SA1	SA1
47	MWTC*	MWTC*
48	MRDC*	MRDC*
50	IOWC*	IOWC*
52	IORC*	IORC*
53	EXRDY	EXRDY
55	EX16*	EX16*
56	EX32*	EX32*
57	SLBURST*	SLBURST*
58	MSBURST*	MSBURST*
60	BE0*	BE0*

Table 3-1. EBC Signal Cross Reference *(continued)*

Pin No.	EBC Signal Name	DECpc 400ST Signal Name
61	BE1*	BE1*
62	BE2*	BE2*
63	BE3*	BE3*
64	W/R*	WR
65	CHRDY	CHRDY
66	MASTER16*	MASTER16*
69	EMSTR16*	EMSTR16*
70	EXMASTER*	EXMASTER*
71	GT1M*	GT1M*
72	HADS0*	EBCP72
73	M/IO*	MIO
75	CLKB	Not used
76	AENLE*	AENLE*
77	DRDY	DRDY
79	ST0	ST0
80	ST1	ST1
81	ST2	ST2
82	ST3	ST3
83	BCLKIN	BCLK6
86	BCLK	OBBCLK
89	HCLKCPU	OSC33EBC
90	RST	RST
91	RST385	Not used
93	RSTCPU	EBCP93
94	CPU0	EBCP94

Table 3-1. EBC Signal Cross Reference *(continued)*

Pin No.	EBC Signal Name	DECpc 400ST Signal Name
95	CPU1	EBCP95
96	CPU2	EBCP96
97	CPU3	EBCP97
98	RSTAR*	SWRST*
101	SPWROK	SYSRES*
102	HLOCMEM*	HLOCMEM*
103	HLOCIO*	EBCP103
104	HSTRETCH*	HSTRETSH*
105	DHOLD	DHOLD
106	HNA*/SBMODE*	EBC106
108	HD/C*	HDC
109	HM/IO*	HWRD
110	HW/R*	HMRD*
111	RDE*	EBCP111
112	HRDYO*	Not used
114	HERDYO*	HERDYO*
115	HHOLD	HHOLD
116	HSSTRB*	Not used
118	HBE3*	HBE3*
120	HBE2*	HBE2*
121	HBE1*	HBE1*
122	HBE0*	HBE0*
123	PWEN	EBCP123

Table 3-1. EBC Signal Cross Reference *(continued)*

Pin No.	EBC Signal Name	DECpc 400ST Signal Name
124	AMODE	EBCP124
126	HKEN*	HKEN*
127	HRDYI*	HRDYI*
128	HADS1*	HADS*
129	HHLDA	SDHLDA
130	HLOCK	BSHLOCK*
131	HGT16M*	GT16M*

4

Integrated System Peripheral

Introduction

The DECpc 400ST Series system board uses an 82357 Integrated System Peripheral (ISP) that provides a high performance seven-channel programmable DMA controller, a 16 level programmable interrupt controller, refresh address generation and control, and five counter/timers. The ISP also supplies non-maskable interrupts (NMIs) for certain error conditions. It contains the following functional blocks (see Figure 4-1):

- Bus interface
- DMA controller and refresh generator
- System arbiter
- Timer/counters
- NMI logic
- Clock
- Interrupt controller

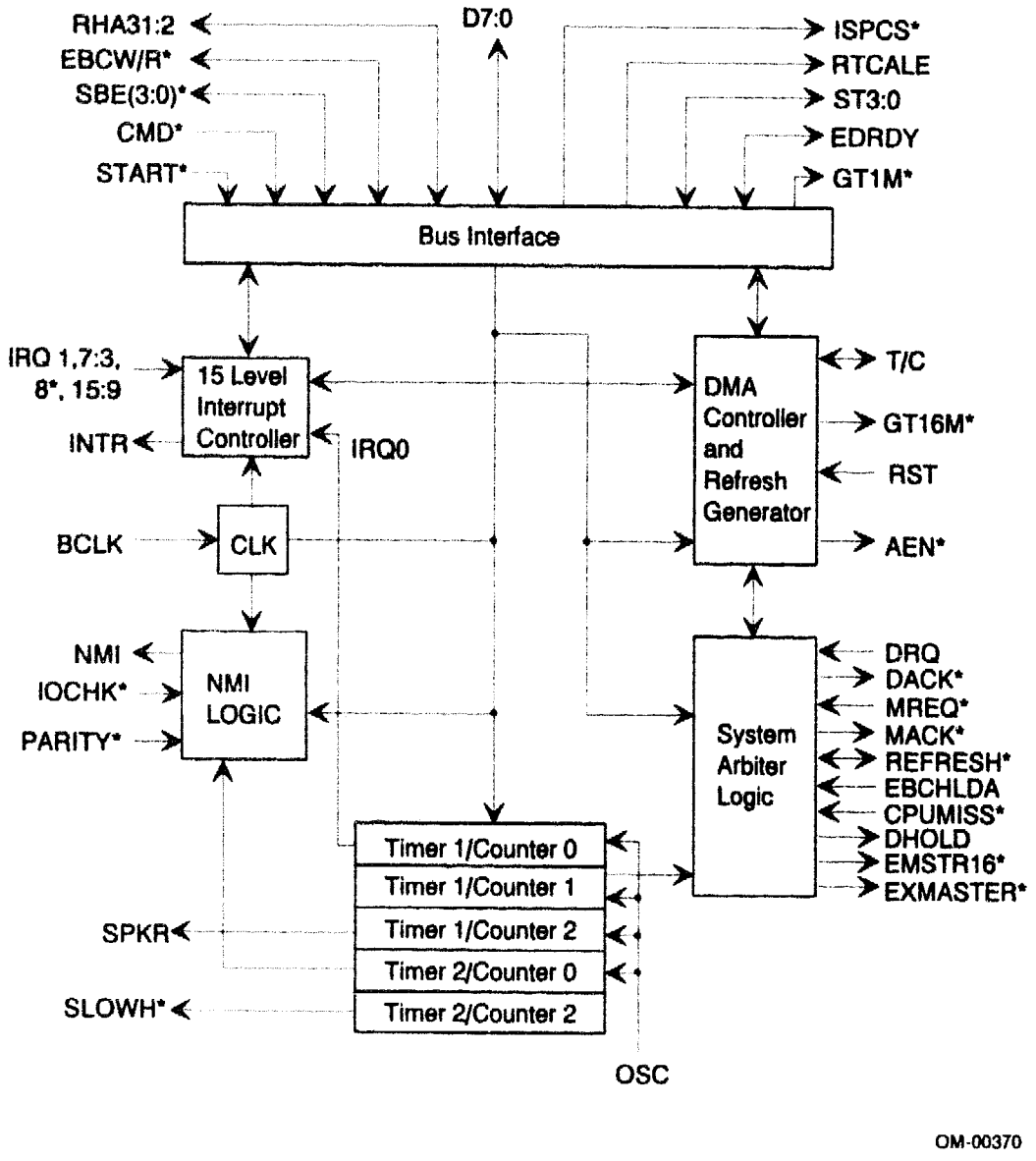


Figure 4-1. 82357 Integrated System Peripheral Block Diagram

Bus Interface

The bus interface logic interfaces the ISP with the EISA bus and MEM bus.

DMA Controller and Refresh Generator

The ISP DMA controller has seven DMA channels that are accessed and addressed as though they were contained in two separate 82C37 DMA controllers. DMA controller one contains channels zero through three. DMA controller two contains channels four through seven. Channel four cascades the two controllers together.

The refresh generator uses the combined functions of the interval timer/counters, the system arbiter, and DMA controller two. Timer/counter one generates internal refresh requests. The arbiter detects refresh requests from timer/counter 1 and external devices, and determines which refresh request should be executed.

Table 4-1 lists the address map for the DMA controller registers. Table 4-2 lists the address map for the DMA channel registers.

Table 4-1. DMA Controller Register Address Map

Channels 3-0 Address (in hex)	Channels 7-4 Address (in hex)	R/W	Function
08	0D0	R	Status register
08	0D0	W	Command register
09	0D2	W	Request register
0A	0D4	W	Write single mask bit register
0B	0D6	W	Mode register
0C	0D8	W	Clear byte pointer flip-flop
0D	0DA	W	Master clear command
0E	0DC	W	Clear mask register
0F	0DE	R/W	Write all mask register
040A	—	R	Channel interrupt status register
040A	04D4	W	Set chaining mode register
040B	04D6	W	Extended mode register
040C	—	R	Chain buffer expiration control register
04D4	—	R	Port address register

Table 4-2. DMA Channel Registers Address Map

Address (in hex)	R/W	Register	DMA Channel
0000	R	Current address	0
	W	Base address	
0001	R	Current word count	0
	W	Base word count	
0002	R	Current word count	1
	W	Base word count	
0003	R	Current word count	1
	W	Base word count	
0004	R	Current word count	2
	W	Base word count	
0005	R	Current word count	2
	W	Base word count	
0006	R	Current word count	3
	W	Base word count	
0007	R	Current word count	3
	W	Base word count	
008F	R/W	Page low refresh	—
048F	R/W	Page high refresh	—
0081	R	Current page low	2
	W	Base page low	
0082	R	Current page low	3
	W	Base page low	
0083	R	Current page low	1
	W	Base page low	

Table 4-2. DMA Channel Registers Address Map *(continued)*

Address (In hex)	R/W	Register	DMA Channel
0087	R	Current page low	0
	W	Base page low	
0089	R	Current page low	6
	W	Base page low	
008A	R	Current page low	7
	W	Base page low	
008B	R	Current page low	5
	W	Base page low	
00C4	R	Current word count	5
	W	Base word count	
00C6	R	Current word count	5
	W	Base word count	
00C8	R	Current word count	6
	W	Base word count	
00CA	R	Current word count	6
	W	Base word count	
00CC	R	Current word count	7
	W	Base word count	
00CE	R	Current word count	7
	W	Base word count	
0401	R	Current word count high	0
	W	Base word count high	
0403	R	Current word count high	1
	W	Base word count high	
0405	R	Current word count high	2
	W	Base word count high	
0407	R	Current word count high	3
	W	Base word count high	

Table 4-2. DMA Channel Registers Address Map *(continued)*

Address (in hex)	R/W	Register	DMA Channel
0481	R	Current page high	2
	W	Base page high	
0482	R	Current page high	3
	W	Base page high	
0483	R	Current page high	1
	W	Base page high	
0487	R	Current page high	0
	W	Base page high	
0489	R	Current page high	6
	W	Base page high	
048A	R	Current page high	7
	W	Base page high	
048B	R	Current page high	5
	W	Base page high	
04C6	R	Current word count high	5
	W	Base word count high	
04CA	R	Current word count high	6
	W	Base word count high	
04CE	R	Current word count high	7
	W	Base word count high	

System Arbiter

The system arbiter monitors system bus requests and establishes bus ownership priority using a programmable rotating scheme. This scheme depends on a programmable order and is independent of the request order allowing bus access by all masters. Programming is via the DMA controller.

Timer/Counters

The timer/counters provide all system timing functions and are accessed and addressed as though they were contained in two separate 82C54 Programmable Interval Counters (timer 1 and timer 2). Timer 1 contains three counters. Timer 2 contains two counters (counter 1 is not implemented). Table 4-3 lists the address map for the timer/counters.

Table 4-3. Timer/Counter Address Map

Address (in hex)	R/W	Register
040	W	System timer initial count
040	R	System timer status
041	W	Refresh request initial count
041	R	Refresh request status
042	W	Speaker tone initial count
042	R	Speaker tone status
043	W	Timer 1 control word
048	W	Fail-safe timer initial count
048	R	Fail-safe timer status
049		Not used
04A	W	CPU speed initial count
04A	R	CPU speed status
04B	W	Timer 2 control word

NMI Logic

The NMI logic generates an interrupt that has priority over the normal interrupts. A NMI occurs when the following error condition exists:

1. Onboard memory has a parity error. The system board reports parity errors on the PARITY* line.
2. An EISA memory expansion board has a parity error. IOCHK* is driven low when this error occurs.
3. Fail-safe timer 2 counter 0 has timed-out. This NMI is sensed with a rising, edge-detecting latch.

NOTE

An NMI is not generated when the CPU holds the bus longer than 64 BCLKs

4. Writing to the NMI I/O interrupt port 0462h when the port is enabled by bit seven of I/O port 070h.

Clock

The clock logic receives bus clock (BCLK), and outputs timing signals required by the ISP.

Interrupt Controller

The interrupt controller handles up to 16 interrupts and is accessed and addressed as though it were two separate 82C59 Interrupt Controllers (CNTRL1 and CNTRL2) cascaded together. Table 4-4 lists the address map for interrupt controller registers.

Table 4-4. Interrupt Controller Address Map

Address (in hex)	Register
0020	CNTLR-1 control register
0021	CNTLR-1 mask register
04D0	CNTLR-1 edge/level control register
00A0	CNTLR-2 control register
00A1	CNTLR-2 mask register
04D1	CNTLR-2 edge/level control register

Register Descriptions

The following sections describe the register bit assignments for these ISP functions:

- DMA
- NMI
- Interrupt controller
- Interval timer/counter

DMA Registers

DMA channel four cascades the DMA controllers together and cannot be programmed.

Chain Buffer Expiration Control

This register is 8-bits wide, read only, and contains what signal is issued when a chain buffer expires. Refer to Table 4-5 for its bit assignments.

Table 4-5. Chain Buffer Expiration Control Register Bit Assignments

Bit	Function	Definition
7	Channel 7	0 = IRQ13 1 = terminal count
6	Channel 6	0 = IRQ13 1 = terminal count
5	Channel 5	0 = IRQ13 1 = terminal count
4	Not used	
3	Channel 4	0 = IRQ13 1 = terminal count
2	Channel 3	0 = IRQ13 1 = terminal count
1	Channel 2	0 = IRQ13 1 = terminal count
0	Channel 1	0 = IRQ13 1 = terminal count

Channel Interrupt Status

This register is 8-bits wide, read only, and contains the DMA interrupt (IRQ13) source. Refer to Table 4-6 for its bit assignments.

Table 4-6. Channel Interrupt Status Register Bit Assignments

Bit	Function	Definition
7	Channel 7	0 = no interrupt 1 = interrupt
6	Channel 6	0 = no interrupt 1 = interrupt
5	Channel 5	0 = no interrupt 1 = interrupt
4	Not used	
3	Channel 4	0 = no interrupt 1 = interrupt
2	Channel 3	0 = no interrupt 1 = interrupt
1	Channel 2	0 = no interrupt 1 = interrupt
0	Channel 1	0 = no interrupt 1 = interrupt

Command Register

This register is 8-bits wide, write only, and controls DMA operation. Refer to Table 4-7 for its bit assignments.

Table 4-7. Command Register Bit Assignments

Bit	Function	Definition
7	Data acknowledge	0 = active low 1 = active high
6	Data request	0 = active low 1 = active high
5	Not used	
4	Priority	0 = fixed priority 1 = rotating priority
3	Not used	
2	DMA channel enable	0 = channels 0-3 1 = channels 4-7
1:0	Not used	

Extended Mode Register

This register is 8-bits wide, write only, and programs DMA data size and timing mode. Refer to Table 4-8 for its bit assignments.

Table 4-8. Extended Mode Register Bit Assignments

Bit	Function	Definition
7	Stop register	0 = disable 1 = enable
6	End of process (EOP) source	0 = output 1 = input
5:4	Timing	0 0 = compatible 0 1 = type A 1 0 = type B 1 1 = burst
3:2	Number of bits and count type	0 0 = 8-bit I/O, byte count 0 1 = 16-bit I/O, word count (shifted address) 1 0 = 32-bit I/O, byte count 1 1 = 16-bit I/O, byte count
1:0	Channel select	0 0 = channel 0 (4) 0 1 = channel 1 (5) 1 0 = channel 2 (6) 1 1 = channel 3 (7)

Mask Register

This register is 8-bits wide, write only, and disables the incoming data request (DREQ). Refer to Table 4-9 for its bit assignments.

Table 4-9. Mask Register Bit Assignments

Bit	Function	Definition
7:3	Not used	
2	Mask bit	0 = clear 1 = set
1:0	Channel select	0 0 = channel 0 (4) 0 1 = channel 1 (5) 1 0 = channel 2 (6) 1 1 = channel 3 (7)

Mode Register

This register is 8-bits wide, write only, and sets the DMA mode. Refer to Table 4-10 for its bit assignments.

Table 4-10. Mode Register Bit Assignments

Bit	Function	Definition
7:6	DMA mode	0 0 = demand 0 1 = single 1 0 = block 1 1 = cascade
5	Address	0 = increment 1 = decrement
4	Autoinitialize	0 = disable 1 = enable
3:2	Transfer	0 0 = verify 0 1 = write 1 0 = read 1 1 = illegal x x = If cascade mode
1:0	Channel select	0 0 = channel 0 (4) 0 1 = channel 1 (5) 1 0 = channel 2 (6) 1 1 = channel 3 (7)

Request Register

This register is 8-bits wide, write only, and initiates a DMA request. Refer to Table 4-11 for its bit assignments.

Table 4-11. Request Register Bit Assignments

Bit	Function	Definition
7:3	Not used	
2	Request bit	0 = clear 1 = set
1:0	Channel select	0 0 = channel 0 (4) 0 1 = channel 1 (5) 1 0 = channel 2 (6) 1 1 = channel 3 (7)

Set Chaining Mode Register

This register is 8-bits wide, write only, and sets chaining mode. Refer to Table 4-12 for its bit assignments.

Table 4-12. Set Chaining Mode Register Bit Assignments

Bit	Function	Definition
7:5	Not used	
4	Response to end of DMA transfer	0 = generate IRQ13 1 = generate TC
3	Programming complete	0 = don't start chaining 1 = programming complete
2	Chaining mode	0 = disable 1 = enable
1:0	Channel select	0 0 = channel 0 (4) 0 1 = channel 1 (5) 1 0 = channel 2 (6) 1 1 = channel 3 (7)

Set Chaining Mode Status

This register is 8-bits wide, read only, and holds chaining mode status information for the DMA channels. Refer to Table 4-13 for its bit assignments.

Table 4-13. Set Chaining Mode Status Register Bit Assignments

Bit	Function	Definition
7	Channel 7	0 = disabled 1 = enabled
6	Channel 6	0 = disabled 1 = enabled
5	Channel 5	0 = disabled 1 = enabled
4	Not used	
3	Channel 4	0 = disabled 1 = enabled
2	Channel 3	0 = disabled 1 = enabled
1	Channel 2	0 = disabled 1 = enabled
0	Channel 1	0 = disabled 1 = enabled

Status Register

This register is 8-bits wide, read only, and holds channel status information. Refer to Table 4-14 for its bit assignments.

Table 4-14. Status Register Bit Assignments

Bit	Function	Definition
7	Channel 7 (3) DMA request	0 = no 1 = yes
6	Channel 6 (2) DMA request	0 = no 1 = yes
5	Channel 5 (1) DMA request	0 = no 1 = yes
4	Channel 4 (0) DMA request	0 = no 1 = yes
3	Channel 7 (3) at terminal count	0 = no 1 = yes
2	Channel 6 (2) at terminal count	0 = no 1 = yes
1	Channel 5 (1) at terminal count	0 = no 1 = yes
0	Channel 4 (0) at terminal count	0 = no 1 = yes

Stop Registers

This register is 22-bits wide (A23:2), write only, and contains the DMA stop address. Each channel has a stop register and is enabled by a bit in the extended mode register. Table 4-15 lists the address map for the stop registers.

Table 4-15. Stop Register I/O Port Addresses

Address (bits 23:16)	Address (bits 15:8)	Address (bits 7:2)	DMA Channel
04E0	04E1	04E2	0
04E4	04E5	04E6	1
04E8	04E9	04E	2
04EC	04ED	03EE	3
04F4	04F5	04F6	5
04F8	04F9	04FA	6
04FC	04FD	04FE	7

NMI Registers

There are four 8-bit registers that control the NMI logic. Table 4-16 lists the NMI register I/O addresses. Refer to Tables 4-17 through 4-20 for these register bit assignments.

Table 4-16. NMI Register I/O Addresses

I/O Address (in hex)	R/W	Register
061	R/W	Status and control
070	W	Enable/disable and real time clock address
0461	R/W	Extended status and control
0462	W	Software NMI generation

Table 4-17. Status and Control Register Bit Assignments

Bit	R/W	Function	Definition
7	R	System board parity error	0 = no 1 = yes
7	W	Not used	Must be 0
6	R	EISA slot (IOCHK* interrupt)	0 = no 1 = yes
6	W	Not used	Must be 0
5	R	State of interval timer 1 counter 2 OUT	
5	W	Not used	Must be 0
4	R	Toggles every refresh cycle	
4	W	Not used	Must be 0
3	R/W	Enable IOCHK* interrupt	0 = enable 1 = disable
2	R/W	Enable parity error interrupt	0 = enable 1 = disable
1	R/W	Enable SPKR output (AND'ed with interval timer 1 counter 2 OUT	0 = enable 1 = disable
0	R/W	Gate signal for interval timer 1 counter 2	0 = enable 1 = disable

Table 4-18. Enable/Disable and Real-Time Clock Register Bit Assignments

Bit	Function	Definition
7	NMI	0 = enabled 1 = disabled
6:0	Real-time clock index	

Table 4-19. Extended Status and Control Register Bit Assignments

Bit	R/W	Function	Definition
7	R	NMI fail-safe interrupt	0 = no 1 = yes
7	W	Not used	Must be 0
6	R	EISA bus master interrupt time-out	0 = no 1 = yes
6	W	Not used	Must be 0
5	R	NMI interrupt	0 = no 1 = yes
5	W	Not used	Must be 0
4	R	8 msec EISA bus master time-out	0 = no 1 = yes
4	W	Not used	Must be 0
3	R/W	Enable EISA bus master time-out interrupt	0 = enable 1 = disable
2	R/W	Enable fail-safe NMI interrupt	0 = enable 1 = disable
1	R/W	Enable NMI I/O port	0 = enable 1 = disable
0	R/W	System bus reset	0 = no 1 = yes

Table 4-20. Software NMI Generation Register Bit Assignments

Bit	Function	Definition
7:0	Initiate NMI	0 = no 1 = yes

Timer/Counters

The timer/counters 8-bit read/write control word registers specify the counter, the operating mode, the order and size of the count value, and type of countdown. Refer to Table 4-21 for its bit assignments.

Table 4-21. Control Word Bit Assignments

Bit	Function	Definition
7:6	Counter select	0 0 = counter 0 0 1 = counter 1 1 0 = counter 2 1 1 = read back
5:4	Counter latch	0 0 = latch command 0 1 = R/W LSB 1 0 = R/W MSB 1 1 = R/W LSB then MSB
3:1	Operating mode	0 0 0 = OUT signal at count end 0 0 1 = hardware retriggerable one-shot 0 1 0 = rate generator 0 1 1 = square wave output 1 0 0 = s/w triggered strobe 1 0 1 = h/w triggered strobe 1 1 0 = not used 1 1 1 = not used
0	Countdown	0 = binary 1 = BCD

Pinouts

Table 4-22 lists the difference between the standard ISP signal pinouts and the DECpc 400ST signal pinouts.

Table 4-22. ISP Signal Cross Reference

Pin No.	ISP Signal Name	DECpc 400ST Series Signal Name
3	INT	INTR
4	EMSTR16*	EMSTR16*
5	EXMASTER*	EXMASTER*
6	NMI	NMI
7	SPKR	SPKDAT
8	RTCALE	RTCALE
9	CSOUT*	ISPCS*
10	SLOWH*	SLOWH*
11	GT16M*	GT16M*
12	GT1M*	GT1M*
13	IOCHK*	IOCHK*
14	PARITY*	LERROR*
16	BCLK	BCLK
18	RST	RST
19	CMD*	CMD*
20	START*	START*
23	A31	ISP31
24	A30	ISP30
25	A29	ISP29

Table 4-22. ISP Signal Cross Reference *(continued)*

Pin No.	ISP Signal Name	DECpc 400ST Series Signal Name
26	A28	ISP28
27	A27	ISP27
28	A26	ISP26
29	A25	ISP25
30	A24	ISP24
31	A23	ISP23
32	A22	ISP22
35	A21	ISP21
36	A20	ISP20
37	A19	ISP19
38	A18	ISP18
39	A17	ISP17
40	A16	ISP16
41	A15	ISP15
42	D7	BXD7
43	D6	BXD6
44	D5	BXD5
45	D4	BXD4
46	D3	BXD3
47	D2	BXD2
48	D1	BXD1
49	D0	BXD0
50	A14	ISP14

Table 4-22. ISP Signal Cross Reference *(continued)*

Pin No.	ISP Signal Name	DECpc 400ST Series Signal Name
51	A13	ISP13
52	A12	ISP12
55	A11	ISP11
56	A10	ISP10
57	A9	ISP9
58	A8	ISP8
59	A7	ISP7
60	A6	ISP6
61	A5	ISP5
62	A4	ISP4
63	A3	ISP3
64	A2	ISP2
67	BE0*	BE0*
68	BE1*	BE1*
69	BE2*	BE2*
70	BE3*	BE3*
72	ST3	ST3
73	ST2	ST2
74	ST1	ST1
75	ST0	ST0
78	DRDY	EDRDY
79	HW/R*	HWRD*
80	EOP	T/C

Table 4-22. ISP Signal Cross Reference *(continued)*

Pin No.	ISP Signal Name	DECpc 400ST Series Signal Name
82	AEN*	AEN*
83	DACK7*	DAK7*
84	DACK6*	DAK6*
85	DACK5*	DAK5*
86	DACK3*	DAK3*
87	DACK2*	DAK2*
88	DACK1*	DAK1*
89	DACK0*	DAK0*
92	MACK5*	MAK5*
93	MACK4*	MAK4*
94	MACK3*	MAK3*
95	MACK2*	MAK2*
96	MACK1*	MAK1*
97	MACK0*	IMAK*0
98	DHOLD	DHOLD
100	DREQ7	DRQ7
101	DREQ6	DRQ6
102	DREQ5	DRQ5
103	DREQ3	DRQ3
104	DREQ2	DRQ2
105	DREQ1	DRQ1
106	DREQ0	DRQ0

Table 4-22. ISP Signal Cross Reference *(continued)*

Pin No.	ISP Signal Name	DECpc 400ST Series Signal Name
107	MREQ5*	IMRQ5*
108	MREQ4*	IMRQ4*
109	MREQ3*	IMRQ3*
110	MREQ2*	IMRQ2*
111	MREQ1*	IMRQ1*
112	MREQ0*	IMRQ0*
113	CPUMISS*	CPUMISS*
114	DHLDA	HLDA
115	IRQ15	IRQ15
116	IRQ14	IRQ14
117	IRQ13	IRQ13
118	IRQ12	IRQ12
119	IRQ11	IRQ11
120	IRQ10	IRQ10
121	IRQ9	IRQ9
122	IRQ8*	IRQ8*
123	IRQ7	IRQ7
124	IRQ6	IRQ6
125	IRQ5	IRQ5
126	IRQ4	IRQ4
127	IRQ3	IRQ3
128	IRQ1	IRQ1
129	OSC	OSC14B
131	REFRESH*	REFRESH*
132	RSTDRV	RSTDRV

5

WD16C552 or TL16C552 Asynchronous Communications Element

Introduction

The DECpc 400ST Series system board uses either a Western Digital™ WD16C552 or a Texas Instruments™ TL16C552 Asynchronous Communications Element (ACE) to provide two RS-232C serial communication ports (COM1 and COM2) and a single parallel communication port (LPT1).

Serial Communication Ports

Table 5-1 lists the serial communication ports address map.

Table 5-1. Serial Communication Ports Address Map

Port	Address (in hex)	Interrupt
COM1	3F8 to 3FF	IRQ4
	2F8 to 2FF	IRQ3
	3E8 to 3EF	IRQ10
COM2	2F8 to 2FF	IRQ3
	3E8 to 3EF	IRQ10
	2E8 to 2EF	IRQ11

Serial Port Register Descriptions

The address lines XD(2:0) and the divisor latch access bit (DLAB) determine access to the serial communication port registers. Each communication port has its own set of registers. Table 5-2 lists the address map for the serial communication port registers.

Table 5-2. Serial Communication Port Register Selection

DLAB	XD2	XD1	XD0	R/W	Register
0	0	0	0	R	Receive buffer
0	0	0	0	W	Transmit buffer
0	0	0	1	R/W	Interrupt enable
x	0	1	0	R	Interrupt identification
x	0	1	0	W	FIFO control
x	0	1	1	R/W	Line control
x	1	0	0	R/W	Modem control
x	1	0	1	R	Line status
x	1	1	0	R/W	Modem status
x	1	1	1	R/W	Scratch pad
1	0	0	0	R/W	Divisor (LSB)
1	0	0	1	R/W	Divisor (MSB)

Receive Buffer Register

The receive buffer register holds the incoming data byte. Bit zero is the least significant bit and is transmitted and received first. An additional shift register assembles the incoming byte before loading it into the receive buffer register.

Transmit Buffer Register

The transmit buffer register holds the data byte to be sent. Bit zero is the least significant bit and is transmitted and received first. An additional shift register shifts the outgoing byte out to the TDX pin.

Interrupt Enable Register

This register enables one of four interrupt types. Refer to Table 5-3 for its bit assignments.

Table 5-3. Interrupt Enable Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:4	Not used		
3	EDSSI	Enable modem status interrupt	0 = no 1 = yes
2	ERLSI	Enable receive line status interrupt	0 = no 1 = yes
1	ETBEI	Enable transmitter holding register empty interrupt	0 = no 1 = yes
0	ERBFI	Enable received data available interrupt	0 = no 1 = yes

Interrupt Identification Register

This register reports an interrupt source and the highest pending interrupt. Refer to Table 5-4 for its bit assignments.

Table 5-4. Interrupt Identification Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:6	FCR(0)	FIFO control register bit 0	
5:4	Not used		
3:2	IIDB3:2	Interrupt ID bits 3:2	
1	IIDB0	Interrupt ID bit 0	
0	IP	Interrupt pending	0 = yes 1 = no

FIFO Control Register

This register controls how the 16-byte FIFO buffers operate. Refer to Table 5-5 for its bit assignments.

Table 5-5. FIFO Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:6	RT	Receiver FIFO trigger level	0 0 = 01 bytes 0 1 = 04 bytes 1 0 = 08 bytes 1 1 = 14 bytes
5:4	Reserved		
3	DMS	DMA mode selected	0 = no 1 = yes
2	TFR	Transmitter FIFO reset	0 = no 1 = yes
1	RFR	Receiver FIFO reset	0 = no 1 = yes
0	FEWO	FIFO enable write only	0 = no 1 = yes

Line Control Register

This register contains format information for the serial line. Refer to Table 5-6 for its bit assignments.

Table 5-6. Line Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7	DLAB	Divisor latch access	0 = all other registers 1 = divisor latch only
6	SBR	Set break control	0 = end break condition 1 = force break
5	STP	Stick parity bit	0 = force odd parity 1 = force even parity
4	EPS	Even parity select	0 = odd parity 1 = even parity
3	PEN	Parity enable	0 = no 1 = yes
2	STB	Number of stop bits	0 = 1 stop bit generated 1 = 1.5 stop bits if WLS= 5-bits 1 = 2 stops bit if WLS = 6, 7, or 8-bits
1:0	WLS1:0	Word length select	0 0 = 5 bits 0 1 = 6 bits 1 0 = 7 bits 1 1 = 8 bits

Modem Control Register

This register manages the connection to an external modem or data set. Refer to Table 5-7 for its bit assignments.

Table 5-7. Modem Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:5	Not used		
4		Loop	0 = disabled 1 = enabled
3	OUT2*	Output 2	0 =force OUT2* high 1 = force OUT2* low
2	OUT1*	Output 1	0 = force OUT1* high 1 = force OUT1* low
1	RTS*	Ready to send	0 = force RTS* high 1 = force RTS* low
0	DTR*	Data terminal ready	0 = force DTS* high 1 = force DTS* low

Line Status Register

This register supplies serial link status information to the CPU module. Refer to Table 5-8 for its bit assignments.

Table 5-8. Line Status Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7	EIRF	Error in receiver FIFO	0 = no 1 = yes
6	TEMT	Transmitter empty	0 = no 1 = yes
5	THRE	Transmitter holding register empty	0 = no 1 = yes
4	BI	Break interrupt	0 = no 1 = yes
3	FE	Framing error	0 = no 1 = yes
2	PE	Parity error	0 = no 1 = yes
1	OE	Overrun error	0 = no 1 = yes
0	DR	Data ready	0 = no 1 = yes

Modem Status Register

This register holds the current value of the modem control lines. Each time one of the modem control lines changes state, the modem status register sets the corresponding bit to one. Reading the modem status register clears the previously set bits. When set to one, bits 0, 1, 2, and 3 generate an interrupt if the corresponding interrupt bit is enabled. Refer to Table 5-9 for its bit assignments.

Table 5-9. Modem Status Register Bit Assignments

Bit	Signal Mnemonic	Function	Description
7	RLSD	Receive line signal detect	0 = no 1 = yes
6	RI	Ring indicator	0 = no 1 = yes
5	DSR	Data set ready	0 = no 1 = yes
4	CTS	Clear to send	0 = no 1 = yes
3	DRLSD	Delta receive line signal detect	0 = no 1 = yes
2	TERI	Trailing edge ring indicator	0 = no 1 = yes
1	DDSR	Delta data set ready changed	0 = no 1 = yes
0	DCTS	Delta clear to send	0 = no 1 = yes

Divisor Registers (LSB and MSB)

The two divisor registers contain a 16-bit divisor used to generate the serial ports baud rate at three different clock frequencies. Table 5-10 lists the resulting baud rate based on the divisor register contents and the percentage of error. All values in the table are decimal.

Table 5-10. Baud Rates Using 1.846 MHz Clock

Baud Rate	Divisor	Percentage of Error
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

Parallel Printer Port

The read, write, status, and control signal registers control data and status transmissions to and from the printer. System software executes all printer controls. Address lines XA(1:0) and input/output read/write strobe lines (IOR*/IOW*) control parallel port register accesses. Table 5-11 lists the parallel port register address map. Table 5-12 lists the parallel port registers bit assignments.

Table 5-11. Parallel Port Register Address Map

XA1	XA0	IOR*	IOW*	CS2*	Register
0	0	0	1	0	Read data
0	1	0	1	0	Read status
1	0	0	1	0	Read control
0	0	1	0	0	Write data
1	0	1	0	0	Write control

Table 5-12. Parallel Port Register Bit Assignments

Bit	Read Data	Read Status	Read/ Control	Write Control	Write Data
7	PD7	BUSY*	1(1)	1(1)	PD7
6	PD6	ACK*	1(1)	1(1)	PD6
5	PD5	PE	1(2)	1(2)	PD5
4	PD4	SLCT	Interrupt enable	IRQ enable	PD4
3	PD3	Error*	SLIN	Select	PD3
2	PD2	1(3)	INIT*	Initialize*	PD2
1	PD1	1	AFD	Autofeed	PD1
0	PD0	1	STB	Strobe	PD0

(1) For TL16C552, this bit equals 0
(2) For TL16C552, this bit equals DIR
(3) For TL1616C552 , this bit equals PRINT*

6

82077 Diskette Drive Controller

Introduction

A DECpc 400ST Series system board uses an integrated Intel 82077 Diskette Drive Controller (DDC) operating in PC/AT mode. The DDC contains all the logic required for diskette drive control, including 2.88 MB diskette drive and floppy tape. It also provides the connection between the onboard EISA bus and the diskette drive connector. The DDC contains the following functional blocks (see Figure 6-1):

- FIFO
- Interface logic
- Serial interface logic
- Drive interface controller
- General registers

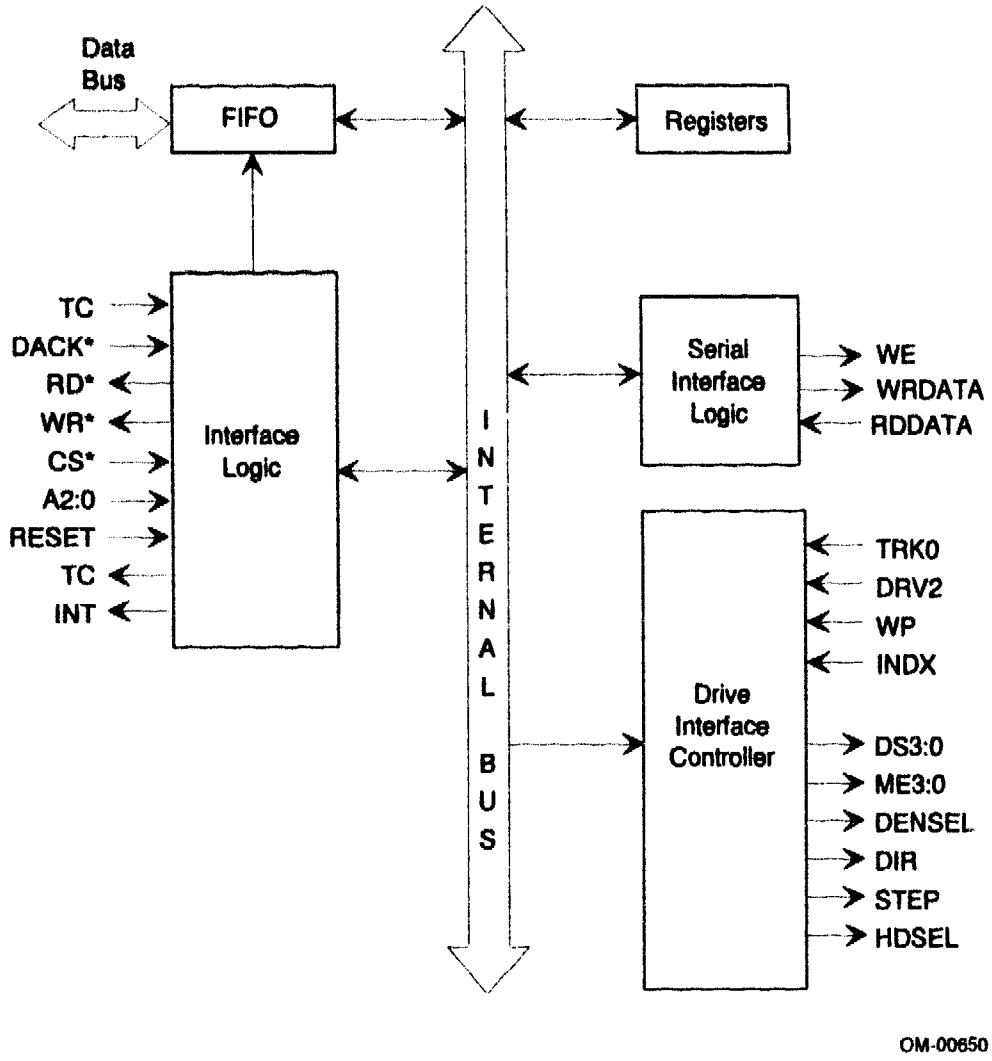


Figure 6-1. Diskette Drive Controller Block Diagram

FIFO

This 16-byte first-in-first-out (FIFO) is the gateway to the DDC. All command data and diskette data goes through the FIFO. In addition, the FIFO has programmable threshold values.

Interface Logic

The interface logic receives the asynchronous CPU signals TC, DACK*, RD*, WR*, CS*, and A2:0. Input TC and output INT cause the current diskette transfer to terminate or cause an interrupt.

Serial Interface Logic

The serial interface logic controls data flow between the internal bus and the diskette drive (see Figure 6-1). The diskette drive receives serial data (RDDATA) during read operations. The diskette drive outputs serial data (WRDATA) and write enable (WE) during write operations.

Drive Interface Controller

The drive interface controller outputs the various control signals for the diskette drive. It also receives index (INDX), track 0 (TRK0), and write protect (WP) signals from the diskette drive. Input signal DRV2 indicates the presence of a second diskette drive.

General Registers

Six general purpose registers control DDC operations. Access these registers between addresses 3F0h and 3F7h. Table 6-1 lists the DDC register I/O addresses, specifies the I/O function required to access the registers, and briefly describes the registers. The following registers control DDC operations in AT mode:

- Digital output register (DOR)
- Tape drive register (TDR)
- Main status register (MSR)
- Data rate select register (DRS)
- Data register (FIFO)
- Digital input/configuration control register (DIR/CCR)

Table 6-1. DDC Register Address Map

Address (in hex)	R/W	Register Mnemonic	Description
3F0			Reserved
3F1			Reserved
3F2	R/W	DOR	Digital output register
3F3	R/W	TSR	Tape drive register
3F4	R	MSR	Main status register
3F4	W	DSR	Data select rate register
3F5	R/W	FIFO	Data register
3F6			Reserved
3F7	R	DIR	Digital input register
3F7	W	CCR	Configuration control register

Digital Output Register

This read/write register contains the motor enable bits, a DMA gate bit, a reset bit, and drive selection bits. Refer to Table 6-2 for its bit assignments.

Table 6-2. Digital Output Register (DOR) Bit Assignments

Bit	Signal Mnemonic	Function
7:4	MOT EN3:0	Motor enable 3:0
3	DMAGATE*	DMA gate
2	RESET*	Reset
1:0	DRIVE SEL1:0	Drive select 1:0

Tape Drive Register

This read/write register selects one of three possible tape drives (tape drive 1, 2, or 3). Refer to Table 6-3 for its bit assignments.

Table 6-3. Tape Drive Register (TDR) Bit Assignments

Bit	Signal Mnemonic	Function
7:2	Reserved	
1:0	Tape SEL1:0	Tape drive select 1:0

Main Status Register

This read only register controls the data input and output modes. It also passes ready information to the CPU. Refer to Table 6-4 for its bit assignments.

Table 6-4. Main Status Register (MSR) Bit Assignments

Bit	Signal Mnemonic	Function
7	RQM	Request for master
6	DIO	Data in/out
5	NON DMA	Non DMA
4	CMD BUSY	Command busy
3	DRV 3 BUSY	Drive 3 busy
2	DRV 2 BUSY	Drive 2 busy
1	DRV 1 BUSY	Drive 1 busy
0	DRV 0 BUSY	Drive 0 busy

Data Rate Select Register

This write only register specifies the data transfer rate and precompensation delay for data transfers between the controller and the diskette drive. It also contains power down and software reset information. Refer to Table 6-5 for its bit assignments.

Table 6-5. Data Rate Select (DRS) Register Bit Assignments

Bit	Signal Mnemonic	Function
7	S/W RESET	Software reset
6	POWER DOWN	Power down
5	Reserved	
4:2	PRECOMP 2:0	Precompensation selection
1:0	DRATE SEL 1:0	Data rate selection

Data Register

This read/write register is also the FIFO. All data and command information pass through the data register.

Digital Input Register

This read only register senses the state of the DSKCHG at bit 7. All other bits are tri-stated.

Configuration Control Register

This write only register sets the data rate. Refer to Table 6-6 for its bit assignment.

Table 6-6 Configuration Control Register (CCR) Bit Assignments

Bit	Signal Mnemonic	Function
7:2	Reserved	
1:0	DRATE SEL 1:0	Data rate selection 1:0

7

8742 Keyboard and Mouse Controller

Introduction

The DECpc 400ST system board uses an Intel 8742 Universal Peripheral Interface Microcontroller (also known as the keyboard and mouse controller) to communicate with the PS/2 keyboard and PS/2 mouse. The 8742 contains a microcomputer and internal memory. The 8742 controller communicates with the EISA bus by a status register, an output buffer, and an input buffer. Communication among the 8742 controller and the keyboard and mouse is through an input port and an output port. Figure 7-1 shows a block diagram of the 8742 keyboard and mouse controller.

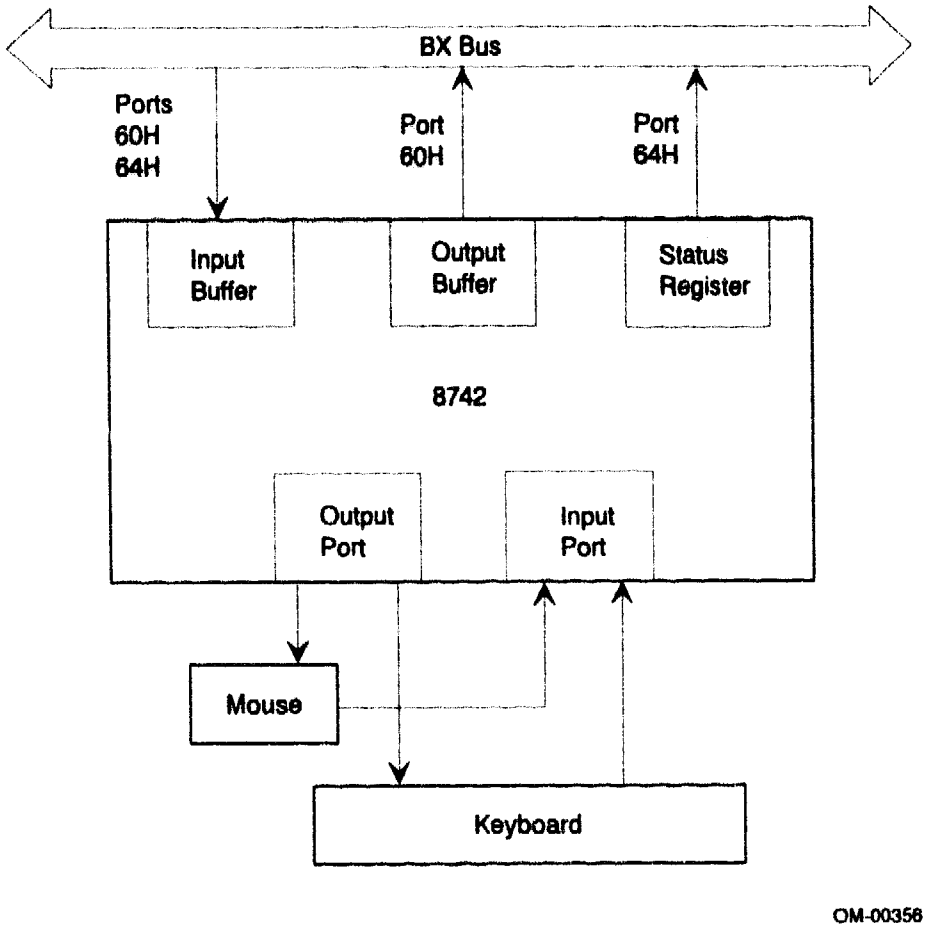


Figure 7-1. Keyboard and Mouse Controller Block Diagram

Status Register

The status register is an 8-bit read-only register that contains controller and system interface information. Address the status register at I/O port 64h. Table 7-1 lists the status register bit definitions.

Table 7-1. Status Register Bit Definitions

Bit	Function	Definition
7	Receive parity error	0 = no error 1 = parity error
6	General time-out	0 = no time-out 1 = time-out
5	Output buffer source	0 = keyboard 1 = mouse
4	Keyboard enable	0 = disabled 1 = enabled
3	Command/data	0 = data or idle 1 = command or active
2	System flag	0 = hot reset 1 = no hot reset
1	Input buffer full	0 = empty 1 = full
0	Output buffer full	0 = empty 1 = full

Output Buffer

The output buffer is an 8-bit read-only register at I/O port 60h. The controller sends keyboard scan codes, command-requested data bytes, and mouse data to the EISA bus via the output buffer. The data in the output buffer is valid when status register bit zero equals one.

Input Buffer

The input buffer is an 8-bit write-only register at I/O ports 60h and 64h. You can write data to the input buffer only when status register bit one equals zero.

Writing to port 60h clears status register command/data bit (bit three). Once cleared, the controller processes the data in the input buffer as a data byte. The data byte then goes to the keyboard, unless a system command instructs the controller to wait for a data byte.

Writing to port 64h sets the command/data bit (bit three) of the status register to one. Once set, the controller processes the data in the input buffer as a command byte.

Input and Output Ports

The input port consists of two signals to the controller driven by the keyboard and mouse, and three signals indicating the keylock state, the password on/off state, and the color/monochrome setting. The output port consists of eight signals driven by the controller to the keyboard, mouse, or system interface. Access both ports by sending the appropriate read or write command to the controller. Tables 7-2 and 7-3 list the input and output port bit assignments.

Table 7-2. Input Port Bit Assignments

Bit	Function	Definition
7	Keylock	0 = on 1 = off
6	Monitor type	0 = color 1 = monochrome
5	MG test	Manufacturing test
4	Clear CMOS	Clear CMOS
3	Password	0 = password set 1 = no password set
2	Pull-up	
1	Mouse data input	
0	Keyboard data input	

Table 7-3. Output Port Bit Assignments

Bit	Function
7	Keyboard data output
6	Keyboard clock input
5	Mouse interrupt
4	Keyboard interrupt
3	Mouse clock output
2	Mouse data output
1	Gate A20
0	Software reset

Controller Commands

The CPU issues controller commands to control the operation of the 8742 and to sense its status. Write controller commands into the input buffer at I/O port 64h; if there is a following data byte, the CPU writes it to I/O port 60h. Table 7-4 lists and briefly describes the controller commands.

Table 7-4. Controller Commands

Command	Description
20h	Read controller command byte
21 to 3Fh	Read controller RAM locations 3F to 21h
60h	Write controller command byte
61 to 7Fh	Write controller RAM locations 3F to 21h
A4h	Test password
A5h	Load password
A6h	Enable password
A7h	Disable mouse
A8h	Enable mouse
A9h	Mouse interface test
AAh	Self test
ABh	Keyboard interface test
ACh	Diagnostic dump
ADh	Disable keyboard
AEh	Enable keyboard
C0h	Read input port
C1h	Poll input port low bits
C2h	Poll input port high bits
D0h	Read output port
D1h	Write output port
D2h	Write keyboard output buffer
D3h	Write mouse output buffer
D4h	Write to mouse
E0h	Read test inputs
F0 to FFh	Pulse output port

Keyboard and Mouse Data Stream

The controller, keyboard, and mouse communicate using data and clock lines for synchronous serial communication. There are separate data and clock lines for the mouse and the keyboard.

The 8-bit data stream, transferred serially over the data line, consists of one start bit, eight data bits, one odd parity bit, and one stop bit. Table 7-5 lists the data stream bit assignments. A logical one indicates an active level and a logical zero indicates an inactive level. Odd parity is used. The keyboard and mouse clock signals synchronize the data transfer.

Table 7-5. Data Stream Bits

Bit	Function
11	Stop bit (always 1)
10	Parity bit
9	Data bit 7 (MSB)
8	Data bit 6
7	Data bit 5
6	Data bit 4
5	Data bit 3
4	Data bit 2
3	Data bit 1
2	Data bit 0 (LSB)
1	Start bit (always 0)

Sending Data to the Keyboard

There are 17 commands to the keyboard. A data byte that sets keyboard conditions follows some commands. Before sending another byte the keyboard must respond to all commands and data bytes with an ACK command. There is a programmable time limit for the keyboard to respond without a timeout error. The following paragraphs describe the commands and accompanying data bytes to the keyboard by the controller. The number in parenthesis following the command name is the transmitted code in hexadecimal.

Set/Reset Status Indicators (EDh)

The set/reset status indicators command activates or deactivates the three LED indicators (Num Lock, Caps Lock, and Scroll Lock) on the keyboard.

The keyboard responds to the command byte with the ACK command (described later), discontinues scanning, and waits for the status indicator data byte. The optional data byte determines the state of the keyboard LEDs. Table 7-6 lists the bit definitions for the status indicator data byte.

Table 7-6. Status Indicator Bits

Bit	Function	Definition
7:3	Not used	Set to 0
2	Caps Lock LED	0 = off 1 = on
1	Num Lock LED	0 = off 1 = on
0	Scroll Lock LED	0 = off 1 = on

Echo (EEh)

The echo command tests the keyboard command process. When the keyboard receives this command, it issues an EEh response and continues scanning.

Select Alternate Scan Codes (F0h)

The select alternate scan codes command instructs the keyboard to select one of three sets of scan codes. The keyboard acknowledges receipt of this command with an ACK, then clears both the output buffer and the typematic key (if active). When the controller sends the option byte, the keyboard responds with another ACK. An option byte value of 01h selects scan code set 1, 02h selects set 2, and 03h selects set 3. Byte value 00h causes the keyboard to respond with an ACK and send a byte to the controller indicating that scan code set is in use.

Read ID (F2h)

The read ID command requests identification information from the keyboard. The keyboard responds with an ACK, discontinues scanning, and sends the two keyboard ID bytes. After the output of the second ID byte, the keyboard resumes scanning.

Set Typematic Rate/Delay (F3h)

This command sets the typematic rate and delay. The keyboard responds with an ACK, stops scanning, and waits for the controller to issue the rate/delay value byte. Once issued, the keyboard responds with another ACK, sets the rate and delay to the values indicated, and resumes scanning.

Table 7-7 lists the typematic rate/delay bit definitions.

Table 7-7. Typematic Rate/Delay Bit Definitions

Bit	Function	Definition
7	Not used	Set to 0
6:5	Delay parameter	00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms
4:0	Typematic rate (repeats per second)	See Table 7-8

Table 7-8. Typematic Rate

Value	Rate	Value	Rate
00000	30.0	10000	7.5
00001	26.7	10001	6.7
00010	24.0	10010	6.0
00011	21.85	10011	5.5
00100	20.0	10100	5.0
00101	18.5	10101	4.6
00110	17.1	10110	4.3
00111	16.0	10111	4.0
01000	15.0	11000	3.7
01001	13.3	11001	3.3
01010	12.0	11010	3.0
01011	10.9	11011	2.7
01100	10.0	11100	2.5
01101	9.2	11101	2.3
01110	8.5	11110	2.1
01111	8.0	11111	2.0

Enable (F4h)

The enable command clears the keyboard output buffer, clears the last typematic key, and starts scanning.

Default Disable (F5h)

The default disable command sets the keyboard to the power-on default state and keyboard scanning.

Set Default (F6h)

The set default command is similar to the default disable command; however, the keyboard continues scanning.

Set All Keys (F7h, F8h, F9h, and FAh)

The set all keys commands F7h, F8h, F9h, and FAh instruct the keyboard to set all keys to typematic, make/break, make, and typematic/make/break, respectively. Send these commands using any scan code set and they affect only scan code set 3.

Set Key Type (FBh, FCh, and FDh)

The set key type commands, FBh, FCh, and FDh, instruct the keyboard to set individual keys to typematic, make/break, and make respectively. The keyboard responds with an ACK, clears its output buffer, and prepares to receive key The controller identifies each key by its scan code value as defined in scan code set 3. Only scan code set 3 values are valid for key identification. The type of each identified key is set to the value indicated by the command.

Resend (FEh)

The resend command causes the keyboard to resend the previous output.

Reset (FFh)

The reset command initiates the keyboard internal self-test. The keyboard remains disabled from the time it receives the reset command until the controller responds to the ACK. Then the keyboard initializes and performs the Basic Assurance Test (BAT). Finally, the keyboard returns and sets its default to scan code set 2.

Receiving Data from the Keyboard

The keyboard transfers data to the controller only when both the clock and data signals are active. At the end of a transfer, the controller disables the interface until the system accepts the data byte.

If a parity check error occurs, the controller signals the keyboard to transfer the data again and sets the status register parity error bit. When the controller receives the data correctly (after a set number of retries), the controller output buffer receives an FFh code. The controller's RAM address 21h stores the number of retries and has a default value of one.

The controller times each data byte transfer from the keyboard. If a keyboard transfer does not end within 2 ms, the controller sets the receive time-out bit in the status register and writes an FFh code to its output buffer. No retries are attempted on a receive time-out error.

The following paragraphs describe the commands and accompanying data bytes sent from the keyboard to the controller. The number in parenthesis following the command name is the transmitted code in hexadecimal.

Overrun or Key Detection Error (00h Or FFh)

When an overrun or key detection error occurs and scan code 1 is set, the keyboard sends command 00h to the controller. The overrun or key detection error occurs and scan code is 2 or 3, the keyboard sends command FFh to the controller.

Keyboard ID (83ABh)

The keyboard sends ID command 83ABh to the controller in response to a read ID command. The keyboard sends the low bytes first, followed by the high bytes.

BAT Completion Code (AAh)

The keyboard sends the Basic Assurance Test (BAT) completion command to the controller following satisfactory completion of the BAT. The system performs a BAT each time power is applied to the system and consists of a keyboard processor test, a ROM checksum test, and a RAM test.

Echo (EEh)

When the controller issues the echo command to the keyboard, the keyboard sends EEh as a response to the controller.

BAT Failure Code (FCh)

If a BAT failure occurs, the keyboard sends, discontinues scanning and waits for a reset command or some other response from the controller.

Acknowledge (FAh)

The keyboard issues an acknowledge (ACK) to any valid input other than an echo or a resend command. Interrupting the keyboard while it is sending an ACK causes it to discard the ACK and respond to the new command.

Resend (FEh)

The keyboard sends the resend command when it receives an invalid input or any input with a parity error.

System-To-Mouse Commands

The write to auxiliary device command (D4h) instructs the 8742 to transmit the next byte it receives to the mouse device. Precede all commands to the mouse with a data write of D4h to port 64h. Write all mouse commands to port 60h. Execute a write of D4h to port 64h first; otherwise, subsequent mouse commands go to the keyboard.

Reset Scaling (E6h)

The reset scaling command resets the X-Y scaling factor of the mouse to 1:1.

Set Scaling (E7h)

The set scaling command sets the scaling to 2:1. You can use this command only when the mouse is in stream mode. When scaling is set, the current X-Y coordinate values are converted to new values each time the sample period expires. Table 7-9 lists the relationship between the input and output values when scaling is set.

Table 7-9. Scaling Input and Output Relationships

Input	Output
0	0
1	1
2	1
3	3
4	6
5	9
N (≥ 6)	2.0 × N

Set Resolution (E8h)

The set resolution command consists of two bytes. The second byte (also written to port 60h) is interpreted as a resolution in counts per millimeter. Table 7-10 lists the relationship between the second byte and the resolution.

Table 7-10. Byte/Resolution Relationship

Byte	Resolutions
00h	1 count per mm
01h	2 counts per mm
10h	4 counts per mm
11h	8 counts per mm

Status Request (E9h)

The status request command generates a three-byte status report. Table 7-11 lists the mouse status request bytes format.

Table 7-11. Format of Mouse Status Request Bytes

Byte	Function	
3	Sampling rate	
2	Resolution	
1	Mouse status	
	Bit 7	Not used
	Bit 6 = 0	Stream mode
	1	Remote mode
	Bit 5 = 0	Disabled
	1	Enabled
	Bit 4 = 0	Scaling 1:1
	1	Scaling 2:1
	Bit 3	Not used
	Bit 2 = 1	Left mouse button pressed
	Bit 1	Not used
	Bit 0 = 1	Right mouse button pressed

Set Stream Mode (EAh)

In stream mode, the mouse transmits data to the system each time you press or released a mouse button, or each time the mouse detects a unit of movement. The mouse data sample rate determines the maximum number of times per second that mouse data can be transmitted to the system. If no button is pressed or if the mouse is not moved, no data is transmitted. The set stream mode command enables stream mode.

Read Data (EBh)

The read data command forces the transmission of one mouse data packet. The read data command is valid in both stream mode and remote mode.

Reset Wrap Mode (ECh)

The reset wrap mode command resets the mouse to normal operation.

Set Wrap Mode (EEh)

This command sets wrap mode, i.e., the mouse echo mode. With the exception of the reset wrap mode (ECh) and reset mouse (FFh) commands, the mouse echoes all data and commands received from the system.

Set Remote Mode (F0h)

This command sets remote mode. In remote mode, mouse data is only transmitted in reply to a read data command.

Read Device Type (F2h)

The read device type command reads the mouse ID byte. The mouse returns a value of 00h to the read device command.

Set Sampling Rate (F3h)

This command sets the sampling rate of the mouse. The sampling rate is the number of times per second that the system checks for mouse data. This is a two-byte command. The set sampling rate command (F3h) must be followed by a second byte that contains the value of the sampling rate. Table 7-12 lists the sampling rates.

Table 7-12. Mouse Sampling Rates

Byte	Sampling Rate
0Ah	10 samples per second
14h	20 samples per second
28h	40 samples per second
3Ch	60 samples per second
50h	80 samples per second
64h	100 samples per second
C8h	200 samples per second

Enable (F4h)

The enable command enables data transmissions if stream mode is set. This command has no effect in remote mode.

Disable (F5h)

The disable command disables data transmissions if the mouse has been set to stream mode. This command has no effect in remote mode.

Set Default (F6h)

The set default command reinitializes the mouse to its power-on default state. The mouse power-on defaults are: sampling rate, 100 samples per second; scaling, 1:1; mode, stream; resolution, 4 counts per mm; and transmissions, disabled.

Resend (FEh)

The resend command is in response to transmission errors from the mouse. The mouse responds to this command by retransmitting its last data packet.

Reset (FFh)

The reset command instructs the mouse to run its internal self-test routine. This command puts the mouse into reset mode.

Mouse-To-System Replies

There are two mouse-to-system replies. Both replies relate to command processing and can be read by the system at I/O port 60h.

Acknowledge (FAh)

The mouse replies with an acknowledge (FAh) each time it receives a valid command from the system. Unlike mouse serial data packets, the acknowledge reply is not stored in an internal memory buffer, but is discarded immediately after it is transmitted. If a new command is received while the mouse is in the acknowledge reply process, the mouse discards the acknowledge reply and begins processing the new command immediately.

NOTE

The reset wrap mode (ECh) and reset (FFh) commands are exceptions to mouse acknowledge response. The mouse does not respond with an acknowledge to either of these commands.

Resend (FEh)

The mouse replies with a resend (FEh) when it receives an invalid command from the system. Two invalid commands in succession cause the mouse to send the error code FCh to the system. The mouse ignores single invalid commands and maintains its present operational state.

8

Common Local I/O ASIC

Introduction

The DECpc 400ST Series system board uses a Common Local I/O ASIC (CLASIC) to control devices on the local I/O bus (see Figure 8-1). The CLASIC decodes the EISA address bus, generates buffer control signals, and provides chip selects for local I/O bus devices. It also conditions and steers interrupts from local I/O bus devices.

This chapter provides the following information about the CLASIC:

- Functional description
- System control port descriptions
- System control register descriptions
- Configuration register descriptions

NOTE

Default values given in this chapter are IC power-up defaults. The computer's BIOS might change these defaults based on specific hardware configurations.

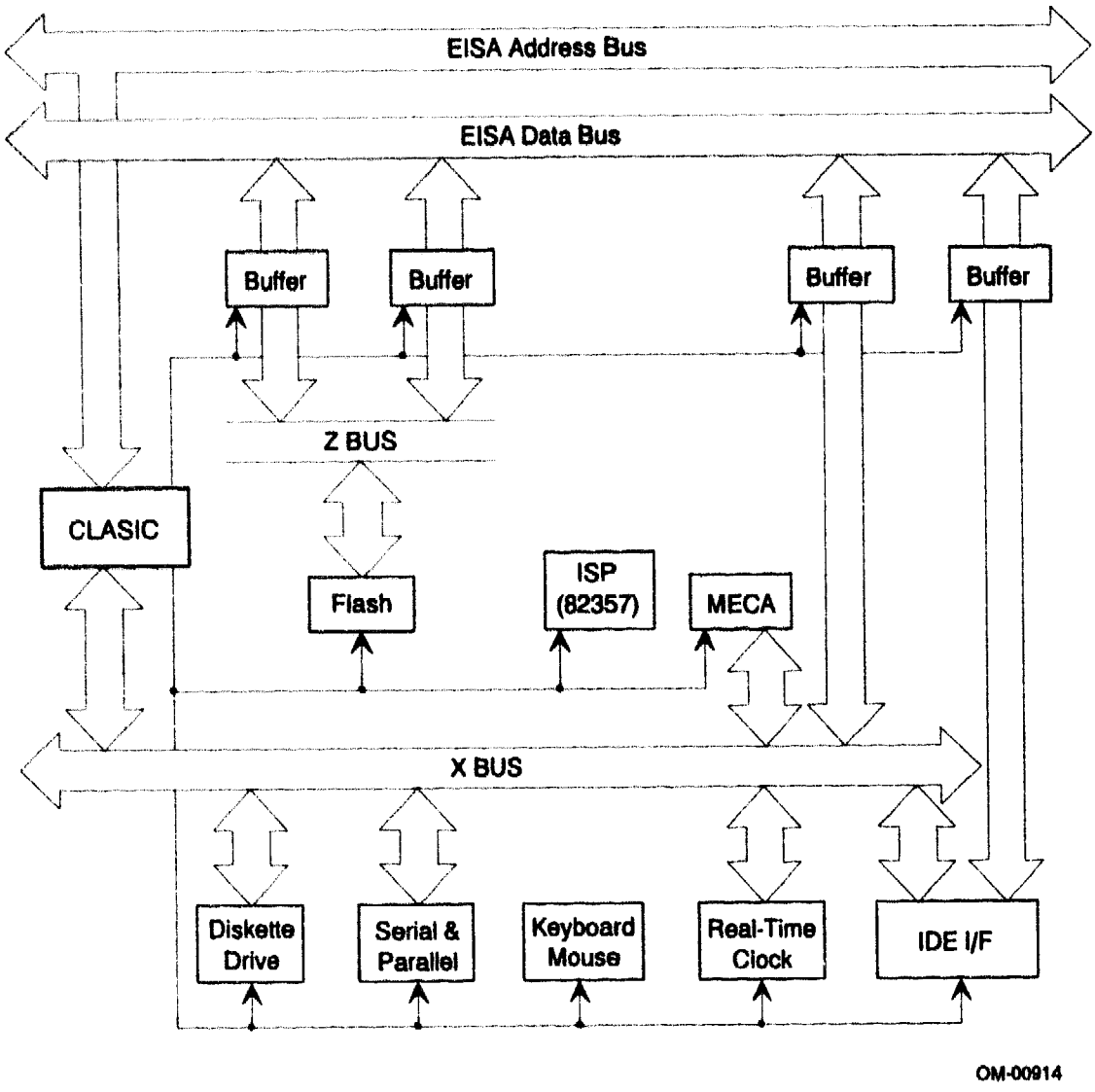


Figure 8-1. Local I/O Bus Architecture

Functional Description

The CLASIC consists of the following functional blocks (see Figure 8-2):

- Address decode
- Boundary scan test
- Buffer control
- Clock divider
- Interrupt control
- Peripheral support
- Ports and registers

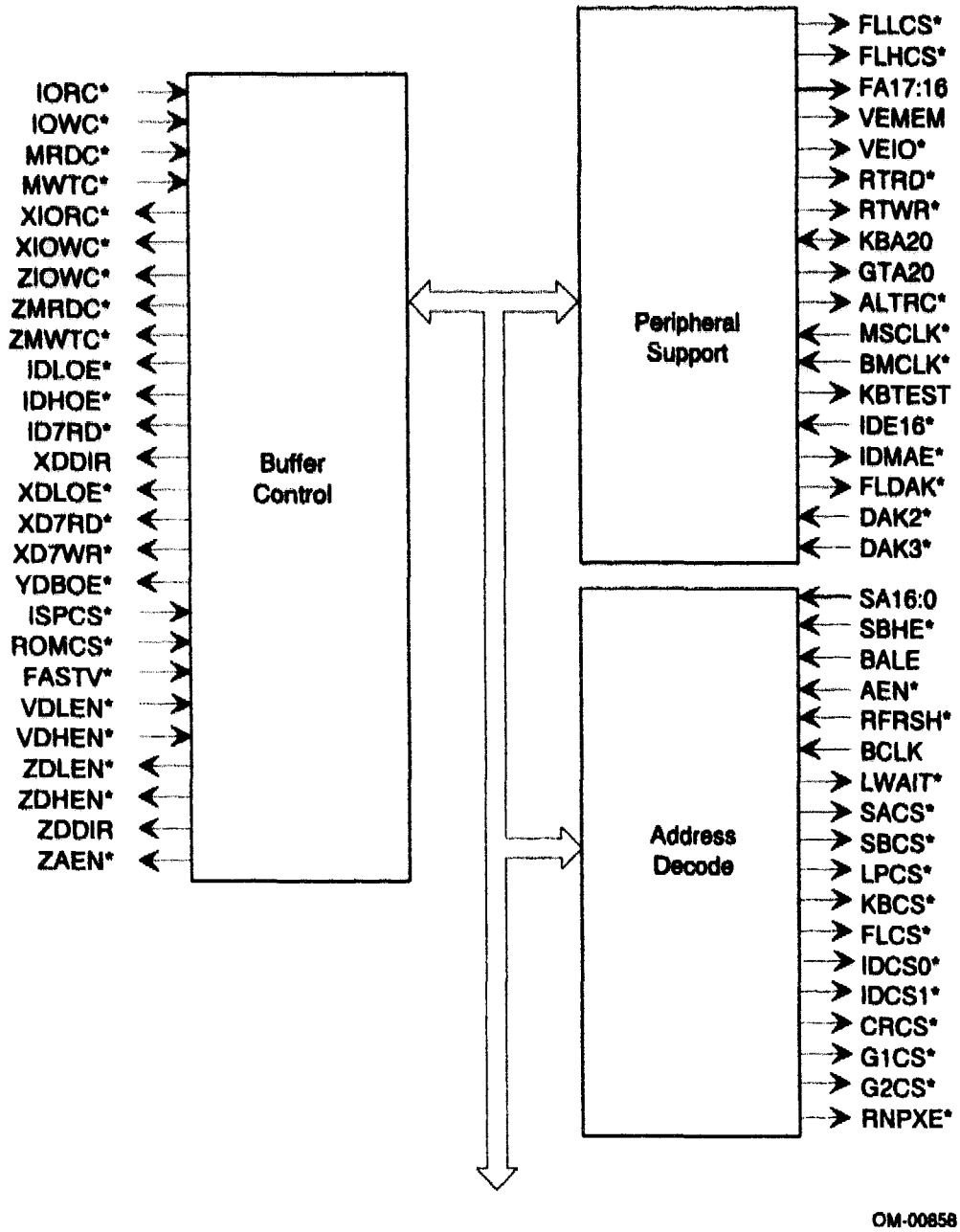


Figure 8-2. CLASIC Functional Block Diagram (Sheet 1 of 2)

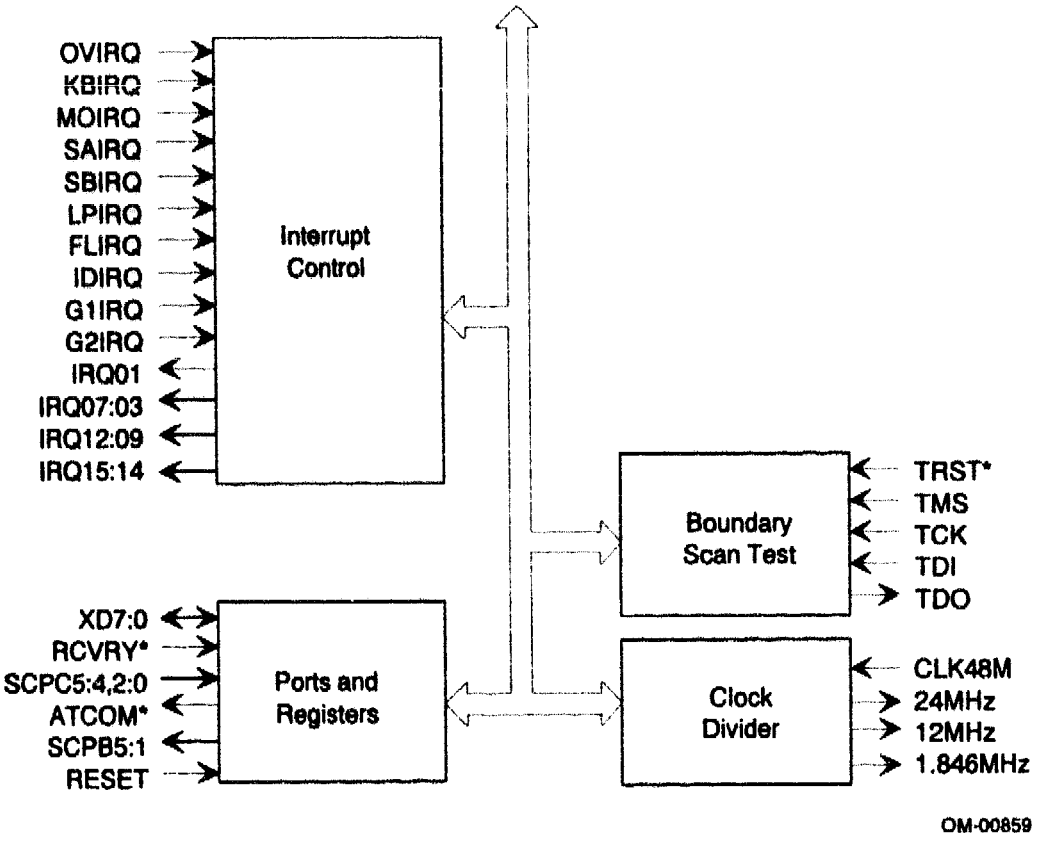


Figure 8-2. CLASIC Functional Block Diagram (Sheet 2 of 2)

Address Decode

The address decode block monitors the 16-bit system address SA15:0 for local I/O device address decodes, and generates the appropriate chip select signal. Table 8-1 lists the address map for device addresses decoded by the CLASIC.

Table 8-1. CLASIC Address Decode Map

Address (in hex)	R/W	Function
0026	R/W	Configuration Index Register
0027	R/W	Configuration Data Register
0060	R/W	Keyboard controller
0064	R/W	Keyboard controller
0070	R/W	RTC address
0071	R/W	RTC data
0078	R/W	BIOS counter port
0092	R/W	System control port A (PC/AT control port)
00F0	W	Reset numeric coprocessor error
01F0 to 01F7	R/W	IDE interface
0278 to 027B	R/W	Parallel port 2
02E8 to 02EF	R/W	Serial port 4
02F8 to 02FF	R/W	Serial port 2
0370 to 0377	R/W	Secondary diskette drive
0378 to 037B	R/W	Parallel port 1
03C0 to 03BF	R/W	Alternate parallel port 1
03E8 to 03EF	R/W	Serial port 3
03F0 to 03F5	R/W	Primary diskette drive, secondary IDE interface

Table 8-1. CLASIC Address Decode Map *(continued)*

Address (in hex)	R/W	Function
03F6	R/W	IDE
03F7 (bit 7)	R/W	Diskette controller status
03F7 (bits 6:0)	R	IDE status
03F7 (bits 1:0)	W	Diskette data rate (write)
03F8 to 03FF	R/W	Serial port 1
0C02	R/W	System control port B (generic output port)
0C03	R/W	System control port C (generic input port)
0C04	R/W	System control port D (CLASIC control port)
0C26	R/W	CLASIC alternate configuration index register
0C27	R/W	CLASIC alternate configuration data register
0C80	R	EISA ID register byte 0
0C81	R	EISA ID register byte 1
0C82	R	EISA ID register byte 2
0C83	R	EISA ID register byte 3

Boundary Scan

The boundary scan block implements the IEEE Standard 1149.1-1990 Boundary Scan test method.

Buffer Control

The buffer control block controls buffers that transfer data between the 16-bit wide Z bus or the 8-bit wide X bus and the EISA bus.

Clock Divider

The clock divider receives a 48 MHz clock input signal from the system board clock and generates 24 MHz, 12 MHz, and 18.846 MHz by dividing the input frequency by 2, 4, and 26, respectively. The 82077 diskette drive controller uses the 24 MHz clock, the 8742 keyboard/mouse controller uses the 12 MHz clock, and the WD16C552 serial/parallel controller uses the 1.846 MHz clock.

Interrupt Control

The interrupt control logic selects, enables, conditions, and steers interrupts from the local I/O devices. Its programmable configuration registers define interrupt polarity, type (edge verses level), and the system interrupt level assigned to the I/O device.

Peripheral Support

The peripheral support logic supplies special features and/or requirements for the local I/O devices. These special features include:

- FLASH memory chip selects
- Real-time clock read/write commands
- Enable for the A20 gate
- Keyboard/mouse clock signals
- I/O device data width
- Diskette drive controller DMA acknowledge

Ports and Registers

There are five system control ports and eight system control registers. Table 8-2 lists the address map of these ports and registers.

In addition, you can access 23 configuration registers through the Configuration Index Register (CIR) at I/O address 26h and the Configuration Data Register (CDR) at I/O address 27h (refer to Table 8-3).

Table 8-2. System Control Ports and Registers Address Map

Address (in hex)	Port/Register Name
0026	Configuration Index Register (CIR)
0027	Configuration Data Register (CDR)
0078	BIOS counter
0092	System control port A
0C02	System control port B
0C03	System control port C
0C04	System control port D
0C26	Configuration Index Register (CIR) — alternate address
0C27	Configuration Data Register (CDR) — alternate address
0C80	EISA ID register byte 0
0C81	EISA ID register byte 1
0C82	EISA ID register byte 2
0C83	EISA ID register byte 3

Table 8-3. CLASIC Configuration Register Indexes

Index (in hex)	Configuration Register
00	ID
01	Feature control A
02	Feature control B
03	Not used
04	Serial port 1
05	Serial port 2
06	Parallel port
07	Keyboard and mouse
08	Diskette drive
09	IDE
0A	General purpose peripheral 1
0B	General purpose peripheral 2
0C	General purpose chip 1 select mask
0D	General purpose chip 1 select low address
0E	General purpose chip 1 select high address
0F	General purpose chip 2 select mask
10	General purpose chip 2 select low address
11	General purpose chip 2 select high address
12	Shadow
13 to 1B	Reserved
1C	EISA ID byte 0
1D	EISA ID byte 1
1E	EISA ID byte 2
1F	EISA ID byte 3

System Control Port Descriptions

The system control ports are:

- BIOS counter
- System control port A
- System control port B
- System control port C
- System control port D

BIOS Counter Port

This port is for microprocessor-independent timing loops for the BIOS code. The port is an 8-bit count-down counter that runs at 2 MHz and stops counting when it reaches zero. Data writes to the port loads an eight bit count-down value. Data reads from the port return the current counter value. The counter default value is 00h.

System Control Port A

This port controls the fast A20 gate and the alternate reset signals. Refer to Table 8-4 for its bit assignments.

Table 8-4. System Control Port A Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:6		Reserved (read as 0)	
5		Reserved (read as 1)	
4:3		Reserved (read as 0)	
2		Reserved (read as 1)	
1	GTA20	Fast A20 gate enable	0 = disable (default) 1 = enable
0	ALTRC*	Alternate reset command	0 = enable (default) 1 = disable

Bits 7:2 are read only

System Control Port B

This is a general purpose output port with read-back capability. Refer to Table 8-5 for its bit assignments.

Table 8-5. System Control Port B Bit Assignments

Bit	Signal Mnemonic	Function	Description
7	HDENDRV1	High density diskette (2.88 MB) B media detection support	0 = no 1 = yes
6	HDENDRV0	High density diskette (2.88 MB) A media detection support	0 = no 1 = yes
5	SPKRENA	Speaker enable	0 = no 1 = yes
4	LCDEN	LCD power enable	0 = no 1 = yes
3	ISASLOT4	Slot 4 compatibility control	0 = ISA slot 1 = EISA slot
2	LPTOE*	Parallel port configuration	0 = PS/2 compatible 1 = AT compatible
1	COLOR*	Monitor type	0 = color 1 = monochrome
0		Not used	

System Control Port C

This port is a general purpose input port. Refer to Table 8-6 for its bit assignments.

Table 8-6. System Control Port C Bit Assignments

Bit	Signal Mnemonic	Function	Description
7:6		Reserved	
5	VID3C3	Onboard video type (if present)	0 = WD90C30 1 = WD90C11
4	KBVCC	Keyboard voltage (power available to keyboard, fuse ok)	0 = no 1 = yes
3		Reserved	
2	FLAWP	Flash write enable	0 = no 1 = yes
1	OBVIDEN*	Onboard video enable	0 = no (default) 1 = yes
0	RCVRY*	FLASH recovery mode (jumper E0191 position)	0 = recover flash (1-2) 1 = normal flash (2-3)

System Control Port D

This port controls five CLASIC features. Refer to Table 8-7 for its bit assignments.

Table 8-7. System Control Port D Bit Assignments

Bit	Description	Definition
7	ISP data bus select	0 = x bus (default) 1 = y bus
6	Keyboard controller bus select	0 = x bus (default) 1 = y bus
5	RTC bus select	0 = x bus (default) 1 = y bus
4	CLASIC and MECA bus select	0 = x bus (default) 1 = y bus
3:1	Reserved	
0	CIR and CDR address select	0 = 0026h and 0027h (default) 1 = 0C26h and 0C27h

System Control Register Descriptions

The system control registers are:

- Configuration data
- Configuration index
- ESIA ID

Configuration Data Register (CDR)

The CDR is a data gateway for the configuration register selected by the contents of the Configuration Index Register (CIR). Access all configuration registers by writing the CLASIC identification (03h) to the CLASIC ID configuration register. Program the CDR address at either 0027h (default) or 0C27h with system control port D bit zero.

Configuration Index Register (CIR)

The contents of the CIR selects any of the specific configuration registers to be accessed by the CDR through an indexing scheme. The CIR content is not valid after every CDR access and must be re-written before you can access the CDR again. Program the CIR at either address 0026h (default) or 0C26h.

EISA ID Registers

The EISA ID configuration registers initialize the four read-only EISA ID registers. The default values of these registers are 00h.

Configuration Register Descriptions

There are 23 configuration registers that maintain CLASIC configuration information. A specific offset (index) number accesses these write and read-back registers. The offset value in the CIR points to a configuration register and then is accessible through the CDR.

Because other ASICs use this indexed scheme, do not access the CLASIC configuration registers until the CLASIC identifier is written to the ID configuration register. The CLASIC identifier is 03h.

ID Register

You must write 03h to the ID register before accessing the other configuration registers. The following is an example of the configuration register indexed scheme:

```
CIR     EQU    26h
CDR     EQU    27h
MOV     AL, 00h
OUT     CIR, AL        ; Load CIR with index of ID register
MOV     AL, 03h
OUT     CDR, AL        ; Write CLASIC ID thru CDR - Select CLASIC
MOV     AL, 04h
OUT     CIR, AL        ; Load CIR with index of Serial Port 1 Reg.
MOV     AL, 07h
OUT     CDR, AL        ; Addr = 3F8-3FF, IRQ03, level, enable
MOV     AL, 05h
OUT     CIR, AL        ; Load CIR with index of Serial Port 2 Reg.
MOV     AL,  57h
OUT     CDR, AL        ; Addr = 2F8-2FF, IRQ04, level, enable
MOV     AL, 00h
OUT     CIR, AL        ; Load CIR with index of ID register
MOV     AL, 00h
OUT     CDR, AL        ; Deselect CLASIC - all done ...
```

Feature Control A Register

This register controls three CLASIC features. Refer to Table 8-8 for its bit assignments.

Table 8-8. Feature Control A Register Bit Assignments

Bit	Function	Definition
7:6	Reserved	
5	FLASH page register 1	default is 0
4	FLASH page register 0	default is 0
3	FLASH erase and write enable	0 = disable (default) 1 = enable
2:1	Reserved	
0	Fast I/O recovery	0 = disable (default) 1 = enable

Feature Control B Register

This register controls eight CLASIC features. Refer to Table 8-9 for its bit assignments.

Table 8-9. Feature Control B Register Bit Assignments

Bit	Function	Definition
7	Port 92h enable	0 = disable (default) 1 = enable
6	Port 78h enable	0 = disable (default) 1 = enable
5	Keyboard controller command interception	0 = disable (default) 1 = enable
4	Diskette drive DMA shadowing enable	0 = disable (default) 1 = enable
3	IDE interrupt control bit shadowing enable	0 = disable (default) 1 = enable
2	Parallel port interrupt bit shadowing enable	0 = disable (default) 1 = enable
1	Serial port 2 interrupt bit shadowing enable	0 = disable (default) 1 = enable
0	Serial port 1 interrupt bit shadowing enable	0 = disable (default) 1 = enable

Serial Port 1 Register

This register controls the serial communication port 1 chip select, base address assignment, interrupt assignment, and interrupt type selection. Refer to Table 8-10 for its bit assignments.

Table 8-10. Serial Port 1 Register Bit Assignments

Bit	Function	Definition
7:6	I/O address	0 0 = 03F8h to 03FFh (default) 0 1 = 02F8h to 02FFh 1 0 = 03E8h to 03EFh 1 1 = 02E8h to 02EFh
5:4	System interrupt select	0 0 = IRQ03 (default) 0 1 = IRQ04 1 0 = IRQ10 1 1 = IRQ11
3	Internally invert interrupt	0 = no (default) 1 = yes
2	Interrupt mode select	0 = level, non-sharable (default) 1 = edge, sharable
1	Interrupt enable	0 = no (default) 1 = yes
0	Port enable	0 = no (default) 1 = yes

Serial Port 2 Register

This register controls the serial communication port 2 chip select, base address assignment, interrupt assignment, and interrupt type selection. Refer Table 8-11 for its bit assignments.

Table 8-11. Serial Port 2 Configuration Register Bit Assignments

Bit	Function	Definition
7:6	I/O address	0 0 = 03F8h to 03FFh (default) 0 1 = 02F8h to 02FFh 1 0 = 03E8h to 03EFh 1 1 = 02E8h to 02EFh
5:4	System interrupt select	0 0 = IRQ03 (default) 0 1 = IRQ04 1 0 = IRQ10 1 1 = IRQ11
3	Internally invert interrupt	0 = no (default) 1 = yes
2	Interrupt mode select	0 = level, non-sharable (default) 1 = edge, sharable
1	Interrupt enable	0 = no (default) 1 = yes
0	Port enable	0 = no (default) 1 = yes

Parallel Port Register

This register controls the parallel port chip select, base address assignment, interrupt assignment, and interrupt type selection. Refer to Table 8-12 for its bit assignments.

Table 8-12. Parallel Port Register Bit Assignments

Bit	Function	Definition
7:6	I/O address	0 0 = 03BCh to 03BFh 0 1 = 0378h to 037Fh (default) 1 0 = 0278h to 027Fh 1 1 = Not used
5	Reserved	
4	System interrupt select	0 = IRQ05 1 = IRQ07 (default)
3	Internally invert interrupt	0 = no (default) 1 = yes
2	Interrupt mode select	0 = level, non-sharable (default) 1 = edge, sharable
1	Interrupt enable	0 = no (default) 1 = yes
0	Port enable	0 = no (default) 1 = yes

Keyboard and Mouse Register

This register controls the keyboard and mouse controller chip select, interrupt enable, and interrupt type selection. Refer to Table 8-13 for its bit assignments.

Table 8-13. Keyboard and Mouse Register Bit Assignments

Bit	Function	Definition
7	Internally invert mouse interrupt (IRQ12)	0 = no (default) 1 = yes
6	Mouse interrupt mode select	0 = level, non-sharable (default) 1 = edge, sharable
5	PS/2 Mouse interrupt (IRQ12) enable	0 = no (default) 1 = yes
4	Enable PS/2 mouse interface	0 = no (default) 1 = yes
3	Internally invert keyboard interrupt (IRQ1)	0 = no, non-sharable (default) 1 = yes, sharable
2	Reserved	
1	Keyboard interrupt (IRQ01) enable	0 = no (default) 1 = yes
0	Enable keyboard and mouse controller interface	0 = no (default) 1 = yes

Diskette Register

This register controls the diskette drive controller chip select, interrupt enable, and interrupt type selection. Refer to Table 8-14 for its bit assignments.

Table 8-14. Diskette Register Bit Assignments

Bit	Function	Definition
7:6	I/O address	0 0 = 03F0h to 03F5H, 03F7h (default) 0 1 = 0370h to 0375H, 0377h 1 0 = 03F2h to 03F5H, 03F7h 1 1 = 0372h to 0375H, 0377h
5:4	Reserved	
3	Internally invert interrupt	0 = no (default) 1 = yes
2	Interrupt (IRQ6) mode select	0 = level, non-sharable (default) 1 = edge, sharable
1	Enable interrupt (IRQ6)	0 = no (default) 1 = yes
0	Enable diskette drive controller interface	0 = no (default) 1 = yes

IDE Register

This register controls the onboard IDE chip select, interrupt enable, and interrupt type selection. Refer to Table 8-15 for its bit assignments.

Table 8-15. IDE Register Bit Assignments

Bit	Function	Definition
7	Enable DMA mode	0 = no (default) 1 = yes
6	I/O address	0 = 01F0h to 01F7h (default) 03F0h to 03F7h 1 = 01F0h to 01F7h 03F6h to 03F7h
5	Reserved	
4	Select interrupt	0 = IRQ14 (default) 1 = IRQ15
3	Internally invert interrupt	0 = no (default) 1 = yes
2	Select interrupt mode	0 = level, non-sharable (default) 1 = edge, sharable
1	Interrupt enable	0 = no (default) 1 = yes
0	Enable IDE interface	0 = no (default) 1 = yes

General Purpose Peripheral 1 Register

This register controls the functionality of general purpose peripheral interface 1. Refer to Table 8-16 for its bit assignments.

Table 8-16. General Purpose Peripheral 1 Register Bit Assignments

Bit	Function	Definition
7:6	Peripheral bus select	0 0 = ISA/EISA bus (default) 0 1 = X bus 1 0 = Y bus 1 1 = Z bus
5:4	Peripheral bus interrupt (G1IRQ) select	0 0 = IRQ9 (default) 0 1 = IRQ10 1 0 = IRQ11 1 1 = IRQ15
3	Internally invert interrupt	0 = no, non-sharable (default) 1 = yes, sharable
2	Interrupt mode select	0 = level (default) 1 = edge
1	Enable peripheral bus interrupt	0 = no (default) 1 = yes
0	Enable general purpose peripheral bus interface	0 = no (default) 1 = yes

General Purpose Peripheral 2 Register

This register controls the functionality of general purpose peripheral interface 2. Refer to Table 8-17 for its bit assignments.

Table 8-17. General Purpose Peripheral 2 Register Bit Assignments

Bit	Function	Definition
7:6	Bus select	0 0 = ISA/EISA bus (default) 0 1 = X bus 1 0 = Y bus 1 1 = Z bus
5:4	Interrupt (G2IRQ) select	0 0 = IRQ09 (default) 0 1 = IRQ10 1 0 = IRQ11 1 1 = IRQ15
3	Invert interrupt	0 = no (default) 1 = yes
2	Interrupt mode select	0 = level (default) 1 = edge
1	Enable interrupt	0 = no (default) 1 = yes
0	Enable general purpose peripheral 2	0 = no (default) 1 = yes

General Purpose Chip 1 and 2 Select Mask Registers

These registers futher define which general purpose chip 1 and 2 select low address registers bits are compared with SA7:0 to generate chip select signals G1CS* and G2CS*. Setting one of register bits eliminates the comparison. The default value of each register is 00h.

General Purpose Chip 1 and 2 Select Low Address Registers

These registers define the low order address bits to compare with SA7:0 to generate the general purpose chip select signals G1CS* and G2CS*. The select mask registers further define address bit comparison. The default value of each register is 00h.

General Purpose Chip 1 and 2 Select High Address Registers

These registers define the high order address bits to compare with SA15:8 to generate the general purpose chip select signals G1CS* and G2CS*. The default value of each register is 00h.

Shadow Register

This register contains shadow bit information. Read this register to sample the current shadow bit settings or write to this register to force the shadow control bits to known states. Refer to Table 8-18 for its bit assignments.

Table 8-18. Shadow Register Bit Assignments

Bit	Default	Description
7	0	Reserved
6	0	Shadow of the IDE device control register bit one
5	0	Shadow of the diskette digital output register bit three
4	0	Shadow of the parallel printer port control register bit four
3:2	0:0	Shadow of the serial communication port 2 modem control register bits 4:3
1:0	0:0	Shadow of the serial communication port 1 modem control register bits 4:3

EISA ID Configuration Registers

These four registers initialize the contents of the EISA ID registers. Values written to these registers pass on to the read-only EISA System ID registers located at I/O address 0C83 to 0C80h. The default value of each register is 00h. The DECpc 400ST Series system ID is DEC1101.

9

MEM Bus-To-EISA Control Array

Introduction

The DECpc 400ST Series system board uses a MEM bus-to-EISA Control Array ASIC (MECA). The MECA contains control logic that connects the EISA bus to the MEM bus (see Figure 9-1), and provides control for concurrent refresh cycles, posted cycles, and MEM bus arbitration.

NOTE

Default values given in this chapter are IC power-up defaults. The computer's BIOS might change these defaults based on specific hardware configurations.

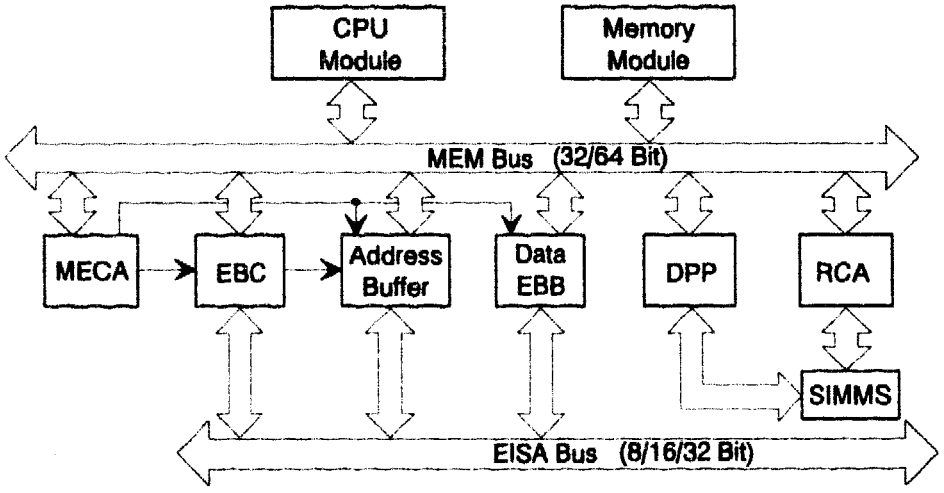


Figure 9-1. MECA/System Interface

Functional Description

The MECA consists of the following functional blocks (see Figure 9-2):

- Boundary scan test
- EISA/MEM bus control
- EISA snoop
- Memory decode
- Ports and registers
- Reset and configuration
- System arbitrator

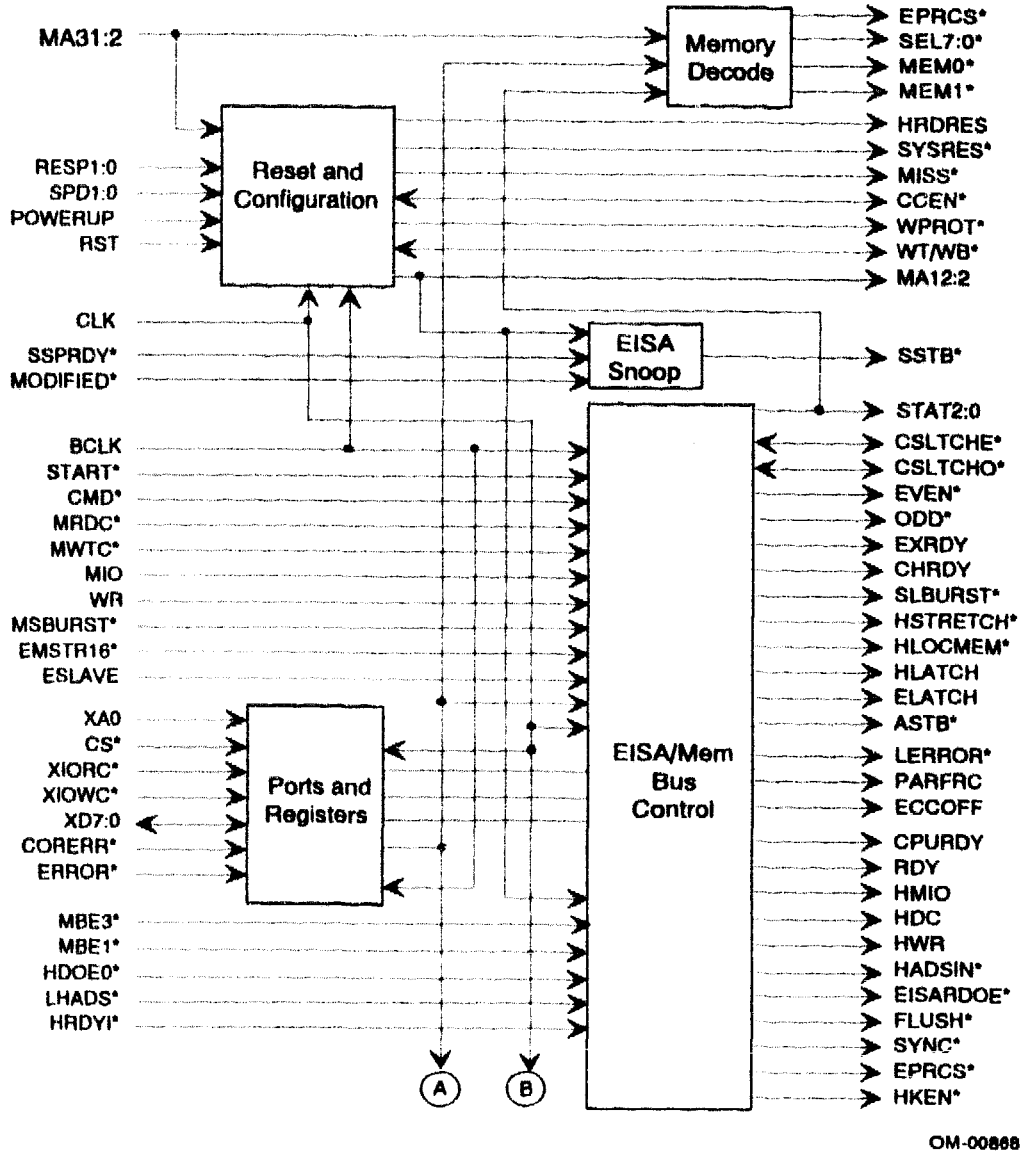


Figure 9-2. MECA Block Diagram (Sheet 1 of 2)

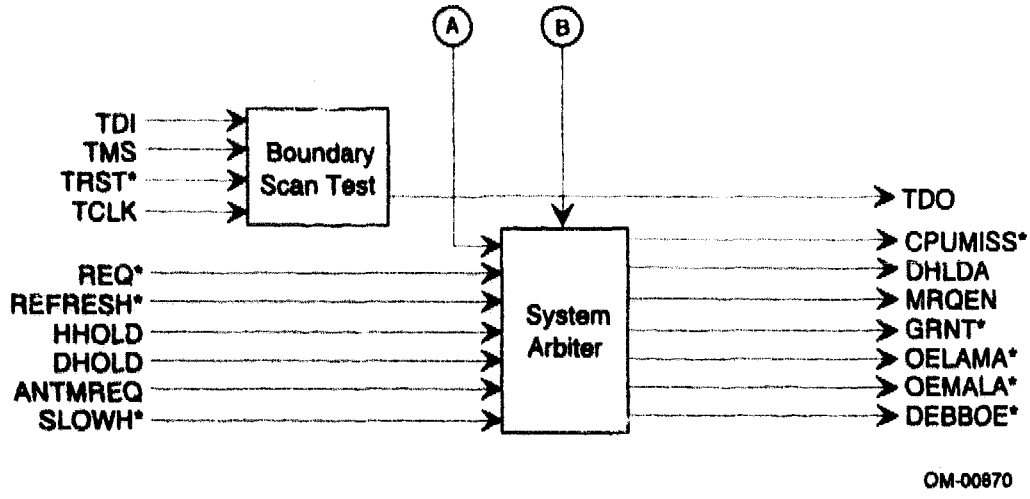


Figure 9-2. MECA Block Diagram (Sheet 2 of 2)

Boundary Scan Test

The boundary scan block implements a subset of the IEEE Std. 1149.1-1990 Boundary Scan test method. The test method is limited to those tests that do not require control of data values on the boundary scan test block output pins.

EISA/MEM Bus Control

The EISA/MEM bus control block contains state machines that provide protocol and timing for memory transfers across the MEM bus for EISA bus masters and the ISP. In addition, it provides cycle control signals for the MEM bus interface and tri-state and latch control during bus exchanges and write-back operations.

Memory Decode

The memory decode block monitors MEM bus address lines MA31:2, memory decode and control register settings, and BIOS shadow control register settings. It outputs memory partition selects and memory drive signals that enable specific memory range accesses.

Ports and Registers

There are two MECA I/O ports and 60 configuration registers. The CLASIC decodes the address range 26h and 27h or C26h and C27h and provides MECA with chip select signals when these I/O addresses are accessed. Table 9-1 lists the address map of the I/O ports. Access the configuration registers through the Configuration Index Register (CIR) and the Configuration Data Register (CDR). The CIR contains an offset (index) to the register being addressed and the CDR contains the register data. Table 9-2 lists the configuration register indexes.

Table 9-1. MECA I/O Ports Address Map

Address (in hex)	I/O Port Name
0026	CIR
0027	CDR

Table 9-2. MECA Configuration Register Indexes

Index (in hex)	Configuration Register
00	ID
01	Memory attribute 1 (0000 0000h to 0003 FFFFh), 256 KB
02	Memory attribute 2 (0004 0000h to 0007 FFFFh), 256 KB
03	Memory attribute 3 (0008 0000h to 0008 7FFFh), 64 KB
04	Memory attribute 4 (0009 0000h to 0009 7FFFh), 32 KB
05	Memory attribute 5 (0009 8000h to 0009 FFFFh), 32 KB
06	Memory attribute 6 (000A 0000h to 000B FFFFh), 128 KB
07	Memory attribute 7 (000C 0000h to 000C 7FFFh), 32 KB
08	Memory attribute 8 (000C 8000h to 000C FFFFh), 32 KB
09	Memory attribute 9 (000D 0000h to 000D 7FFFh), 32 KB
0A	Memory attribute 10 (000D 8000h to 000D FFFFh), 32 KB
0B	Memory attribute 11 (000E 0000h to 000E 7FFFh), 32 KB
0C	Memory attribute 12 (000E 8000h to 000E FFFFh), 32 KB
0D	Memory attribute 13 (000F 0000h to 000F FFFFh), 64 KB
0E	Memory attribute 14 (programmable range)
0F	Memory attribute 15 (programmable range)
10	Memory attribute 16 (programmable range)
11	Memory attribute 17 (programmable range)
12	Memory attribute range 14, lower limit address (MA27:20)
13	Memory attribute range 14, lower limit address (MA28)
14	Memory attribute range 14, upper limit address (MA27:20)
15	Memory attribute range 14, upper limit address (MA28)

Table 9-2. MECA Configuration Register Indexes *(continued)*

Index (in hex)	Configuration Register
16	Memory attribute range 15, lower limit address (MA27:20)
17	Memory attribute range 15, lower limit address (MA28)
18	Memory attribute range 15, upper limit address (MA27:20)
19	Memory attribute range 15, upper limit address (MA28)
1A	Memory attribute range 16, lower limit address (MA27:20)
1B	Memory attribute range 16, lower limit address (MA28)
1C	Memory attribute range 16,upper limit address (MA27:20)
1D	Memory attribute range 16, (upper limit address MA28)
1E	Memory attribute range 17, lower limit address (MA27:20)
1F	Memory attribute range 17, lower limit address (MA28)
20	Memory attribute range 17, upper limit address (MA27:20)
21	Memory attribute range 17, upper limit address (MA28)
22	BIOS shadow control
23	Memory decode and control
24	Memory error control
25	Memory error address, LSB (MA19:12)
26	Memory error address, middle byte (MA27:20)
27	Memory error address, MSB (MA31:28)
28	Memory partition disable
29	CPU module speed
2A	CPU module ID
2B	Memory partition 0 configuration
2C	Memory partition 1 configuration

Table 9-2. MECA Configuration Register Indexes *(continued)*

Index (in hex)	Configuration Register
2D	Memory partition 2 configuration
2E	Memory partition 3 configuration
2F	Memory partition 4 configuration
30	Memory partition 5 configuration
31	Memory partition 6 configuration
32	Memory partition 7 configuration
33	Memory partition boundary 0, (MA28:21)
34	Memory partition boundary 1, (MA28:21)
35	Memory partition boundary 2, (MA28:21)
36	Memory partition boundary 3, (MA28:21)
37	Memory partition boundary 4, (MA28:21)
38	Memory partition boundary 5, (MA28:21)
39	Memory partition boundary 6, (MA28:21)
3A	Memory partition boundary 7, (MA28:21)
3B	General control

Reset and Configuration

The reset and configuration block generates reset signals and configuration signals. Reset signals are output to the MEM bus and the system board in response to power-up, front panel reset, and keyboard reset. Configuration signals configure the boundary scan test block and determine the system memory map and its attributes.

System Arbitrator

The system arbitrator block provides the arbitration protocol between the CPU module and EISA/ISA bus masters. This protocol also permits concurrent accesses for EISA bus refresh cycles.

Register Descriptions

There are 60 configuration registers that maintain MECA configuration information. These registers are write and read-back registers that are accessed by an offset (index). The CIR holds the configuration register index. Access to the configuration register is through the CDR.

Because other ASICs use this indexed scheme, the MECA configuration registers can not be accessed until the MECA identification is written to the ID configuration register. The MECA identification is 05h.

ID Register

The ID register must be written with 05h before you can access other configuration registers. The following is an example of the configuration register indexed scheme:

```
OUT     26h, 00h      ; Load CIR with index of ID register
OUT     27h, 05h      ; Write MECA ID thru CDR - Select MECA
OUT     26h, 01h      ; Select memory attribute 1 register
OUT     27h, 05h      ; Write to memory attribute 1 register
OUT     26h, 00h      ;Load CIR with index of ID register
OUT     27h, 00h      ; Deselect MECA by writing wrong ID
```

Memory Attribute Registers

The 17 memory attribute registers control the system memory map attributes for the 13 fixed memory ranges and the four user programmable memory ranges. The three system memory map attributes are: write protect, cacheability, cache type (write-back or write-thru). Refer to Table 9-3 for its bit assignments. However, some system memory map attributes are not valid in all address range. Table 9-4 lists the system memory map attribute programmability for each memory address range.

Table 9-3. Memory Attribute Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7:3		Not used	
2	WPROT	Write protect	0 = no (default) 1 = yes
1	CCEN	Cacheable	0 = no (default) 1 = yes
0	WB/WT*	Write back/write thru	0 = write thru 1 = write back (default)

Table 9-4. Memory Attribute Programmability

Range (in hex)	Cache-able	Write Protect	Write back/thru	Shadow	Notes
Programmable ranges (000F 0000 to 0FFF FFFF)	Yes	Yes	Yes	No	Memory between 640 KB to 768 KB and 928 KB to 960 KB should not be programmed.
000F 0000 to 000F FFFF	Yes	Yes	Yes	Yes	
000E 8000 to 000E FFFF	No	No	No	No	Can not shadow this range
000E 0000 to 000E 7FFF (version 1.1 only)	Yes	Yes	Yes	Yes	Write protected only if shadowed
000E 0000 to 000E 7FFF	No	No	Yes	Yes	Programmable if shadowed
000D 8000 to 000D FFFF	No	No	No	No	
000D 0000 to 000D 7FFF	No	No	No	No	
000C 8000 to 000C FFFF (version 1.1 only)	Yes	Yes	Yes	Yes	Write protected only if shadowed
000C 8000 to 000C FFFF	No	No	No	Yes	
000C 0000 to 000C 7FFF	Yes	Yes	Yes	Yes	Programmable if shadowed

Table 9-4. Memory Attribute Programmability *(continued)*

Range (in hex)	Cache-able	Write Protect	Write back/thru	Shadow	Notes
000A 0000 to 000B FFFF	No	No	No	No	
0009 8000 to 0009 FFFF	Yes	Yes	Yes	No	If enabled, use write-thru; write protect has no effect.
0009 0000 to 0009 7FFF	Yes	Yes	Yes	No	If enabled, use write-thru; write protect has no effect.
0008 0000 to 0008 7FFF	Yes	Yes	Yes	No	If enabled, use write-thru; write protect has no effect.
0004 0000 to 0007 FFFF	Yes	Yes	Yes	No	
0000 0000 to 0003 FFFF	Yes	Yes	Yes	No	

Memory Attribute Range Registers

The 16 memory attribute range registers set the upper and lower addressing limits of four user programmable range memory attribute registers. The range defined includes all memory locations greater than or equal to the lower limit address and less than or equal to the upper limit address. Default value for each register is 00h. Refer to Table 9-5 for lower limit address register bit assignments and Table 9-6 for upper limit address register bit assignments.

Table 9-5. Memory Range Lower Limit Register Bit Assignments

Bit	Signal Mnemonic	Definition
7	RA27	0 = match when MA27 = 0 1 = match when MA27 = 1
6	RA26	0 = match when MA26 = 0 1 = match when MA26 = 1
5	RA25	0 = match when MA25 = 0 1 = match when MA25 = 1
4	RA24	0 = match when MA24 = 0 1 = match when MA24 = 1
3	RA23	0 = match when MA23 = 0 1 = match when MA23 = 1
2	RA22	0 = match when MA22 = 0 1 = match when MA22 = 1
1	RA21	0 = match when MA21 = 0 1 = match when MA21 = 1
0	RA20	0 = match when MA20 = 0 1 = match when MA20 = 1

Table 9-6. Memory Range Upper Limit Register Bit Assignments

Bit	Signal Mnemonic	Definition
7:1	Not used	
0	RA28	0 = match when MA28 = 0 1 = match when MA28 = 1

BIOS Shadow Control Register

This register controls shadowing for the system BIOS, the video BIOS, memory address range C800h to CFFFh, and memory address range E000h to E7FFh. It also contains the ASIC version bit and the COPYUP bit that directs read and write accesses when regions of memory are shadowed. When COPYUP is disabled and a region is shadowed, all read access to the region are from the MEM bus and all writes go to the EISA bus. When COPYUP is enabled and the region is shadowed, all read accesses to the region are from the EISA bus and all writes are to the MEM bus. COPYUP has no effect on a region when it is not shadowed. Refer to Table 9-7 for its bit assignments.

Table 9-7. BIOS Shadow Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7	Version	Version Control Bit (hardwired)	0 = Version 1.0 1 = Version 1.1
6	REMAP	On-board video BIOS location	0 = 0E000h to 0E7FFh (default) 1 = 0C000h to 0C7FFh
5	DIS_OBVB	Disable on-board video	0 = yes (default) 1 = no
4	E0_SHDW	Shadow 0E000h to 0E7FFh	0 = no (default) 1 = yes (1)
3	C8_SHDW	Shadow 0C800h to 0CFFF	0 = no (default) 1 = yes
2	COPYUP	Copyup enable	0 = no (default) 1 = yes, if one or more shadow bits are set
1	VBSHDW	Shadow video BIOS (0C000h to 0C7FFh)	0 = no (default) 1 = yes
0	SBSHDW	Shadow system BIOS (0F000h to 0FFFFh)	0 = no 1 = yes (default) (2)

(1) If REMAP = 0 and DIS_OBVB =0, then SHSHDW also determines whether shadowing is enabled.
(2) If REMAP = 0 and DIS_OBVB =0, then SBSHDW also determines shadowing in the range 0E000h to 0E7FFh.

Memory Decode and Control Register

This register controls CPU module cache operations and configures the system memory map. Refer to Table 9-8 for its bit assignments.

Table 9-8. Memory Decode and Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7	EPROM16M	EPROM just below 16MB	0 = no 1 = yes (default)
6	LINE32	CPU cache module line size	0 = 16 bytes (default) 1 = 32 bytes
5	FLUSHEN	Flush cache	0 = no (default) 1 = yes
4	EN640K	Enable system memory between 512 KB and 640 KB	0 = no 1 = yes (default)
3	WB_OFF	Cache write-back mode	0 = as specified by memory attribute registers 1 = disable (default)
2	FASTSNP	Snoop cycle support	0 = asynchronous (default) 1 = fast (deterministic)
1	SYNCEN	Synchronize cache	0 = no (default) 1 = yes
0	CACHE_OFF	Cache enable	0 = as specified by memory attribute registers 1 = no (default)

Memory Error Control Register

This register configures and controls memory module error detection and reporting logic. Refer to Table 9-9 for its bit assignments.

Table 9-9. Memory Error Control Register

Bit	Signal Mnemonic	Function	Definition
7	ERR_CLR	Clear bits 0 and 2 of this register	0 = no (default) 1 = yes
6		Not used	
5	ECC_DIAG	ECC memory diagnostic	For ECC, bits 5:4 define: 0 0 = enable (default) 0 1 = force single error 1 0 = disable 1 1 = force double error
4	PAR_FRC	Force parity memory error	0 = no (default) 1 = yes
3		Not used	
2	L_CORRECT	Corrected memory error	0 = no error (default) 1 = error
1	ECCPRES	ECC installed	0 = no (default) 1 = yes
0	L_ERROR	Uncorrected memory error	0 = no (default) 1 = yes

Memory Error Address Registers

The three memory error address registers hold the memory page address each time an uncorrectable memory error occurrs. This address is latched until cleared. Refer to Tables 9-10 through 9-12 for their bit assignments. The default value for each register is 00h.

Table 9-10. Memory Error Address LSB Register Bit Assignments

Bit	Signal Mnemonic	Function
7	MA19	MA19 state when error occurred
6	MA18	MA18 state when error occurred
5	MA17	MA17 state when error occurred
4	MA16	MA16 state when error occurred
3	MA15	MA15 state when error occurred
2	MA14	MA14 state when error occurred
1	MA13	MA13 state when error occurred
0	MA12	MA12 state when error occurred

Table 9-11. Memory Error Address Middle Byte Register Bit Assignments

Bit	Signal Mnemonic	Function
7	MA11	MA11 state when error occurred
6	MA10	MA10 state when error occurred
5	MA9	MA9 state when error occurred
4	MA8	MA8 state when error occurred
3	MA7	MA7 state when error occurred
2	MA6	MA6 state when error occurred
1	MA5	MA6 state when error occurred
0	MA4	MA4 state when error occurred

Table 9-12. Memory Error Address MSB Register Bit Assignments

Bit	Signal Mnemonic	Function
7	CPU_REL	0 = CPU is bus master (default) 1 = CPU not bus master
6-4		Not used
3	MA31	MA31 state when error occurred
2	MA30	MA30 state when error occurred
1	MA29	MA29 state when error occurred
0	MA28	MA28 state when error occurred

Memory Partition Disable Register

This register disables memory partitions. Refer to Table 9-13 for its bit assignments.

Table 9-13. Memory Partition Disable Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7	MEMDIS7	Disable partition 7	0 = no (default) 1 = yes
6	MEMDIS7	Disable partition 6	0 = no (default) 1 = yes
5	MEMDIS5	Disable partition 5	0 = no (default) 1 = yes
4	MEMDIS4	Disable partition 4	0 = no (default) 1 = yes
3		Not used	
2		Not used	
1	MEMDIS1	Disable partition 1	0 = no (default) 1 = yes
0	MEMDIS0	Disable partition 0	0 = no (default) 1 = yes

CPU Speed Register

This register is read only and contains the CPU operating frequency in hexadecimal. Its default value is 00h. Refer to Table 9-14 for its bit assignments.

Table 9-14. CPU Speed Register Bit Assignments

Bit	Signal Mnemonic	Bus Signal Mnemonic	Definition
7	SPD7	RESP1*	MSB
6	SPD6	RESP0*	Speed bit 6
5	SPD5	SPD1*	Speed bit 5
4	SPD4	SPD0*	Speed bit 4
3	SPD3	RESP1	Speed bit 3
2	SPD2	RESP0*	Speed bit 2
1	SPD1	SPD1*	Speed bit 1
0	SPD0	SPD0*	LSB

CPU Module ID Register

This register is read only and contains CPU module information. Refer to Table 9-15 for its bit assignments.

Table 9-15. CPU Module ID Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7:5	MODID7:5	CPU 1 secondary cache size	0 0 0 = reserved 0 0 1 = 512 KB 0 1 0 = 256 KB 0 1 1 = 128 KB 1 0 0 = 64 KB 1 0 1 = 32 KB 1 1 0 = 16 KB 1 1 1 = none (default)
4	MODID4	CPU 1 coprocessor present	0 = no (default) 1 = yes
3	MODID3	CPU 2 microprocessor present	0 = no (default) 1 = yes
2	MODID2	CPU 2 coprocessor present	0 = no (default) 1 = yes
1:0	MODIC1:0	CPU 2 secondary cache size	0 0 = 512 KB 0 1 = 256 KB 1 0 = 128 KB 1 1 = none

Memory Partition Configuration Registers

These read-only registers contain memory partition size. There is one register for each possible memory partition. Note that memory partition configuration registers for partitions 2 and 3 are not used. Refer to Table 9-16 for its bit assignments.

Table 9-16. Memory Partition Configuration Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7:4		Reserved	
3:0	MSIZE3:0	Partition size	0 0 0 0 = no memory 0 0 0 1 = 2 MB 0 0 1 0 = 4 MB 0 0 1 1 = 8 MB 0 1 0 0 = 16 MB 0 1 0 1 = 32 MB 0 1 1 0 = 64 MB 0 1 1 1 = 128 MB 1 x x x = reserved

Memory Partition Boundary Registers

There are eight memory partition boundary registers, one for each partition. Each register is read-only and is programmed during a hard reset. Note that memory partition boundary registers for partitions 2 and 3 are not used. Each register contains an 8-bit value that is compared with memory addresses MA28:21 to determine if the partition should be selected. Refer to Table 9-17 for its bit assignments.

Table 9-17. Memory Partition Boundary Register Bit Assignments

Bit	Signal Mnemonic	Definition
7	PA28	0 = match when MA28 = 0 1 = match when MA28 = 1
6	PA27	0 = match when MA27 = 0 1 = match when MA27 = 1
5	PA26	0 = match when MA26 = 0 1 = match when MA26 = 1
4	PA25	0 = match when MA25 = 0 1 = match when MA25 = 1
3	PA24	0 = match when MA24 = 0 1 = match when MA24 = 1
2	PA23	0 = match when MA23 = 0 1 = match when MA23 = 1
1	PA22	0 = match when MA22 = 0 1 = match when MA22 = 1
0	PA21	0 = match when MA21 = 0 1 = match when MA21 = 1

General Control Register

This register is used for factory testing and to issue a software initiated hard reset. Bit 5 is reserved in version 1.0. In Version 1.1 D_CHRDY will be deasserted for all memory accesses to an ISA slave by an EISA or DMA master and will remain deasserted until the CPU module has finished it snooping of the current cache line. Refer to Table 9-18 for its bit assignments.

Table 9-18. General Control Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7	COMPAT1	Posted writes enable	0 = yes 1 = no (default)
6	COMPAT0	Concurrent refresh enable	0 = yes 1 = no (default)
5	D_CHRDY	EISA channel ready deassertion enable	0 = yes (default) 1 = no (Version 1.0 mode)
4		Reserved	
3	INHIBITEN	Time for other bus masters to wait before taking control of the bus	0 = immediate (default) 1 = wait 16 BCLK (2 ms)
2	HSTR_EN	HSTRETCH logic enable	0 = no (default) 1 = yes
1	TST_EN	Special test mode enable (read-only register can be written)	0 = no (default) 1 = yes
0	HRD_RST	Generate hard reset	0 = no (default) 1 = yes

10

DPP, EBB, and RCA

Introduction

This chapter describes the data path parity (DPP), 82352 EISA Bus Buffer (EBB), and RAS, CAS Address (RCA) ASIC used by a DECpc 400ST Series system board.

The DPP ASIC provides the interface between the MEM bus and the memory array. Included in the interface are bidirectional latching transceivers, data multiplexing, parity generation, and parity checking. Each DPP supports 16-bits of MEM bus data and 32-bits of memory array data.

The EBB provides data latching and buffering between the MEM bus and the EISA bus. It operates in mode zero

The RCA ASIC contains logic for generating DRAM control signals. These signals include column address strobe (CAS), row address strobe (RAS), write enable (WE), multiplexing for the DRAM address, and MEM bus response signals. The RCA also generates control signals that activate RAS for double sided SIMMs, control local byte enable signals, and multiplex size and speed information onto the MEM bus during reset and initialization.

DPP Functional Description

The DPP consists of the following blocks (see Figure 10-1):

- Bus latches
- Multiplexer/demultiplexer
- Parity generation and checking

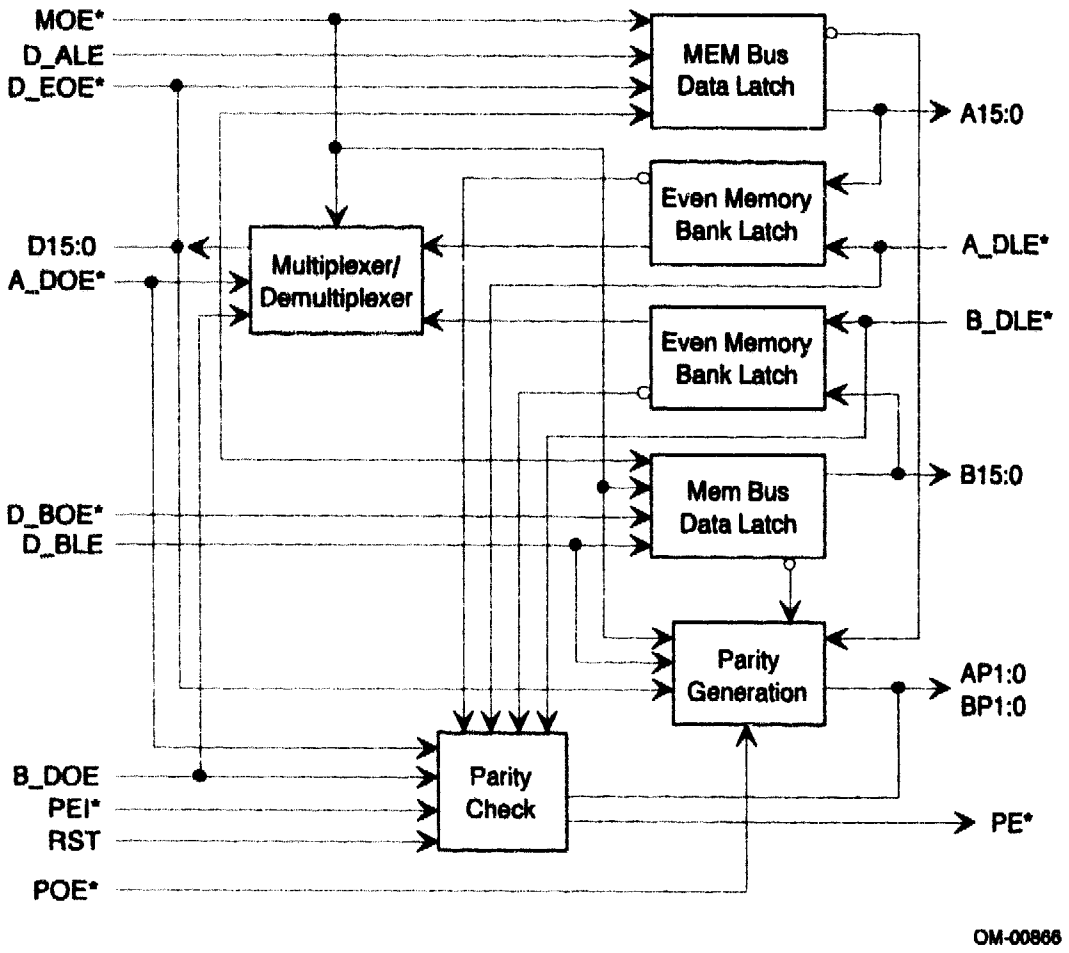


Figure 10-1. DPP Block Diagram

Bus Latches

This block allows bidirectional data transfers and latching between the MEM bus and the memory array.

Multiplexer/Demultiplexer

This block multiplexes and demultiplexes MEM bus data.

Parity Generation and Checking

These blocks generate even parity for data transfers from the MEM bus to the memory array. They also compare parity during data transfers from the memory array to MEM bus.

EBB Functional Description

Figure 10-2 shows the EBB inputs and outputs.

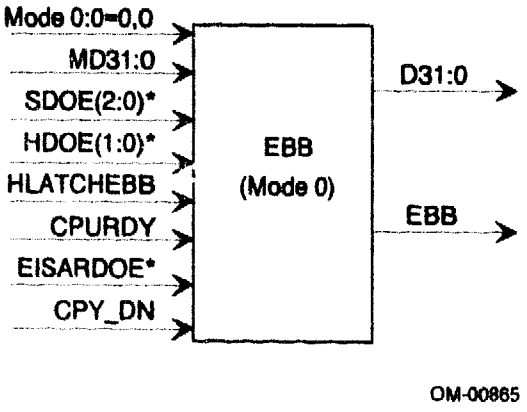


Figure 10-2. EBB Block Diagram

RCA Functional Description

The RCA consists of the following functional blocks (see Figure 10-3):

- Address multiplexer and latch
- CAS generation
- Double detect
- RAS generation
- Response generation

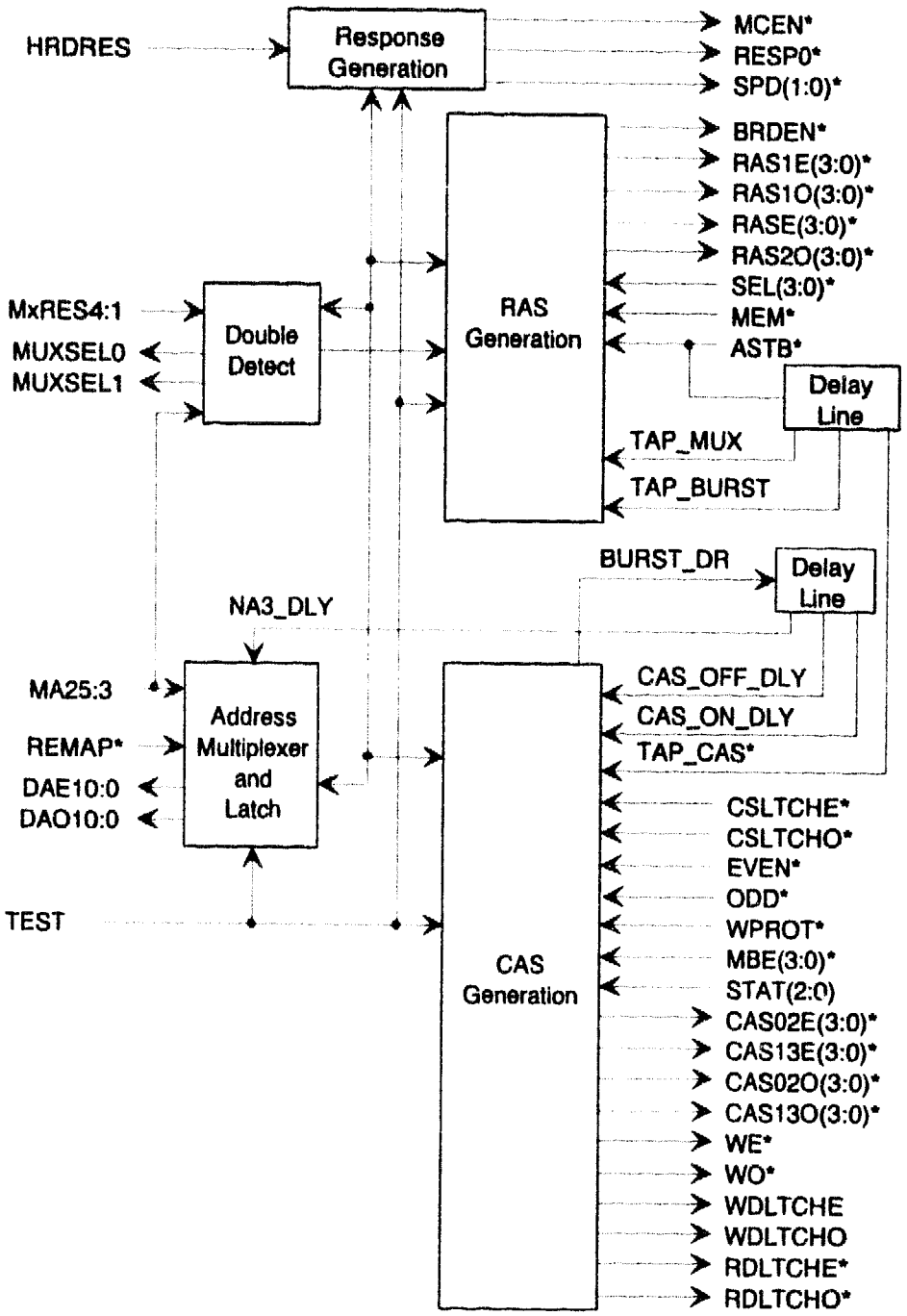


Figure 10-3. RCA Block Diagram

Address Multiplexer and Latch

This block multiplexes row addresses and column addresses into the memory array. It also latches column addresses.

CAS Generation

This block generates CAS and WE signals to the memory array. It also generates control signals for the external transceivers.

Double Detect

This block detects the presence of single-sided and double-sided SIMMs by decoding address lines MA25, MA23, MA21 and SIMM presence bits RESP3:2.

RAS Generation

This block generates RAS signals to the memory array and provides timing strobes for the different memory cycles. Different memory cycles result because the system board is not restricted to a particular memory array.

Response Generation

This block provides memory array information to the CPU module via the MEM bus. This information includes memory size and speed.

11

DS1287 Real-Time Clock

Introduction

The DECpc 400ST Series system board uses a Dallas DS1287 Real-Time Clock (RTC) to provide battery-backed, nonvolatile RAM (NVRAM) for storing system configuration parameters and a time-of-day clock. NVRAM is powered by an integral lithium battery that lasts approximately ten years. The battery is not rechargeable and must be replaced when it fails.

RTC I/O Operations

Values can be written to or read from all 64 bytes except:

- Status registers C and D
- Status register A bit 7
- Seconds byte bit 7

To write data to the RTC, write the RTC RAM address to I/O port 70h then write the data byte to I/O port 71h.

To read data from the RTC, write the RTC RAM address to I/O port 70h then read the data at I/O port 71h.

The RTC contains a time-of-day clock with alarm, a 100-year calendar, a programmable periodic interrupt, and 64 bytes of RAM (including the dedicated bytes used for clock functions). Table 11-1 lists the RTC address map. Tables 11-2 through 11-20 list the bits for the registers in the address map.

Table 11-1. RTC Address Map

Address (in hex)	Function	Range	Default
0	Seconds (time)	59 to 0	-
1	Seconds (alarm)	59 to 0	-
2	Minutes (time)	59 to 0	-
3	Minutes (alarm)	59 to 0	-
4	Hours (time)	12 to 1 (12 hour mode)	-
4	Hours (time)	23 to 0 (24 hour mode)	-
5	Hours (alarm)	23 to 0	-
6	Day of week	7 to 1	-
7	Date of month	31 to 1	-
8	Month	12 to 1	-
9	Year	99 to 0	-
0A	Status register A	Read/write	-
0B	Status register B	Read/write	-
0C	Status register C	Read only	-
0D	Status register D	Read only	-
0E	Diagnostic status	Read/write	-
0F	Reason for shutdown	Read/write	-
10	Type of diskette	Read/write	40h
11	Reserved		-
12	Type of hard disk	Read/write	00h
13	Language	Read/write	00h
14	Installed hardware	Read/write	03h
15	Low byte of base memory in KB	Read/write	80h

Table 11-1. RTC Address Map *(continued)*

Address (in hex)	Function	Range	Default
16	High byte of base memory in KB	Read/write	02h
17	Low byte of extended memory in KB	Read/write	00h
18	High byte of extended memory in KB	Read/write	00h
19	Drive C extended byte	Read/write	00h
1A	Drive D extended byte	Read/write	00h
1B	Reserved	Read/write	
1C	Shadow control byte	Read/write	00h
1E:1D	Reserved	Read/write	
1F	BIOS options	Read/write	07h
20	Manufacturer option 1	Read/write	3Eh
21	Manufacturer option 2	Read/write	00h
22	Manufacturer option 3	Read/write	00h
23	Manufacturer option 4	Read/write	20h
24	Manufacturer option 5	Read/write	1Ch
27:25	Reserved		
28	Low byte of extended memory in KB	Read/write	00h
29	Mid byte of extended memory in KB	Read/write	00h
2A	High byte of extended memory in KB	Read/write	00h
2B	Low byte of actual memory in KB	Read/write	00h

Table 11-1. RTC Address Map (*continued*)

Address (in hex)	Function	Range	Default
2C	Mid byte of actual memory in KB	Read/write	00h
2D	High byte of actual memory in KB	Read/write	00h
2E	High byte of CMOS RAM checksum for 10h to 2Dh	Read/write	00h
2F	Low byte of CMOS RAM checksum for 10h to 2Dh	Read/write	00h
30	Low byte of extended memory in KB	Read/write	00h
31	High byte of extended memory in KB	Read/write	00h
32	Century-BCD byte	Read/write	19h
33	Setup information	Read/write	00h
34	CPU Speed, cache, and extended CMOS control	Read/write	09h
3F:35	Reserved		

Status Register A Bit Assignments

This register contains an RTC update in process, the time-based frequency divider, and rate selection information. Refer to Table 11-2 for its bit assignments.

Table 11-2. Status Register A Bit Assignments

Bit	Function	Description
7	Update in progress	0 = no 1 = yes
6:4	Time-based frequency divider	
3:0	Rate selection for output frequency and periodic interrupt rates	

Status Register B Bit Assignments

This register contains RTC halted, interrupt enable, calendar format, and time format information. Refer to Table 11-3 for its bit assignments.

Table 11-3. Status Register B Bit Assignments

Bit	Function	Description
7	Halted	0 = no 1 = yes
6	Periodic interrupt enabled	0 = no 1 = yes
5	Alarm interrupt enabled	0 = no 1 = yes
4	Update ended interrupt enabled	0 = no 1 = yes
3	Square wave interrupt enabled	0 = no 1 = yes
2	Calendar format	0 = BCD 1 = Binary
1	Time format	0 = 12 hour mode 1 = 24 hour mode
0	Daylight saving enabled	0 = no 1 = yes

Status Register C Bit Assignments

This register hold four interrupt flags. Refer to Table 11-4 for its bit assignments.

Table 11-4. Status Register C Bit Assignments

Bit	Function	Description
7	IRQR flag	0 = no 1 = yes
6	Periodic interrupt flag	0 = no 1 = yes
5	Alarm interrupt flag	0 = no 1 = yes
4	Update interrupt flag	0 = no 1 = yes
3:0	Reserved	

Status Register D Bit Assignments

This register hold the RTC power-on flag. Refer to Table 11-5 for its bit assignments.

Table 11-5. Status Register D Bit Assignments

Bit	Function	Description
7	RTC has power	0 = no 1 = yes
6:0	Reserved	

Diagnostic Status

This register holds RTC diagnostic information. Table 11-6 for its bit assignments.

Table 11-6. Diagnostic Status Bit Assignments

Bit	Function	Description
7	RTC has lost power	0 = no 1 = yes
6	CMOS checksum bad	0 = no 1 = yes
5	Invalid configuration information during POST	0 = no 1 = yes
4	Memory size error at POST	0 = no 1 = yes
3	Fixed disk or adapter failure	0 = no 1 = yes
2	Invalid CMOS time	0 = no 1 = yes
1:0	Reserved	

Reason for Shut Down Bit Assignments

The hexadecimal value of this byte indicates the reason for shutdown. Refer to Table 11-7 for byte value assignments.

Table 11-7. Reason for Shutdown Bit Assignments

Byte Value (in hex)	Function
C	Returned via XROM_SEG:XROM_OFF
B	Undefined
A	Jump to address
9	IBM block move compatible reentry
8	POST real mode entry
7	Int 15 block move reentry
6	Non-compatible reentry
5	Flush keyboard buffer and jump to address
4	Reboot
3	Shutdown after memory error
2	Shutdown after memory test
1	Shutdown after memory size
0	Soft reset or unexpected shutdown

Type of Diskette Drive

This register holds diskette drive type information. Refer to Table 11-8 for its bit assignments.

Table 11-8. Type of Diskette Drive Bit Assignments

Bit	Function	Description
7:4	Drive A type	0 0 0 0 = no drive present 0 0 0 1 = 5 1/4-inch 360 MB 0 0 1 0 = 5 1/4-inch 1.2 MB 0 0 1 1 = 3 1/2-inch 720 MB 0 1 0 0 = 3 1/2-inch 1.44 MB (default) 0 1 0 1 = reserved 0 1 1 0 = 3 1/2-inch 2.88 MB 0 1 1 1 to 1 1 1 1 = reserved
3:0	Drive B type	0 0 0 0 = no drive present (default) 0 0 0 1 = 5 1/4-inch 360 MB 0 0 1 0 = 5 1/4-inch 1.2 MB 0 0 1 1 = 3 1/2-inch 720 MB 0 1 0 0 = 3 1/2-inch 1.44 MB 0 1 0 1 = reserved 0 1 1 0 = 3 1/2-inch 2.88 MB 0 1 1 1 to 1 1 1 1 = reserved

Type of Hard Disk Bit Assignments

This register holds hard disk type information. Refer to Table 11-9 for its bit assignments .

Table 11-9. Type of Hard Disk Bit Assignments

Bit	Function	Description
7:4	Drive C type	0 0 0 0 = no drive present (default) 0 0 0 1 thru 1 1 1 0 = drive type 1 though 14, respectively 1 1 1 1 = drive type in extended byte 19h
3:0	Drive D type	0 0 0 0 = no drive present (default) 0 0 0 1 thru 1 1 1 0 = drive type 1 though 14, respectively 1 1 1 1 = drive type in extended byte 1Ah

Language Bit Assignments

This register holds type of language in use information. Table 11-10 for its bit assignments.

Table 11-10. Language Bit Assignments

Bit	Function	Description
7:4	Language	0 0 0 0 = English (default) 0 0 0 1 = French 0 0 1 0 = German 0 0 1 1 = Italian 0 1 0 0 = Spanish 0 1 0 1 thru 1 1 1 1 = reserved
3	Reserved	
2	Scan FLASH user area	0 = no (default) 1 = yes
1	Network password valid	0 = no (default) 1 = yes
0	Power-on password valid	0 = no (default) 1 = yes

Installed Hardware Bit Assignments

This register holds system hardware information. Refer to Table 11-11 for its bit assignments.

Table 11-11. Installed Hardware Bit Assignments

Bit	Function	Description
7:6	Number of diskette drives	0 0 = one (default) 0 1 = two 1 0 = reserved 1 1 = reserved
5:4	Primary display type	0 0 = primary has own BIOS (default) 0 1 = color, 40 columns 1 0 = color, 80 columns 1 1 = monochrome
3:2	Reserved	
1	Math coprocessor installed	0 = no 1 = yes (default)
0	Diskette drive present	0 = no 1 = yes (default)

Shadow Control Byte Bit Assignments

This register holds memory shadowing information. Refer to Table 11-12 for its bit assignments.

Table 11-12. Shadow Control Byte Bit Assignments

Bit	Function	Description
7:5	Reserved	
4	Shadow E000:0000h to E000:7FFFh	0 = no (default) 1 = yes
3:2	Reserved	
1	Shadow C000:8000h to C000:FFFFh	0 = no (default) 1 = yes
0	Shadow C000:0000h to C000:7FFFh	0 = no (default) 1 = yes

BIOS Options Bit Assignments

This register holds BIOS option information. Refer to Table 11-13 for its bit assignments.

Table 11-13. BIOS Options Bit Assignments

Bit	Function	Description
7:6	Reserved	
5	Numlock on at boot	0 = no (default) 1 = yes
4:3	Reserved	
2	Report diskette drive errors	0 = no 1 = yes (default)
1	Report video errors	0 = no 1 = yes (default)
0	Report keyboard errors	0 = no 1 = yes (default)

Manufacturer Option 1 Bit Assignments

This register holds memory mapping to the EISA bus, speaker, hard drive, and video BIOS mapping information. Refer to Table 11-14 for its bit assignments.

Table 11-14. Manufacturer Option 1 Bit Assignments

Bit	Function	Description
7	Reserved	
6	Map 15 M to 16 M to EISA bus	0 = no (default) 1 = yes
5	Speaker enable	0 = no 1 = yes (default)
4	512 KB to 640 KB enable	0 = no 1 = yes (default)
3:2	Reserved	
1	Alias hard drive type 48 and 49 to 2 and 3, respectively	0 = no 1 = yes (default)
0	Onboard video BIOS mapped from E0000h to C0000h	0 = no (default) 1 = yes

Manufacturer Option 2 Bit Assignments

This register holds parallel port and LCD configuration information. Refer to Table 11-15 for its bit assignments.

Table 11-15. Manufacturer Option 2 Bit Assignments

Bit	Function	Description
7:6	Parallel port 1 configuration	0 0 = disabled (default) 0 1 = address 378h and IRQ7 1 0 = address 278h and IRQ5 1 1 = reserved
5:4	Parallel port 2 configuration	0 0 = disabled (default) 0 1 = address 378h and IRQ7 1 0 = address 278h and IRQ5 1 1 = reserved
3	Parallel port 1 bi-directional	0 = no (default) 1 = yes
2	Parallel port 2 bi-directional	0 = no (default) 1 = yes
1:0	LCD configuration	0 0 = disabled (default) 0 1 = enabled and suppress POST messages 1 0 = reserved 1 1 = enabled

Manufacturer Option 3 Bit Assignments

This register holds UART configuration information. Refer to Table 11-16 for its bit assignments.

Table 11-16. Manufacturer Option 3 Bit Assignments

Bit	Function	Description
7:6	UART 1 configuration	0 0 = disabled (default) 0 1 = address 3F8h and IRQ4 1 0 = address 2F8h and IRQ3 1 1 = address 3E8h and IRQ 10
5:4	UART 2 configuration	0 0 = disabled (default) 0 1 = address 2F8h and IRQ3 1 0 = address 3E8h and IRQ10 1 1 = address 2E8h and IRQ 11
3:0	Reserved	

Manufacturer Option 4 Bit Assignments

This register holds disk drives and the mouse enable information. Refer to Table 11-17 for its bit assignments.

Table 11-17. Manufacturer Option 4 Bit Assignments

Bit	Function	Description
7:6	Reserved	
5	Onboard diskette drive enable	0 = no 1 = yes (default)
4	Onboard IDE hard drive enable	0 = no (default) 1 = yes
3	Reserved	
2	Hard drive DMA enable	0 = no (default) 1 = yes
1	Reserved	
0	Mouse enable	0 = no (default) 1 = yes

Manufacturer Option 5 Bit Assignments

This register holds cache controller option information. Refer to Table 11-18 for its bit assignments.

Table 11-18. Manufacturer Option 5 Bit Assignments

Bit	Function	Description
7:5	Reserved	
4	Concurrent refresh	0 = no 1 = yes (default)
3	Posted I/O writes	0 = no 1 = yes (default)
2	I/O recovery time	0 = standard 1 = enhanced (default)
1:0	Cache enabled	0 0 = disabled (default) 0 1 = write through 1 0 = reserved 1 1 = write back

Setup Information Bit Assignments

This register holds serial port baud rate information. Refer to Table 11-19 for its bit assignments.

Table 11-19. Setup Information Bit Assignments

Bit	Function	Description
7:4	Reserved	
3:2	COM2 redirection	0 0 = disabled (default) 0 1 = 1200 baud 1 0 = 2400 baud 1 1 = 9600 baud
1:0	COM1 redirection	0 0 = disabled (default) 0 1 = 1200 baud 1 0 = 2400 baud 1 1 = 9600 baud

CPU Speed, Cache, and Extended CMOS Control Bit Assignments

This register holds CPU speed, cache, and last boot information. Refer to Table 11-20 for its bit assignments.

Table 11-20. CPU Speed, Cache, and Extended CMOS Control Bit Assignments

Bit	Function	Description
7:5	Reserved	
4	Last boot failed	0 = no (default) 1 = yes
3	Cache good	0 = no 1 = yes (default)
2:0	CPU speed	0 0 0 = slow 0 0 1 = fast 010 to 111 are reserved

Time-Of-Day Registers

The time-of-day registers can be binary or BCD. Table 11-21 lists the time-of-day registers address map.

Table 11-21. Time-Of-Day Registers Address Map

Address	BCD Mode	Binary Mode	Function/Time
0	60 to 0	3B to 0h	Seconds
1	60 to 0	3B to 0h	Seconds/alarm
2	60 to 0	3B to 0h	Minutes
3	60 to 0	3B to 0h	Minutes/alarm
4	12 to 1	0C to 01h	Hours/am
4	92 to 81	8C to 81h	Hours/pm
5	12 to 1	0C to 01h	Hours/alarm/am
5	92 to 81	8C to 81h	Hours/alarm/pm
6	7 to 1	7 to 1h	Day-of-week
7	31 to 1	1F to 1h	Date
8	12 to 1	0C to 1h	Month
9	99 to 0	63 to 0h	Year

A

Specifications

Introduction

This appendix provides information about the technical characteristics of a typical DECpc 400ST Series computer. For CPU module specifications refer to Appendix G. Information includes:

- Computer specifications
- Expansion slot current limitations
- Computer component current requirements

Computer Specifications

Tables A-1 through A-4 list a typical DECpc 400ST Series computer's performance, dimensional, environmental, and acoustical specifications.

Table A-1. Computer Performance Specifications

Attributes	Specification
Microprocessor	Intel486
EISA bus speed	8.33 MHz
Data I/O	8-bits , 16-bits, and 32-bits
Interrupts	15
Physical addressing	4 GB
Virtual addressing	64 terabytes
Supported addressing	512 MB
ROM BIOS Size	128 KB
System board memory	4 MB to 64 MB (using 16 MB SIMMs)
Total computer memory	384 MB (using 32 MB SIMMs)

Table A-2. Computer Dimensions

Dimension	Specification
Width	7.0 inches (17.78 cm)
Length	18.3 inches (46.48 cm)
Height(1)	18.5 inches (46.99 cm)
Weight(1)	39.25 pounds (17.80 kg)

(1) With chassis feet attached

Table A-3. Computer Environmental Specifications

Attributes	Specification
Operating temperature	10 ° C to 35 ° C (50 ° F to 95 ° F)
Storage temperature	-20 ° C to 60 ° C (-4 ° F to 140 ° F)
Operating humidity (non-condensing)	20% to 80% relative humidity, max. wet bulb 33 ° C
Storage humidity (non-condensing)	95% relative humidity, max. wet bulb 35 ° C
Altitude	10,000 feet (3,048 m) maximum (operating)
Operating shock	2.0 G, 11 ms, 1/2 sine
Non-operating shock	30 G, trapezoidal wave, 170 ips D velocity

Table A-4. Acoustics: Preliminary Declared Values per ISO 9296 and ISO 7779

Attributes(1)	LwAd	LpAm(2)
Idle	5.5 bels	46 dBA
Operating	5.5 bels	46 dBA

(1) Current values for specific configurations are available from Digital representatives
(2) Operator position

Expansion Slots

The system board contains six EISA bus master expansion slots, which are also ISA-compatible. The maximum available +5 V dc current allowed for any expansion slot depends on the following parameters:

- Power supply capacity of 35 A at +5 V dc
- The +5 V dc requirements of the board set, including CPU and memory modules
- The +5 V dc requirements of all mass storage devices
- The power demands of additional expansion slots in use

System Component Current Requirements

Table A-8 lists typical current requirements for the computer components.

CAUTION

Do not exceed 254 Watts of total power at 35 A +5 V dc power. Be sure to include power consumed by boards installed in the EISA expansion slots, the system board, the memory module, and CPU module when calculating power consumption. The power limitation is a function of the power connectors not the power supply. Exceeding this limit can damage the computer.

Table A-8. Typical Current Requirements

Assembly	+5 V dc	+12 V dc	-12 V dc	Total Power (w/o surge)
System board (32 MB memory)	6.0 A	0.06 A	0.06 A	31.4 W
DECpc 450ST, 256 KB cache	4.7 A			23.5 W
DECpc 433ST, 128 KB cache	4.2 A			21.0 W
DECpc 425ST, 128 KB cache	4.0 A			20.0 W
Memory module with 64 MB memory	3.0 A			15 W
3 1/2-inch diskette drive	0.8 A	1.00 A		16 W
5 1/4-inch diskette drive	0.2 A	0.20A		3.4 W
Keyboard and mouse	0.5 A			2.5 W
1 EISA slot	2.0 A	0.06 A	0.06 A	11.4 W
6 EISA slots	12 A	0.36 A	0.36 A	69 W
3 1/2-inch hard drive	1.1 A	0.80 A (2 A surge)		15.1 W
5 1/4-inch hard drive (half-height)	1.0 A	1.50 A (4.5 A surge)		23 W
5 1/4-inch hard drive (full-height)	1.5 A	2.00 A (4.5 A surge)		31.5 W

B

BIOS Routines

Introduction

This appendix describes the interrupt service routines available in the system BIOS. Information includes:

- Interrupt vector table
- Summary of BIOS services

Interrupt Vector Table

Table B-1 identifies each interrupt by function and type. Where applicable, it lists the interrupt vector address initialized by the BIOS at POST. System software might re-vector an interrupt at or shortly after the boot process completes, so these values might not be the same in every computer on every occasion.

Table B-1. Interrupt Functions and Types

INT	Function	Type	Vector
00h	Divide by zero	Exception	
01h	Single step	Exception	
02h	Nonmaskable interrupt (NMI)	Exception	FE2C3h
03h	Breakpoint	Exception	
04h	Overflow	Exception	
05h	Print screen	Software	FFF54h
05h	Bounds exception	Hardware	

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
06h	Invalid op code	Hardware	
06h	Reserved (PC only)	Hardware	
07h	Reserved (PC only)	Hardware	
07h	Math coprocessor not present	Hardware	
08h	Double exception error	Hardware	
08h	System timer (IRQ 0)	Hardware	FFEA5h
09h	Keyboard (IRQ 1)	Hardware	FE987h
09h	Math coprocessor segment overrun	Logical	
0Ah	IRQ 2 cascade from second programmable interrupt controller	Hardware	
0Ah	Invalid task segment state	Logical	
0Bh	Serial communications (COM2)	Hardware	
0Bh	Segment not present	Logical	
0Ch	Serial communications (COM1)	Hardware	
0Ch	Stack segment overflow	Logical	
0Dh	Parallel printer (LPT2)	Hardware	
0Dh	General protection fault	Logical	
0Eh	IRQ 6 diskette	Hardware	FEF57h
0Fh	Parallel printer (LPT1) IRQ 7	Hardware	
10h	Video	Software	FF065h
10h	Numeric coprocessor fault	Logical	
11h	Equipment list	Software	FF84Dh
12h	Memory size	Software	FF841h

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
13h	Hard disk/diskette	Software	FE3FEh
14h	Serial communication	Software	FE739h
15h	System services	Software	FF859h
16h	Keyboard	Software	FE82Eh
17h	Parallel printer	Software	FEFD2h
18h	Process boot failure	Software	F1C90h
19h	Bootstrap loader	Software	FE6F2h
1Ah	Time-of-day	Software	FFE6Eh
1Bh	Keyboard break	Software	FFF53h
1Ch	User timer tick	User	FFF53h
1Dh	Video parameter table	BIOS table	FF0A4h
1Eh	Diskette parameter table	BIOS table	FEFC7h
1Fh	Video graphics characters	User	F7F67h
20h to 3Fh	Reserved for DOS		
40h	Diskette BIOS revector	Software	FEC59h
41h	Hard disk parameter table	BIOS table	FE401h
42h	EGA default video driver	BIOS table	
43h	Video graphics characters	User	
44h to 45h	Reserved		
46h	Hard disk parameter table	BIOS table	FE401h
47h to 49h	Reserved		
4Ah	User alarm	User	
4Bh to 59h	Reserved		

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
5Ah	Cluster adapter		
5Bh to 5Fh	Reserved		
60h to 66h	Reserved for user program Interrupts	User	
67h	LIM EMS driver		
68h to 6Fh	Reserved		
70h	Real-time clock (IRQ 8)	Hardware	(1)
71h	Redirect cascade (IRQ 9)	Hardware	(1)
72h	Reserved (IRQ 10)	Hardware	(1)
73h	Reserved (IRQ 11)	Hardware	(1)
74h	Reserved (IRQ 12)	Hardware	(1)
75h	80287 exception (IRQ 13)	Hardware	(1)
76h	Hard disk (IRQ 14)	Hardware	(1)
77h	Reserved (IRQ 15)		(1)
78 to 7Fh	Reserved (IRQ 15)		
80h to F0h	Reserved for BASIC	BASIC	
F1h to FFh	Reserved for user program interrupts	User	

(1) At FFF23h is a table of 8 vectors (offsets only) for interrupts 77 to 70h (IRQ 15:8)

BIOS Services

Each BIOS service runs at least one function. When a BIOS service is capable of running more than one function, functions are selected by placing the proper function number in the AH register. Subfunctions are selected via either the AL register or the BL register.

Tables B-2 through B-11 briefly define each BIOS service and lists each BIOS function and subfunction.

Table B-2. Print Screen Service

Int	Parameter	Function
05h	None	Print screen

Table B-3. Equipment List Service

INT	Parameter	Function
11h	None	Read equipment list

Table B-4. Memory Size Service

INT	Parameter	Function
12h	None	Read memory size

Table B-5. Diskette Service

INT	Parameter	Function
13h	AH = 00h	Reset diskette system
	AH = 01h	Read diskette status
	AH = 02h	Read diskette sectors
	AH = 03h	Write diskette sectors
	AH = 04h	Verify diskette sectors
	AH = 05h	Format diskette track
	AH = 06h to 07h	Reserved
	AH = 08h	Read drive parameters
	AH = 09h to 14h	Reserved
	AH = 15h	Read drive type
	AH = 16h	Detect media change
	AH = 17h	Set diskette type
	AH = 18h	Set media type for format
	AH = 19h toFFh	Reserved

Table B-6. Hard Disk Service

INT	Parameter	Function
13h	AH = 00h	Reset diskette(s) and hard disk
	AH = 01h	Read hard disk status
	AH = 02h	Read sectors
	AH = 03h	Write sectors
	AH = 04h	Verify sectors
	AH = 05h	Format cylinder
	AH = 08h	Read drive parameters
	AH = 09h	Initialize drive parameters
	AH = 0Ah	Read long sectors
	AH = 0Bh	Write long sectors
	AH = 0Ch	Seek to cylinder
	AH = 0Dh	Alternate hard disk reset
	AH = 10h	Test for drive ready
	AH = 11h	Recalibrate drive
	AH = 14h	Controller internal diagnostic
	AH = 15h	Read hard disk type
	AH = 16h to FFh	Reserved

Table B-7. Serial Communication Service

INT	Parameter	Function
14h	AH = 00h	Initialize serial communications port
	AH = 01h	Send character
	AH = 02h	Receive character
	AH = 03h	Read serial port status
	AH = 04h to FFh	Reserved

Table B-8. System Services

INT	Parameter	Function
15h	AH = 04h to 4Eh	Reserved
	AH = 4Fh	Keyboard intercept
	AH = 50h to 7Fh	Reserved
	AH = 80h	Device open
	AH = 81h	Device close
	AH = 82h	Program termination
	AH = 83h	Set event wait interval
	AH = 84h	Joystick support
	AH = 85h	System request key
	AH = 86h	Wait

Table B-8. System Services *(continued)*

INT	Parameter	Function
	AH = 87h	Move block
	AH = 88h	Read extended memory size (× 1 KB)
	AH = 89h	Switch processor to protected mode
	AH = 8Ah to 8Fh	Reserved
	AH = 90h	Device busy
	AH = 91h	Interrupt complete
	AH = 92h to BFh	Reserved
	AH = C0h	Return system configuration parameters

Table B-9. Keyboard Service

INT	Parameter	Function
16h	AH = 00h	Read keyboard input
	AH = 01h	Return keyboard status
	AH = 02h	Return shift flag status
	AH = 03h	Set typematic rate and delay
	AH = 05h	Store key data
	AH = 06h to 0Fh	Reserved
	AH = 10h	Read extended keyboard input
	AH = 11h	Return extended keyboard status
	AH = 12h	Return extended shift flag status
	AH = 13h to FFh	Reserved

Table B-10. Parallel Printer Service

INT	Parameter	Function
17h	AH = 00h	Print character
	AH = 01h	Initialize printer
	AH = 02h	Read printer status
	AH = 03h to FFh	Reserved

Table B-11. Time-Of-Day Service

INT	Parameter	Function
1Ah	AH = 00h	Read system timer time counter
	AH = 01h	Set system timer time counter
	AH = 02h	Read real-time clock time
	AH = 03h	Set real-time clock time
	AH = 04h	Read real-time clock date
	AH = 05h	Set real-time clock date
	AH = 06h	Set real-time clock alarm
	AH = 07h	Reset real-time clock alarm

C

Device Mapping

This appendix contains four tables that list the system memory map, I/O address map, interrupt map, and DMA channel assignment.

NOTE

The DECpc 400ST Series computers do not support use of the 000E 0000 to 000E FFFF address ranges for DEC EtherWORKS (DEPCA) controllers. DEC EtherWORKS controllers should be configured for the 000D 0000 to 000D FFFF address range to run in the 64 KB mode or for 00C 8000 to 00C FFFF to run in the 32 KB mode.

Table C-1. System Memory Map

Address Range (in hex)	Function	Size	Shadow	Cache
0010 0000 to 01FF FFFF	Extended memory(1)	192 MB	No	Yes
000F 0000 to 000F FFFF	System BIOS	64 KB	Yes	Yes
000E 8000 to 000E FFFF	EISA configuration information(2)	32 KB	No	No
000E 0000 to 000E 7FFF	Adapter BIOS extension	32 KB	Yes(3)	Yes
000D 0000 to 000D FFFF	Adapter BIOS extension	64 KB	No	No
000C 8000 to 000C FFFF	Adapter BIOS extension	32 KB	Yes(3)	Yes
000C 0000 to 000C 7FFF	Video BIOS or adapter BIOS extension	32 KB	Yes(3)	Yes
000A 0000 to 000B FFFF	Video RAM	128 KB	No	No
0000 0000 to 0009 FFFF	Base memory	640 KB	No	Yes

(1) The SCU provides an option for creating a 1 MB open space between 15 MB and 16 MB to which you can map expansion board BIOS
(2) Not available for mapping expansion board memory or BIOS
(3) User configurable

Table C-2. I/O Address Map

Address (in hex)	Function
0000 to 000F	ISP DMA controller 1
0020 to 0021	ISP interrupt controller 1
0026	MECA and CLASIC configuration index
0027	MECA and CLASIC configuration data
0040 to 0043	ISP timer 1
0048 to 004B	ISP timer 2
060	Keyboard data
0061	ISP NMI
0064	Keyboard command/status
0070 (bit7)	ISP enable NMI
0072 (bits 6:0)	Real-time clock address
0071	Real-time clock data
0078	BIOS timer
0080 to 008F	ISP DMA
0092	System control port
00A0 to 00A1	ISP interrupt
00C0 to 00DE	ISP DMA
00F0	Reset numeric error
01F0 to 01F7	IDE controller
0278 to 027B	Parallel 2
02E8 to 02 :F	Serial 4
02F8 to 02FF	Serial 2

Table C-2. I/O Address Map *(continued)*

Address (in hex)	Function
0378 to 037F	Parallel 2
03B0 to 03BB	Video registers
03C0 to 03BF	Parallel 1
03E8 to 03EF	Serial 3
03F0 to 03F5	Diskette controller
03F6	IDE
03F7 (bit 7)	Diskette controller status
03F7 (bits 6:0)	IDE status
03F7 (bits 1:0)	Diskette data rate (write)
03F8	Serial 1
0400 to 040B	ISP high DMA
040C to 040F	ISP control and test
0461 to 0464	ISP extended NMI
0464 to 0465	ISP bus master
0480 to 048F	ISP high DMA
04C2 to 04CE	ISP extended DMA
04D0 to 04D1	ISP interrupt edge/level
04D2 to 04FF	ISP extended DMA
0C01 to 0C07	Baseboard configuration
0C09 to 0C79	Baseboard configuration
0C80 to 0C83	Baseboard EISA Identification
0C84	Baseboard enable
0C85 to 0CFF	Baseboard configuration

Table C-3. System Interrupt Levels

Priority	Interrupt Controller	Interrupt Number	Interrupt Source
1	1	IRQ0	System timer
2	1	IRQ1	Keyboard controller
3 to 10	1	IRQ2	Interrupt controller 2
3	2	IRQ8	Real-time clock (RTC)
4	2	IRQ9	EISA connector
5	2	IRQ10	COM (x)/EISA connector
6	2	IRQ11	COM (x)/EISA connector
7	2	IRQ12	Mouse/EISA connector
8	2	IRQ13	Numeric coprocessor
9	2	IRQ14	Hard disk drive/EISA connector
10	2	IRQ15	EISA connector
11	1	IRQ3	COM(*x*)/EISA connector (1)
12	1	IRQ4	COM (*x*)/EISA connector (1)
13	1	IRQ5	LPT(*y*)/EISA connector (2)
14	1	IRQ6	Diskette drive/EISA connector
15	1	IRQ7	LPT(*y*)/EISA connector(2)

(1) Can be COM1 through COM4
(2) Can be either LPT1 or LPT2

Table C-4. DMA Channel Assignment

Channel	Controller	Function
0	1	Refresh
1	1	Not used
2	1	Diskette controller
3	1	Not used
5	2	Not used
6	2	Not used
7	2	Not used

D

Configuring the Computer

Introduction

The System Configuration Utility (SCU), which is used to configure the system board as well as EISA and ISA options, is contained on five language-specific System Configuration Diskettes. The SCU stores configuration settings in both FLASH memory and CMOS RAM. Digital recommends that you use the language-specific SCU to configure the computer when you add, remove, or replace hardware or change system settings.

The system board BIOS also contains a Setup program that enables you to change configuration settings that are stored in CMOS RAM. BIOS Setup options are a subset of those provided in the Configure Computer option of the SCU with the exception of password.

Since values configured with the BIOS Setup Utility are written only to CMOS RAM and will be overwritten when the SCU is run, it is recommended that the BIOS Setup utility be used only if you:

- Need to enable your diskette drive
- Do not have access to a diskette drive
- Have only ISA expansion boards and will not be using the SCU

Configuring Your Computer

This section describes general instructions for configuring the computer using the SCU. For more detailed information, refer to the DECpc 400ST Series User's Guide.

EISA computers identify hardware using a unique product identification code. The SCU matches this product identifier with the appropriate configuration files on the System Configuration Diskette and attempts to automatically configure the system board and EISA expansion boards.

The SCU automatically detects any EISA expansion boards installed in your computer. It does not automatically detect ISA expansion boards.

1. Insert a copy of the System Configuration Diskette into drive A.
2. Soft boot the computer (CTRL + ALT + DEL). After a short wait, the SCU introductory screen will be displayed on your monitor screen.

NOTE

The SCU contains help pop-up screens for any selected menu item. Press F1 at anytime to display them and Esc to remove them.

3. Press Enter to display the SCU Welcome screen.

   If no configuration errors appear, the Welcome screen will display information about the SCU. Press Enter to display the Main menu.

NOTE

If a configuration error appears, the Welcome screen will display information about the error and tell you to reconfigure your computer. Press Enter to display the Main menu, select the View and Edit Details menu item from the Configure Computer option, make any changes as indicated by POST error messages, then exit to boot the computer so changes take effect.

4. Using the Select Keyboard Type option, select the keyboard type that best describes the keyboard you are using.

5. Select the Configure Computer option to configure your computer. The SCU will prompt you for any option configuration (CFG) files it cannot find on the System Configuration Diskette.

NOTE

If the message "Unable to update configuration information in FLASH memory" appears on the monitor screen while configuring the computer, make sure the FLASH Memory Write jumper is correctly set before continuing. Refer to Appendix E for additional information on the FLASH Memory Write jumper.

6. After properly configuring your computer, select the "Exit From This Utility" option to end the SCU session.

Advanced Features

The SCU provides three advanced features. Pressing CTRL/A at the Welcome screen provides access to these features. Details of these features are listed below.

Extended Memory Range Definition

This feature is used to display and change the address ranges defined as extended memory. These address ranges define the extended memory that is available for use by memory management software. This feature can be used on both the system board extended memory and, if applicable, for the memory module. When memory is added or removed, the SCU automatically updates these ranges.

Use this feature to display the address ranges for extended memory and to verify that extended memory has been modified when the "Expansion Board Address Space" option is enabled.

CAUTION

The SCU automatically checks extended memory and lists the default address ranges for it. We recommend using the default address ranges whenever possible. Use caution when modifying these extended memory ranges.

Expansion Board Address Space

Certain expansion boards require 128 KB of address space to run. Because this address space may not be available in certain situations, it can be re-mapped into extended memory.

If expansion boards are installed that require 128 KB of address space and at least 16 MB of memory is available, select the "Enabled" option. This option has no effect if your computer has less than 16 MB of memory.

Enabling this option opens a 1 MB space between 15 MB and 16 MB in memory (F00000h to FDFFFFh). The upper 128 KB is reserved for the system BIOS, the remaining 896 KB provides up to seven 128 KB blocks for use by expansion boards.

If your computer has less than 16 MB of memory, map the expansion boards requiring 128 KB of address space to an address range outside the actual extended memory but within the 16 MB range.

CAUTION

Certain operating systems are incompatible with an open 1 MB space in extended memory.

Expansion Slot 4 Operation

This feature sets the operation of expansion slot 4 depending on the type of expansion board installed.

The available options for slot 4 are "EISA Compatible" and "ISA Compatible." Setting the option to EISA Compatible implements the EISA addressing scheme. The default setting is "EISA Compatible." This setting enables the fourth slot to accept EISA expansion boards as well as ISA expansion boards that do not use I/O addresses in the 0 to 255 range.

If you install an ISA expansion board that uses I/O addresses between 0 and 255, install the board in slot 4 and set this option to "ISA Compatible."

E

System Board Jumpers

Introduction

The system board contains jumper blocks. Each jumper block is a group of pins that can be connected in several combinations with a jumper. The jumper physically connects or disconnects system board circuits that relate to the jumper block function. These circuits enable or disable specific system operations or set hardware parameters that are not controlled with software.

To change a jumper, do the following:

1. Power off the computer.
2. Gain access to the jumper blocks.
3. Remove the jumper from its current location.
4. Position the jumper over its new location and press the jumper evenly onto the pins. Be careful not to bend the pins.

System Board Jumpers

Jumper pins on the system board allow you to:

- Reset the system configuration to default values
- Clear the system password
- Write protect FLASH memory
- Write protect the diskette drives
- Specify the SIMM size
- Enable FLASH recovery boot mode

Figure E-1 shows the location of the system board jumper pins. Note that the square pin is pin 1. Table E-1 lists the jumper settings and their descriptions.

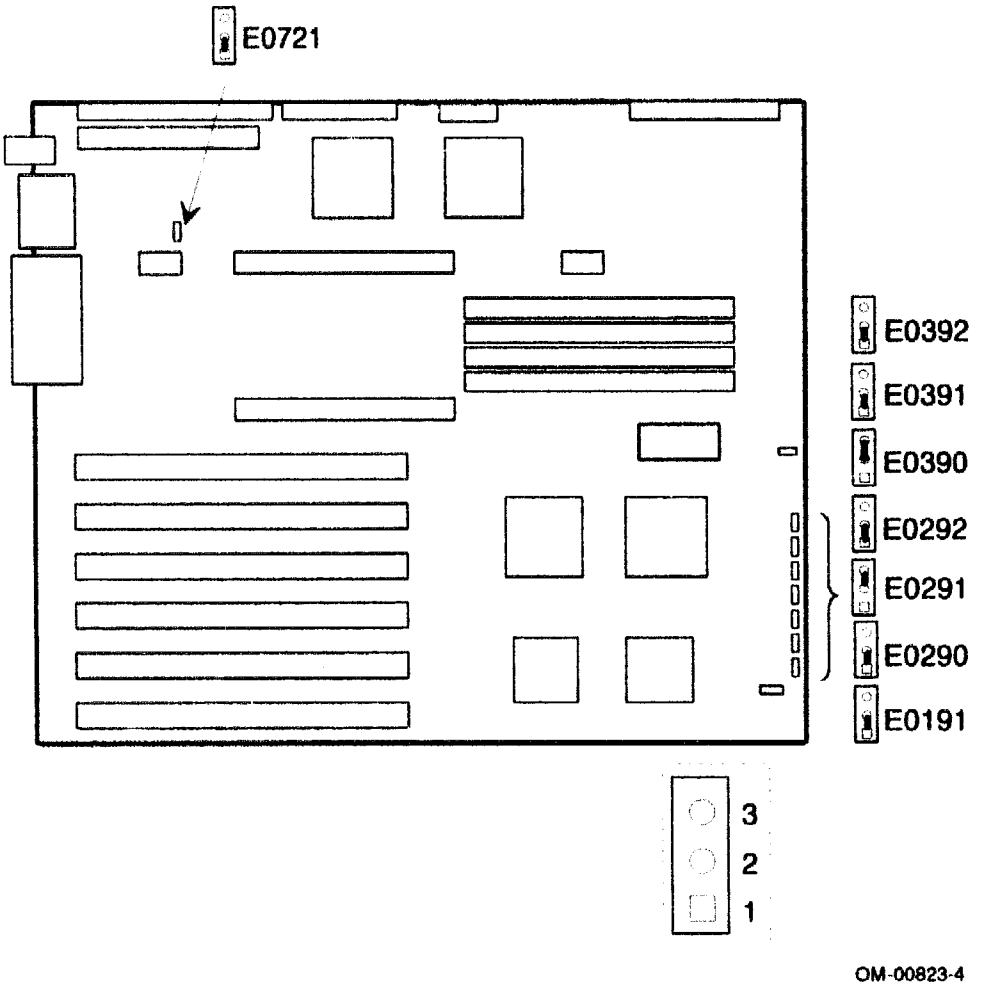


Figure E-1. System Board Jumper Locations

Table E-1. System Board Jumper Settings

Jumper Block	Jumper Setting	Description
E0191	1, 2 (1)	FLASH normal boot
	2, 3	FLASH recovery boot
E0290	1, 2 (1)	Not implemented
E0291	1, 2	Diskette write protect
	2, 3 (1)	Diskette write enable
E0292	1, 2 (1)	System configuration reset disabled
	2, 3	System configuration reset enabled
E0390	1, 2	Password disable/clear
	2, 3 (1)	Password enable
E0391		Memory bank 1 SIMM size
	1, 2 (1)	2, 4, or 8 MB
	2, 3	16 or 32 MB
E0392		Memory bank 0 SIMM size
	1, 2 (1)	2, 4, or 8 MB
	2, 3	16 or 32 MB
E0721	1, 2 (1)	FLASH memory write enable
	2, 3	FLASH memory write protect

(1) Factory setting

Diskette Write Protect

This jumper enables writing to all installed diskette drives. Setting this jumper to the write-protect position, pins 1 and 2, implements a security lock on the onboard diskette controller, thereby providing computer security. For example, users would not be able to copy information from the computer's hard disk drive to a diskette. See Figure E-1 for the jumper location.

System Configuration Reset

This jumper resets the system configuration information stored in FLASH memory and CMOS RAM to the factory default settings every time the computer boots. The FLASH Memory Write jumper (E0721) must be set in the enabled position to allow the configuration information stored in FLASH memory to be reset.

Set the System Configuration Reset jumper (E0292) between pins 2 and 3 to reset the system configuration information. After the factory defaults are restored, run the SCU to restore any user specified system configuration information. Reset the jumper to pins 1 and 2 after the factory defaults have been restored. See Figure E-1 for the jumper location.

Password

This jumper enables setting the power-on and network password (both are the same). It can also be used to clear the password if it is forgotten. Clear the system password by using the following procedure:

1. Power off the computer.
2. Gain access to the Password jumper block.
3. Move the Password jumper from "enabled" to "disabled/clear" (pins 1 and 2). See Figure E-1 for the jumper location.
4. Power up the computer and wait for POST to complete.
5. Power off the computer.
6. Move the jumper from "disabled/clear" to "enabled" (pins 2 and 3).

7. Power up the computer.

8. Run the SCU to specify a new password.

Memory Bank 0, 1

Jumper blocks E0391 and E0392 specify the size of the SIMMs installed in the SIMM sockets. See Table E-1 for jumper settings and Figure E-1 for jumper locations.

FLASH Memory Write

This jumper enables writing to FLASH memory. Writing to FLASH memory is necessary for BIOS upgrades, running the BIOS Setup utility to configure user-defineable hard drives, configuring the system with the SCU, and resetting the system configuration to its default values. See Figure E-1 for the jumper location. For additional information on upgrading the BIOS, refer to Appendix F.

This jumper also provides security by protecting system configuration information. By default, the jumper is set to "FLASH memory write enable." To protect configuration information, set the jumper to "FLASH memory write protect" (pins 2 and 3).

FLASH Recovery Boot

There are two portions of FLASH memory: protected and non-protected. The protected portion contains the recovery BIOS that enables the CPU to boot from a diskette installed in drive A. Follow the FLASH recovery boot procedure described in Appendix F if the system BIOS becomes corrupt. This procedure uses the FLASH Memory Update utility to restore the system BIOS from diskette.

See Figure E-1 for the jumper location. For additional information on recovering the system BIOS, refer to Appendix F.

F

Updating the System BIOS

Introduction

This appendix contains instructions for updating the system BIOS and instructions for recovery of the system BIOS if it becomes corrupt.

System BIOS updates are distributed on the FLASH Memory Update diskette. This diskette contains the update utility (FMUP.EXE), the BIOS update files, and other required files (refer to Table F-1). The README.TXT file provided with the FLASH Memory Update diskette may contain additional information.

Table F-1. Contents of FLASH Memory Update Utility Diskette

File Types	File Names	Description
Utility files	FMUP.EXE	FLASH memory update utility
	FLASH.PCX	Startup banner
	AUTOEXEC.BAT	Starts FLASH update software
	COMMAND.COM	MS-DOS commands used to update the system BIOS
	BEEP.COM	Utility used to make speaker beep
	SHOWHDR.EXE	Displays header information on system BIOS update files
	README.TST	System BIOS update information
	(system boot files)	Any files required to boot the computer
BIOS recovery files	BIOSR0F.REC	System BIOS recovery files
	BIOSR0F.RE1	
	BIOSR0F.RE2	
BIOS update files	(*BIOS version*)R0F.BIO	System BIOS update files
	(*BIOS version*)R0F.BI1	
	(*BIOS version*)R0F.BI2	

BIOS File Header Information

The SHOWHDR.EXE utility is provided on the FLASH Memory Update diskette to display the header information on specified BIOS recovery or update files. Use this utility to check the time stamp and other data in the header of the specified files.

Invoke the utility from the DOS prompt using the following syntax:

```
SHOWHDR filename
```

where `filename` is the name of the BIOS recovery or update file.

For example:

```
A:>showhdr 99999ROF.BIO

SHOWHDR (Show FLASH Data Image Header -- Release x.x)
Image Title: Sample Title 00.00.00.R0 RELEASE BIOS
BIOS INFO
        Logical Area Type: 1
        Logical Area Size: 0x38000
        Load From File --- : TRUE
        Reboot Required -- : TRUE
        Update All Of Image: TRUE
Time Stamp --------- : 01/01/99-12:00
This File Start Addr : 0x0
This File Data Length: 0x10000
Last File in Chain   : FALSE
Next File Name ----- : 99999ROF.BI1
BIOS Reserved String : 0.00.00.R0
```

FLASH Memory Update Utility

CAUTION

To avoid memory conflicts, do not run the FLASH update utility from your operating system prompt. Use the following procedure to boot your system and invoke the FLASH update utility.

1. Insert the FLASH Memory Update diskette into drive A.
2. Boot the computer.

The FLASH update utility will automatically be invoked. The main menu provides the following selections:

- Verify FLASH Memory Area With a File
- Save FLASH Memory Area To a File
- Update FLASH Memory Area From a File

You can verify, save, and update both the system BIOS area and the user area of FLASH memory. The user area is currently unused and does not need to be verified, saved, or updated.

Verify FLASH Memory Area With a File

Select "Verify FLASH Memory Area With a File" menu item to verify that the FLASH memory area matches the contents of the BIOS update file you specify.

If the FLASH memory area doesn't match the specified files, you may want to compare the system BIOS date and version number (displayed briefly when the computer is booting) with the date and version number in the header of the update files. To show the header information in the update files, exit the FLASH update utility and run the SHOWHDR.EXE utility from the DOS prompt.

Save FLASH Memory Area to a File

Select "Save FLASH Memory Area to a File" to save the contents of the FLASH memory to a file.

Run this procedure to create a backup of the system BIOS before updating it.

Update FLASH Memory Area from a File

The "Update FLASH Memory Area from a File" menu item is used to update the system BIOS in FLASH memory. To update the sytem BIOS, do the following:

1. Run the SCU on your System Configuration Diskette to create a backup file (SYSTEM.SCI) of your system configuration. Refer to the DECpc 400ST Series User's Guide or the SCU help screens for information on creating this file.
2. Power off the computer.
3. Ensure that jumper E0721 is in the "FLASH memory write enable" position (this is the default position). The jumper should be between pins 1 and 2.
4. Ensure that jumper E0191 is in the "FLASH normal boot" position (this is the default position). The jumper should be between pins 1 and 2.
5. Insert the FLASH Memory Update diskette into drive A.
6. Power up the computer. The computer will boot off the diskette and start the FLASH update utility.
7. Select the "Save FLASH Memory Area to a File" option to backup the current system BIOS to a file. Use the tab key to select the desired options on this and other FLASH update utility menus.
8. Select the "Update FLASH Memory Area from a File" option.
9. Select the "Update System BIOS" option.
10. You will be prompted for the desired BIOS update. You may enter the title yourself or select from those the FLASH update utility has found on the diskette.

11. Once a BIOS update is selected, information is displayed about the selected BIOS update file. If this is the correct BIOS update file, select the "Continue with programming" option.

12. Wait for approximately one minute while the update process completes.

13. Select "Exit Program" on the main menu to exit the FLASH update utility.

14. Run the SCU to configure the computer.

If the system BIOS becomes corrupted during the update procedure, e.g., a power outage occurs, follow the recovery procedure in the following section.

BIOS Recovery Procedure

The BIOS recovery procedure described in this section is used to restore the system BIOS from a diskette in the event it becomes corrupted.

NOTE

If you are attempting to recover a BIOS version 1.00.05 or above and an installed expansion board's BIOS is mapped to any part of the E0000h to EFFFFh address range, you must remap it to another area or physically remove the expansion board before this procedure can be completed.

The system BIOS is located in upgradeable FLASH memory and contains the normal boot procedure. The system BIOS can become corrupted, for example, when the update procedure is aborted due to a power outage. The FLASH memory also contains a protected area that cannot be corrupted. The code in this protected area is used to boot the computer from drive A when the system BIOS has been corrupted. After booting, the FLASH update utility is used to automatically recover the system BIOS from the BIOS recovery files on the diskette.

To recover the system BIOS, do the following:

1. Power off the computer.

2. Ensure that jumper E0721 is in the "FLASH memory write enable" position (this is the default position). The jumper should be between pins 1 and 2. See Figure F-1 for the location of jumper E0721.

3. Move jumper E0191 to the "FLASH recovery boot" position . The jumper should be between pins 2 and 3. See Figure F-1 for the location of jumper E0191.

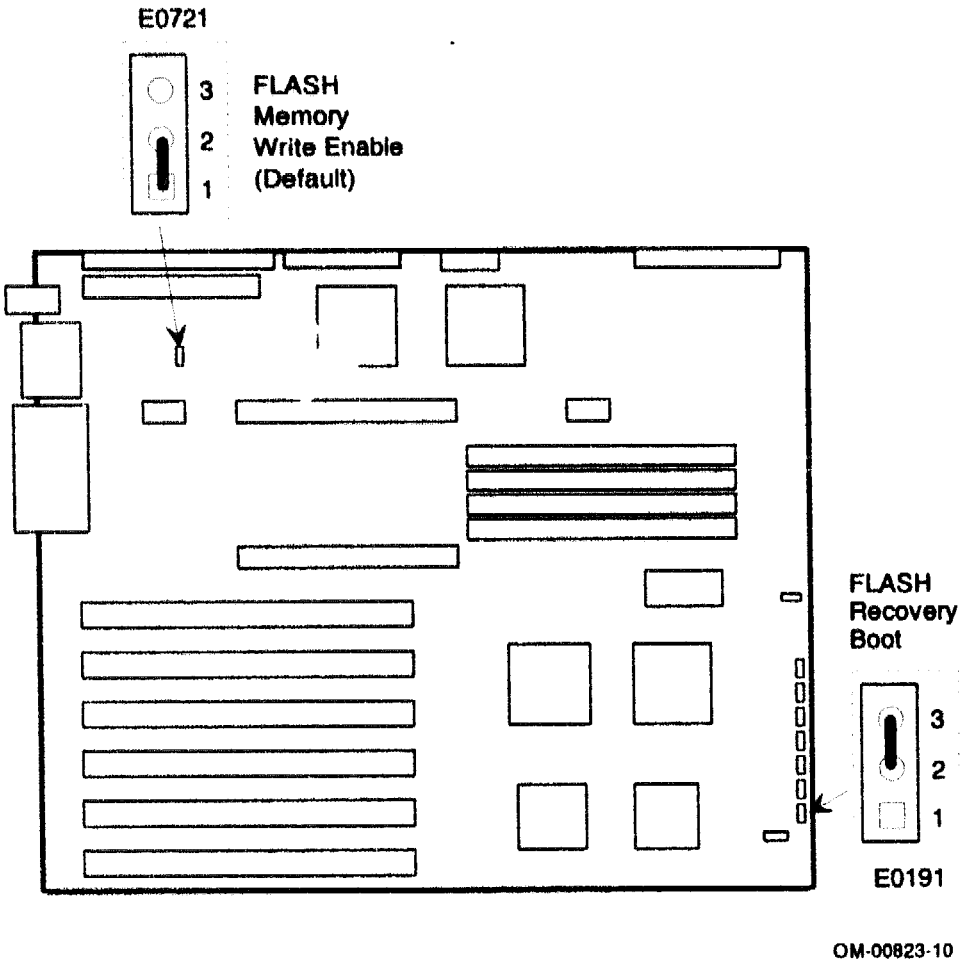


Figure F-1. Location of FLASH Write Enable and Recovery Jumpers

1. Insert the FLASH Memory Update diskette in drive A.

2. Power up the computer.
3. A single beep will signal that the system has booted successfully.
4. Wait 2 - 3 minutes for the recovery process to take place.

NOTE

During the recovery process, no video output is displayed and the keyboard is disabled as the system automatically attempts to recover the BIOS. Because there is no video displayed, the recovery status is identified through beep codes. Table F-2 lists the beep codes used during the recovery procedure.

5. When the process is finished, two beeps will sound signalling successful completion.
6. Power off the computer.
7. Move jumper E0191 to the "FLASH normal boot" position . The jumper should be between pins 1 and 2. See Figure F-1 for the location of jumper E0191.
8. Return jumper E0721 to its original position (the default position for this jumper is between pins 1 and 2).
9. Remove the update diskette from drive A.
10. Power up the computer.

Table F-2. Recovery Procedure Beep Codes

Beep Code	Meaning
2 beeps	Successful completion, no errors
4 long beeps	The computer could not boot from the diskette. The diskette may not be bootable
Continuous series of low beeps	The wrong BIOS recovery files are being used and/or the FLASH Memory Write Enable jumper (E0721) is not set properly.

G

CPU Modules

Introduction

This appendix contains the following information about the DECpc 400ST Series computer CPU modules:

- Description
- Specifications
- Jumper settings

CPU Module Descriptions

Each CPU module has an Intel486 microprocessor that operates at a different speed. Table G-1 identifies the currently available CPU modules and lists the external cache components available for each.

Table G-1. CPU Module Features

Model Number	Primary Microprocessor	External Cache
DECpc 425ST	25 MHz Intel486SX	Optional
DECpc 433ST	33 MHz Intel486DX	Optional
DECpc 450ST	50 MHz Intel486DX	Standard
DECpc 452ST	50 MHz Intel486DX2	Optional
DECpc 466ST	66 MHz Intel486DX2	Standard

External caches also vary among the CPU modules. The 25 MHz, 33 MHz, Intel486 DX2 50 MHz, and Intel486DX2 66MHz CPU modules feature an optional 64 KB or 128 KB write-through external cache. The 50 MHz CPU modules feature a standard 256 KB write-back external cache.

25 MHz CPU Module

Table G-2 lists the performance specifications for a 25 MHz CPU module found in a DECpc 425ST computer.

Table G-2. DECpc 425ST CPU Module Specifications

Attributes	Specification
Microprocessor	25 MHz Intel486SX
Cache	Optional external cache 64 or 128 KB Zero wait-state cache hit Write-through cache technique
Memory interface	486 burst-mode support using fast page mode, 64-bit dual-bank memory Zero wait-state one deep-posted memory write 6-1-1-1 burst reads

33 MHz CPU Module

Table G-3 lists the performance specifications for a 33 MHz CPU module found in a DECpc 433ST computer.

Table G-3. DECpc 433ST CPU Module Specifications

Attributes	Specification
Microprocessor	33 MHz Intel486DX
Cache	Optional external cache 64 or 128 KB Zero wait-state cache hit Write-through cache technique
Memory interface	486 burst-mode support using fast page mode, 64-bit dual-bank memory Zero wait-state one deep-posted memory write 7-1-2-1 burst reads

50 MHz CPU Module

Table G-4 lists the performance specifications for a 50 MHz CPU module found in a DECpc 450ST computer.

Table G-4. DECpc 450ST CPU Module Specifications

Attributes	Specification
Microprocessor	50 MHz Intel486DX
Cache	82490DX/82495DX based 256 KB Zero wait-state cache hit Write-back cache technique
Memory interface	486 burst-mode support using fast paged mode, 64-bit dual-bank memory Zero wait-state one deep-posted memory write 10-2-2-2 burst reads

Intel486 DX2 50 MHz CPU Module

Table G-5 lists the performance specifications for a 50 MHz CPU module found in a DECpc 452ST computer.

Table G-5. Intel486 DX2 50 MHz CPU Module Specifications

Attributes	Specification
Microprocessor	50 MHz Intel486 DX2
Cache	Optional external cache 64 or 128 KB Zero wait-state cache hit Write-through cache technique
Memory interface	486 burst-mode support using fast paged mode, 64-bit dual-bank memory Zero wait-state one deep-posted memory write 6-1-1-1 burst reads

Intel486 DX2 66 MHz CPU Module

Table G-6 lists the performance specifications for a 66 MHz CPU module found in a DECpc 466ST computer.

Table G-6. Intel486 DX2 66 MHz CPU Module Specifications

Attributes	Specification
Microprocessor	66 MHz Intel486 DX2
Cache	Standard external cache 128 KB Zero wait-state cache hit Write-through cache technique
Memory interface	486 burst-mode support using fast page mode, 64-bit dual-bank memory Zero wait-state one deep-posted memory write 7-1-2-1 burst reads

CPU Module Jumpers

Some DECpc 400ST Series CPU modules have jumper blocks that designate the CPU type and cache memory size. The following sections describe the jumper blocks on the currently available CPU modules.

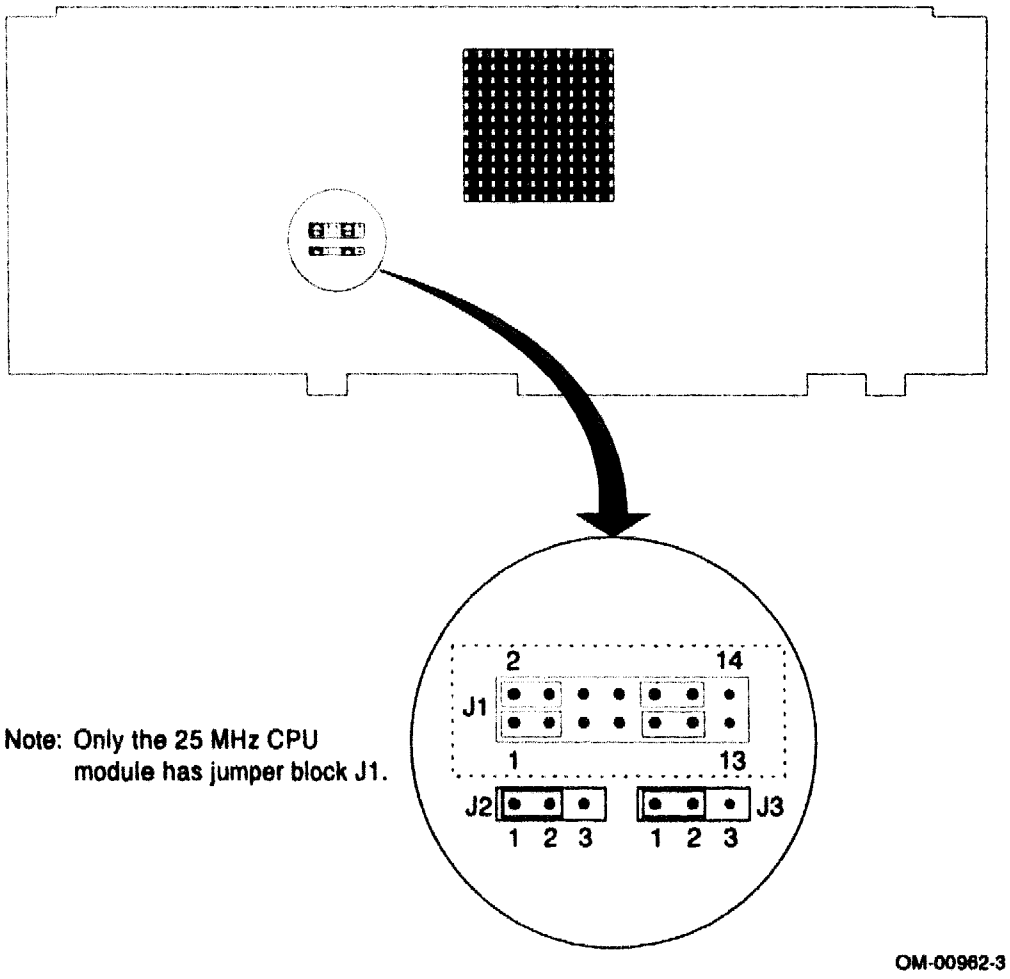
25 MHz CPU Module Jumpers

Jumper block J1 sets the type of CPU installed on the CPU module. Jumper block J3 sets the size of the external cache. Table G-7 lists the jumper settings and their descriptions. Figure G-1 shows the jumper locations.

Table G-7. 25 MHz CPU Module Jumpers

Jumper Block	Jumper Setting	Description
J1	1, 3 (1) 2, 4 (1) 9, 11 (1) 10, 12 (1)	CPU type
J2		Not used
J3	1, 2 (1) 2, 3	128 KB cache memory 64 KB cache memory

(1) Factory setting



Note: Only the 25 MHz CPU module has jumper block J1.

Figure G-1. 25 MHz and 33 MHz CPU Module Jumper Settings

33 MHz CPU Module Jumpers

Jumper block J2 sets the type of CPU installed on the CPU module. Jumper block J3 sets the size of external cache, if one is installed. Table G-8 lists the jumper settings and their descriptions. Figure G-1 shows the jumper locations.

Table G-8. 33 MHz CPU Module Jumper Settings

Jumper Block	Jumper Setting	Description
J2	1, 2 (1)	CPU type
J3 (2)	1, 2 (1)	128 KB cache memory
	2, 3	64 KB cache memory

(1) Factory setting
(2) If no cache is installed, the jumper can be in either position

Intel486 DX2 50MHz and 66 MHz CPU Module Jumpers

Jumper block J3 sets the size of external cache, if one is installed. Table G-9 lists the jumper settings and their descriptions. Figure G-2 shows the jumper location.

Table G-9. Intel486 DX2 50 MHz and 66 MHz CPU Module Jumper Settings

Jumper Block	Jumper Setting	Description
J3(1)	1, 2 installed	Cache memory size — 128 KB
	2, 3 installed	Cache memory size — 64 KB

(1) If no cache is installed, jumper can be in either position (Intel486 DX2 50 MHz CPU module only)

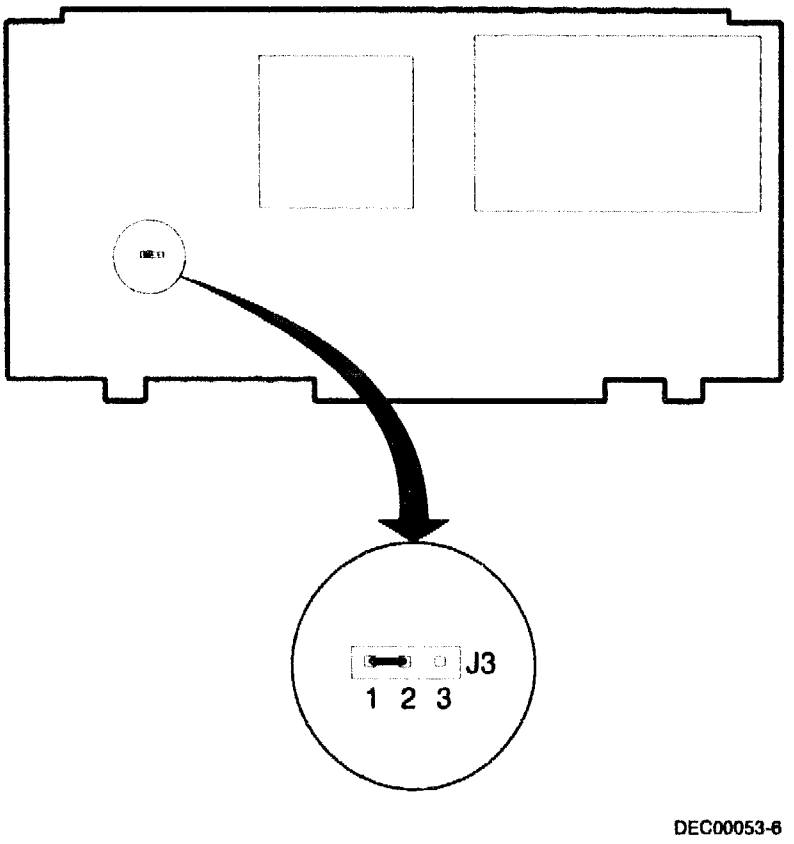


Figure G-2. Intel486 DX2 50 MHz and 66 MHz CPU Module Jumper Locations

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