
DECpc 316SX

DECpc 316SX

Technical Reference Manual

Order Number ER-PC44Y-DD-001

Digital Equipment Corporation

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Contents

INTRO

Introduction

Introduction

This manual is written for software developers, systems integrators and others who require technical knowledge of the DECpc 316SX computer system. The manual is not intended as a tutorial or tool for teaching microcomputer architecture.

The following documents provide more detailed information about the standard components used in the DECpc 316SX computer system:

Intel 386SX Data Book
Headland HT21 Data Book
Intel 8042 Microcontroller Data Sheet
Western Digital WD37C65 Diskette Controller Data Sheet
Dallas Semiconductor DS1285Q Real-time Clock Data Sheet
Western Digital WD90C00 VGA Controller Data Sheet

We recommend you have these documents readily available when you use this manual.

About This Manual

The purpose of this manual is to provide technical information about the hardware architecture and device programming of the DECpc 316SX. The manual is divided into the following sections:

Introduction	Describes the purpose of the manual and notational conventions used.
Specifications and Features	Provides a basic technical description of the system equipment.
Theory of Operation	Describes the individual components of the system and their interaction.
System Configuration	Lists the default configuration settings. Describes modification of the standard configuration.

Device Programming	Describes the registers and programming of all programmable components in the system.
BIOS Services	Provides a detailed listing of BIOS services and error messages available to programmers.

Conventions

This section describes the notations, abbreviations, and special print styles used in this manual.

Abbreviations and Acronyms

A variety of abbreviations and acronyms are used throughout this manual. They are listed here for convenient reference.

Abbreviation or Acronym	Full Meaning
A	Amperes (amps)
b	bit(s)
B	byte(s)
BCD	Binary Coded Decimal
Btu	British Thermal Unit
BPI	Bits per Inch
Hz	Hertz
IDE	Integrated Drive Electronics
in.	inch(es)
ISA	Industry Standard Architecture
SCSI	Small Computer Systems Interface
SIMM	Single In-line Memory Module
V	Volts

Abbreviations and Acronyms

Standard Prefixes

This manual uses standard prefixes to indicate multiples of fundamental units. The standard prefixes are listed in the following table:

Prefix	Symbol	Multiple
Tera- (binary sense)	T	2^{64}
giga-	G	10^{9}
mega- (decimal sense)	M	10^{6}
Mega- (binary sense)	M	2^{20}
kilo- (decimal sense)	k	10^{3}
Kilo- (binary sense)	K	2^{10}
centi-	c	10^{-2}
milli-	m	10^{-3}
micro-	μ	10^{-6}
nano-	n	10^{-9}

Standard Prefixes

Special Notations

Signal names are specified in uppercase letters, such as HIGH. A signal name followed by a minus sign, as in LOW–, indicates an active low signal. A signal name without a minus sign indicates an active high signal.

Special Print Styles

The following print styles are used to differentiate various types of information:

- Words that are printed in small bold capital letters represent keys on your keyboard. For example: ENTER.
- Groups of keys are printed like this: CTRL+ALT+DEL. Press and hold the keys (CTRL, ALT, and DEL in this example) in the order shown.
- Information that you should type or that is shown on the screen is printed as in the following example:

  Type `3` at the `Select the Desired Action` prompt.

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SPECS AND FEATURES

Specifications and Features

Specifications and Features

This section lists the major subassemblies and components in the DECpc 316SX and provides detailed specifications for most subassemblies and components.

System Specifications

This section includes a summary of the standard configuration of the DECpc 316SX. Refer to "*Device and Component Specifications*" for detailed specifications of each component listed.

This section also summarizes the physical and electrical characteristics of the system unit and defines the environmental requirements for safe operation.

Configuration Overview

The following devices and components are included in the standard configuration of the DECpc 316SX.

Devices in standard configuration	◦ 386SX microprocessor ◦ 1MB DRAM (80 ns) ◦ 1.44MB 3½-inch diskette drive ◦ 100-watt power supply ◦ 101-key enhanced keyboard ◦ Built-in diskette drive controller and IDE Drive interface ◦ Built-in 16-bit Super VGA graphics
Expansion support	◦ Three ISA 16/8-bit expansion slots ◦ Four SIMM sockets for system memory expansion ◦ Two 3½-inch drive bays and one 5¼-inch drive bay ◦ 387SX math coprocessor socket

Self-test diagnostic procedures	◦ ROM-based; perform memory tests and verify operation on power-up and after reset
Clock speeds	
CPU	◦ 16 or 8 MHz, software selectable
Expansion bus	◦ 8 MHz
I/O ports	◦ Centronics-compatible parallel port ◦ RS-232 serial port ◦ PS/2-style keyboard port ◦ PS/2-style mouse port

Available System Upgrades

The following lists describe some of the internal options and examples of external options that are available for the DECpc 316SX.

Internal options supported	◦ SIMM memory upgrades ◦ 3½- and 5¼-inch storage including diskette drives, IDE hard disk drives, and tape cartridge systems ◦ 387SX (16 MHz) math coprocessor ◦ Network adapters
External options supported	◦ Printers ◦ Modems ◦ PS/2-style serial mouse

Physical Specifications

Dimensions of system unit	Depth: 38.2 cm (15 in.) Width: 39.4 cm (15½ in.) Height: 10.7 cm (4¼ in.)
Weight	
Total system unit, keyboard, power cord, manual, and packing material	10.4 kg (23 lbs.)
System unit only with one 1.44MB, 3½-inch diskette drive	6.6 kg (14.5 lbs.)

Electrical Specifications

Power output (maximum)	100 Watts continuous 138.5 Watts peak
Input surge current	50 A peak

Input Voltage		Frequency	
Nominal	**Range**	**Nominal**	**Range**
120 VAC 230 VAC	90 to 135 VAC 190 to 264 VAC	60 Hz 50 Hz	47 to 63 Hz 47 to 63 Hz

Environmental Requirements

Acceptable temperature range	
Operating:	10°C to 35°C (50°F to 95°F)
Storage:	-40°C to 66°C (-40°F to 150°F)
Humidity tolerance	
Operating:	20% to 80% (non-condensing)
Storage:	10% to 90% (non-condensing)

Operational Characteristics

Heat output	297.3 Btu/hr, typical
Workspace clearance requirements	12 inches top, back, and sides
Valid operating positions	upright on bottom
Industry certification	UL, CSA, FCC Class B, VDE Class B

Device and Component Specifications

This section provides physical, electrical and operational specifications for most devices and components in the standard configuration.

Processor

Processor type	Intel 386SX, 16 MHz
Data types supported	Bit, byte, word, doubleword
Registers	34 base architecture registers
Address space	16MB physical address space
	64 Terabytes (64×2^{64} bytes) virtual address space

System Memory

Standard configuration	1MB
Memory type	Eight 256KB X 4 DRAMs (SOJ package) plus four 256 X 1 parity DRAMs on main logic board 256KB X 9 or 1MB X 9 DRAMs (SIMM package) in memory expansion sockets
Memory speed	80 ns (or faster)

Memory upgrade support	Expandable to 5MB on system board
Memory organization	Page mode, two- or four-way interleave
Local bus type	16 dedicated data lines 24-bit address bus

BIOS ROM

Source	Phoenix
Version	1.10

Expansion Slots

Type	Three 98-pin 16/8-bit ISA slots

Diskette Drive

Model	SONY MP-F17W-04, or equivalent
Recording method	MFM
Capacity	1.44MB formatted
Average access time (including settling time)	95 ms
Transfer rate	500K bits per second
Mean Time Between Failure	30,000 power-on hours

Power Supply

Power output (maximum)	100 Watts continuous 138.5 Watts peak
Input voltage	
Nominal	120/230 VAC
Range	90–135 VAC at 60 Hz 190–264 VAC at 50 Hz
Frequency Range	47–63 Hz

Output Voltages and Currents

Voltage	Ripple/Noise Voltage 400 Hz or less	Current
+12 VDC (± 5%)	50 mV p-p	0.15 A to 1.53 A*
+ 5 VDC (+5%/–4%)	100 mV p-p	1.25 A to 9.0 A
–12 VDC (± 10%)	150 mV p-p	0 A to 0.3 A
* The +12 VDC line will have a constant current load of 2.75 A for 5 seconds at startup.		

Keyboard

Model (US 101-key)	DEC PCXAL-AA
Power requirements	+5 VDC ±10%, 300 mA max.

Battery

Model	CR2032 (lithium) or equivalent
Life expectancy	5 years
Voltage rating	3 Volts DC

DMA Controller

Model	HT21 internal, equivalent to 2 X Intel 8237A-5 cascaded
Number of channels	7

Interrupt Controller

Model	HT21 internal, equivalent to 2 X Intel 8259 cascaded
Number of interrupt levels	15

Ports

Parallel	Centronics-compatible
Serial	Standard RS-232 Data length: 5-, 6-, 7-, and 8-bits Stop bits: 1, 1½, or 2 Parity: odd, even, or none Transmission rates: 50 to 56,000 baud UART: 16451 equivalent

Video Support

All models are factory equipped with a standard VGA adapter with 512KB video memory built in to the main logic board. With an appropriate monitor, the DECpc 316SX can support Super VGA modes, including 132-column text, 800 x 600 graphics, and 1024 x 768 interlaced graphics. The following tables describe the various video modes.

Standard VGA Modes

Mode (Hex)	Video Std.	Type	Colors	Reso-lution	Columns x Rows	Buffer	Char. Size	Monitor	Notes
	Hercules	graphics	mono	720x348	80x25	B0000	9x14	A-C	
0,1	CGA	text	16	320x200	40x25	B8000	8x8	A-C	1
0,1	EGA	text	16	320x350	40x25	B8000	8x14	A-C	
0,1	VGA	text	16	360x400	40x25	B8000	9x16	A-C	
2,3	CGA	text	16	640x200	80x25	B8000	8x8	A-C	1
2,3	EGA	text	16	640x350	80x25	B8000	8x14	A-C	
2,3	VGA	text	16	720x400	80x25	B8000	9x16	A-C	2
4,5	CGA	graphics	4	320x200	40x25	B8000	8x8	A-C	1
6	CGA	graphics	mono	640x200	80x25	B8000	8x8	A-C	1
7	MDA	text	4	720x350	80x25	B0000	9x14	A-C	3
7	VGA	text	4	720x400	80x25	B0000	9x16	A-C	1
D	EGA	graphics	16	320x200	40x25	A0000	8x8	A-C	1
E	EGA	graphics	16	640x200	80x25	A0000	8x8	A-C	
F	EGA	graphics	4	640x350	80x25	A0000	8x14	A-C	
10	EGA	graphics	16	640x350	80x25	A0000	8x14	A-C	
11	VGA	graphics	mono	640x480	80x30	A0000	8x16	A-C	
12	VGA	graphics	16	640x480	80x30	A0000	8x16	A-C	
13	VGA	graphics	256	320x200	40x25	A0000	8x8	A-C	1

Super VGA Modes

Mode (VESA)	Video Std.	Type	Colors	Resolution	Columns x Rows	Buffer	Char. Size	Monitor	Notes
54	SVGA	text	16	924x387	132x43	B8000	7x9	A-C	
54	SVGA	text	16	1056x387	132x43	B8000	8x9	A-C	4
55	SVGA	text	16	924x400	132x25	B8000	7x16	A-C	
55	SVGA	text	16	1056x400	132x25	B8000	8x16	A-C	4
56	SVGA	text	4	924x387	132x43	B0000	7x9	A-C	
56	SVGA	text	4	1056x387	132x43	B0000	8x9	A-C	4
57	SVGA	text	4	924x400	132x25	B0000	7x16	A-C	
57	SVGA	text	4	1056x400	132x25	B0000	8x16	A-C	4
58(6A)	SVGA	graphics	16	800x600	100x75	A0000	8x8	B	
58(102*)	SVGA	graphics	16	800x600	100x75	A0000	8x8	B	
59(6B)	SVGA	graphics	mono	800x600	100x75	A0000	8x8	B	
5A	SVGA	graphics	mono	1024x768	128x48	A0000	8x8	C	5
5B	SVGA	graphics	4	1024x768	128x48	A0000	8x16	C	5
5D(104*)	SVGA	graphics	16	1024x768	128x48	A0000	8x16	C	5
5E(100*)	SVGA	graphics	256	640x400	80x25	A0000	8x16	A-C	
5F(101*)	SVGA	graphics	256	640x480	80x30	A0000	8x16	A-C	

* Requires use of VESA.EXE TSR file

Monitors

A: Fixed-frequency analog
B: Multi-frequency analog (horizontal frequency = 35.2 kHz,
C: Multi-frequency analog (horizontal frequency = 35.5 kHz)

Notes:

1. All 200-line modes are double scanned to display 400 lines.
2. Default mode for color monitors
3. Default mode for monochrome monitors
4. Multi-frequency monitor setting
5. Interlaced mode

Video Sync Frequencies

Video sync frequencies are listed in the following table.

	Monitor Type Jumper							
	E19-E20 Installed (default)				E20-E21 Installed			
Display Mode	H Sync (kHz)	(+/−)	V Sync (Hz)	(+/−)	H Sync (kHz)	(+/−)	V Sync (Hz)	(+/−)
350 line	31.5	+	70.1	−	31.5	+	62.3	−
200 line	31.5	−	70.1	+	31.5	−	62.3	+
400 line	31.5	−	70.1	+	28.0	−	62.3	+
480 line	31.5	−	59.9	−	31.5	−	59.9	−
132 column	31.5	−	70.0	+	27.6	−	61.5	+
600 line	31.5	−	56.0	−	35.2	−	56.2	−
768 line (interlaced)	35.5	+	87.0	+	35.5	+	86.9	+

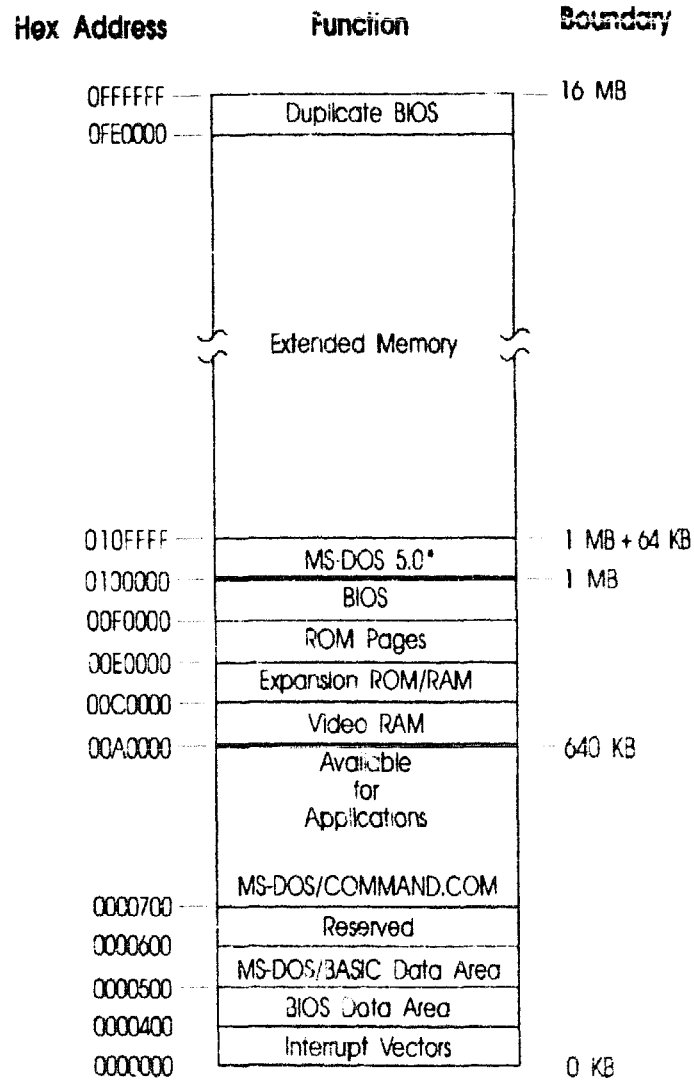

THEORY OF OPERATION

Theory of Operation

Theory of Operation

This section describes the major functional blocks and components of the DECpc 316SX. If you need more information about specific components, refer to the manufacturers' data sheet(s).

System Memory Map



* *CONFIG.SYS must contain* DOS=HIGH *statement.*

System I/O Map

The following tables describe the I/O space of the DECpc 316SX. Any addresses not listed may be considered undefined.

System Board (0000-00FF)	
Hex Range	**Device**
0000-000F	DMA Controller 1
0020-0021	Interrupt Controller 1
0040-0047	Counter/Timer
0060	Keyboard/Mouse Data Port
0061	Port B Status Port
0064	Keyboard/Mouse Status Port
0070	Real-Time Clock Index/NMI Mask Port
0071	Real-Time Clock Data Port
0073,0075	System Configuration Registers (GESUALDO)
0077,0079	Reserved
0080-008F	DMA Page Registers
0092	System Control Port
00A0-00A1	Interrupt Controller 2
00C0-00DF	DMA Controller 2
00F0-00FF	Numeric Processor Extension (387SX)

ISA/X-Bus (0100-03FF)	
Hex Range	**Device**
0170-017F	Hard Drive Port 2
01E0-01E7	Reserved
01EC-01EF	HT21 Control Registers
01F0-017F	Hard Drive Port 1
01F8-01FF	PSSJ Configuration Registers
0200-0207	Game I/O
0278-027F	Parallel Port 2
02F8-02FF	Serial Port 2 (COM2)
0300-031F	Prototype Card
0370-0377	Diskette Drive Port 2
0378-037F	Parallel Port 1 (LPT1)
0380-038F	SDLC, Bisynchronous 2
03A0-03AF	Bisynchronous 1
03B0-03BF	Monochrome Display
03C0-03DF	VGA Controller and RAMDAC
03F0-03F7	Diskette Drive Port 1
03F8-03FF	Serial Port 1 (COM1)

Direct Memory Access (DMA)

The system supports seven DMA channels. The HT21 contains the equivalent of two 8237A-5 DMA controllers, with four channels for each controller. The DMA channels are assigned as follows:

Controller 1	Controller 2
Ch 0 - Spare	Ch 4 - Cascade for Controller 1
Ch 1 - Spare	Ch 5 - Spare
Ch 2 - Diskette	Ch 6 - Spare
Ch 3 - Spare	Ch 7 - Spare

DMA Channels

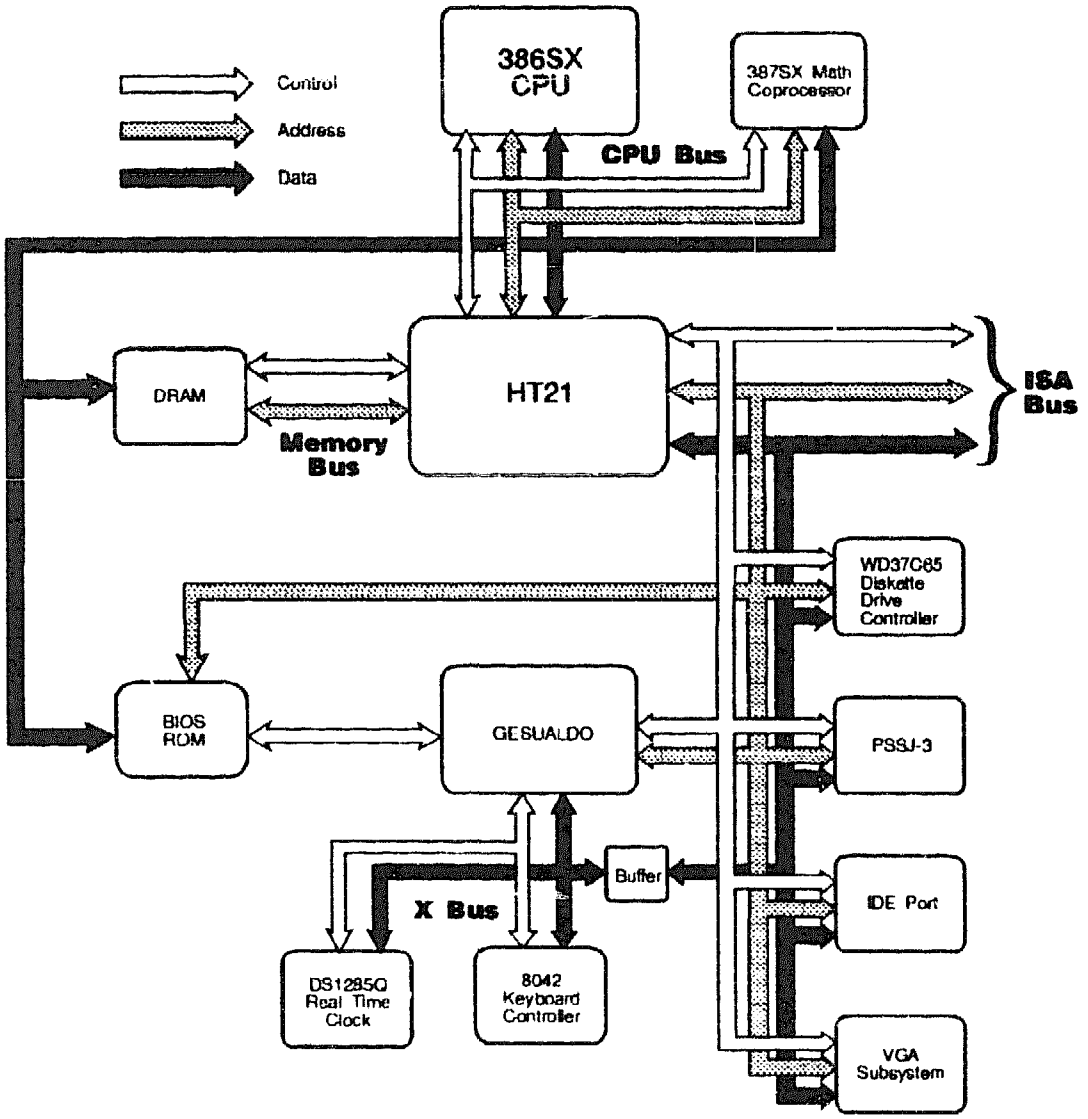
IRQ Assignments

The following table lists the interrupt request assignments for the DECpc 316SX. Interrupt requests from controller 2 are transferred to interrupt 2 on controller 1.

CTLR1	CTLR2	Function
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR2
	IRQ 8	Real-time Clock
	IRQ 9	Software redirected to IRQ 2
	IRQ 10	ISA bus (pin D03)
	IRQ 11	ISA bus (pin D04)
	IRQ 12	Mouse
	IRQ 13	Coprocessor
	IRQ 14	Hard Disk Controller
	IRQ 15	ISA bus (pin D06)
IRQ 3		Bus (typically COM2)
IRQ 4		Serial Port 1 (COM1)
IRQ 5		Bus (typically Parallel Port 2)
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1 (LPT1)

IRQ Assignments

System Block Diagram



Components on the Main Logic Board

386SX Microprocessor

The Intel 386SX microprocessor is a 32-bit CPU with a 16-bit external data bus and a 24-bit external address bus. The 386SX in the DECpc 316SX operates at a maximum clock frequency of 16 MHz.

The 386SX is code compatible with the 8086, 80286, and 386DX microprocessors. Instruction pipelining, high bus bandwidth, and a high-performance ALU facilitate shorter execution times and high system throughput. The 386SX is capable of execution at sustained rates of 2.5 to 3.0 MIPS (Millions of Instructions Per Second).

Operating Modes

The 386SX can operate in two modes – 8086 Real Address Mode (**Real Mode**) and Protected Virtual Address Mode (**Protected Mode**). To maintain compatibility with the 8086, the processor "wakes up" (i.e. at power-up or reset) in Real Mode. In Real Mode, the microprocessor functions as a high-speed 8086 microprocessor and can address only 1MB of physical memory.

Protected Mode provides access to the sophisticated memory management and task protection capabilities of the microprocessor. In Protected Mode, the 386SX can map 64 Terabytes (TB) of *virtual memory* into 16MB of physical memory. This means that programs can access up to 64TB of memory by letting the processor swap unused code or data to disk. Protected Mode also supports multiple task protection through four privilege levels. The task protection enables the 386SX to perform **Virtual 8086 Mode** tasks.

In Virtual 8086 Mode, the 386SX allows the simultaneous execution of 8086 operating systems, 8086 applications, a 386 Protected Mode operating system, and 80286/386/486 Protected Mode applications. In other words, the 386SX can set-up multiple "virtual 8086 machines" with a shared 8086 operating system while running under a 386 Protected Mode operating system. Each virtual machine is simply a Protected Mode task.

Functional Units

Internally the microprocessor consists of three basic functional units: the Bus Interface, the Central Processing Unit, and the Memory Management Unit.

The Bus Interface

The Bus Interface is the microprocessor's link to the external CPU bus. It contains the address latches and drivers, the data transceivers, the bus control logic, and the coprocessor interface.

The Central Processing Unit (CPU)

The central processing unit consists of the Instruction Unit (IU) and the Execution Unit (EU).

The Instruction Unit decodes instructions from the prefetch queue and routes them to the Execution Unit. The IU also contains circuitry to reset the prefetch queue whenever the IU decodes a relocation instruction (for example, JUMP).

The Execution Unit (EU) contains the arithmetic/logic unit (ALU), the registers, and the interrupt control logic.

The 386SX has eight general- purpose registers, four memory segment registers, and two status/control registers. Four of the 32-bit general purpose registers can be used as eight 8-bit registers. The other four general purpose registers can be used as memory offset pointers.

The interrupt handler is within the Execution Unit. When an interrupt is asserted, the EU saves the current state of execution on a stack and transfers program execution to an interrupt service routine (ISR) pointed to by an internal table of 256 interrupt vectors. When the ISR is finished, the program state is *popped* off the stack, and execution continues.

The Memory Management Unit (MMU)

The Memory Management Unit manages the logical address space used by the microprocessor. The MMU consists of the Paging Unit and the Segmentation Unit. The Paging Unit controls memory paging (hardware based); the Segmentation Unit handles indexed memory addressing (software based).

In addition to the functions described above, the 386SX supports a few ancillary signals. These include:

- a RESET signal which allows the microprocessor to stabilize before executing any program instructions
- an external clock input for timing reference
- various power inputs

387SX Math Coprocessor (Optional)

The 387SX is a processor extension to the 386SX microprocessor. It enhances the 386SX's numeric processing abilities, particularly in floating point precision. The 387SX also extends the 386SX instruction set to include transcendental (trigonometric and logarithmic) functions. ***This system requires a 387SX that will run at 16 MHz or faster.***

The 387SX coprocessor interfaces to the system through a reserved I/O address (00F0h-00FFh). When the 386SX receives a 387SX instruction, it passes control to the 387SX. The math coprocessor receives the math instruction and operands and begins execution while the 386SX resumes execution of the main program code. The 387SX asserts a BUSY– signal during execution. When the 387SX is finished, it asserts the PEREQ signal. The 386SX then retrieves the result from the 387SX.

Headland HT21 Single Chip PC/AT Compatible

The HT21 combines most of the system support functions on a single chip. The chip provides memory control, address buffers, data buffers, bus control, DMA control, Interrupt control, and clock generation logic.

DRAM Memory Control

The HT21 generates RAS, CAS, and MA0-MA9 multiplexed address lines to support 256K X 4 or 1M X 4 DRAMs. Memory Data Parity (MDP0, MDP1) signals support 256K X 1 and 1M X 1 parity DRAMs. The use of page interleaving reduces the effective wait states for system board memory accesses to less than 1. Shadow RAM support for system and video BIOS is also provided.

Bus Control

The bus control functions of the HT21 include:

- command/control signal generation
- wait state logic
- reset logic

Command and Control Signal Generator

The HT21 decodes the W/R–, D/C–, and M/IO– signals from the 386SX and generates the appropriate command signals (MEMR–, MEMW–, IOR–, IOW–, INTA–). The HT21 also generates all the required control signals for the ISA bus.

The 387SX control logic decodes the signals that select and reset the 387SX. This logic also handles the PEREQ, BUSY– and ERROR– signals from the 387SX to the CPU.

Wait State and Ready Logic

The Wait State logic matches the speed of the CPU to the speed of devices being accessed by inserting wait states in the CPU cycles. A device on the expansion bus can request additional wait states using the IOCHRDY signal on the I/O channel. A fast device can terminate a cycle early and reduce wait states by asserting the 0WS– signal.

The default wait state numbers for ISA bus cycles are shown in the following chart.

	Memory		I/O		Interrupt
	8-bit	16-bit	8-bit	16-bit	Acknowledge
Command Delay	Yes	No	Yes	Yes	Yes
Wait States	4	1	4	1	–

Default ISA Bus Wait States

Reset Logic

The reset logic coordinates the system initialization functions and timing at power-up or reboot.

DMA Controller

This block within the HT21 is the equivalent of two Intel 8237A-5 DMA controllers in a cascaded arrangement. It provides seven DMA channels for use by the diskette controller and other devices.

8259 Interrupt Controller

This block within the HT21 is the equivalent of two Intel 8259 Programmable Interrupt Controllers. It provides 15 IRQ channels for use by various devices. The first interrupt controller is accessed through I/O port 020h-021h. The second interrupt controller is accessed through I/O port 0A0h-0A1h.

8254 Programmable Interval Timer

This block within the HT21 is the equivalent of an Intel 8254 Programmable Interval Timer. It provides three independent 16-bit counters. Each counter can operate in any one of six programmable modes. The counters generate time delays under software control. The Timer is accessed via I/O port 040h-047h.

Clock Generator

The HT21 generates the output signals PROCLK and SYSCLK from a 32 MHz input clock. PROCLK is the clock reference for the microprocessor and the local bus. PROCLK can run at 32 MHz or 16 MHz depending on the CPU speed selected. SYSCLK provides an 8 MHz clock for devices on the expansion bus.

The clock generator includes the switching circuitry and logic required to toggle the 386SX microprocessor between 16 MHz and 8 MHz modes. This logic also prevents any short cycling during a clock switch cycle.

GESUALDO Controller

This custom chip consolidates DECpc-specific logic into a single chip. The chip implements special configuration registers, performs I/O decoding, and provides clock generation/muxing.

GESUALDO Pin Assignments

Pin Number	Name	Pin Number	Name
1	N/C	51	GND
2	SA0	52	TONE
3	SA1	53	KYBVDIR
4	SA2	54	KYBVEN
5	SA3	55	VOLDE-
6	SA4	56	VOLUP
7	SA5	57	IOR-
8	SA6	58	IOW-
9	SA7	59	BTEST
10	EROMCS-	60	XD3
11	FROMCS-	61	RESET-
12	FEROMCS-	62	DEC0-
13	INT1OUT	63	ROMA19
14	INT2OUT	64	ROMA18
15	VCC	65	VCC
16	VCC	66	VCC
17	COPRCLK	67	ROMA17
18	GND	68	SA15
19	COPCLK2	69	DEC1-
20	GND	70	DEC2-
21	COPCLK1	71	XD4
22	COPCLKSW	72	XD5
23	NOVDI	73	MEMR-
24	NOVCE	74	SA16
25	NOVDO	75	LCSROM-
26	NOVCK	76	AEN
27	SA8	77	VOLEN75
28	SA9	78	INT2IN
29	SA10	79	INT1IN
30	GND	80	GND
31	VCC	81	VCC
32	SA11	82	IOCS16-
33	SA12	83	XD6
34	SA13	84	XD7
35	SA14	85	HD7
36	ROMA16	86	HDCS1-
37	RTCWR-	87	HDCS0-
38	RTCRD-	88	HISPEED
39	GND	89	C184OUT
40	C143OUT0	90	GND
41	GND	91	GND
42	C143X2	92	C184X2
43	C143X1	93	C184X1
44	GND	94	DBENH-
45	C143OUT1	95	DBENL-
46	CTEST	96	SD7
47	XD0	97	FDCS2
48	XD1	98	FDCS1
49	XD2	99	FDCS0
50	VCC	100	VCC

GESUALDO Signal Descriptions

Signal	Type	Pin	Function
XD0-XD7	I/O	47-49,60, 71,72,83,84	X data bus lines 0-7
SD7	I/O	96	ISA data bus line 7
HD7	I/O	85	Hard drive data bus line 7
SA0-SA16	I	2-9,27-29, 32-35,68,74	ISA address bus lines 0-16
AEN	I	76	Address latch enable, ISA bus AEN
LCSROM–	I	75	ROM chip select
MEMR–	I	73	ISA bus signal MEMR–
IOR–	I	57	ISA bus signal IOR–
IOW–	I	58	ISA bus signal IOR–
NOVDI	I	23	Serial EEPROM data input
COPCLK1	I	21	Not used - Grounded
COPCLK2	I	19	Not used - Grounded
COPCLKSW	I	22	Not used - Grounded
RESET–	I	61	Reset input signal
BTEST	I	59	Reserved - pulled down
KYBVEN	I	54	Reserved
KYBVDIR	I	53	Reserved
IOCS16–	I	82	ISA bus signal IOCS16–
INT1IN	I	79	Not used - Grounded
INT2IN	I	78	Not used - Grounded
CTEST	I	46	Reserved - Grounded
TONE	O	52	Reserved
INT1OUT	O	13	N/C
INT2OUT	O	14	N/C
VOLCE–	O	55	Reserved
VOLUP	O	56	Reserved
HISPEED	O	88	CPU speed output
ROMA16	O	36	N/C
ROMA17	O	67	N/C
ROMA18	O	64	N/C
ROMA19	O	63	N/C
COPRCLK	O	17	N/C
VOLEN75	O	77	Reserved
RTCRD	O	39	Real time clock read strobe
RTCWR	O	37	Real time clock write strobe
EROMCS	O	10	EPROM chip select for Exxxx
FROMCS	O	11	EPROM chip select for Fxxxx
FEROMCS	O	12	EPROM chip select for Exxxx or Fxxxx

GESUALDO Signal Descriptions (continued)

Signal	Type	Pin	Function
HDCS0	O	87	Hard drive select 0
HDCS1	O	86	Hard drive select 1
DBENL–	O	95	IDE buffer low byte
DBENH–	O	94	IDE buffer high byte
FDCS0-FDCS2	O	99-97	Floppy drive select 0-2
DEC0-DEC2	O	62,69,70	PSSJ decode 0-2
NOVCE–	O	24	Serial EEPROM chip enable
NOVDO	O	25	Serial EEPROM data output
NOVCK	O	26	Serial EEPROM data clock
C143X1	I	43	14.318 MHz oscillator input (crystal)
C143X2	O	42	14.318 MHz oscillator output (crystal)
C143OUT0	O	40	14.318 MHz oscillator output, ISA bus OSC
C143OUT1	O	45	14.318 MHz oscillator output to PSSJ and VGA clock
C184X1	I	93	1.8432 MHz oscillator input (crystal)
C184X2	O	92	1.8432 MHz oscillator output (crystal)
C184OUT	O	89	1.8432 MHz oscillator output to PSSJ
VCC	PWR	15,16,31,50, 65,66,100	Power inputs
GND	PWR	1,18,19,20, 21,22,30,39, 41,44,45,51, 78,79,80,90,91,	Grounds

PSSJ-3 IC

The PSSJ-3 custom ASIC controls the serial port and the parallel printer interface.

The RS-232 serial port is a single channel asynchronous communications port. The PSSJ contains a 16450 asynchronous communications element that controls the operation of the serial port.

The parallel printer interface provides the data and handshaking signals required to support parallel printers. The PSSJ generates the printer interrupt to the CPU (if enabled).

PSSJ Pin Assignments

Pin Number	Name	Pin Number	Name
1	A7	41	PE
2	AEN	42	PSEL–
3	IOR–	43	PD7
4	IOW–	44	PD6
5	PINT–	45	PD5
6	SINT–	46	PD4
7	D0	47	PD3
8	D1	48	N/C
9	D2	49	PD2
10	TEST	50	PD1
11	D3	51	PD0
12	GND	52	GND
13	D4	53	SLCTIN–
14	D5	54	FAULT–
15	D6	55	GND
16	D7	56	AUDIOIN
17	DRQ	57	GAINOUT
18	WAIT–	58	SINT2
19	RESET	59	DACOUT
20	DACK–	60	VBB
21	GC0	61	JP1
22	GC1	62	GND
23	GC2	63	FDCS–
24	TC	64	JP2
25	DSR–	65	JP3
26	RI–	66	JP4
27	DCD–	67	JS1
28	RXD–	68	JS2
29	CTS–	69	JS3
30	RTS–	70	JS4
31	TXD–	71	PPITIM
32	VCC	72	VCC
33	DTR–	73	VCC
34	N/C	74	CLK14M
35	CLK2IN	75	CS0
36	STROBE–	76	CS1
37	AUTOFD–	77	CS2
38	INIT	78	A0
39	ACK–	79	A1
40	BUSY–	80	A2

PSSJ Signal Descriptions

Signal	Type	Pin	Function
VCC	PWR	32,72,73	Power inputs
VBB	PWR	60	Analog Power input
GND	PWR	12,52,55,62	Grounds
RESET	I	19	PSSJ reset signal
CLK14M	I	74	14.318 MHz clock input, 50% duty cycle
CLK2IN	I	35	1.8432 MHz clock input, 50% duty cycle
D0-D7	I/O	7-9,11,13-16	ISA bus data lines 0-7
IOR–	I	3	ISA bus signal
IOW–	I	4	ISA bus signal
A0-A2,A7	I	78-80,1	ISA bus address lines 0-2 and 7
AEN	I	2	ISA bus signal
CS0-CS2	I	75-77	Address decode inputs
PINT–	O	5	Printer interrupt output, ISA bus IRQ7
SINT–	O	6	Serial 1 interrupt output, ISA bus IRQ4
SINT2	O	58	Serial 2 interrupt output, ISA bus IRQ3
PPITIM	I	71	Low frequency sound input
AUDIOIN	I	56	Analog audio input
GAINOUT	O	57	Analog audio output, not used
DRQ	O	17	DMA request output, ISA bus DRQ1
TC	I	24	Terminal count input, ISA bus TC
DACK–	I	20	DMA acknowledge input, ISA bus DACK1–
WAIT–	O	18	ISA bus IOCHRDY
PD0-PD7	I/O	51-43	Printer port data lines 0-7
INIT	I/O	38	Printer initialization
AUTOFD–	I/O	37	Printer auto feed
STROBE–	I/O	36	Printer strobe
PSEL–	O	42	Printer select
ACK–	I	39	Printer acknowledge
PE	I	41	Printer paper empty
SLCTIN–	I	53	Printer select input

PSSJ Signal Descriptions (continued)

Signal	Type	Pin	Function
BUSY–	I	40	Printer busy
FAULT–	I	54	Printer fault
DTR–	O	33	RS-232 data terminal ready
RTS–	O	30	RS-232 request to send
TXD–	O	31	RS-232 transmit data
RI–	I	26	RS-232 ring indicator
DCD–	I	27	RS-232 carrier detect
DSR–	I	25	RS-232 data set ready
CTS–	I	29	RS-232 clear to send
RXD–	I	28	RS-232 receive data
GS0-GS1	O	21-23	N/C
JP1-JP4	I	61,64-66	N/C
JS1-JS4	I	67-70	N/C
DACOUT	O	59	N/C
FDCS–	O	63	N/C

Intel 8042 Keyboard/Mouse Controller

The keyboard interface is accessed through I/O port 060h. The data stream is 9-bits, consisting of 1 start bit and 8 data bits.

The PS/2-style mouse interface supports a PS/2 mouse or compatible serial device. The mouse interface uses an 11-bit data stream consisting of 1 start bit, 8 data bits, 1 parity bit, and 1 stop bit.

BIOS ROM Subsystem

The Basic Input/Output System (BIOS) functions as the low-level interface for hardware I/O. The BIOS provides a device independent set of routines which ensures compatibility with the IBM PC/AT. The BIOS ROM consists of two 64K x 8 EPROMs, with the code for even and odd addresses on separate EPROMs. The EPROMs also contain the video BIOS and the Setup utility. Accessing the BIOS is discussed in *BIOS Services*.

DS1285Q Real Time Clock

The system's real time clock (RTC) is a Dallas Semiconductor DS1285Q. The RTC requires a 32.768 kHz crystal oscillator as a timing reference. A 3-volt lithium battery maintains the clock and configuration data when system power is removed. To clear the contents of the RTC, short the jumper pins E4-E5 when the system power is off.

WD90C00 Enhanced VGA Controller

The WD90C00 Enhanced VGA Controller provides enhanced VGA capability for the DECpc 316SX. It is completely hardware and software compatible with the IBM PS/2 VGA Display Adapter. In addition to basic VGA modes, it provides extended modes for 132-column text, 1024 x 768 x 16-color graphics, 800 x 600 x 16-color graphics, and 640 x 480 x 256 color graphics. The 1024 x 768 graphics mode is supported only on *interlaced* multi-frequency monitors; and the 800 x 600 graphics mode is supported only on multi-frequency monitors.

The WD90C00 has four major interfaces: the CPU/BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video/RAMDAC interface.

The board has a 16-bit interface to the system bus. Since the WD90C00 arbitrates video memory accesses between the system microprocessor and the CRT Controller contained within the WD90C00, all data passes through the WD90C00 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using standard DRAMs.

Video RAMDAC

The Video RAMDAC contains the color look-up tables. The DAC converts the digital signals from the WD90C00 video controller to analog signals for the analog VGA video output. The RAMDAC is a socketed component.

WD37C65 Diskette Drive Controller

The diskette drive controller is compatible with IBM PC/XT/AT diskette drive systems. Up to two diskette drives can be used. 3½ in. and 5¼ in. drives can be used. 1.44MB, 1.2MB, 720KB, and 360KB formats are supported.

IDE Interface

The on-board IDE connector provides chip-select, data bus (SD0-SD15), and control signals to interface to a 16-bit (AT-type) IDE hard drive.

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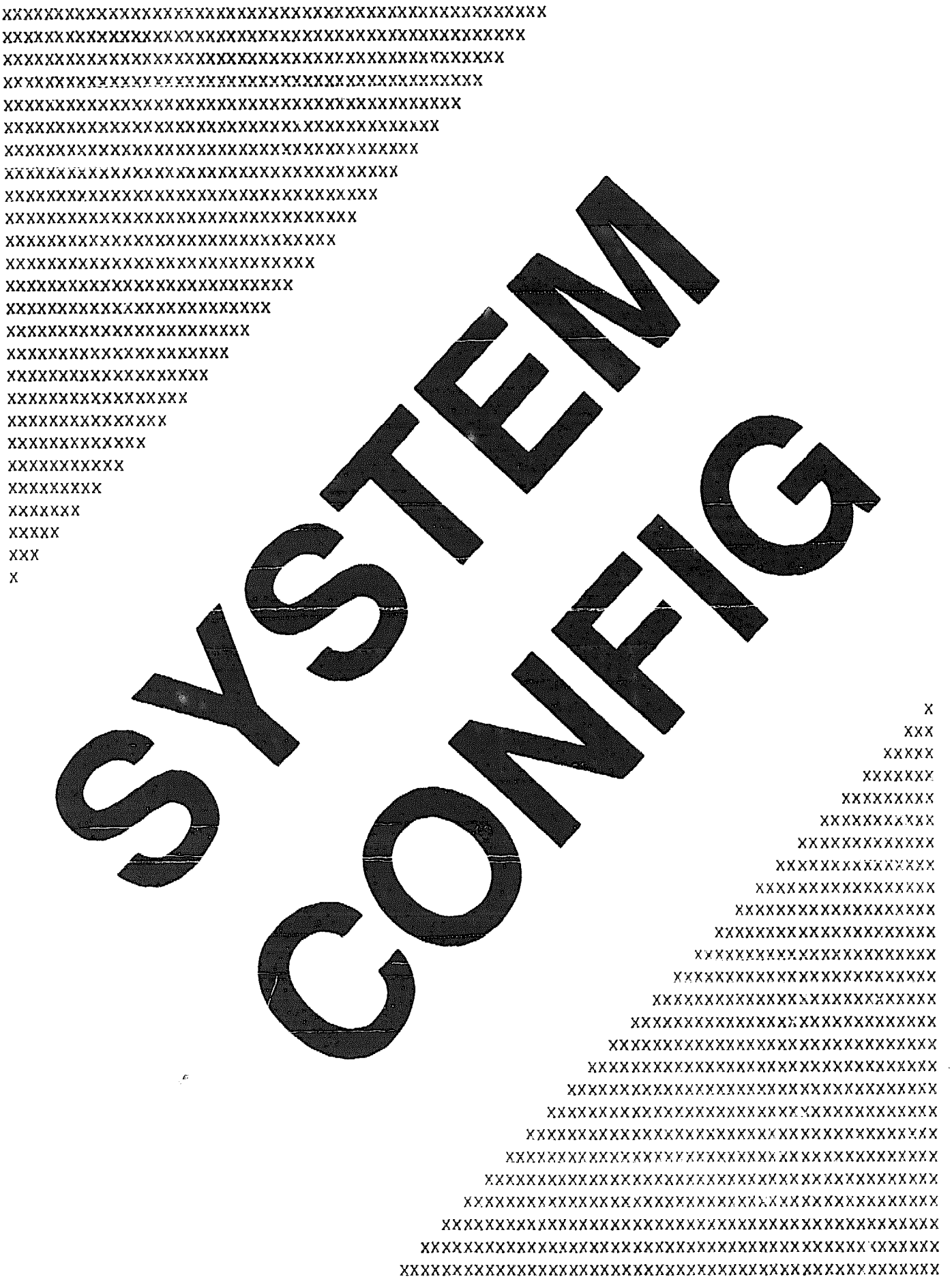

SYSTEM
CONFIG

System Configuration

System Configuration

This section describes the standard configuration of the system as shipped from the factory, and explains how to change configuration settings when necessary.

If you add internal or external options to the system, it may be necessary to change some of the factory default configuration settings. You may also want to change the configuration settings to suit your personal preferences or to meet certain application requirements.

Jumper Settings

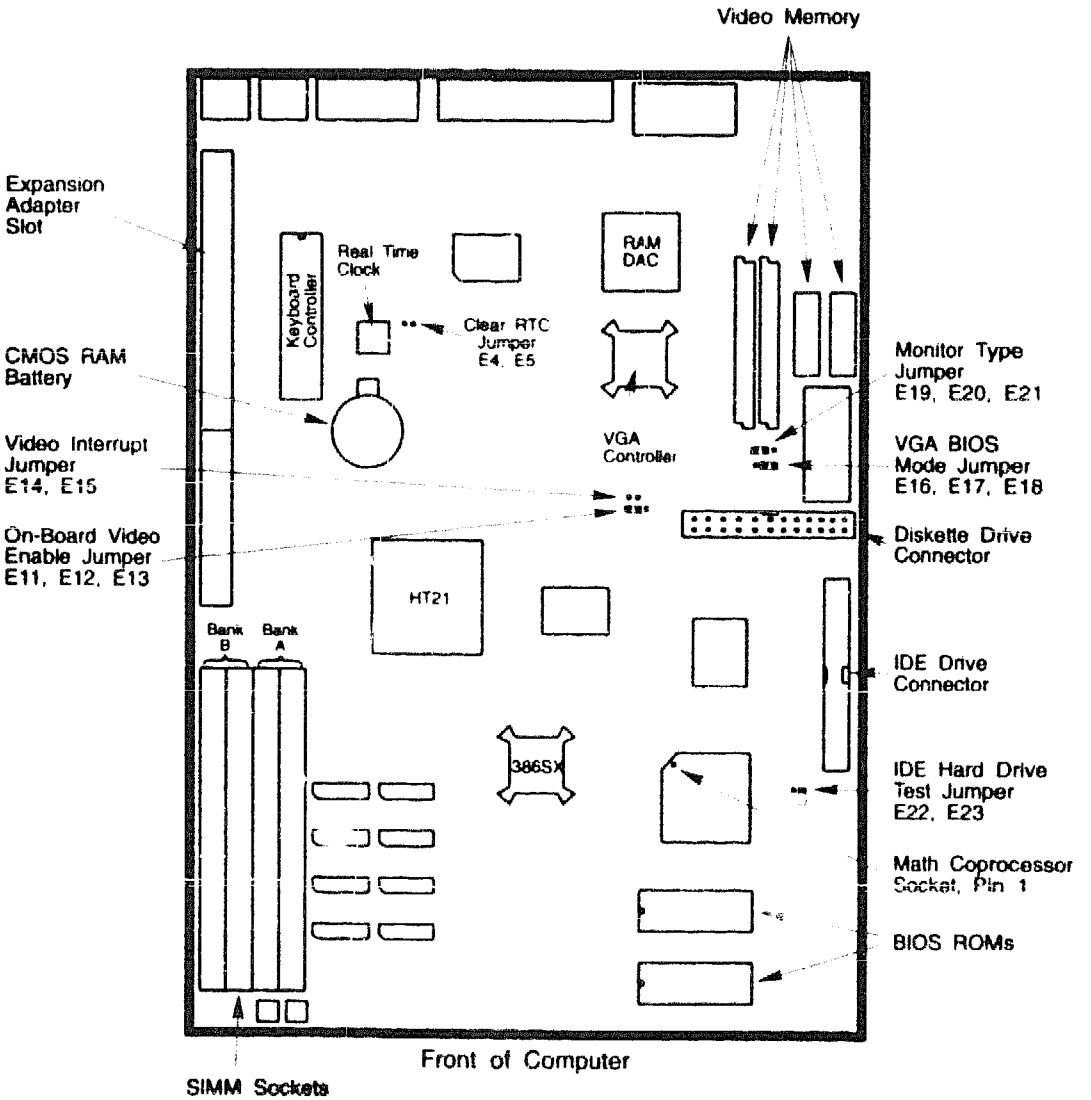
The main logic board diagram illustrates the location of all jumpers.

The following table lists the default jumper connections and their functions. Many of the default settings are critical to the system's operation. Exercise caution when changing any jumper or switch setting.

Feature	Description	Jumper Setting
Video Interrupt	Standard/none	*E14,E15 no connection
	IRQ9	E14-E15 installed
On-Board Video	Enabled	*E11-E12 installed
	Disabled	E12-E13 installed
Monitor Type	VGA analog monitor or standard multiple-frequency monitor	*E19-E20 installed
	Non-standard multiple-frequency monitor	E20-E21 installed
VGA BIOS	PS/2 mode	*E17-E18 installed
	AT mode	E16-E17 installed
Clear RTC/CMOS RAM	Normal Operation	*E4,E5 no connection
	Clear RTC/CMOS RAM	E4-E5 bridged **(momentarily only)**
IDE Hard Drive Test	Disable activity indicator	*E22,E23 no connection
	Enable activity indicator	E22-E23 installed
* Indicates factory default setting.		

Factory default jumper settings

Main Logic Board Layout



Components on the Main Logic Board

The 386SX microprocessor is a 100-pin Plastic Quad Flat Pack (PQFP) type package. The HT21 PC/AT-Compatible Single Chip is a 208-pin PQFP-type package. The WD90C00 VGA controller is a 100-pin PQFP-type package. The 8042 keyboard/mouse controller is a 40-pin DIP package. The locations of these and other components are shown on the main logic board diagram.

The BIOS code is divided between two 64K x 8 EPROMs (even and odd addresses). The 28-pin DIP EPROM sockets are located on the main logic board toward the front of the computer next to the barcode label. The configuration data is stored in battery-backed CMOS RAM contained in the DS1285Q Real Time Clock (RTC) chip. The RTC is a 28-pin PLCC package located toward the back of the computer next to the battery socket.

Programmable configuration settings

The computer uses programmable registers to define the system configuration. Use the Setup utility to change the configuration settings.

The computer stores configuration information in the battery-backed CMOS RAM of the Real Time Clock chip. To clear the contents of the CMOS RAM, short the jumper pins E4 and E5 on the main logic board when the system power is off.

The battery should last about three years with normal use. When the battery fails, the computer will not retain the configuration information correctly. Refer to the user's Guide for instructions on replacing the battery.

The Setup Utility

The Setup utility is contained in the system ROM and on the Utilities diskette provided with the system (SETUPX16.COM). To run the Setup utility from ROM, press F2 at startup when the memory count is displayed. Alternately, you can run SETUPX16.COM from the command prompt. Refer to the computer user's guide for more information on running the Setup utility.

The Setup utility enables you to:

- Set the date and time (Real Time Clock)
- Identify the hard drive type(s) from a drive table
- Enable/disable shadow RAM
- Verify the amount of base and extended memory
- Specify the number and type of diskette drive(s) installed
- Specify the startup diskette drive
- Specify the type of video components
- Specify the power-up default CPU clock speed
- Disable the serial port or specify the serial port as COM1 or COM2
- Disable the parallel port or specify bidirectional/unidirectional operation

The SPEEDX16.COM Utility

Some copy-protected software and other applications depend on an 8 MHz CPU speed to function properly. The SPEEDX16.COM utility included with the system can be used to slow the CPU clock speed to 8 MHz. The slow CPU speed remains in effect until you run SPEEDX16.COM again, or until you turn off or reset the computer. When the CPU is powered up it operates at the default speed specified in CMOS RAM. Refer to the computer user's guide for more information on running SPEEDX16.COM.

Memory Configurations

The main logic board has 1MB of memory permanently installed and four empty SIMM sockets. You can increase the memory on the main logic board by installing 80 ns (or faster) SIMMs in the sockets.

The computer has four banks of memory. Banks 1 and 2 consist of the 1MB of permanently installed memory. Banks A and B consist of two SIMM sockets each.

If 256KB SIMMs were previously installed in the main logic board SIMM sockets, you must remove them to upgrade the system to the 3MB or 5MB configuration. Do not mix the 256KB SIMMs with any other type of SIMMs.

After installing additional memory, run the Setup utility.

The following table defines all valid system memory configurations:

Total System Memory (MB)	Install two of this type of SIMMs (256KB or 1MB) in this bank:			
	Bank 1*	Bank 2*	Bank A	Bank B
1	256KB	256KB	none	none
1.5	256KB	256KB	256KB	none
2	256KB	256KB	256KB	256KB
3	256KB	256KB	1MB	none
5	256KB	256KB	1MB	1MB

* Banks 1 and 2 are permanently installed on the main logic board. 256KB DRAMs are installed in these banks at the factory.

Interleave

The memory controller in the HT21 operates in page interleaved mode. 256K memories use a 4K page size; 1M memories use an 8K page size. The following table describes the interleave for all memory configurations:

Total Memory Installed	Interleave
*1MB 1.5MB 2MB 3MB 5MB	2-way none 4-way none 2-way
* Factory default	

Supported Hardware Peripherals

The DECpc 316SX supports most IBM PC/AT-compatible peripherals. However, some peripherals are not compatible with the 316SX. For example, do not install a *Hard Card* in the expansion slots. The expansion slot connector cannot support the weight of a Hard Card.

Valid Hard Disk Drive Combinations

IDE, ESDI, and ST-506 (MFM and RLL) hard drives cannot be used in the same system.

SCSI drives can be used in a system that also includes an IDE, an ESDI, or an ST-506 drive. However, the IDE, ESDI, or ST-506 (non-SCSI) drive must be configured as the primary drive.

Internal Connector Pin Assignments

This section describes the pin assignments for connectors on the main logic board that are only accessible by opening the system case.

Diskette Drive Interface connector

The pin assignments for the 34-pin diskette drive connector are given in the following table:

Pin	Signal	Pin	Signal
1	GND	2	NDEN–
3	GND	4	GND
5	N/C	6	GND
7	N/C	8	IDX–
9	N/C	10	DSO–
11	N/C	12	DS1–
13	GND	14	DS2– (GND)
15	GND	16	MOTEN–
17	GND	18	DIR–
19	GND	20	STEP–
21	GND	22	WD–
23	GND	24	FDCWE–
25	GND	26	TRK00–
27	GND	28	WP–
29	GND	30	RDD–
31	GND	32	HS–
33	GND	34	DCHNG

Diskette drive interface pin assignments

IDE Connector

The pin assignments for the 40-pin IDE connector are given in the following table:

Pin	Signal Name	Pin	Signal Name
1	HDRESET–	2	GND
3	HDD7	4	HDD8
5	HDD6	6	HDD9
7	HDD5	8	HDD10
9	HDD4	10	HDD11
11	HDD3	12	HDD12
13	HDD2	14	HDD13
15	HDD1	16	HDD14
17	HDD0	18	HDD15
19	GND	20	GND
21	GND	22	GND
23	HDIOW–	24	GND
25	HDIOR–	26	GND
27	HIOCRDY	28	HDALE
29	GND	30	GND
31	IRQ14	32	IOCS16–
33	HDA1	34	GND
35	HDA0	36	HDA2
37	HHDCS0–	38	HHDCS1–
39	ACTIVE–	40	GND

IDE connector pin assignments

ISA 16/8-bit Expansion Slots

This section identifies the I/O interface requirements for PC- and AT-compatible option cards. The system contains three ISA 16/8-bit expansion slots. Each slot has one 62-pin connector and one 36-pin connector.

The following are signal descriptions for the system I/O bus. Note that all signal lines are TTL compatible levels and that I/O adapters should not exceed two low power Schottky (LS) loads per line.

Signal Name	Pin	Pin	Signal Name
IOCHCK-	A1	B1	GND
SD7	A2	B2	RSTDRV
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	GND
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRSH-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	GND

62-pin connector pin assignments

Signal Name	Pin	Pin	Signal Name
SBHE–	A1	B1	MEMCS16–
LA23	A2	B2	IOCS16–
LA22	A3	B3	IRQ10
LA21	A4	B4	IRQ11
LA20	A5	B5	IRQ12
LA19	A6	B6	IRQ15
LA18	A7	B7	IRQ14
LA17	A8	B8	DACK0–
MEMR–	A9	B9	DRQ0
MEMW–	A10	B10	DACK5–
SD8	A11	B11	DRQ5
SD9	A12	B12	DACK6–
SD10	A13	B13	DRQ6
SD11	A14	B14	DACK7–
SD12	A15	B15	DRQ7
SD13	A16	B16	+5V
SD14	A17	B17	MASTER–
SD15	A18	B18	GND

36-pin connector pin assignments

62-pin connector signals

SYSCLK (B20). SYSCLK is the SYStem CLocK. SYSCLK has a frequency of 8 MHz with a normal duty cycle of 50 percent. The SYSCLK period is sometimes extended for synchronization with the CPU or other system board devices. SYSCLK should not be used for applications that require a fixed frequency.

SA0 through **SA19** (A31-A12). These 20 address signals are used to address memory and I/O devices on the ISA bus. They are gated on the system bus when the BALE signal is high and are latched on the falling edge of the BALE signal. SA0 through SA19 are active high.

BALE (B28). BALE is a Buffered Address Latch Enable signal. It is used to latch valid addresses on the bus. BALE is pulled to a high state during DMA cycles, including refresh cycles. BALE is active high.

AEN (A11). AEN is an Address ENable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus, the READ command lines, and the WRITE command lines. AEN is active high.

SD0 through **SD7** (A2-A9). These bidirectional signals are the data bits 0 through 7. These are the lowest eight data bus bits for all memory and I/O devices. SD0 is the least significant bit (lsb), and SD7 is the most significant bit (msb).

RSTDRV (B2). RSTDRV is used to reset or initialize the expansion logic during power-up, line voltage outage, or when the RESET switch on the front panel is pressed. RSTDRV is active high.

IOCHCK– (A1). The IOCHCK– signal alerts the system to parity and other non-recoverable errors through a non-maskable interrupt. IOCHCK– is active low.

IOCHRDY (A10). This signal is used by memory and I/O devices to generate wait states. Any slow device using this line should drive it low (NOT Ready) immediately upon detecting its valid address and a read or write command. This signal should not be held low more than 2.1 microseconds. IOCHRDY is active high (Ready condition).

IRQ3 through **IRQ7**, and **IRQ9** (B25-B21, B4). Six maskable interrupt request lines. An interrupt request is generated when an IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IOR– (B14). I/O Read Command. This is a read signal that instructs an I/O device to drive its data onto the data bus. IOR– is active low.

IOW– (B13). I/O Write Command. This is a write signal that instructs an I/O device to latch the data on the data bus. IOW– is active low.

SMEMR– (B12). Memory Read Strobe. This is a read signal that instructs a memory device to drive its data onto the data bus. SMEMR– is active only when the memory address is within the first 1 megabyte (000000h-0FFFFFh). SMEMR– is active low.

SMEMW– (B11). Memory Write Strobe. This is a write signal that instructs a memory device to latch the data on the data bus. SMEMW– is active only when the memory address is within the first 1 megabyte (000000-0FFFFFH). SMEMW– is active low.

DRQ1, **DRQ2**, and **DRQ3** (B18, B6, B16). DMA request lines 1 through 3. DRQ1 has the highest priority and DRQ3 has the lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform 8-bit transfers only. These DRQ lines are active high.

DACK1–, **DACK2**–, and **DACK3**– (B17, B26, B15). DMA acknowledge. These lines are used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. These signals are active low.

REFRSH– (B19). This signal is used to indicate a DRAM refresh cycle. REFRSH– is active low.

0WS– (B8). This signal is used by 16-bit I/O and memory cards to indicate 0 wait state capability. 0WS– is active low.

TC (B27). Terminal Count. This signal provides a high pulse when the terminal count for any DMA channel is reached. TC is active high.

OSC (B30). 14.31818 MHz clock (used by some video boards). This signal is not synchronized to any other signals on the bus.

36-pin connector signals

SBHE– (A1). Bus High Enable. This signal indicates to 16-bit devices that they should drive data onto the D8 through D15 data lines. SBHE– is active low.

LA17 through **LA23** (A2 through A8). These signals are used to address memory and I/O devices on the ISA bus. These signals are valid when BALE is high. Because the signals are not latched during microprocessor cycles, they do not stay valid for the entire cycle. LA17 through LA23 are active high.

MEMR– (A9). Memory Read Command. This signal is used to instruct 16-bit ISA memory devices to drive data onto the data bus. The address lines on the bus must be valid for at least one system clock period before MEMR– is asserted. MEMR– is active low.

MEMW– (A10). Memory Write Command. This signal is used to instruct 16-bit ISA memory devices to store data present on the data bus. The address lines on the bus must be valid for at least one system clock period before MEMW– is asserted. MEMW– is active low.

SD8 through **SD15** (A11 through A18). These bidirectional signals are the data bits 8 through 15. These are the highest eight data bits for 16-bit memory and I/O devices.

MEMCS16– (B1). This signal is used to tell the system that a peripheral is capable of 16-bit memory transfers. MEMCS16– is active low.

IOCS16– (B2). This signal is used to tell the system that a peripheral is capable of 16-bit I/O transfers. IOCS16– is active low.

IRQ10 through **IRQ12**, **IRQ14**, **IRQ15** (B3–B5, B7, B6). Five additional maskable interrupt request lines. An interrupt request is generated when any IRQ signal is driven high and held high until the CPU acknowledges the interrupt. IRQ13 is reserved for the math coprocessor.

DRQ0, **DRQ5** through **DRQ7** (B9, B11, B13, B15). DMA request lines. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ0 will perform 8-bit transfers, and DRQ5-DRQ7 will perform 16-bit transfers. These signals are active high.

DACK0–, **DACK5–** through **DACK7–** (B8, B10, B12, B14). These lines are used to acknowledge DRQ0 and DRQ5 through DRQ7. These signals are active low.

MASTER– (B17). This signal is used by 16-bit ISA bus masters to gain control of the bus. An ISA bus master issues a DMA request (DRQ) to a DMA channel and receives a DMA acknowledge (DACK–). In response to DACK–, the ISA bus master asserts MASTER–, enabling the ISA bus master to control the system data, address, and control buses. The ISA bus master negates MASTER– when the system board negates DACK–. The bus master must relinquish the bus periodically to allow for DRAM refresh cycles. If MASTER– is held low for more than 15 microseconds, system memory can be lost due to lack of refresh.

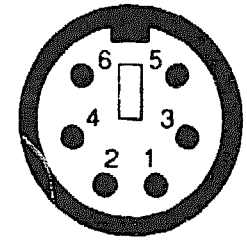
External Connector Pin Assignments

This section describes the pin assignments for connectors that are accessible at the rear of the system chassis.

Keyboard and Mouse Connectors

The keyboard and mouse connectors are standard 6-pin miniature DIN connectors with the following pin assignments:

Pin	Signal Name
1	Data
2	N/C
3	GND
4	+5 VDC
5	Clock
6	N/C



Keyboard/mouse connector pin assignments

Parallel Port Connector

The following are signal definitions for the 25-pin parallel port connector:

Pin	Signal	Function
1	STROBE–	Strobe
2	PRTDAT0	Data bit 0
3	PRTDAT1	Data bit 1
4	PRTDAT2	Data bit 2
5	PRTDAT3	Data bit 3
6	PRTDAT4	Data bit 4
7	PRTDAT5	Data bit 5
8	PRTDAT6	Data bit 6
9	PRTDAT7	Data bit 7
10	PRTACK–	Acknowledge
11	PRTBSY	Busy
12	PRTPE	Paper end
13	PRTSEL–	Select
14	PRTAF–	Auto feed
15	PRTFLT–	Fault
16	PRTINIT	Initialize
17	PRTSEL–	Select input
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

Parallel port pin assignments

RS-232 Serial Port Connector

The following are signal definitions for the 9-pin serial port connector:

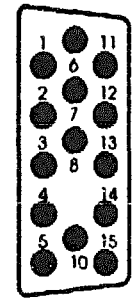
Pin	Signal	Function
1	DCD	Data carrier detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator

Serial port pin assignments

Monitor (VGA Video Port) Connector

The video port uses a standard 15-pin D-shell connector with the following pin assignments:

Pin	Signal Name
1	Red video
2	Green video
3	Blue video
4	N/C
5	GND
6	GND
7	GND
8	GND
9	Key (no pin)
10	GND
11	GND
12	GND
13	HSYNC
14	VSYNC
15	N/C



Monitor connector pin assignments

Power Supply Connectors

The following two tables list the pin assignments for the connectors from the power supply to the main logic board and to the hard disk (and/or diskette) drives.

Pin	Value
1	+5 VDC
2	+5 VDC
3	+5 VDC
4	GND
5	GND
6	GND
7	GND
8	−12 VDC
9	+12 VDC

System board power connector (J20)

Pin	Value
1	+12 VDC
2	GND
3	GND
4	+5 VDC

Disk drive power connector


DEVICE
PROGRAMMING

Device Programming

Device Programming

This section includes information about register level programming of components in the DECpc 316SX.

386SX Microprocessor

It is beyond the scope of this manual to describe 386SX programming. Detailed information about programming the 386SX is available from Intel Corporation. This section provides a brief overview of the 386SX operating modes and registers.

Modes of Operation

The microprocessor operates in two modes - 8086 Real Address Mode (**Real Mode**) and Protected Virtual Address Mode (**Protected Mode**). To maintain compatibility with the 8086, the processor "wakes up" (i.e. at power-up or reset) in Real Mode. In Real Mode, the 386SX functions as a high-speed 8086 microprocessor. In this mode, the processor can address only 1MB of memory, which must be linear.

Protected Mode provides access to the sophisticated memory management paging and privilege capabilities of the microprocessor. In Protected Mode, the 386SX can map 64 Terabytes of virtual memory into 16 MB of physical memory. This means that programs have access to an enormous amount of memory (64 TB) by letting the microprocessor swap unused code or data to disk. Protected Mode also supports multiple task protection through four privilege levels. The task protection feature enables the 386SX to perform **Virtual 8086 Mode** tasks.

In Virtual 8086 Mode, the 386SX allows the simultaneous execution of 8086 operating systems, 8086 applications, a 386 Protected Mode operating system, and 80286/386/486 Protected Mode applications. In other words, the 386SX can set-up multiple "virtual 8086 machines" with a shared 8086 operating system while running under a 386 Protected Mode operating system. Each virtual machine is simply a Protected Mode task.

In Virtual 8086 Mode, the paging unit of the 386SX can break up the 8086 1MB contiguous linear address space into pages (up to 256) and map each page into free areas within the physical address space. In addition, each Virtual 8086 Mode task can use a different mapping scheme to map pages

specific to that task. The paging hardware also allows the sharing of 8086 operating system code between 8086 applications.

386SX Registers

The 386SX provides 34 registers for data manipulation, system control and configuration, and instruction execution. These registers are described in the following sections.

Base Architecture Registers

The base architecture registers are accessible to applications programs at any privilege level. The base architecture registers consist of eight general purpose registers, six segment registers and 2 flag registers. The contents of these registers are task specific and are automatically loaded with a new context upon a task switch operation.

General Purpose Registers

Register Name	Size (in bits)
EAX (AX,AH,AL)	32 (16,8,8)
EBX (BX,BH,BL)	32 (16,8,8)
ECX (CX,CH,CL)	32 (16,8,8)
EDX (DX,DH,DL)	32 (16,8,8)
ESI (Source Index)	32 (16)
EDI (Destination Index)	32 (16)
EBP (Base Pointer)	32 (16)
ESP (Stack Pointer)	32 (16)

Segment Registers

Register Name	Size (in bits)
CS (Code Segment)	16
SS (Stack Segment)	16
DS (Data Segment)	16
ES (Extra Segment)	16
FS (Extra Segment)	16
GS (Extra Segment)	16

Flag Registers

Register Name	Size (in bits)
EFLAGS (Flags)	32 (16)
EIP (Instruction Pointer)	32 (16)

System Level Registers

The system level registers are only accessible at privilege level 0 (the highest privilege level). The system level registers consist of three control registers and four system address registers. These registers control operation of the memory management unit.

Control Registers	
Register Name	**Size (in bits)**
CR0	32
CR2 Page Fault Linear Address	32
CR3 Page Directory Base Register	32

System Address Registers	
Register Name	
GDTR	Global Descriptor Table Register
IDTR	Interrupt Descriptor Table Register
LDTR	Local Descriptor Table Register
TR	Task State Segment Register

Debugging and Testing Registers

The debugging and test registers are for advanced applications and systems level programs. These registers are only accessible at privilege level 0.

Debugging Registers
Register Name
DR0 Linear Break Point Address 0
DR1 Linear Break Point Address 1
DR2 Linear Break Point Address 2
DR3 Linear Break Point Address 3
DR6 Break Point Status
DR7 Break Point Control

Test Registers
Register Name
TR6 Test Control TR7 Test Status

Headland HT21 PC/AT Compatible Single Chip

The Headland Technologies' HT21 PC/AT Compatible Single Chip provides a variety of system support functions. This section explains how to include the HT21 in the development of applications.

DMA Control

The following pages describe the addressing and command scheme for the DMA controllers. References to I/O ports 000h through 00Fh indicate DMA Controller 1 (DMA1) and references to I/O ports 0C0h through 0DEh indicate DMA Controller 2 (DMA2).

DMA Controller 2, Channel 0 is used to cascade the two controllers and should not be programmed for any mode other than cascade mode.

The DMA subsystem of the HT21 chip includes a large number of internal registers. To expedite operations involving the count register or the address register, the HT21 uses an internal byte-pointer flip-flop to add an extra bit. This bit selects between the high and low bytes of these registers. The flip-flop toggles each time a read or write command that involves any of the Word Count or Address Registers in the DMA subsystem is issued. The internal flip-flop is cleared when the CPU issues either a reset or a Master Clear command.

DMA1	DMA2	IOR-	IOW-	Flip-flop	Register Function
000h	0C0h	0	1	0	Read Ch 0 current address low byte
		0	1	1	Read Ch 0 current address high byte
		1	0	0	Write Ch 0 base and current address low byte
		1	0	1	Write Ch 0 base and current address high byte
001h	0C2h	0	1	0	Read Ch 0 current word count low byte
		0	1	1	Read Ch 0 current word count high byte
		1	0	0	Write Ch 0 base and current word count low byte
		1	0	1	Write Ch 0 base and current word count high byte
002h	0C4h	0	1	0	Read Ch 1 current address low byte
		0	1	1	Read Ch 1 current address high byte
		1	0	0	Write Ch 1 base and current address low byte
		1	0	1	Write Ch 1 base and current address high byte
003h	0C6h	0	1	0	Read Ch 1 current word count low byte
		0	1	1	Read Ch 1 current word count high byte
		1	0	0	Write Ch 1 base and current word count low byte
		1	0	1	Write Ch 1 base and current word count high byte
004h	0C8h	0	1	0	Read Ch 2 current address low byte
		0	1	1	Read Ch 2 current address high byte
		1	0	0	Write Ch 2 base and current address low byte
		1	0	1	Write Ch 2 base and current address high byte
005h	0CAh	0	1	0	Read Ch 2 current word count low byte
		0	1	1	Read Ch 2 current word count high byte
		1	0	0	Write Ch 2 base and current word count low byte
		1	0	1	Write Ch 2 base and current word count high byte
006h	0CCh	0	1	0	Read Ch 3 current address low byte
		0	1	1	Read Ch 3 current address high byte
		1	0	0	Write Ch 3 base and current address low byte
		1	0	1	Write Ch 3 base and current address high byte
007h	0CEh	0	1	0	Read Ch 3 current word count low byte
		0	1	1	Read Ch 3 current word count high byte
		1	0	0	Write Ch 3 base and current word count low byte
		1	0	1	Write Ch 3 base and current word count high byte

DMA Registers

DMA1	DMA2	IOR-	IOW-	Flip-flop	Register Function
008h	0D0h	0	1	X	Read Status Register
		1	0	X	Write Command Register
009h	0D2h	0	1	X	Read DMA Request Register
		1	0	X	Write DMA Request Register
00Ah	0D4h	0	1	X	Read Command Register
		1	0	X	Write single bit DMA Request Mask Register
00Bh	0D6h	0	1	X	Read Mode Register
		1	0	X	Write Mode Register
00Ch	0D8h	0	1	X	Set byte pointer flip-flop
		1	0	X	Clear byte pointer flip-flop
00Dh	0DAh	0	1	X	Read temporary register
		1	0	X	Master Clear
00Eh	0DCh	0	1	X	Clear mode register counter
		1	0	X	Clear all DMA Request Mask Register bits
00Fh	0DEh	0	1	X	Read all DMA Request Mask Register bits
		1	0	X	Write all DMA Request Mask Register bits

DMA Registers

008h (0D0h) Command/Status Register

Write (Command)

Bit	Description	1/0	Notes
7	DACK sense	high/low	
6	DREQ sense	low/high	
5	Extended Write	enable/disable	
4	Priority	rotating/fixed	
3	Reserved	must be 0	
2	Controller	disable/enable	
1	Reserved	must be 0	
0	Reserved	must be 0	

Read (Status)

Bit	Description	1/0
7	CH 3 request status	DRQ3/DRQ3-
6	CH 2 request status	DRQ2/DRQ2-
5	CH 1 request status	DRQ1/DRQ1-
4	CH 0 request status	DRQ0/DRQ0-
3	Ch 3 terminal count	TC3/TC3-
2	Ch 2 terminal count	TC2/TC2-
1	Ch 1 terminal count	TC1/TC1-
0	Ch 0 terminal count	TC0/TC0-

009h (0D2h) DMA Request Register (Write)

Bit	Description	1/0
7-3	Reserved	must be 0
2	Request bit	set/reset
1-0		bit 1 bit 0
	Ch 0 select	0 0
	Ch 1 select	0 1
	Ch 2 select	1 0
	Ch 3 select	1 1

009h (0D2h) DMA Request Register (Read)

Bit	Description	1/0
7-4	Reserved	
3	Ch 3 request bit status	
2	Ch 2 request bit status	
1	Ch 1 request bit status	
0	Ch 0 request bit status	

00Ah (0D4h) Write single bit DRQ Mask

Bit	Description	1/0
7-3	Reserved	must be 0
2	Mask bit	set/reset
1-0		bit 1 bit 0
	Ch 0 select	0 0
	Ch 1 select	0 1
	Ch 2 select	1 0
	Ch 3 select	1 1

00Ah (0D4h) Read Command Register

refer to Command Register description (Port 008h)

00Bh (0D6h) Mode Register

Bit	Description	1/0	
7-6	Mode select	bit 7	bit 6
	Demand mode	0	0
	Single cycle	0	1
	Block mode	1	0
	Cascade mode	1	1
5	Address counter	decrement/increment	
4	Autoinitialize	enable/disable	
3-2	Transfer type	bit 3	bit 2
	Verify transfer	0	0
	Write transfer	0	1
	Read transfer	1	0
	Illegal - don't use	1	1
1-0	Channel select	bit 1	bit 0
	Ch 0 select	0	0
	Ch 1 select	0	1
	Ch 2 select	1	0
	Ch 3 select	1	1

00Fh (0DEh) Write All Mask Register Bits

Bit	Description	1/0
7-4	Reserved	must be 0
3	Ch. 3 mask bits	set/reset
2	Ch. 2 mask bits	set/reset
1	Ch. 1 mask bits	set/reset
0	Ch. 0 mask bits	set/reset

Interrupt Controller

The interrupt controller recognizes two types of commands: initialization command words (ICWs) and operational command words (OCWs). The initialization process consists of writing a sequence of four bytes to the interrupt controller.

The initialization sequence is started by writing the first initialization command word (ICW1) to Address 020 hex with a 1 on Bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1. Resets the Initialization Command Word Counter to 0
2. Latches ICW1 to the device
3. Selects Fixed Priority Mode
4. Assigns IRQ7 the highest priority
5. Clears the Interrupt Mask Register
6. Sets the Slave Mode address to 7
7. Disables Special Mask Mode
8. Selects the Interrupt Request Register for status read operations

The next three I/O writes to Address 021 hex will load ICW2-ICW4. (All four bytes must be written for the controller to be properly initialized.) The initialization sequence can be terminated at any point by writing to Address 020 hex with a 0 in Data Bit 4. Note that this will allow OCW2 or OCW3 to be written. Operational Command Words (OCWs) allow the interrupt controller to be controlled or reconfigured at any time during operation.

Initialization Command Words (ICWs)

Note: Initialization words are defined by the operating system and are generally not to be changed. Writing an initialization word might cancel pending interrupts.

Port 020h (0A0h) ICW1
Bit Description 0 = 0 ICW4 Not Needed = 1 ICW4 Needed 1 = 0 Cascade Mode = 1 Single Mode 2 Not Used 3 = 0 Edge Triggered Mode = 1 Level Triggered Mode 4 = 0 & Operation Command Word 2 = 1 Initialization Command Word 1 5-7 Not Used
Port 021h (0A1h) ICW2
Bit Description 0-2 Set by interrupt controller per IRQ 3-7 V3-V7 Of Interrupt Vector Address
Port 021h ICW3 (Master Device - INTC1)
Bit Description 0-7: = 1 Indicated IR input has a slave = 0 Indicated IR input does not have a slave

Port 0A1h ICW3 (Slave Device - INTC2)

Bit	Description			
0-2:	Bit2	Bit1	Bit0	Slave ID #
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7

3-7 = 0 (Not Used)

Port 021h (0A1h) ICW4

Bit	Description
0:	Not Used
1:	=0 Automatic EOI Enabled =1 Automatic EOI Disabled
2-3:	Not Used
4:	=0 Disable Fully Nested Mode =1 Enable Fully Nested Mode
5-7:	Not Used

Operational Command Words (OCWs)

Operational Command Words (OCWs) allow the interrupt controller to be controlled or reconfigured at any time during operation.

Port 021h (0A1h) OCW1

Bit	Description
0-7:	Interrupt Mask For IRQ0-IRQ7 = 0 Mask Reset (Enable IRQn) = 1 Mask Set (Disable IRQn)

Port 020h (0A0h) OCW2

Bit	Description	
0-2:	Interrupt Level =	0 1 2 3 4 5 6 7
	Bit0 (L0):	0 1 0 1 0 1 0 1
	Bit1 (L1):	0 0 1 1 0 0 1 1
	Bit2 (L2):	0 0 0 0 1 1 1 1
3	= 0	
4	= 0	
5-7:	Control Rotate And End Of Interrupt Modes	

7 6 5	
0 0 1	Non-Specific EOI Command End Of Interrupt
0 1 1	Specific EOI Command End Of Interrupt
1 0 1	Rotate On Non-Specific EOI Auto Rotation
1 0 0	Rotate In Automatic EOI Mode (Set) Auto Rotation
0 0 0	Rotate In Automatic EOI Mode (Clear) Auto Rotation
1 1 1	*Rotate On Specific EOI Command Specific Rotation
1 1 0	*Set Priority Command Specific Rotation
0 1 0	No Operation

(*L0 - L2 Are Used)

Port 020h (0A0h) OCW3

Bit	Description
0-1	Read Register Command b1 b0 0 0 No Action 0 1 No Action 1 0 Read IR Register On Next IOR- Pulse 1 1 Read IS Register On Next IOR- Pulse
2	= 0: Disable Polled Mode = 1: Enable Polled Mode
3	= 1
4	= 0
5-6	Special Mask Mode b6 b5 0 0 No Action 0 1 No Action 1 0 Disable Special Mask Mode 1 1 Enable Special Mask Mode
7	= 0

Port B Status Port 061h

This register is located at I/O address 061h. The register is defined as follows:

061h	NMI Status/Control Register

Bits 4-7 are read only (must be 0 for writes)
Bits 0-3 are read/write

Bit	Description
7	System memory parity check status
6	IOCHCK- (I/O channel check) status
5	Timer 1, Counter 2 output status
4	Refresh status
3	I/O channel check NMI 1 = IOCHCK- NMI disabled 0 = IOCHCK- NMI enabled
2	System memory parity check 1 = Parity check disabled 0 = Parity check enabled
1	Speaker (Timer 1, Counter 2) 1 = on 0 = off
0	Gate signal for speaker timer 1 = Timer 1, Counter 2 (Speaker) enabled 0 = Timer 1, Counter 2 (Speaker) disabled

Counter/Timer

The timer is programmed by writing a control word and then an initial count. To set the control register of a counter, write to the control word address. The control register is a write-only location. The following table shows the addresses and format of the control words and the control word register.

Address	Function
040h-043h	Timer
040h	Counter 0 System Clock
041h	Counter 1 Refresh Request
042h	Counter 2 Speaker Tone
043h	Control Register (Write Only)

Control Register

Bit	Description
0	1 = BCD Select 0 = Binary Select
1-3	Mode Select

Bit 3	Bit 2	Bit 1	Mode
0	0	0	Mode 0 Interrupt on terminal count
0	0	1	Mode 1 Hardware retriggerable one-shot
x	1	0	Mode 2 Rate generator
x	1	1	Mode 3 Square wave generator
1	1	0	Mode 4 Software triggered strobe
1	1	1	Mode 5 Hardware retriggerable strobe

4-7 Command

Bit 7	Bit 6	Bit 5	Bit 4	Command
0	0	0	0	Latch Counter 0
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read Back Command

Read/Write Counter Command

When writing to a counter, observe the following conventions:

- Write each counter's control word before writing the initial count.
- When writing the initial count, follow the format specified in the control word (for example, least significant byte only or least significant byte, then most significant byte).
- Providing the programming format is observed, a new initial count can be written into the counter at any time after programming without rewriting the control word.

Latch Counter Command

When a Latch Counter command is issued, the current state of the counter element is latched. The count remains latched until read by the CPU or until the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the counter element can be read directly.

Read Back Command

The Read Back command allows you to check the count value, mode, and state of the OUT signal, and the Null Count Flag of the selected counter(s). The format for the Read Back command is:

Read Back Command

Bit	Description
7	Must be set To 1
6	Must be set To 1
5	0 = Latch count of selected counter
4	0 = Latch status
3	1 = Counter 3 select
2	1 = Counter 2 select
1	1 = Counter 1 select
0	Must Be 0

Status Byte

Bit	Description
7	OUT Signal State
6	Null Count Flag
4-5	Command Status
1-3	Mode Status
0	BCD/Binary Status

System Control Port 092h

The system control port can be used for gating the A20 line and resetting the CPU when switching between Real Mode and Protected Mode. This is a faster alternative to using the 8042 keyboard controller. The register is compatible with the IBM PS/2 architecture.

092h System Control Port

Bit	Description
7-2	Reserved
1	Alternate GATEA20 0 = CPUA20 is forced low. (if A20 Gate pin is low) 1 = Address bit A20 (on the CPU) goes directly to the CPUA20 pin.
0	Alternate CPU RESET 0 to 1 transition will reset the CPU after a minimum delay of 6.72 μs. Bit remains latched high until cleared or upon system reset.

Control Registers

Reading the control registers is accomplished by writing a register select byte to 01EDh and then reading from I/O address 01EFh. Writing to the control registers is similar. First write the register select index to I/O address 01EDh. Then write to I/O address 01EFh.

01EDh Control Register Index Port

Bit	Description			
7-3	Reserved			
2-0	Control Register Select			
	bit 2	bit 1	bit 0	Register
	0	0	0	Control Register 0 (CR0)
	0	0	1	Control Register 1 (CR1)
	0	1	0	Control Register 2 (CR2)
	0	1	1	Control Register 3 (CR3)
	1	0	0	Control Register 4 (CR4)
	1	0	1	Control Register 5 (CR5)

01EFh Control Register 0

Bit	Description
7	DRAM type 1 = 1M DRAMs 0 = 256K DRAMs
6-5	DRAM bank-count

6	5	Banks enabled	Interleave mode
0	0	1	0
0	1	2	2
1	0	3	0
1	1	4	4

4	Shadow enable F0000h-FFFFFh
3	Shadow enable E0000h-EFFFFh
2	Extra 384K control 1 = Relocates 384KB between 640KB and 1MB (A0000h-FFFFFh) above 1MB 0 = Leaves 384KB between 640KB and 1MB
1	Reserved (must be 0)
0	Reserved (must be 0)

01EFh Control Register 1

Bit	Description
7	Page mode enable
6	Mixed DRAM 0 = Same type all four banks 1 = Selected type for first two banks, other type for last two banks
5-3	RAS precharge timing for page misses

5	4	3	CPU clock cycles
0	0	0	16
0	0	1	14
0	1	0	12
0	1	1	10
1	0	0	8
1	0	1	6
1	1	0	4
1	1	1	2

2-0	Reserved (must be 0)

01EFh Control Register 2

Bit	Description
7-6	Reserved (must be 1)
5	Non-page mode wait states 0 = 1 wait state 1 = 0 wait states
4	Page mode wait states (when page hit) 0 = 1 wait state 1 = 0 wait states
3-2	CAS precharge time

3	2	CPU clock cycles
0	0	4
0	1	3
1	0	2
1	1	1

1-0 CAS active time

b1	b0	CPU clock cycles
0	0	4
0	1	3
1	0	2
1	1	1

Note: CAS active plus CAS precharge cycles must total 4 or less for 0 wait states and 6 or less for 1 wait state. Bits 0-3 and bit 5 have no effect when page mode is disabled (Control Register 1 - bit 7).

01EFh Control Register 3

Bit	Description
7-0	Starting address of expansion RAM (Number of 64KB segments (0-255) before expansion memory should be decoded.)

01EFh Control Register 4

Bit	Description
7-4	HT21 chip ID 0001 for Rev. C,D 0010 for Rev. E
3	I/O speed 0 = CPU clock is divided by 2 for all I/O cycles 1 = CPU clock runs at full speed for all cycles
2	Co-processor select
1	Interleave mode 0 = Word interleave 1 = Page interleave (default)
0	ROM chip select disable

01EFh Control Register 5

Bit	Description				
7	Sleep mode enable				
6-4	Frequency of sleep mode				
	6	5	4	CPU clock	I/O bus clock
	0	0	0	8 MHz	4 MHz
	0	0	1	4 MHz	2 MHz
	0	1	0	2 MHz	1 MHz
	0	1	1	1 MHz	0.5 MHz
	1	0	0	0.5 MHz	0.25 MHz
3	Hispeed switch 1 = Enable switch to Hispeed on idle (HT21 Rev. E)				
2	Parity checking disable				
1	Page interleave CAS sharing enable				
0	Reserved				

DS1285Q Real Time Clock with RAM (RTC)

Most of the setup information stored in the Real Time Clock with RAM (RTC) can be accessed through BIOS or operating system calls. However, the RTC can be accessed directly by issuing software I/O commands. Reading the RTC is accomplished by writing an index byte to 070h and then reading from I/O address 071h. Writing to the RTC is similar. First write the index to I/O address 070h. Then write to I/O address 071h.

This section lists the index values for the storable configuration bytes and defines the bit-parameters of the configuration bytes.

RTC Index Definitions

The index bytes for the RTC are defined as follows:

Index	Function
00h-09h	Time functions
0Ah-0Dh	RTC Control Registers
0Eh	Diagnostic status byte
0Fh	Shutdown status byte
10h	Diskette drive type byte (Drives A and B)
11h	Reserved
12h	Hard disk type byte (Drives C and D)
13h	Reserved
14h	Equipment byte
15h	Low base memory byte
16h	High base memory byte
17h	Low expansion memory byte
18h	High expansion memory byte
19h	Disk C extended byte
1Ah	Disk D extended byte
1Bh-2Bh	Reserved
2Ch	Bit 0 = swap disk bit
2Dh	Reserved
2Eh-2Fh	2-byte CMOS checksum
30h	Low expansion memory byte
31h	High expansion memory byte
32h	Date century byte
33h	Information flags (set during power on)
34h-3Fh	Reserved

RTC Byte Definitions

Time Functions

The RTC time functions are defined in the following table. All entries are in binary coded decimal format.

Index	Function	Range
00h	Seconds	00-59
01h	Reserved	N/A
02h	Minutes	00-59
03h	Reserved	N/A
04h	Hours	00-23
05h	Reserved	N/A
06h	Day of the week (01=Sunday)	01-07
07h	Date of the month	01-31
08h	Month	01-12
09h	Year	00-99

Diagnostic Status Byte (Index 0Eh)

Bit	Function
7	Power Loss
6	Checksum Status Indicator
5	Incorrect Configuration
4	Memory Size Compare Error
3	Fixed Disk Initialization
2	Time Status Indicator
1	Reserved
0	Reserved

Bits 0-1 - Reserved.

Bit 2 - A 0 in this bit location indicates that the time is valid. A 1 in this bit location indicates that the time is invalid.

Bit 3 - A 0 in this bit location indicates that the fixed disk and adapter are operating properly, and the system can attempt a boot up. A 1 in this bit location indicates that either the fixed disk or the adapter has failed initialization.

Bit 4 - A 0 in this bit location indicates that the power on check has determined the memory size to be the same as that stored in the configuration. A 1 in this bit location indicates that the memory size is different than that stored in the configuration.

Bit 5 - A 0 in this bit location indicates that the configuration information is correct. A 1 in this bit location indicates that the configuration information is incorrect.

Bit 6 - A 0 in this bit location indicates that the configuration checksum is good. A 1 in this bit location indicated that the configuration checksum is bad.

Bit 7 - A 0 in this bit location indicates that the Real Time Clock has not lost power. A 1 in this bit location indicates that the Real Time Clock has lost power.

Shutdown Status Byte (Index 0Fh)

The bits in this byte are defined by the power on diagnostics.

Diskette Drive Type Byte (Index 10h)

Bit	Function
4-7	Drive A Type
0-3	Drive B Type

Bits 4-7 and bits 0-3 - These bits indicate the type of diskette drive installed in the following manner:

Bit 7(3)	Bit 6(2)	Bit 5(1)	Bit 4(0)	Drive Type
0	0	0	0	No Drive Installed
0	0	0	1	Double Sided 48 TPI
0	0	1	0	High-Capacity 96 TPI
0	1	0	0	High-Density 1.44MB

Hard Disk Type Byte(Index 12h)

Bit	Function
4-7	Drive C Type
0-3	Drive D Type

Bits 4-7 - These bits define the hard disk drive type for drive C .. the following manner:

Bit 7	Bit 6	Bit 5	Bit 4	Drive Type
0	0	0	0	(0h) No Drive Installed
0	0	0	1	(1h-Eh) Define type 1-14
		TO		
1	1	1	0	
1	1	1	1	(Fh) Define type 16-255 (as defined by the Extended Drive Type Byte at 019h)

Bits 0-3 - These bits define the hard disk drive type for drive D in the following manner:

Bit 3	Bit 2	Bit 1	Bit 0	Drive Type
0	0	0	0	(0h) No Drive Installed
0	0	0	1	(1h-Eh) Define type 1-14
		TO		
1	1	1	0	
1	1	1	1	(Fh) Define type 16-255 (as defined by the Extended Drive Type Byte at 01Ah)

Drive C (19h) and Drive D (1Ah) Extended Bytes

These bits define the hard disk drive type for drive C and drive D in the following manner:

Bit 7	6	5	4	3	2	1	0	Drive Type
0	0	0	0	0	0	0	0	(00h-0Fh) Reserved
				TO				
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	(10h-FFh) defines type 16-255
				TO				
1	1	1	1	1	1	1	1	

Equipment Byte (Index 14h)

Bit	Function
7	Number Of Diskette Drives
6	Number Of Diskette Drives
5	Primary Display
4	Primary Display
3	Not Used
2	Not Used
1	Coprocessor Present
0	Diskette Drive Present

Bits 6-7 - These bits define the number of diskette drives installed in the system in the following manner:

Bit 7	Bit 6	Number Of Diskette Drives
0	0	1 Drive
0	1	2 Drives
1	0	Reserved
1	1	Reserved

Bits 4-5 - These bits define the type of display connected to the system in the following manner:

Bit 5	Bit 4	Display Type
0	0	Adapter has its own BIOS (EGA or VGA)
0	1	40 Column CGA
1	0	80 Column CGA
1	1	Monochrome Display

Bits 2-3 - Not Used.

Bit 1 - A 1 in this bit location indicates that a coprocessor is installed. A 0 in this bit location indicates that a coprocessor is not installed.

Bit 0 - A 1 in this bit location indicates that a diskette drive is installed. A 0 in this bit location indicates that a diskette drive is not installed.

Low (15h) and High (16h) Base Memory Bytes

Index 15h contains the Low Base Memory Byte and index 16h contains the High Base Memory Size Byte. The Base Memory Size bytes are defined in the following manner:

Value In 15-16h	Memory Size
0100h	256 KB
0200h	512 KB
0280h	640 KB
0400h	1024 KB

Low (17h) and High (18h) Expansion Memory Bytes

Index 17h contains the Low Expansion Memory Byte and index 18h contains the High Expansion Memory Size Byte. The Expansion Memory Size bytes are defined in the following manner:

Value In 17-18h	Expansion Memory Size
0400h	1024KB
0600h-3C00h	1536KB to 15360KB

Checksum Bytes (2Eh-2Fh)

Index 2Fh contains the Low Checksum Byte and index 2Eh contains the High Checksum Byte. The Checksum is calculated on addresses 10h-2Dh.

Date Century Byte (Index 32h)

These bits are read and set by BIOS and contain the BCD value for the century.

Information Flag (Index 33h)

Bit	Function
7	Top 128KB Memory Installed
6	First User Message Enable
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Bit 7 - A 1 in this bit location indicates that the top 128KB of base memory is installed. A 0 in this bit location indicates that the top 128KB of base memory is not installed.

Bit 6 - A 1 in this bit location causes a first user message to be displayed after initial setup. A 0 in this bit location omits the first user message displayed after initial setup.

Bits 0-5 - Reserved.

GESUALDO Custom ASIC

The GESUALDO Custom ASIC has four registers. Two registers, at 0077h and 0079h, are reserved. The other two are dedicated to system configuration. These registers are located at 0073h and 0075h and are defined in the following table:

0073h		
Bit	**Description**	**1/0**
7	Not used	
6	Configuration enable	
5-4	Not used	
3	Diskette controller CS enable	
2-1	Not used	
0	Hard disk CS enable	
0075h		
Bit	**Description**	**1/0**
7	CPU Speed	Fast/Slow
6	Serial port address	02F8h/03F8h
5-4	Reserved	Must be 0
3-0	ROM Paging (RP3-RP0)	

Diskette Drive Controller

There are several registers contained in the WD37C65 Floppy Disk Controller for configuration, status information, and command execution. These registers are listed below with their I/O addresses.

Address	Register
03F2h	Operations Register (W)
03F4h	Main Status Register (R)
03F5h	Data Register (W/R)
03F7h	Control Register (W)

Operating Modes

There are two basic operating modes of the Floppy Disk Controller. They are as follows:

Non-DMA Mode

DMA Mode

These modes comprise two basic methods of data handling between the system microprocessor, in this case the CPU, and the disk controller. In the DMA mode, the command that is to be executed need only be loaded into the controller by the CPU. The controller, along with the 8237A DMA sections of the HT21, then handle all of the controls and handshaking necessary to complete the command and transfer the data. In the Non-DMA mode of operation, the 37C65 will issue an interrupt to the CPU every time a data byte is to be transferred. It is then the responsibility of the CPU, its support peripherals, and the programmer to generate the proper handshaking and control signals to transfer the data to or from the 37C65.

Diskette Drive Controller Registers

Operations Register (03F2h)

This register is used to control drive motors, drive selection, DMA enable, and Reset. The format of this Register is as follows:

Bit	Function
7	Mode Select
6	Reserved (not used)
5	Motor Enable 2–
4	Motor Enable 1–
3	DMA Enable
2	Controller Reset–
1	Reserved (must be 0)
0	Drive Select

Bit 7 A 0 in this bit location selects AT mode. A 1 selects Special mode. This bit should be 0.

Bit 6 This bit is not used.

Bit 5 A 0 in this bit location enables the motor for Floppy Drive 2. A 1 disables it.

Bit 4 A 0 in this bit location enables the motor for Floppy Drive 1. A 1 disables it.

Bit 3 A 1 in this bit location selects DMA operation. A 0 in this bit location selects non-DMA operation.

Bit 2 A 0 in this bit location resets the 37C65. A 1 in this bit location enables normal operation.

Bit 1 Reserved. This bit should be 0.

Bit 0 This bit is used to select the Floppy Drive.

Bit 5	Bit 4	Bit 0	Drive
0	1	0	Drive 1
1	0	1	Drive 2

Main Status Register (03F4h)

The Main Status Register is a read only register that is used to support the transfer of data between the system and the controller. This register has the following format:

Bit	Function
7	Request for Master
6	Data In/Out
5	Non-DMA Mode
4	Controller Busy
3	Drive 3 Busy (not used)
2	Drive 2 Busy (not used)
1	Drive 1 Busy
0	Drive 0 Busy

Bit 7 When this bit is a 1, the Data register is ready for transfer with the system

Bit 6 This bit determines the direction of the data transfer between the data register and the system. A 1 in this bit indicates the transfer is from the data register to the system. A 0 indicates a transfer from the system to the data register.

Bit 5 When this bit is a 1, the controller is in the non-DMA mode.

Bit 4 When this bit is set to 1, a read or write command is being executed by the controller.

Bit 3 When set to 1, this bit indicates that diskette drive 3 is in the seek mode.

Bit 2 When set to 1, this bit indicates that diskette drive 2 is in the seek mode.

Bit 1 When set to 1, this bit indicates that diskette drive 1 is in the seek mode.

Bit 0 When set to 1, this bit indicates that diskette drive 0 is in the seek mode.

Data Register (03F5h)

The Data Register is a storage area that is read from or written to one byte at a time. It is used to store data, commands, parameters, and status. Data bytes are passed through the Data Register to program the Floppy Disk Controller or to obtain status after a command has been executed.

Control Register (03F7h)

When written to, this register is used to set the data transfer rate. The format of the Data Rate Register is as follows:

Bit(s)	Function
7-3	Reserved
2	Write Precompensation
1-0	Rate Select

Bits 0-1 These bits are used to select the data transfer rate of the floppy disk drive in the following manner:

Bit 1	Bit 0	Rate
0	0	500 Kbits/sec
0	1	300 Kbits/sec
1	0	250 Kbits/sec
1	1	125 Kbits/sec

Commands

The Floppy Disk Controller is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The result after the execution of the command can also be a multibyte transfer back to the processor.

Command operation consists of three phases:

Command Phase – The Floppy Disk Controller receives all information required to perform a particular operation from the processor.

Execution Phase – The Floppy Disk Controller performs the operation as instructed.

Result Phase – After completion of the operation, status and other housekeeping information are made available to the processor.

For information on specific programming commands for the floppy disk controller, please refer to the Western Digital WD37C65 Data Sheet.

Keyboard Controller

The Keyboard Controller transfers data to and from the system through the data ports at I/O addresse 060h (keyboard and mouse). A command/status port is provided at location 064h for issuing of commands to the keyboard, and reading of status from the keyboard. When the system reads the information at address 064h, it receives status from the keyboard. When the system writes data to address 064h, the Keyboard Controller interprets the data as a command.

Status Register

This is a register located at address 064h. The following is a description of the status bit definitions.

Bit	Status
7	Parity Error
6	General Time Out
5	Transmit Error
4	Inhibit Switch
3	Command Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Bit 7 - A 0 indicates the last byte received from the keyboard had odd parity. A 1 indicates the last byte received had even parity. The keyboard should send data with odd parity.

Bit 6 - A 1 indicates that a transmission was started by the keyboard but did not finish within the programmed time limit.

Bit 5 - A 1 in this bit indicates that a keyboard controller transmission was not properly completed.

Bit 4 - This bit is updated when data is placed in the output buffer. It reflects the state of the keyboard inhibit switch. A 0 in this bit means the keyboard is inhibited.

Bit 3 - The input buffer may be addressed as I/O address 60h or 64h. Address 60h is defined as a data port while address 64h is a command port. Writing to address 64h sets this bit to a 1, and writing to address 60h sets

this bit to 0. The controller uses this bit to determine if the byte in the input buffer is a data or command byte.

Bit 2 - This bit may be set to 0 or 1 by writing to the flag bit in the controller's command byte. It is set to 0 on power up reset.

Bit 1 - A 0 in this position means the input buffer at I/O address 60h or 64h is empty. A 1 indicates that data has been written into the buffer but the controller (7042) has not read it yet. When the data is read by the controller this bit is reset to 0.

Bit 0 - When this bit is a 0 it indicates that the output buffer is empty. A 1 indicates that there is data in the output buffer but the system has not yet read the data. When the system does read the data, this bit is reset to 0.

Keyboard Controller Command Summary

20-3F -- Read Keyboard Controller's RAM. Bits D5-D0 specify the address.

20 -- Read Keyboard Controller's Command Byte. The controller sends the current command byte to the output buffer.

60-7F -- Write Keyboard Controller's RAM. Bits D5-D0 specify the address.

60 -- Write Keyboard Controller's Command Byte. The next byte of data written to I/O address 60h is put in the controller's command byte. Bit definitions for the command byte are as follows:

Bit 7 - Reserved. Should be a 0.

Bit 6 - IBM Personal Computer Compatibility Mode. Writing a 1 to this bit causes the controller to convert the scan codes it receives to those used by the IBM Personal Computer.

Bit 5 - IBM Personal Computer Mode. Writing a 1 to this bit programs the keyboard to support the IBM Personal Computer keyboard interface. The controller will not check parity or convert scan codes.

Bit 4 - Disable Keyboard. Writing a 1 to this bit disables the keyboard interface by driving the clock line low. Data is not sent or received.

Bit 3 - Inhibit Override. A 1 in this bit disables the keyboard inhibit function.

Bit 2 - System Flag. The value written to this bit is put in the system flag bit of the status register.

Bit 1 - Reserved. Should be a 0.

Bit 0 - Enable Output Buffer Full Interrupt. Writing a 1 to this bit causes the controller to generate an interrupt when it places data into the output buffer.

A4 -- Test Password. This command checks if there is a password currently installed in the 7042. The test result is placed in the output buffer (I/O Address 060h). FAh means the password is installed. F1h means no password is installed.

A5 -- Load Security. This command starts the load password procedure. Following this command the 7042 will receive input from the data port until a null (0) is detected, which terminates the password entry.

A6 -- Enable Security. This command enables the 7042 security feature. This command is only valid when a password pattern is currently loaded into the 7042.

AA -- Self Test. Causes the controller to perform internal diagnostics. 55h is placed in the output buffer if no errors are encountered.

AB -- Interface Test. Causes the controller to test the keyboard clock and data lines. The result is placed in the output buffer as follows:

00 - No error detected

01 - keyboard clock line stuck low

02 - keyboard clock line stuck high

03 - keyboard data line stuck low

04 - keyboard data line stuck high

AC -- Diagnostic Dump. Sends 16 bytes of the controller's RAM, current state of the input port, current state of the output port, and the controller's program status word to the system. All items are sent in scan code format.

AD -- Disable Keyboard Interface. This disables keyboard interfacing by driving the clock line low. Data will not be sent or received.

AE -- Enable Keyboard Interface. This releases the keyboard interface.

C0 -- Read Input Port. Tells the controller to read the input port and place the data in the output buffer. This command should be used only if the output buffer is empty.

C1 -- Poll Input Port Low. Port 1 bits 0-3, in Status bits 4-7.

C2 -- Poll Input Port High. Port 1 bits 4-7, in Status bits 4-7.

D0 -- Read Output Port. Causes the controller to read the output port and place the contents in the output buffer. This command should only be used if the output buffer is empty.

D1 -- Write Output Port. The next byte of data written to I/O address 60h is placed in the output port. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

E0 -- Read Test Inputs. This causes the controller to read its T0 and T1 inputs. The data is placed in the output buffer with data bit 0 representing T0 and data bit 1 representing T1.

F0-FF -- Pulse Output Port. Bits 0-3 of the controller's output port may be pulsed low for approximately 6 microseconds. Bits 0-3 of this command indicate which bits are to be pulsed. A 0 causes the bit to be pulsed, and a 1 causes the bit not to be pulsed. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

PSSJ-3 Serial/Parallel Interface

This section describes the configuration registers of the PSSJ-3 and programming the serial and parallel printer interfaces.

PSSJ Configuration Registers

The PSSJ-3 contains three configuration registers. These registers are write protected by the configuration enable bit of the GESUALDO custom ASIC (0073h - bit 6). The configuration enable bit must be set (=1) before writing to these registers. Refer to "GESUALDO Custom ASIC" for more information.

01FBh UART clock/AT printer select

Bit	Description
0	UART clock divide by 13– 0 = serial clock/13 1 = serial clock/1
1-2	Reserved (must be 0)
3	AT compatible printer select (must be 1)
4-7	Reserved

01FDh Port enables

Bit	Description
0	Reserved
1	Printer port enable
2-3	Reserved
4	Serial port enable
5-6	Reserved
7	Printer output enable

01FE Serial Port Interrupt	
Bit	**Description**
0-1	Reserved
2	Serial port interrupt 0 = IRQ4 1 = IRQ3
3-7	Reserved

Note: The GESUALDO custom ASIC port 0075h - bit 6 should match the state of the serial port interrupt. Refer to "GESUALDO Custom ASIC" for more information.

Serial Port Registers

The following chart lists the addresses of the Serial Port registers. They are listed in hexadecimal format. The serial port can be set as COM1 or COM2.

Register	I/O Address	
	COM1	**COM2**
Receiver Buffer	3F8h	2F8h
Transmitter Holding	3F8h	2F8h
Interrupt Enable	3F9h	2F9h
Interrupt Identification	3FAh	2FAh
Line Control	3FBh	2FBh
Modem Control	3FCh	2FCh
Line Status	3FDh	2FDh
Modem Status	3FEh	2FEh
Scratch	3FFh	2FFh
Divisor Latch LSB	3F8h	2F8h
Divisor Latch MSB	3F9h	2F9h

The following is a table of register bit definitions for the serial port. The first address is for COM1, and the addresses in parentheses are for COM2.

03F8 (02F8) Read Receiver Buffer Register (Character Received)
Note: Line Control Register (3FBh/2FBh) bit 7 (DLAB) must be 0

Bit	Description
0-7	Data bits 0-7 (first bit received serially is bit 0, last is bit 7)

03F8 (02F8) Write Transmitter Holding Register (CTS)
Note: Line Control Register (3FBh/2FBh) bit 7 (DLAB) must be 0

Bit	Description
0-7	Data bits 0-7 (first bit sent serially is bit 0, last is bit 7)

03F9 (02F9) Interrupt Enable Register

Bit	Description
0	1 = Enables the Received Data Available Interrupt
1	1 = Enables the Transmitter Holding Register Empty Interrupt
2	1 = Enables Receive Line Status Interrupt
3	1 = Enables the Modem Status Interrupt
4-7	Always Logical 0

03FA (02FA) Interrupt Identification Register

Bit	Description		
0	0 = Interrupt Pending		
1-2	**Bit 2**	**Bit 1**	
	0	0	Fourth Level Priority
	0	1	Third Level Priority
	1	0	Second Level Priority
	1	1	Highest Level Priority
3-7	Always Logical 0		

03FB (02FB) Line Control Register

Bit	Description		
0-1	**Bit 1**	**Bit 0**	
	0	0	Five Bit Word Length
	0	1	Six Bit Word Length
	1	0	Seven Bit Word Length
	1	1	Eight Bit Word Length
2	0 = One Stop Bit 1 = 1 1/2 Stop Bits When Five Bit Word Length Selected. 2 Stop Bits With Six, Seven, or Eight Bit Word Length		
3	1 = Parity Enable		
4	0 = Odd Parity Select 1 = Even Parity Select		
5	Stick Parity Bit		
6	1 = Set Break Enable		
7	1 = Divisor Latch Access Bit (DLAB) Enable		

03FC (02FC) Modem Control Register

Bit	Description
0	1 = Data Terminal Ready Set (DTR) 0 = Data Terminal Ready Reset (DTR)
1	1 = Request To Send Set (RTS) 0 = Request To Send Reset (RTS)
2	Out 1 (not used)
3	Interrupt Out (Out 2) 1 = Enables Interrupt 0 = Tri-states Interrupt
4	Loop
5-7	Always Logical 0

03FD (02FD) Line Status Register	
Bit	**Description**
0	Data Ready (DR)
1	Overrun Error (OR)
2	1 = Detect Parity Error (PE)
3	1 = Detect Framing Error (FE)
4	1 = Break Interrupt (BI)
5	Transmitter Holding Register Empty 1 = Character Transferred From Holding To Shift Register 0 = Loading Transmitter Holding Register
6	Transmitter Shift Register Empty 1 = Shift Register and Holding Register are idle (empty) 0 = Transmitting data
7	Always Logical "0"

03FE (02FE) Modem Status Register

Bit	Description
0	Delta Clear To Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge Ring Indicator 1 = On 0 = Off
3	Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a 1 modem status interrupt is generated)
4	Clear To Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Received Line Signal Detect (RLSD)

03F8 (02F8) Divisor Latch LSB

Note: Line Control Register (3FBh/2FBh) bit 7 (DLAB) must be 1

Bit	Description
7-0	Bits 7-0 Least Significant Byte of the Divisor Latch - refer to "Divisor Latch Table" on the following page

03F9 (02F9) Divisor Latch MSB

Note: Line Control Register (3FBh/2FBh) bit 7 (DLAB) must be 1

Bit	Description
7-0	Bits 7-0 Most Significant Byte of the Divisor Latch refer to "Divisor Latch Table" on the following page

Divisor Latch Table (Clock is 1.8432 MHz)		
Desired Baud Rate	**Divisor Used (decimal)**	**% Error**
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19,200	6	–
38,400	3	–
56,000	2	2.860

Parallel Interface

The following table lists the address of the parallel port registers.

Register	Address
Printer Data Latch	378h
Printer Read Status	379h
Printer Control Latch	37Ah

Transfer direction

The parallel port allows either one-way or two-way data transfer:

- **Unidirectional (one-way)**. The computer uses the port only to send output to the parallel device. It does not receive input through the port.

- **Bidirectional (two-way).** The computer uses the port both to send output to the parallel device and to receive input from the device.

In the default configuration, the parallel port is set up as a two-way port. For two-way data transfer, the port must be programmed by the following method:

To receive input through the port, enable input data by writing a 1 to bit 5 of the printer control latch (37Ah).

To send output through the port, enable output data by writing a 0 to bit 5 of the printer control latch (37Ah).

The parallel port can be configured as a one-way port using the Setup utility. Refer to "The Setup Utility" for more information.

Parallel Port Registers

The following is a table of register bit definitions for the parallel port.

0378h: Printer - Data Latch	
Bit	**Description**
7-0	Data Bits 7-0
0379h: Printer - Read Status	
Bit	**Description**
0	Not Used
1	Not Used
2	Not Used
3	0 = Error
4	1 = Printer Select
5	1 = Out of Paper
6	0 = Acknowledge
7	0 = Busy

037Ah: Printer - Control Latch Bit	Description
0	1 = Strobe Low to high latches character High to low prints character
1	1 = Auto FD XT
2	0 = Initialize
3	1 = Select Printer
4	1 = Enable Interrupt
5	Directional Control 0 = Enable Output Data 1 = Enable Input Data
6	Not Used
7	Not Used


BIOS
SERVICES

BIOS Services

BIOS Services

The Basic Input/Output System (BIOS) is the lowest-level interface between other software (application programs and the operating system) and the hardware. BIOS routines provide device input/output services, as well as bootstrap, print screen, and other services. Some BIOS services, such as graphics routines, are not available through the operating system.

All BIOS calls are made through software interrupts (assembly-language "INT x" instructions). Each I/O device is provided with a software interrupt, that transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Exit parameters are generally returned in CPU registers. To ensure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS routine. To execute a BIOS call, load the registers according to the entry conditions specified in the function description. (Register AH contains the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. For example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16h
```

Upon return, AL contains the ASCII character and AH contains the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Software Interrupt Summary

The following table is a quick reference list of software interrupts for all device I/O and system status services.

Service	Software Interrupts
Video Display	10 hex (16 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)
Floppy Disk	13 hex (19 dec)
Hard Disk	13 hex (19 dec)
Serial Communications	14 hex (20 dec)
System Support	15 hex (21 dec)
Joystick	15 hex (21 dec)
Microsecond Delay	15 hex (21 dec)
Extended Memory	15 hex (21 dec)
Virtual Mode	15 hex (21 dec)
Keyboard	16 hex (22 dec)
Line Printer	17 hex (23 dec)
System Clock	1A hex (26 dec)
Floppy Disk Parameter	1E hex (30 dec)
Hard Disk 0 Parameter	41 hex (65 dec)
Hard Disk 1 Parameter	46 hex (70 dec)

Software Interrupt Classes

Interrupt 10h: Video Display Functions

Software interrupt 10h (16 decimal) accesses video display functions, summarized in the following chart. Entry and exit conditions are defined later.

Note: Functions 10h-12h and 1Ah-1Ch are EGA/VGA functions and are contained within the VGA display adapter's BIOS, if present. These functions are included here for completeness.

Routine Group	AH	Function Description
Control Routines	00h	Set CRT mode
	01h	Set cursor type
	02h	Set cursor position
	03h	Get cursor position
	04h	Read light pen position
	05h	Select active page
	06h	Scroll active page up
	07h	Scroll active page down
Text Routines	08h	Read attribute/character
	09h	Write attribute/character
	0Ah	Write character only
Graphics Routines	0Bh	Set color palette
	0Ch	Write dot
	0Dh	Read dot
Other Routines	0Eh	Write TTY* to active page
	0Fh	Get current video state
	10h	Set palette registers
	11h	Character generator
	12h	Alternate select
	13h	Write string
	1Ah	Display combination code
	1Bh	Functionality/State information
	1Ch	Video state

Video Display Function Summary

* Screen width is determined by the mode previously set. Control characters 00h-1Fh ASCII perform the usual special terminal functions. These include (but are not limited to) BEL(07h), BS(08h), LF(0Ah), and CR(0Dh).

Note: AX is modified on all video calls.

Set CRT Mode (AH = 00h)

Sets the CRT video mode.

Entry Conditions:

AH = 00h
AL = mode value, as follows:

Mode	Resolution	Colors /Palette	Text Format	Char Box	Max Pgs	Buffer Addr.
0,1(T)[1]	320x200[2]	16/256K	40x25	8x8	8	B8000
0,1(T)	320x350[2]	16/256K	40x25	8x14	8	B8000
0,1(T)[3]	360x400[2]	16/256K	40x25	9x16	8	B8000
2,3(T)	640x200[2]	16/256K	80x25	8x8	8	B8000
2,3(T)	640x350[2]	16/256K	80x25	8x14	8	B8000
2,3(T)[3]	720x400[2]	16/256K	80x25	9x16	8	B8000
4,5(G)[1]	320x200	4/256K	40x25	8x8	1	B8000
6(G)	640x200	2/256K	80x25	8x8	1	B8000
7(T)	720x350[2]	MDAMono	80x25	9x14	8	B0000
7(T)[3]	720x400[2]	VGAMono	80x25	9x16	8	B0000
D(G)	320x200	16/256K	40x25	8x8	8	A0000
E(G)	640x200	16/256K	80x25	8x8	4	A0000
F(G)	640x350	Mono	80x25	8x14	2	A0000
10(G)	640x350	16/256K	80x25	8x14	2	A0000
11(G)	640x480	2/256K	80x30	8x16	1	A0000
12(G)	640x480	16/256K	80x30	8x16	1	A0000
13(G)	320x200	256/256K	40x25	8x8	1	A0000

[1] (T) indicates a text mode; (G) indicates a graphics mode.
[2] Alternate select (AH = 12h) video BIOS call must be called to select scan lines.
[3] Default modes

Video Modes Supported

Set Cursor Type (AH = 01h)

Sets the cursor type and attribute.

Entry Conditions:
AH = 01h
CH - Bits 6-5 cause an invisible or blinking cursor
Bits 4-0 point to the start line for cursor within character cell
CL - Bits 4-0 point to the end line for cursor within character cell

Set Cursor Position (AH = 02h)

Writes (sets) cursor position.

Entry Conditions:
AH = 02h
BH = page number (see chart under AH = 0)
DH = row (0 = top row)
DL = column (0 = leftmost position)

Get Cursor Position (AH = 03h)

Reads (gets) cursor position.

Entry Conditions:
AH = 03h
BH = page number (see chart under AH = 0)

Exit Conditions:
DH = row of current cursor position (0 represents top row)
DL = column of current cursor position (0 represents left most column)
CH = cursor type currently set - Bits 4-0 point to the start line for cursor within character cell
CL = bit values: Bits 4-0 point to the end line for cursor within character cell

Select Active Page (AH = 05h)

Selects active display page (valid with color graphics adapter in alpha mode).

Entry Conditions:
AH = 05h
AL = new page value (0 based, see AH = 0 for maximum pages for each mode

Scroll Up (AH = 06h)

Scrolls active page up.

Entry Conditions:

AH = 06h
AL = number of lines to scroll; this number of lines will be blank at the bottom of the window. (0 means blank entire window)
CH = row of upper left corner of scroll window
CL = column of upper left corner of scroll window
DH = row of lower right corner of scroll window
DL = column of lower right corner of scroll window
BH = attribute (alpha modes) or color (graphics modes) to be used on blank line

Scroll Down (AH = 07h)

Scrolls active page down.

Entry Conditions:

AH = 07h
AL = number of lines to scroll; (0 means blank entire window)
CH = row of upper left corner of scroll window
CL = column of upper left corner of scroll window
DH = row of lower right corner of scroll window
DL = column of lower right corner of scroll window
BH = attribute (alpha modes) or color (graphics modes) to be used on a blank line

Read Attribute or Color/Character (AH = 08h)

Reads a character and its attribute or color at the current cursor position.

Entry Conditions:

AH = 08h
BH = display page number (0 based)

Exit Conditions:

AL = character read
AH = attribute of character (alpha modes only)

Write Attribute or Color/Character (AH = 09h)

Writes a character and its attribute or color at the current cursor position.

Entry Conditions:
AH = 09h
BH = display page number (0 based)
CX = number of characters to write
AL = character to write
BL = attribute of character (for alpha modes) or color of character (for graphics modes)

Write Character Only (AH = 0Ah)

Writes a character only (no attribute information) at current cursor position.

Entry Conditions:
AH=0Ah
BH=display page number (0 based)
CX=number of characters to write
AL=character to write
BL=color of character (graphics modes only)

Set Color Palette (AH = 0Bh)

Selects the color palette.

Entry Conditions:
AH = 0Bh
BH = 0 (Sets background color for video modes 4 and 5, sets border color for video modes 0, 1, 2, and 3, sets foreground color for video mode 6)
BL = color (0-31)

or

BH = 1 (Sets default palette for modes 4 and 5)
BL = 0 (green/red/brown)
= 1 (cyan/magenta/white)

Write Dot (AH = 0Ch)

Writes a pixel (dot).

Entry Conditions:
AH = 0Ch
BH = display page number
DX = row number
CX = column number

Exit Conditions:
AL = color value. When Bit 7 of AL is set, the resultant color value of the dot is the XOR (exclusive OR) of the current dot color value and the value in AL.

Read Dot (AH = 0Dh)

Reads a pixel (dot).

Entry Conditions:
AH = 0Dh
BH = display page number (0 based)
DX = row number
CX = column number

Exit Conditions:
AL = color value of dot read

Write TTY (AH = 0Eh)

Writes a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions:
AH = 0Eh
AL = character to write
BL = foreground color (graphics mode)

Get CRT Mode (AH = 0Fh)

Get the current video mode.

Entry Conditions:
AH = 0Fh

Exit Conditions:

AL = current video mode. See "Set CRT Mode (AH = 0)" for values.
AH = number of columns on screen
BH = current active display page

Set Palette Registers (AH = 10h)

This class of interrupt is a group of subfunctions that set or read the palette registers. The value in AL determines the item that is set or read.

The first chart in this section summarizes the functions available when AH = 10h. Entry and exit conditions applicable to these functions are defined following the chart.

Summary of Palette Register Functions

AL	Description of function
00h	Set individual palette register
01h	Set overscan register
02h	Set all palette and overscan registers
03h	Set intensity/blink bit
07h	Read individual palette register
08h	Read overscan register
09h	Read all palette and overscan registers
10h	Set individual color register
12h	Set block of color registers
13h	Select color page (not valid for mode 13h)
15h	Read individual color register
17h	Read block of color registers
1Ah	Read color page status
1Bh	Sum color registers to gray shades

Summary of Palette Register Functions

Set Individual Palette Register (AL = 00h)

Entry conditions:

AH = 10h
AL = 00h Set individual palette
BL = palette register to set
BH = value to set

Set Overscan Register (AL = 01h)

Entry conditions:

AH = 10h
AL = 01h
BH = value to set

Set Overscan and All Palette Registers (AL = 02h)

Entry conditions:

AH = 10h
AL = 02h
ES:DX = pointer to 17-byte table:
Byte 16 = overscan value
Bytes 15-0 = palette values

Set Intensity/blink Bit (AL = 03h)

Entry conditions:

AH = 10h
AL = 03h
BL = 00h Enable background intensity
= 01h Enable foreground blinking

Read Individual Palette Register (AL = 07h)

Entry conditions:

AH = 10h
AL = 07h
BL = palette register to be read

Exit conditions:

BH = value read

Read Overscan Register (AL = 08h)

Entry conditions:
AH = 10h
AL = 08h

Exit conditions:
BH = value read

Read Overscan and all Palette Registers (AL = 09h)

Entry conditions:
AH = 10h
AL = 09h

Exit conditions:
ES:DX = pointer to buffer (17-byte) for return values:
Byte 16 = overscan value,
Bytes 15 - 0 = register color values

Set Individual Color Register (AL = 10h)

Entry conditions:
AH = 10h
AL = 10h
BX = color register to set
DH = red value to set
CH = green value to set
CL = blue value to set

Set Block of Color Registers (AL = 12h)

Entry conditions:
AH = 10h
AL = 12h
ES:DX = pointer to table of color values (table format: red, green, blue, red, green, blue)
BX = first color register to set
CX = number of color registers to set

Set Color Page
(AL = 13h, not valid for video mode 13h)

Entry conditions:

AH = 10h
AL = 13h
BL = 00h Set color paging mode
BH = 00h Set 4 blocks of 64 registers
= 01h Set 16 blocks of 16 registers
or

BL = 01h Set color page
BH = Set page number (0-based, see AH = 0 for maximum page)

For 64-block/register mode, select:

00h (First block of 64 color registers)
01h (Second block of 64 color registers)
02h (Third block of 64 color registers)
03h (Fourth block of 64 color registers)
04h (Fifth block of 16 color registers)
05h (Sixth block of 16 color registers)
06h (Seventh block of 16 color registers)
07h (Eighth block of 16 color registers)
08h (Ninth block of 16 color registers)
09h (Tenth block of 16 color registers)
0Ah (Eleventh block of 16 color registers)
0Bh (Twelfth block of 16 color registers)
0Ch (Thirteenth block of 16 color registers)
0Dh (Fourteenth block of 16 color registers)
0Eh (Fifteenth block of 16 color registers)
0Fh (Sixteenth block of 16 color registers)

Note: The SET mode function (INT 10h, AH = 0) defaults to the 64-register/block mode and only sets the first 64 color registers active. When page selection is used, alternate blocks of color registers must be initialized.

Read Individual Color Register (AL = 15h)

Entry conditions:

AH = 10h
AL = 15h
BX = color register to read

Exit conditions:

DH = red value read
CH = green value read
CL = blue value read

Read Block of Color Registers (AL = 17h)

Entry conditions:

AH = 10h
AL = 17h
BX = initial color register to read
CX = number of color registers to read
ES:DX = pointer to a buffer to store the color register values
(format: red, green, blue, red, green, blue)

Exit conditions:

ES:DX = pointer to values read

Read Color Page Status (AL = 1Ah)

Entry conditions:

AH = 10h
AL = 1Ah

Exit conditions:

BL = current paging mode
BH = current page

Sum Color Registers to Gray Shades (AL = 1Bh)

Entry Conditions:

AH = 10h
AL = 1Bh
BX = initial color register to sum
CX = number of registers to sum

Note: This call reads the red, green and blue values stored in the specified color registers and performs a weighted sum:

Gray shade = 30% red + 59% green + 11% blue.

The resulting red, green, and blue values are written to the specified color registers. The original contents of each register are not retained.

Character Generator Functions (AH = 11h)

This class of interrupt is a group of 14 subfunctions that, in one way or another, permit the loading and/or enabling of text mode and graphics mode character generators (fonts). For all these subfunctions, AH = 11h; the value in AL determines the specific subfunction to be performed.

The first table in this section summarizes the character generator subfunctions. The rest of this section summarizes the entry and exit conditions applicable to these functions.

AL	Description of function
00h	Load user specified alphanumeric font
01h	Load ROM 8 x 14 font
10h	Load user font & adjust character height
11h	Load ROM 8 x 14 font & adjust height
12h	Load ROM 8 x 8 double dot font
14h	Load ROM 8 x 16 font
20h	Set user graphics font pointer at INT 1Fh
21h	Set user graphics font pointer at INT 43h
22h	Use ROM 8 x 14 font for graphics
23h	Use ROM 8 x 8 dot font for graphics
24h	Use ROM 8 x 16 font for graphics
30h	Font pointer information

Summary of Character Generator Subfunctions

Load User Specified Alphanumeric Font (AL = 00h)

Entry Conditions:

AH = 11h
AL = 00h
BH = number of bytes per character
BL = block to load (0-7)
CX = number of characters to store
DX = character offset of first character
in ES:BP table
ES:BP = pointer to the user table

Load ROM 8x14 Font (AL = 01h)

Entry Conditions:

AH = 11h
AL = 01h
BL = block to load (0-7)

Load 8x8 Double Dot Font (AL = 02h)

Entry Conditions:

AH = 11h
AL = 03h
BL = select character generator block(s)
If Bit 3(BL)=0, Bits 1,0(BL) select a block, 0-3
If Bit 3(BL)=1, Bits 3,2(BL) select a block, 0-3

Load User Font & Adjust Character Height (AL = 10h)

Entry Conditions:

AH = 11h
AL = 10h
BH = number of bytes per character
BL = block to load (0-7)
CX = number of characters to store
DX = offset to first character in ES:BP table
ES:BP = pointer to table

Load ROM 8x14 Font (AL = 11h)

Entry Conditions:

AH = 11h
AL = 11h
BL = block to load (0-7)

Load ROM 8x8 Double Dot Font (AL = 12h)

Entry Conditions:

AH = 11h
AL = 12h
BL = block to load

Load ROM 8x16 Font (AL = 14h)

Entry Conditions:

AH = 11h
AL = 14h
BL = block to load

Set User Graphics Font Pointer at INT 1Fh (AL = 20h)

This subfunction sets the graphics font pointer to the vector contained in INT 1Fh. The INT 1Fh vector is specified in ES:BP.

Entry Conditions:

AH = 11h
AL = 20h
ES:BP = pointer to store at INT 1Fh vector (which points to the user graphics font table)

Set User Graphics Font Pointer at INT 43h (AL = 21h)

Entry Conditions:

AH = 11h
AL = 21h
BL = rows on screen specifier:
= 00h User supplied value (DL = rows)
= 01h 14 rows
= 02h 25 rows
= 03h 43 rows
ES:BP = pointer to user table
CX = points (bytes/character)

Use ROM 8x14 Font for Graphics (AL = 22h)

Entry Conditions:

AH = 11h
AL = 22h
BL = row specifier

Use ROM 8x8 Double Dot Font for Graphics (AL = 23h)

Entry Conditions:

AH = 11h
AL = 23h
BL = row specifier

Use ROM 8x16 Font for Graphics (AL = 24h)

Entry Conditions:

AH = 11h
AL = 24h
BL = row specifier

Font Pointer Information (AL = 30h)

Entry Conditions:

AH = 11h
AL = 30h
= font pointer
BH = 00h return current INT 1Fh pointer
= 01h return current INT 44h pointer
= 02h return ROM font 8x14 pointer
= 03h return current ROM 8x8 font pointer
= 04h return current ROM 8x8 font pointer (top)
= 05h return current ROM 9x14 font alternate
= 06h return current ROM 8x16 font pointer
= 07h return current ROM 9x16 font alternate

Exit Conditions:

CX = bytes per character
DL = maximum screen row number
ES:BP = pointer to character table

Alternate Select (AH = 12h)

Alternate select allows the user to enable or disable certain operations which are standard video mode defaults.

Return VGA Information:
BL = 10h

Entry Conditions:
AH = 12h
BL = 10h

Exit Conditions:
BL = memory available
= 00h 64K
= 01h 128K
= 02h 192K
= 03h 256K
BH = 00h color mode set
= 01h monochrome mode set
CH = adapter bits
CL = switch setting

Switch to Alternate Print Screen Routine (BL = 20h)

Entry Conditions:
AH = 12h
BL = 20h

Select Scan Lines for Alphanumeric Modes (BL = 30h)

Entry Conditions:
AH = 12h
BL = 30h
AL = 00h 200 scan lines
= 01h 350 scan lines
= 02h 400 scan lines

Exit Conditions:
AL = 12h Function supported

Default Palette Loading During Set Mode (BL = 31h)

Entry Conditions:
AH = 12h
BL = 31h
AL = 00h Enable default palette loading
= 01h Disable default palette loading

Exit Conditions:
AL = 12h Function supported

Video Enable/Disable (BL = 32h)

Entry Conditions:
AH = 12h
BL = 32h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Summing to Gray Shades (BL = 33h)

Entry Conditions:
AH = 12h
BL = 33h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Enable/Disable Cursor Scaling (BL = 34h)

Entry Conditions:
AH = 12h
BL = 34h
AL = 00h Enable
= 01h Disable

Exit Conditions:
AL = 12h Function supported

Display Switch (BL = 35h)

Entry Conditions:

AH = 12h
BL = 35h
AL = 00h Turn off initial video adapter (Must have 128 byte save area pointed to by ES:DX)
= 01h Turn on initial system board video
= 02h Disable active video (Must have save buffer pointer in ES:DX)
= 03h Enable inactive video (Must have ES:DX pointer to previously filled save buffer)
ES:DX= pointer to switch state save area buffer

Exit Conditions:

AL = 12h Function supported

Note: If a conflict arises between the on-board video and an external video adapter, the on-board video is initialized inactive. If no conflict arises, both video systems remain active, and this function allows switching between the two systems.

Video Screen ON/OFF (BL = 36h)

Entry Conditions:

AH = 12h
BL = 36h
AL = 01h Screen OFF
= 00h Screen ON

Exit Conditions:

AL = 12h Function supported

Write String (AH = 13h)

Writes a string of characters.

Entry Conditions:

AH = 13h
ES:BP = pointer to string of characters to write
CX = number of string characters to display
DX = starting cursor position (DH=row, DL=column)
BH = page number (for alpha modes)
BL = attribute for characters (If attributes are not in the string, see below)
AL = 0 Cursor is not moved, string is characters only, attribute is in BL
= 1 Moves cursor to the next character position after the last character written, string is characters only, attribute is in BL
= 2 Cursor is not moved, string has alternating characters and attributes
= 3 Moves cursor to the next character position after the last character written, string has alternating characters and attributes

Read/Write Display Code (AH = 1Ah)

Read and write the display combination code for various combinations of video adapter and monitor hardware.

Display Code Chart

This chart defines the codes used by the display code functions.

Display Codes	Description
00h	No display attached
01h	Monochrome Display Adapter (MDA) with monochrome monitor
02h	Color Graphics Adapter (CGA) with color monitor
03h	Reserved
04h	Enhanced Graphics Adapter (EGA) with color monitor
05h	EGA with monochrome monitor
06h	Professional Graphics Adapter (PGA) with color monitor
07h	Video Graphics Array (VGA) with monochrome analog monitor
08h	VGA with color analog monitor
09h-0Ah	Reserved
0Bh	Multi-color Graphics Array (MCGA) with monochrome analog monitor
0Ch	MCGA with color analog monitor
0Dh-FEh	Reserved
FFh	Reserved

Read Display Combination Code (AL = 00h)

See "Display Code Chart" for definitions of code values.

Entry Conditions:
AH = 1Ah
AL = 00h

Exit Conditions:
AL = 1AhFunction supported
BL = active display code
BH = inactive display code

Write Display Code (AL = 01h)

See "Display Code Chart" for definitions of code values.

Entry Conditions:
AH = 1Ah
AL = 01h
BL = active display code
BH = alternate display code

Exit Conditions:
AL = 1Ah Function supported

Functionality/State Information (AH = 1Bh)

Returns information about the video subsystem. See the functionality/state table below.

Entry Conditions:
AH = 1Bh
BX = 0000h Implementation Type
ES:DI = Pointer to 40h byte Functionality/State Table

Exit Conditions:
Functionality/State Information in buffer
AL = 1Bh Function supported

Offset	Size	Description
DI+00h	1 word	Offset from top of Functionality/State table
DI+02h	1 word	Segment of functionality/state table
DI+04h	1 Byte	Video Mode
DI+05h	1 Word	Number of screen columns
DI+07h	1 Word	Length of display buffer in bytes
DI+09h	1 Word	Starting address of display buffer
DI+0Bh	1 Word	Cursor positions for all 8 video pages
DI+IBh	1 Word	Cursor type
DI+IDh	1 Byte	Active page
DI+IEh	1 Word	CRT controller base address
DI+20h	1 Byte	Current 3x8 register value
DI+21h	1 Byte	Current 3x9 register value
DI+22h	1 Byte	Number of screen rows
DI+23h	1 Word	Character height in scan lines
DI+25h	1 Byte	Active display combination code
DI+26h	1 Byte	Inactive display combination code
DI+27h	1 Byte	# colors available in video mode
DI+29h	1 Byte	Display pages supported for current video mode
DI+2Ah	1 Byte	Number of scan lines in current video mode: 00 = 200 01 = 350 02 = 400 03 = 480
DI+2Bh	1 Byte	Primary character block number (0-255)
DI+2Ch	1 Byte	Secondary character block number (0-255)

Funtionality/State Table

Offset	Size	Description
DI+2Dh	1 Byte	Miscellaneous state information Bits 7-6 Reserved Bit 5=0 Background intensity = 1 Blinking Bit 4=1 Cursor emulation active Bit 3=1 Mode set palette loading is disabled Bit 2=1 Mono display is attached Bit 1=1 Gray scale summing active Bit 0=1 All modes on all displays active
DI+2Eh	1 Byte	Reserved
DI+2Fh	1 Byte	Reserved
DI+30h	1 Byte	Reserved
DI+31h	1 Byte	Video memory available 00 = 64K 01 = 128K 02 = 192K 03 = 256K
DI+32h	1 Byte	Save pointer state info (1=active) Bits 7-6 = Reserved Bit 5 = Display Combination Code Extension Bit 4 = Palette override Bit 3 = Graphics font override Bit 2 = Text mode font override Bit 1 = Dynamic save area Bit 0 = 512-character set
DI+33h to 3Fh	13 Bytes	Reserved
00h		Video modes supported (1=supported) Bit 7 = mode 07h Bit 6 = mode 06h Bit 5 = mode 05h Bit 4 = mode 04h Bit 3 = mode 03h Bit 2 = mode 02h Bit 1 = mode 01h Bit 0 = mode 00h

Functionality/State Table (continued)

Offset	Size	Description
01h		Video modes supported (1=supported) Bit 7 = mode 0Fh Bit 6 = mode 0Eh Bit 5 = mode 0Dh Bit 4 = mode 0Ch Bit 3 = mode 0Bh Bit 2 = mode 0Ah Bit 1 = mode 09h Bit 0 = mode 08h
02h		Video modes supported (1=supported) Bits 7-4 = Reserved Bit 3 = mode 13h Bit 2 = mode 12h Bit 1 = mode 11h Bit 0 = mode 10h
03h-06h		Reserved
07h		Scan line modes available for text modes (1=supported) Bits 7-3 = Reserved Bit 2 = 400 Bit 1 = 350 Bit 0 = 200
08h		Number of character blocks available in text modes
09h		Maximum number of active character blocks available in text modes
0Ah		Miscellaneous (1 = supported) Bit 7 = Color paging Bit 6 = Color palette Bit 5 = EGA palette Bit 4 = Cursor emulation Bit 3 = Default palette loading Bit 2 = Character font loading Bit 1 = Gray scale summing Bit 0 = All modes on all displays

Funtionality/State Table (continued)

0Bh		Miscellaneous (1 = supported) Bits 7-4 Reserved Bit 3 = Display combination codes Bit 2 = Background intensity/blinking control Bit 1 = Save/restore video state Bit 0 = Light pen
0Ch-0Dh		Reserved
0Eh		Save pointer functions(1=supported) Bits 7-6 = Reserved Bit 5 = DCC extension Bit 4 = Palette override Bit 3 = Graphics font override Bit 2 = Text mode font override Bit 1 = Dynamic save area Bit 0 = 512 character set
0Fh		Reserved

Functionality/State Table (continued)

Save/Restore Video State (AH = 1Ch)

These subfunctions save and restore the current video state.

Save/Restore Buffer Size (AL = 00h)

Entry Conditions:

AH =1Ch
AL =00h
CX =video state to store
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state

Exit Conditions:

AL = 1Ch Function is supported
BX = buffer size block count (1 block = 64 bytes)

Save Current Video State (AL = 01h)

Entry Conditions:

AH = 1Ch
AL = 01h
CX = video state to store
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state
ES:BX = pointer to buffer save state

Exit Conditions:

AL = 1Ch Function is supported

Restore Video State (AL = 02h)

Entry Conditions:

AH = 1Ch
AL = 02h
CX = video state to restore
Bit 0 = 1 hardware state
Bit 1 = 1 video BIOS state
Bit 2 = 1 DAC state
ES:BX = pointer to previously saved buffer

Exit Conditions:

AL = 1Ch Function is supported

Interrupt 11h: Equipment Functions

Equipment functions return the equipment flag (hardware configuration of the computer system) in the AX register. Various bits in the equipment flag indicate the presence or absence of particular devices.

Any device bit that is set (has a value of 1) indicates that the specified device is in the system. A device bit that is reset (has a value of 0) indicates the specified device is not in the system.

The equipment flag bits have the following meanings:

Bits	Function
15,14	number of printers
13,12	not used
11,10,9	number of RS-232 cards
8	not used
7,6	number of diskette drives (only if Bit 0=1) 00 = 1 01 = 2
5,4	initial video mode 01 = 40x25 BW on color graphics adapter 10 = 80x25 BW on color graphics adapter 11 = 80x25 BW on monochrome text adapter
3	not used
2	pointing device 0,1
1	math coprocessor 0,1
0	diskette drive 0,1

Interrupt 12h: Memory Size Functions

This service returns the total number of kilobytes of RAM in the computer (contiguous starting from address 0) in AX. The maximum value returned is 640 (280h).

Software Interrupt: 12h (18 dec)

Interrupt 13h: Diskette Drive I/O Support Functions

These routines control diskette drive operation. The function performed depends on the value in AH:

Value in AH	Description of Function
00h	Reset all disks
01h	Return status of last disk operation
02h	Read sectors from disk
03h	Write sectors to disk
04h	Verify sectors on disk
05h	Format track on disk
08h	Read drive parameters
15h	Read disk type
16h	Get diskette change line status
17h	Set diskette type for format
18h	Set media type for format

Reset All Disks

Resets the floppy diskette system, reset associated hardware, and recalibrate all drives.

Entry Conditions:
AH = 00h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Return Status of Last Diskette Operation

Return the status of the last diskette operation in AH.

Entry Conditions:
AH = 01h
DL = 80h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Read Sectors From Disk

Reads the specified sectors from disk into RAM.

Entry Conditions:

AH = 02h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to read (1-18)
ES:BX = pointer to disk buffer

Exit Conditions:

See "Exits From All Floppy Disk Calls."

Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:

AH = 03h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to write (1-18)
ES:BX = pointer to disk buffer

Exit Conditions:

See "Exits From All Floppy Disk Calls."

Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:

AH = 04h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
CL = sector number (1-18)
AL = number of sectors to verify (1-18)

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Format Track On Disk

Format the specified track.

Note: Function Call 23 must be performed before using this routine.

To format 360K diskettes, change the gap length for format and end of track parameters of the Floppy Disk Parameter table (INT 1Eh). Restore these parameters when formatting is complete.

Entry Conditions:
AH = 05h
DL = drive number (0-1)
DH = head number (0-1)
CH = track number (0-79)
AL = number of sectors per track (used only for DMA bound check)
ES:BX = pointer to sector format table consisting of four bytes per sector:
The first byte is the track number
The second byte is the head number
The third byte is the sector number
The fourth byte is the sector size code:
00 = 128 bytes/sector
01 = 256 bytes/sector
02 = 512 bytes/sector
03 = 1024 bytes/sector

Example: For Track 0, Head 1, on a nine-sector/track diskette formatted with an interleave of 1 (512 bytes/sector) the table would be:

00h,01h,01h,02h; 00h,01h,02h,02h; 00h,01h,03h,02h;
00h,01h,04h,02h; 00h,01h,05h,02h; 00h,01h,06h,02h;
00h,01h,07h,02h; 00h,01h,08h,02h; 00h,01h,09h,02h

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Read Drive Parameters

Read parameter table for the selected drive.

Entry Conditions:
AH = 08h
DL = drive number (0-1)

Exit Conditions:
ES:DI = Floppy Disk Parameter table
CH = maximum number of tracks (low 8 bits of 10-bit value)
CL = Bits 7-6: Maximum number of tracks (high 2 bits of 10-bit value)
Bits 5-0: Maximum sectors per track
DH = maximum head number
DL = number of disk drives installed
BH = 0

BL = Bits 7-4: 0
Bits 3-0: Drive type value in CMOS:
0 Drive type known but CMOS type is invalid, CMOS is not present, CMOS battery discharged or CMOS checksum invalid
1 360KB, 5¼-inch, 40 track
2 1.2 Mb, 5¼-inch, 80 track
3 720K, 3½-inch, 80 track
4 1.44 Mb, 3½-inch, 80 track

Read Disk Type

Return the disk type.

Entry Conditions:
AH = 15h
DL = drive number (0-1)

Exit Conditions:
[C] = Error (possibly no drive installed)
[NC] = Operation successful. Status in AH
AH = 0 not present
= 1 diskette with no change line
= 2 diskette with change line
= 3 hard disk

Get Disk Change Line Status

Test to see if diskette has changed.

Entry Conditions:
AH = 16h
DL = drive number (0-1)

Exit Conditions:
AH = 00 [NC] diskette has not changed
= 06 [C] diskette has changed

Also, see "Exits From All Floppy Disk Calls."

Set Disk Type for Format

Set the diskette type for the next FORMAT command.

Entry Conditions:
AH = 17h
AL = 00 not used
= 01 360K media in a 360K drive
= 02 360K media in a 1.2M drive
= 03 1.2M media in a 1.2M drive, or 1.44M media in a 1.44M drive
= 04 720K disk in 720K drive
DL = drive number (0-1)

Exit Conditions:
See "Exits From All Floppy Disk Calls."

Set Media Type for Format

Set the media type for the selected drive.

Entry Conditions:
AH = 18h
DL = drive number (0-1)
CH = number of tracks (low 8 bits of 10-bit value)
CL = Bits 7-6: Number of tracks (high 2 bits of 10-bit value)
Bits 5-0: Sectors per track

Exit Conditions:
ES:DI=Floppy Disk Parameter table

Also, see "Exits From All Floppy Disk Calls."

Exits From All Floppy Disk Calls

[NC] = operation was successful (AH = 00h)
[C] = operation failed
AH = 01h Bad command or parameter
= 02h Address mark not found
= 03h Write protected
= 04h Sector not found
= 06h Diskette has changed
= 08h DMA overrun error
= 09h DMA boundary error
= 10h Bad CRC on disk read
= 20h Controller failed
= 40h Seek failed
= 80h Device timeout

Interrupt 1Eh: Diskette Drive Parameter Functions

This interrupt accesses the double word pointer to the current diskette drive parameter block. To change the way the floppy disk driver operates, build another parameter block and load the segment and offset of this parameter block into the software interrupt 1E hex vector area.

The layout of the Floppy Disk Parameter table is:

Offset	Length	Description
00	1 byte	First specify byte
01	1 byte	Second specify byte
02	1 byte	Number of ticks to wait before turning disk drive motor off
03	1 byte	Number of bytes per sector: 0 = 128 bytes per sector 1 = 256 bytes per sector 2 = 512 bytes per sector 3 = 1024 bytes per sector
04	1 byte	Sectors per track
05	1 byte	Gap length
06	1 byte	Data transfer length
07	1 byte	Gap length for format
08	1 byte	Fill byte for format
09	1 byte	Head settle time (ms)
0A	1 byte	Motor startup time (increments of 1/8 second)

Interrupt 13h: Hard Disk I/O Support

The following routines provide access to hard disk operations, depending on the value in AH:

Value in AH	Description of Function
00h	Reset all disks
01h	Return status of last disk operation
02h	Read sectors from disk
03h	Write sectors to disk
04h	Verify sectors on disk
05h	Format track on disk
06h	Unused
07h	Unused
08h	Return current hard disk parameters
09h	Initialize hard disk parameters
0Ah	Read long
0Bh	Write long
0Ch	Perform seek on hard disk
0Dh	Reset hard disk
0Eh	Unused
0Fh	Unused
10h	Test for hard disk ready
11h	Recalibrate hard disk
12h	Unused
13h	Unused
14h	Controller internal diagnostic
15h	Read disk type

Reset Hard Disks

Reset the hard disk system. Reset associated hardware, and recalibrate all drives.

Entry Conditions:

AH=00h
DL=drive number (80h-81h)

Exit Conditions:

See "Exits From All Hard Disk Calls."

Return Status of Last Hard Disk Operation

Return the status of the last hard disk operation in AL.

Entry Conditions:
AH = 01h
DL = 80h

Exit Conditions:
AL = status of the last operation. See "Exits From All Hard Disk Calls," for values.

Read Sectors From Disk

Read the specified sectors from disk into RAM.

Entry Conditions:
AH = 02h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to read (1-80h)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:
AH = 03h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to write (1-80 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:
AH = 04h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1-17)
AL = number of sectors to verify (1-80 hex)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Format Track On Disk

Formats the specified track.

Entry Conditions:
AH = 05h
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023)
(See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
ES:BX = pointer to sector format table consisting of two bytes for each sector. The first byte is 00 for a good sector, and 80h for a bad sector. The second byte is the sector number.

Example: For a 17-sector track with an interleave of 2, the table is:

```
00h,01h;  00h,0Ah;  00h,02h;  00h,0Bh;  00h,03h;  00h,0Ch;
00h,04h;  00h,0Dh;  00h,05h;  00h,0Eh;  00h,06h;  00h,0Fh;
00h,07h;  00h,10h;  00h,08h;  00h,11h;  00h,09h
```

Exit Conditions:
See "Exits From All Hard Disk Calls."

Return Current Hard Disk Parameters

Returns current parameter values for the specified hard disk.

Entry Conditions:
AH = 08h
DL = drive number (80h-81h)

Exit Conditions:
DL=number of hard disk drives attached
DH=maximum usable value for head number
CH=least significant part of maximum usable value for cylinder number
CL Bits 7-6 = most significant part of maximum usable value for cylinder number
CL Bits 5-0 = maximum usable value for sector number
See also "Exits From All Hard Disk Calls."

Initialize Hard Disk Parameters

Initialize the hard disk parameters for the specified hard disk. The values are taken from the current drive parameter table pointed to by INT 41h for Drive 80h, and INT 46h for Drive 81h.

Entry Conditions:
AH= 09h
DL= drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Read Long

Read specified sectors and four ECC bytes per sector from disk to RAM.

Entry Conditions:
AH = 0Ah
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023). (See CL Bits 7, 6)
CL Bits 7, 6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1 -17)
AL = number of sectors to read (1-79 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Write Long

Write specified sectors plus four ECC bytes per sector from RAM to disk.

Entry Conditions:
AH = 0Bh
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023).
(See CL Bits 7, 6)
CL Bits 7-6 = most significant part of cylinder number
CL Bits 5-0 = sector number (1 -17)
AL = number of sectors to write (1-79 hex)
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Perform Seek On Hard Disk

Seek to the specified hard disk track.

Entry Conditions:
AH = 0Ch
DL = drive number (80h-81h)
DH = head number (0-15)
CH = least significant part of cylinder number (0-1023).
(See CL Bits 7, 6)
CL Bits 7-6 = most significant part of cylinder number
ES:BX = pointer to disk buffer

Exit Conditions:
See "Exits From All Hard Disk Calls."

Reset Hard Disk

Reset the hard disk system. Reset associated hardware, and recalibrate all hard disk drives.

Entry Conditions:
AH = 0Dh
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Test For Hard Disk Ready

Determine whether a specified hard disk is ready.

Entry Conditions:
AH = 10h
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Recalibrate Hard Disk

Recalibrate the specified hard disk drive.

Entry Conditions:
AH = 11h
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Controller Internal Diagnostics

Perform internal hard disk controller diagnostics.

Entry Conditions:
AH = 14h
DL = drive number (80h-81h)

Exit Conditions:
See "Exits From All Hard Disk Calls."

Read Disk Type

Return the disk type and the number of sectors available on the hard disk.

Entry Conditions:
AH = 15h
DL = drive number (80h-81h)

Exit Conditions:
AH = 0 Not present
= 3 Hard disk drive
CX:DX = Number of sectors available on the hard disk.
(Assumes 512 byte sectors)

Exits From All Hard Disk Calls

[NC] = operation was successful (AH = 00h)
[C] = operation failed
AH = 01h Bad command or parameter
= 02h Address mark not found
= 03h Write protect error
= 04h Sector not found
= 05h Reset failed
= 07h Drive parameter command failed
= 08h DMA overrun
= 09h DMA boundary error
= 0Ah Bad sector flag detected
= 0Bh Bad cylinder detected
= 0Dh Invalid number of sectors on format
= 0Eh Control data address mark detected
= 0Fh DMA arbitration level out of range
= 10h Bad ECC on disk read
= 11h Data corrected during read
= 20h Controller failed
= 40h Seek failed
= 80h Device timeout
= AAh Drive not ready
= BBh Undefined error occurred
= CCh Write error

Interrupts 41h and 46h: Hard Disk Parameter Functions

Characteristics of the hard disk are stored in the Hard Disk Parameter table. To read the values, load the segment and offset stored at the INT 41h for hard disk 0 and INT 46h for hard disk 1. The current drive parameters can be found using INT 13h AH=08h, Read Drive Parameters.

The layout of the Hard Disk Parameter table is:

Offset	Length	Description
00h	2 bytes	Maximum number of cylinders
02h	1 byte	Maximum number of heads
03h	2 bytes	Reserved
05h	2 bytes	Starting write precompensation cylinder
07h	1 byte	Reserved
08h	1 byte	Control byte: Bit 7: Disable retries Bit 6: Disable retries Bit 5: Defect map present at Maximum Cylinder+1 Bit 3: More than 8 heads Bits 2-0: Reserved
09h	1 byte	Reserved
0Ah	1 byte	Reserved
0Bh	1 byte	Reserved
0Ch	2 bytes	Landing zone
0Eh	2 bytes	Sectors per track
0Fh	1 byte	Reserved

Interrupt 14h: Serial Communications Functions

These routines provide asynchronous byte-stream I/O to and from the RS-232C serial communications port. The function performed depends on the value in AH, and the port affected depends on the value in DX:

Register and Value	Meaning
AH = 00h	Initialize comm port
AH = 01h	Transmit character
AH = 02h	Receive character
AH = 03h	Get current comm status
DX=0 or 1	Port number

Initialize Comm Port

Initialize the communication port according to the parameters in AL and DX.

Entry Conditions:

DX = Communications port number (0 or 1)
AL = RS-232C parameters, as follows:
AH = 00h

Baud Rate (Bits 7 6 5)	Parity (Bits 4 3)	Stop Bits (Bit 2)	Word Length (Bits 1 0)
000 = 110 baud 001 = 150 baud 010 = 300 baud 011 = 600 baud 100 = 1200 baud 101 = 2400 baud 110 = 4800 baud 111 = 9600 baud	x0 = none 01 = odd 11 = even	0 = 1 bit 1 = 2 bits	10 = 7 bits 11 = 8 bits

Exit Conditions:

AX = RS-232 status; see "Get Current Comm Status" (AH = 03h)

Transmit Character

Transmit (output) the character in AL

Entry Conditions:

AH=01h
AL=character to transmit
DX=port number (0 or 1)

Exit Conditions:

AH=RS-232 status; see "Get Current Comm Status (AH = 03h). If Bit 7 is set, the routine is unable to transmit the character because of a timeout error.
AL is preserved.

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH contains the RS-232 status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout Bit (7), if set, indicates that data set ready was not received. Thus, AH is non zero only when an error occurs. If Bit 7 is set, the other bit values are not meaningful.

Entry Conditions:

AH=02h
DX=port number (0 or 1)

Exit Conditions:

AL=character received
AH=RS-232 status; see "Get Current Comm Status" (AH = 03h)

Get Current Communications Port Status

Read the communication port status in AX.

Entry Conditions:

AH=03h
DX=port number (0 or 1)

Exit Conditions:

AH = RS-232 status, as follows (set = true):
- Bit 7 = timeout occurred
- Bit 6 = transmitter shift register empty
- Bit 5 = transmitter holding register empty
- Bit 4 = break detect
- Bit 3 = framing error
- Bit 2 = parity error
- Bit 1 = overrun error
- Bit 0 = data ready

AL = modem status, as follows (set = true):
- Bit 7 = receive line signal detect
- Bit 6 = ring indicator
- Bit 5 = data set ready
- Bit 4 = clear to send
- Bit 3 = delta receive line signal detect
- Bit 2 = trailing edge ring detector
- Bit 1 = delta data set ready
- Bit 0 = delta clear to send

Interrupt 15h: System Support Functions

The functions in this group control hooks, joystick support, microsecond delay, virtual mode support, extended memory support, and system information. The function performed depends on the value in AH.

Value in AH	Function
80h	Device Open
81h	Device Close
82h	Program Terminate
83h	Event Wait
84h	Joystick Support
85h	System Request Key Support
86h	Wait
87h	Move Block of Memory
88h	Extended Memory Size
89h	Processor to Virtual Mode
90h	Device Busy Wait Loop
91h	Interrupt Complete
C0h	System Configuration Parameters
C1h	Return extended BIOS data area segment address
C2h	Pointing device interface

Device Open

Entry Conditions:

AH = 80h
BX = Device ID
CX = Process ID

Exit Conditions:

None

Device Close

Entry Conditions:
AH = 81h
BX = Device ID
CX = Process ID

Exit Conditions:
None

Program Terminate

Entry Conditions:
AH = 82h
BX = Device ID

Exit Conditions:
None

Event Wait

Entry Conditions:

AH = 83h
AL = 0 Set interval
ES:BX = Pointer to a byte in caller's memory that has the sign bit set after the time interval expires
CX,DX = The number of microseconds to elapse before the high order byte in the caller's memory pointed to by ES:BX is set. Granularity is 976 microseconds
AL = 1 Cancel event wait

Exit Conditions:
None

Joystick Support

Entry Conditions:

AH = 84h
DX = 0 Read the current joystick button setting. On return, AL (Bits 4-7) contains the button settings:
- Bit 4: Joystick A, Button 1
- Bit 5: Joystick A, Button 2
- Bit 6: Joystick A, Button 1
- Bit 7: Joystick B, Button 2

DX = 1 Read the resistive inputs of the game adapter. The following values are returned:
- AX = Joystick A x value
- BX = Joystick A y value
- CX = Joystick B x value
- DX = Joystick B y value

System Request Key Support

Entry Conditions:
AH = 85h

Exit Conditions:
AL = 0 Sys Req key pressed
AL = 1 Sys Req key released

Wait

Wait indicated number of microseconds.

Entry Conditions:
AH = 86h Wait indicated number of microseconds
CX,DX = Number of microseconds to wait before returning. Granularity is 976 microseconds

Exit Conditions:
[C] = Successful wait
[NC] = Wait function already in progress

Move Block of Memory

Transfers the contents of a block of memory from memory addressed above 1024K to memory addressed below 1024K. This uses the 80286 processor "protected" mode.

Entry Conditions:

AH = 87h
ES:SI = A pointer to a Global Descriptor Table (GDT) as defined in the following table. The calling program must have previously set up this table.
CX = Number of 16-bit words to be transferred. (Max count=8000h) The source and destination global descriptors must contain a length field of at least (2 * CX - 1)

Exit Conditions:

AH = 00h Operation successful
AH = 01h RAM parity error
AH = 02h Exception interrupt occurred
AH = 03h Gating of address line 20h failed
Carry flag set if error
Zero flag set if successful

GDT Descriptor	Usage (each entry is 8 bytes)
0	Dummy
1	Segment address of this GDT
2	Pointer to area from which to move data
3	Pointer to segment to receive the data
4	BIOS code segment descriptor
5	BIOS stack segment descriptor

Extended Memory Size

Returns the amount of extended memory starting at address 1024K.

Entry Conditions:

AH = 88h

Exit Conditions:

AX = Amount of contiguous available memory in kilobytes starting at address 1024K

Processor to Virtual Mode

Set the 80286 in protected virtual memory mode.

Entry Conditions:

AH = 89h
ES:SI = Pointer tc a Global Descriptor Table (GDT) set up by the calling program as defined in the following table
BH = Offset within the Interrupt Descriptor Table (IDT) that contains the first eight interrupts
BL = Offset within the Interrupt Descriptor Table that contains the second eight hardware interrupts

Exit Conditions:

AH = 00h Operation successful

Note: All segment registers are changed, AX and BP registers modified.

GDT Descriptor	Usage (each entry is 8 bytes)
0	Dummy
1	Segment address of this GDT
2	Pointer to the IDT
3	Pointer to user's data segment
4	Pointer to user's extra segment
5	Pointer to user's stack segment
6	Pointer to user's code segment
7	Pointer to BIOS code segment

Device Busy Wait Loop

Entry Conditions:

AH=90h
AL=Type code groups
00h - 7Fh = Non re-entrant devices
80h - BFh = Re-entrant devices. ES:BX points to data block
C0h - FFh = Wait only

Exit Conditions:

None

Interrupt Complete

Entry Conditions:

AH = 91h
AL = Type code (See function AH = 90h)
= 00h Disk (time-out)
= 01h Diskette (time-out)
= 02h Keyboard (no time-out)
= 03h Pointing Device (time-out)
= 80h Network (no time-out)
= FDh Diskette Drive Motor Start (time-out)
= FEh Printer (time-out)

Exit Conditions:

None

System Configuration Parameters

Returns pointer to system description vector in ROM.

Entry Conditions:

AH = C0h

Exit Conditions:

AH = 00h
ES:BX = Pointer to system descriptor vector

Offset	Length	Description
0	2 bytes	Byte count of data that follows; minimum length 8
2	1 byte	Model byte
3	1 byte	Sub-Model byte
4	1 byte	BIOS revision level (00 is first release)
5	1 byte	Feature information byte 1: Bit 7: Hard Disk BIOS uses DMA channel 3 Bit 6: 2nd interrupt chip present Bit 5: Real-time clock present Bit 4: Keyboard intercept sequence (INT 15h) called in keyboard interrupt (INT 09h) Bit 3: Wait for external event supported Bit 2: Extended BIOS area is allocated Bit 1: Micro Channel implemented Bit 0: Reserved
6	4 bytes	Feature information byte Bits 2-5 - reserved

Return Extended BIOS Data Area Segment Address (AH = C1h)

Returns the address of the data segment of the extended BIOS DATA AREA.

Entry Conditions:
AH = C1h

Exit Conditions:
ES = extended BIOS data area segment address
CF = 0 No error
= 1 Error

Enable/Disable Pointing Device Interface (AH =C2h)

Entry Conditions:
AH = C2h
AL = 00h
BH = 00h Disable
= 01h Enable

Exit Conditions:
AH = 00h No error

= 01h Invalid function call
= 02h Invalid input error
= 03h Interface error
= 04h Resend
= 05h No far call installed
CF = 00h Operation successfully completed
= 01h Operation unsuccessful

Reset Pointing Device

Entry Conditions:
AH = C2h
AL = 01h

Exit Conditions:
AH = See return for AL = 00
BH = 00h Device ID
BL = Modified
CF = 0 Operation successful
= 1 Operation unsuccessful

Set Sample Rate

Entry Conditions:
AH = C2h
AL = 02h
BH = sample rate value (00h to 06h) where:
00 = 10 reports/second
01 = 20 reports/second
02 = 40 reports/second
03 = 60 reports/second
04 = 80 reports/second
05 = 100 reports/second
06 = 200 reports/second

Exit Conditions:
See return for AL = 00h

Set Resolution

Entry Conditions:

AH = C2h
AL = 03h
BH = resolution value, where:
00h = 1 count/millimeter
01h = 2 counts/millimeter
02h = 4 counts/millimeter
03h = 8 counts/millimeter

Exit Conditions:

AH = 0 See return for AL = 00
CF = 0 Operation successful
= 1 Operation unsuccessful

Read Device Type

Entry Conditions:

AH = C2h
AL = 04h

Exit Conditions:

AH = See return for AL = 00
BH = Device ID
= 00h

Pointing Device Interface Initialization

Entry Conditions:

AH = C2h
AL = 05h
BH = data package size (01h-08h, in bytes)

Exit conditions:

AH = See return for AL = 00h
CF = 0 Operation successful
= 1 Operation unsuccessful

Extended Commands

Entry Conditions:

AH = C2h
AL = 06h
BH = 00h Return status
= 01h Set scaling factor to 1:1
= 02h Set scaling factor 2:1

Exit Conditions:

AH = See return for AL = 00h
CF = 0 Operation successful
= 1 Operation unsuccessful

For return status (BH = 0) subfunction only:
BL = Status Byte 1, where:
Bit 7 = 0 Reserved
Bit 6 = 0 Stream mode
= 1 Remote mode
Bit 5 = 1 Enable
= 0 Disable
Bit 4 = 0 1:1 scaling
= 1 2:1 scaling
Bit 3 = 0 Reserved
Bit 2 = 1 Left button pressed
Bit 1 = 0 Reserved
Bit 0 = 1 Right button pressed
CL = Status Byte 2, where:
00h = 1 count millimeter
01h = 2 counts/millimeter
02h = 4 counts/millimeter
03h = 8 counts/millimeter
DL = Status Byte 3, where:
0Ah = 10 reports/second
14h = 20 reports/second
28h = 40 reports/second
3Ch = 60 reports/second
50h = 80 reports/second
64h = 100 reports/second
C8h = 200 reports/second

Device Driver Far Call Initialization

Entry Conditions:

AH = C2h
AL = 07h
ES:BX = device driver segment and offset address

Exit Conditions:

See returns for AL = 00h

Subsequent to this call, whenever pointing device data is available, the device driver address is called with the following arguments on the stack:

Word	Byte	Bit	Description
1	Low	7	1 Y data overflow
		6	1 X data overflow
		5	1 Negative Y data sign
		4	1 Negative X data sign
		3	1 Reserved (must be 1)
		2	0 Reserved (must be 0)
		1	1 Right button pressed
		0	1 Left button pressed
1	High	7-0	0 Reserved
2	Low	7-0	X data
2	High	7-0	0 Reserved
3	Low	7-0	Y data
3	High	7-0	0 Reserved
4	Low	7-0	0 Reserved
	High	7-0	0 Reserved

Interrupt 16h: Keyboard Functions

The following routines provide access to keyboard functions. The specific function performed depends on the value in AH.

Value in AH	Function Performed
00h	Read Keyboard Input
01h	Read Keyboard Status
02h	Read Shift Status
03h	Set Typematic Rate
05h	Stuff Keyboard Buffer
10h	Read Extended Keyboard Input
11h	Read Extended Keyboard Status
12h	Read Extended Shift Status

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read). Control returns when a keystroke is available.

Entry Conditions:
AH = 00h

Exit Conditions:
AL = ASCII value of character
AH = keyboard scan code

Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to be read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (non-destructive read).

Entry Conditions:
AH = 01h

Exit Conditions:
Z = 1 no character is available
Z = 0 a character is available. in which case:
AL = ASCII value of character
AH = keyboard scan code

Get Shift Status

Return the current shift status.

Entry Conditions:
AH = 02h

Exit Conditions:
AL = current shift status bit settings: set = true, reset = false
Bit 0 = RIGHT SHIFT key pressed
Bit 1 = LEFT SHIFT key pressed
Bit 2 = CTRL (control) key pressed
Bit 3 = ALT (alternate mode) key pressed
Bit 4 = SCROLL state active
Bit 5 = NUMBER lock engaged
Bit 6 = CAPS lock engaged
Bit 7 = INSERT state active

Set Typematic Rate

Entry Conditions:
AH = 03h
AL = 05h
BL = Typematic rate (00 - 1F hex)
BH = Typematic delay (00 - 3 hex)

Exit Conditions:
None

Stuff Keyboard Buffer

Entry Conditions:
AH = 05h
CH = Scan Code to Place in Keyboard Buffer
CL = ASCII Character to Place in Keyboard Buffer

Exit Conditions:
AL = 0 Store is Successful
AL = 1 Store is Unsuccessful
CY = 1 Error

Read Extended Keyboard Input

Control is returned when a keystroke is available. The keystroke is removed from the buffer.

Entry Conditions:
AH = 10h

Exit Conditions:
AL = ASCII Character
AH = Scan Code

Read Extended Keyboard Status

Includes extended read interface for extended keyboard.

Entry Conditions:
AH = 11h

Exit Conditions:
Z = 1 No Character Available
Z = 0 Character Available, in which case:
AL = ASCII Character
AH = Scan Code

Note: The keystroke is not removed from the buffer.

Read Extended Shift Status

Entry Conditions:
AH = 12

Exit Conditions:
AL = Shift Status Byte: Bit = 1, on (key depressed); Bit = 0, off
Bit 7 = Ins(ert)
Bit 6 = Caps Lock
Bit 5 = Num Lock
Bit 4 = Scroll Lock
Bit 3 = Alt (alternate mode) key
Bit 2 = Ctrl (control) key
Bit 1 = Left Shift key
Bit 0 = Right Shift key

AH = Extended Shift Status: Bit = 1, currently depressed; Bit = 0, not depressed
Bit 7 = SysRq key
Bit 6 = Caps Lock key
Bit 5 = Num Lock key
Bit 4 = Scroll Lock key
Bit 3 = Right Alt key
Bit 2 = Right Ctrl key
Bit 1 = Left Alt key
Bit 0 = Left Ctrl key

Interrupt 17h: Line Printer Functions

These routines provide an interface to the parallel line printer. The specific function performed depends on the value in AH:

Value In AH	Description of Function
00h	Print character
01h	Initialize printer port
02h	Get current printer status

Print Character

Print a character.

Entry Conditions:
AH = 00h
AL = character to be printed
DX = printer to be used (0-2)

Exit Conditions:
AH = printer status;
See "Get Current Printer Status (AH = 02h)."
If Bit 0 is set, the character could not be printed because of a timeout error

Initialize Printer Port

Initialize the printer port.

Entry Conditions:
AH = 01h
DX = printer to be used (0-2)

Exit Conditions:
AH = printer status; See "Get Current Printer Status" (AH = 02h)

Get Current Printer Status

Read the printer status in AH.

Entry Conditions:
AH = 02h

Exit Conditions:
AH = printer status, as follows (set = true = 1):
Bit 7 = not busy
Bit 6 = acknowledge
Bit 5 = out of paper
Bit 4 = selected
Bit 3 = I/O error
Bit 2 = [unused]
Bit 1 = [unused]
Bit 0 = timeout occurred

Note: If printer port specified by DX does not exist, the status value is not meaningful.

Interrupt 1Ah: System Clock Functions

These routines provide the means of reading and setting the system clock tick counter, the CMOS real-time clock, and the system alarm function. The specific function performed depends on the value of AH:

Value in AH	Function Description
01h	Set system clock
02h	Read CMOS time of day
03h	Set CMOS time of day
04h	Read CMOS date
05h	Set CMOS date
06h	Set the alarm
07h	Reset the alarm
08h	Set up sound multiplexer

Read System Clock

Read the system clock value kept in RAM.

Note: The clock runs at a rate of 1,193,180/65,536 ticks per second, or about 18.2 ticks per second. 24 hours equals 1800B0h ticks.

Entry Conditions:
AH = 00h

Exit Conditions:
AL = 0 (zero) if the timer has not exceeded 24 hours since the last time this function was called; otherwise AL contains a non-zero value
CX = high (most significant) portion of clock count
DX= low (least significant) portion of clock count

Set System Clock

Set the system clock value kept in RAM.

Entry Conditions:
AH = 01h
CX = high (most significant) portion of clock count
DX = low (least significant) portion of clock count

Read CMOS Time Of Day

Read the time of day kept in CMOS.

Entry Conditions:
AH = 02h

Exit Conditions:
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD
DL = daylight savings time (1 = yes, 0 = no)

Set CMOS Time Of Day

Set the time of day kept in CMOS.

Entry Conditions:
AH = 03h
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD
DL = 1 if daylight savings time, 0 if not.

Read CMOS Date

Read the date kept in CMOS.

Entry Conditions:
AH = 04h

Exit Conditions:
CH = century in BCD
CL = year in BCD
DH = month in BCD
DL = day in BCD

Set CMOS Date

Set the date kept in CMOS.

Entry Conditions:
AH = 05h
CH = century in BCD
CL = year in BCD

DH = month in BCD
DL = day in BCD

Set the Alarm

Set the alarm function to generate an INT 4Ah at the specified time. The user must provide an alarm routine and initialize the vector for interrupt 4Ah to point to this routine.

Entry Conditions:
AH = 06h
CH = hours in BCD
CL = minutes in BCD
DH = seconds in BCD

Exit Conditions:
[NC] = CMOS clock operating correctly, and no other alarm is currently in process
[C] = An alarm is currently in progress, or the CMOS clock is not operating correctly

Reset the Alarm

Reset the alarm function set by Function 6.

Entry Conditions:
AH = 07h

Exit Conditions:
None

KEYBOARD

I. ELECTRICAL

A. POWER

5V ± 10% , 300 mA MAX

B. LOGIC LEVELS

LOGIC "0" - 0.7V MAX @ 8mA MAX TOTAL SINK, 5.7 mA EXTERNAL.
LOGIC "1" - 2.4V MIN @ 0.8 mA MAX.

II. POWER ON ROUTINE

UPON SYSTEM POWER UP THE FOLLOWING ACTIVITIES OCCUR:

A. POWER ON RESET (POR)

THE KEYBOARD WILL PERFORM A POWER ON RESET (POR) WITHIN A MINIMUM OF 150 MSEC AND A MAXIMUM OF 2.0 SECONDS.

B. BASIC ASSURANCE TEST (BAT)

THE KEYBOARD WILL CONDUCT A BASIC ASSURANCE TEST (BAT) OF THE PROCESSOR.

1. TURN THE LEDs (IF SO EQUIPPED) ON AT THE BEGINNING OF THE TEST AND OFF AT THE END OF THE TEST.

2. TRANSMIT THE COMPLETION CODE; AAH IF THE TEST WAS SUCCESSFUL.

THE BAT TAKES A MAXIMUM OF 500 MSEC. DURING THIS TIME ALL ACTIVITY ON THE "CLOCK" AND "DATA" LINES WILL BE IGNORED.

THE COMPLETION CODE WILL BE TRANSMITTED WITHIN 450 MSECONDS AND NOT MORE THAN 2.5 SECONDS AFTER POR, AND WITHIN 500 MSECONDS AFTER A RESET COMMAND IS ACKNOWLEDGED.

C. AUTOSELECT

THE KEYBOARD DETERMINES WHAT KIND OF SYSTEM IT IS CONNECTED TO AS FOLLOWS:

1. TRANSMIT "AAH" IN 11-BIT (MODE 2) FORMAT AND CHECK FOR AN INHIBIT AFTER THE 10TH BIT. IF NO INHIBIT IS RECEIVED (DATA LINE AT LOGIC "0") THE FORMAT WILL REMAIN IN MODE 2 AND SCAN CODE SET 2 IS SELECTED. IF THE SYSTEM RESPONDS WITH AN INHIBIT THEN THE 9-BIT (MODE 1) FORMAT AND SCAN CODE SET 1 ARE SELECTED.

III. DATA TRANSMISSION

A. CLOCK AND DATA LINES

THE "CLOCK" AND "DATA" LINES ARE USED FOR COMMUNICATION IN BOTH DIRECTIONS BETWEEN THE SYSTEM AND THE KEYBOARD. THESE LINES ARE DRIVEN BY AN OPEN COLLECTOR DEVICE WHICH ALLOWS EITHER THE SYSTEM OR THE KEYBOARD TO FORCE THE LINE TO AN INACTIVE (LOW) LEVEL. WHEN NO COMMUNICATION IS OCCURRING BOTH LINES ARE ACTIVE (HIGH). AN INACTIVE SIGNAL (LOGIC 0) IS GREATER THAN 0 BUT LESS THAN +0.7 VOLTS. AN ACTIVE SIGNAL (LOGIC 1) HAS A VALUE OF AT LEAST +2.4 BUT NO GREATER THAN +5.5 VOLTS.

THE KEYBOARD PROVIDES THE CLOCKING SIGNALS USED TO CLOCK SERIAL DATA TO AND FROM THE KEYBOARD. THE HOST SYSTEM CAN INHIBIT THE KEYBOARD BY FORCING THE "CLOCK" LINE TO THE INACTIVE LEVEL. WHEN THE KEYBOARD IS INHIBITED THE STATE OF THE "CLOCK" LINE IS IGNORED.

THE "DATA" LINE IS USED FOR TRANSMISSION OF DATA BY BOTH THE SYSTEM AND THE KEYBOARD. THE SYSTEM ISSUES A "REQUEST TO SEND" (RTS) BY PULLING THE DATA LINE TO THE INACTIVE LEVEL (LOW).

B. DATA FORMAT

TWO MODES ARE USED FOR DATA TRANSMISSION:

1. MODE 1 IS A 10-BIT DATA STREAM THAT CONSISTS OF A LOGIC "0" TEST BIT, A LOGIC "1" START BIT, AND 8 DATA BITS (NO PARITY OR STOP BITS). SCAN CODE SET 1 IS USED WITH MODE 1.

2. MODE 2 IS AN 11-BIT DATA STREAM THAT CONSISTS OF 1 START BIT (ALWAYS LOGIC "0"), 8 DATA BITS (LEAST SIGNIFICANT BIT TO MOST SIGNIFICANT BIT RESPECTIVELY), 1 ODD PARITY BIT, AND ONE STOP BIT (ALWAYS LOGIC 1). MODE 2 IS USED WITH SCAN CODE SETS 2 AND 3.

SEE FIGURE 1, 2, AND 3 FOR GRAPHIC REPRESENTATION OF THESE SIGNALS.

C. KEYBOARD TO SYSTEM LINE PROTOCOL

1. KEYBOARD CHECKS "CLOCK" LINE FOR "CTS" - IF LOGIC "1" CONTINUE, IF LOGIC "0" STORE KEYSTROKES IN BUFFER.

2. KEYBOARD CHECKS "DATA" LINE FOR "RTS" FROM SYSTEM - IF LOGIC "1" CONTINUE, IF LOGIC "0" STORE KEYSTROKES IN BUFFER AND PREPARE TO RECEIVE DATA FROM SYSTEM.

3. KEYBOARD TRANSMITS DATA. DURING TRANSMISSION THE KEYBOARD CHECKS THE "CLOCK" LINE FOR LOGIC LEVEL "1" AT LEAST EVERY 60 MICROSECONDS. (SEE LINE CONTENTION BELOW)

LINE CONTENTION - THE SYSTEM MAY INTERRUPT KEYBOARD DATA TRANSMISSION AT ANY TIME UP TO THE 10th CLOCK BY PULLING THE "CLOCK" LINE TO A LOGIC LEVEL "0". AFTER THE 10th CLOCK THE SYSTEM MUST RECEIVE THE KEYBOARD DATA.

D. SYSTEM TO KEYBOARD LINE PROTOCOL

1. SYSTEM INHIBITS KEYBOARD BY LOWERING THE "CLOCK" LINE TO LOGIC "0" FOR A MINIMUM OF 60 MICROSECONDS.

2. SYSTEM REQUESTS TRANSMISSION BY LOWERING THE "DATA" LINE TO LOGIC LEVEL "0" (RTS) AND ALLOWS THE "CLOCK" LINE TO GO ACTIVE.

3. KEYBOARD MONITORS THE "CLOCK" LINE (10 mSEC INTERVALS) AND DETECTS THE ACTIVE LEVEL.

4. KEYBOARD DETECTS "RTS" ON THE "DATA" LINE AND CLOCKS IT IN AS THE LOGIC "0" START BIT.

5. KEYBOARD CLOCKS IN THE 8 DATA BITS AND THE ODD PARITY BIT.

6. KEYBOARD LOOKS FOR A LOGIC LEVEL "1" ON THE "DATA" LINE THEN FORCES IT LOW (WITHIN 20 mSEC) AND CLOCKS ONE MORE BIT. THIS ACTION SIGNALS THE SYSTEM THAT THE KEYBOARD HAS RECEIVED THE DATA. IF THE "DATA" IS NOT AT A LOGIC LEVEL "0" FOLLOWING THE 10th BIT THE KEYBOARD WILL CONTINUE TO CLOCK BITS INDEFINITELY UNTIL THE LINE BECOMES ACTIVE. THE KEYBOARD THEN PULLS THE "DATA" LINE LOW AND TRANSMITS A "RESEND".

IV. FIFO

THE KEYBOARD CONTAINS AT LEAST A 16-BYTE FIRST-IN-FIRST-OUT (FIFO) BUFFER WHICH STORES THE SCAN CODES UNTIL THE SYSTEM IS READY TO RECEIVE THEM.

A BUFFER-OVERRUN CONDITION OCCURS WHEN THE KEYBOARD TRIES TO PLACE MORE CHARACTERS THAN THE KEYBOARD BUFFER CAN HOLD. WHEN THIS OCCURS, AN OVERRUN CODE (FFH FOR SCAN CODE SET 1, AND 00H FOR SCAN CODE SETS 2 & 3) REPLACES THE LAST BYTE. IF MORE KEYS ARE PRESSED BEFORE THE SYSTEM ALLOWS KEYBOARD OUTPUT, THE ADDITIONAL DATA IS LOST.

WHEN THE KEYBOARD IS ALLOWED TO SEND DATA, THE BYTES IN THE BUFFER WILL BE SENT AS IN NORMAL OPERATION, AND NEW DATA ENTERED IS DETECTED AND SENT. RESPONSE CODES DO NOT OCCUPY A BUFFER POSITION.

IF KEYSTROKES GENERATE A MULTIPLE-BYTE SEQUENCE, THE ENTIRE SEQUENCE MUST FIT INTO THE AVAILABLE BUFFER SPACE OR THE KEYSTROKE IS DISCARDED AND A BUFFER-OVERRUN CONDITION OCCURS.

V. KEYS

ALL THE KEYS ON THE KEYBOARD ARE MAKE/BREAK EXCEPT THE PAUSE KEY. THE MAKE SCAN CODE IS SENT TO THE SYSTEM WHEN THE KEY IS DEPRESSED AND THE BREAK CODE IS SENT WHEN THE KEY IS RELEASED.

ALL KEYS ARE ALSO AUTOREPEAT EXCEPT FOR THE PAUSE KEY. THE KEY WILL AUTOREPEAT AFTER THE INITIAL DELAY HAS EXPIRED. ROLLOVER TO ANOTHER AUTOREPEAT KEY WILL STOP REPEATING OPERATION AND PRODUCE THE SCAN CODE FOR THE SECOND KEY. AFTER AN INITIAL DELAY, THE KEYBOARD WILL REPEAT THE SECOND CODE. ROLLOVER TO A NON-AUTOREPEAT KEY WILL NOT AFFECT THE AUTOREPEAT OPERATION. THE INITIAL DELAY AND REPEAT RATES ARE MODIFIABLE. (SEE MODIFY AUTOREPEAT RATE/DELAY (F3H) COMMAND BELOW.)

VI. SYSTEM COMMANDS

THESE COMMANDS MAY BE SENT TO THE KEYBOARD AT ANY TIME. THE KEYBOARD WILL RESPOND WITHIN 20 mSEC, EXCEPT WHEN PERFORMING THE BASIC ASSURANCE TEST (BAT), OR EXECUTING A RESET.

NOTE: MODE 1 WILL ACCEPT ONLY THE RESET COMMAND. THIS IS ACCOMPLISHED BY PULLING THE CLOCK LINE LOW FOR A MINIMUM OF 12.5 mSEC.

THE COMMANDS ARE DESCRIBED IN ALPHABETICAL ORDER AND HAVE DIFFERENT MEANINGS WHEN ISSUED BY THE KEYBOARD. (SEE KEYBOARD COMMANDS)

COMMANDS (SYSTEM TO KEYBOARD)

COMMAND	HEX VALUE
DEFAULT DISABLE	F5
ECHO	EE
ENABLE	F4
INVALID COMMAND	EF OR F1
READ ID	F2
RESEND	FE
RESET	FF
SET ALT SCAN CODES	F0
SET ALL KEYS (AR)	F7
SET ALL KEYS (M/B)	F8
SET ALL KEYS (M)	F9
SET ALL KEYS (AR, M, M/B)	FA
SET DEFAULT	F6
SET KEY TYPE (AR)	FB
SET KEY TYPE (M/B)	FC
SET KEY TYPE (M)	FD
SET/RESET STATUS IND	ED
SET AR RATE/DELAY	F3

A. DEFAULT DISABLE (F5H)

THIS COMMAND RESETS ALL CONDITIONS TO THE POWER-ON STATE. THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS THE DEFAULT KEY TYPES (SCAN CODE SET 3 OPERATION ONLY) AND AUTOREPEAT RATE/DELAY, AND CLEARS THE LAST AUTOREPEAT KEY. THE KEYBOARD STOPS SCANNING, AND AWAITS FURTHER INSTRUCTIONS.

B. ECHO (EEH)

WHEN THE KEYBOARD RECEIVES THIS COMMAND, IT ISSUES AN ECHO (EEH) RESPONSE AND CONTINUES SCANNING, IF PREVIOUSLY ENABLED.

C. ENABLE (F4H)

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, CLEARS THE LAST AUTOREPEAT KEY, AND STARTS SCANNING.

D. INVALID COMMAND (FEH & F1H)

THESE ARE INVALID COMMANDS AND ARE NOT SUPPORTED. IF ONE OF THESE IS RECEIVED, THE KEYBOARD WILL NOT ACKNOWLEDGE THE COMMAND, BUT RETURNS A "RESEND" AND CONTINUES SCANNING, IF PREVIOUSLY ENABLED. NO OTHER ACTIVITIES OCCUR.

E. READ ID (F2H)

THE KEYBOARD RESPONDS WITH "ACK", DISCONTINUES SCANNING, AND SENDS THE TWO KEYBOARD ID BYTES 83H AND ABH.

THE SECOND BYTE IS TRANSMITTED FOLLOWING THE FIRST WITHIN 500 uSEC. AFTER THE OUTPUT OF THE SECOND ID BYTE, THE KEYBOARD RESUMES SCANNING EVEN IF PREVIOUSLY DISABLED.

F. RESEND (FEH)

THIS COMMAND SHOULD BE SENT FOLLOWING THE OUTPUT OF A CODE AND BEFORE THE SYSTEM ENABLES THE INTERFACE ALLOWING THE NEXT KEYBOARD OUTPUT. THE KEYBOARD WILL RETRANSMIT THE PREVIOUS CODE UNLESS IT WAS A "RESEND" COMMAND, IN THIS CASE THE KEYBOARD WILL RESEND THE LAST BYTE PRIOR TO THE "RESEND" COMMAND.

G. RESET (FFH)

SEE SECTION ON RESET

H. SELECT ALTERNATE SCAN CODES (F0H)

THIS COMMAND INSTRUCTS THE KEYBOARD TO SELECT ONE OF THREE SETS OF SCAN CODES. THE KEYBOARD ACKNOWLEDGES RECEIPT OF THIS COMMAND WITH "ACK", CLEARS BOTH THE OUTPUT BUFFER AND THE AUTOMATIC REPEAT KEY (IF ONE IS ACTIVE). THE SYSTEM THEN SENDS THE OPTION BYTE AND THE KEYBOARD RESPONDS WITH ANOTHER "ACK". AN OPTION BYTE VALUE OF 01H SELECTS SCAN CODE SET 1, 02H SELECTS SET 2, AND 03H SELECTS SET 3.

AN OPTION BYTE VALUE OF 00H CAUSES THE KEYBOARD TO ACKNOWLEDGE WITH AN "ACK" AND SEND A BYTE TELLING THE SYSTEM WHICH SCAN CODE IS CURRENTLY IN USE. AFTER ESTABLISHING THE NEW SCAN CODE SET, THE KEYBOARD RETURNS TO THE SCANNING STATE IT WAS IN BEFORE RECEIVING THE "SELECT ALTERNATE SCAN CODES" COMMAND.

J. SET ALL KEYS (F7H, F8H, F9H, FAH)

THESE COMMANDS INSTRUCT THE KEYBOARD TO SET ALL KEYS TO THE TYPE LISTED BELOW:

F7H = SET ALL KEYS - AUTOREPEAT
F8H = SET ALL KEYS - MAKE/BREAK
F9H = SET ALL KEYS - MAKE
FAH = SET ALL KEYS - AUTOREPEAT/MAKE BREAK

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS ALL KEYS TO THE TYPE INDICATED BY THE COMMAND, AND CONTINUES SCANNING (IF PREVIOUSLY ENABLED). ALTHOUGH THESE COMMANDS CAN BE SENT USING ANY SCAN CODE SET, THEY AFFECT ONLY SCAN CODE SET 3 OPERATION.

K. SET DEFAULT (F6H)

THIS COMMAND RESETS ALL CONDITIONS TO THE POWER-ON DEFAULT STATE. THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, SETS THE DEFAULT KEY TYPES (SCAN CODE SET 3 OPERATION ONLY) AND AUTOREPEAT RATE/DELAY, CLEARS THE LAST AUTOREPEAT KEY, AND CONTINUES SCANNING.

L. SET KEY TYPE (FBH, FCH, FDH)

THESE COMMANDS INSTRUCT THE KEYBOARD TO SET INDIVIDUAL KEYS TO THE TYPE LISTED BELOW:

FBH = SET KEY TYPE - AUTOREPEAT
FCH = SET KEY TYPE - MAKE/BREAK
FDH = SET KEY TYPE - MAKE

THE KEYBOARD RESPONDS WITH "ACK", CLEARS ITS OUTPUT BUFFER, AND PREPARES TO RECEIVE KEY IDENTIFICATION. THE SYSTEM IDENTIFIES EACH KEY BY ITS SCAN CODE VALUE AS DEFINED IN SCAN CODE SET 3. ONLY SCAN CODE SET 3 VALUES ARE VALID FOR KEY IDENTIFICATION. THE TYPE OF EACH KEY IS SET TO THE VALUE INDICATED BY THE COMMAND.

EACH SCAN CODE RECEIVED IS ACKNOWLEDGED BY THE KEYBOARD AND THE IDENTIFIED KEY IS SET TO THE TYPE DEFINED BY THE COMMAND. THE KEYBOARD WILL REMAIN IN A PARTICULAR SET TYPE COMMAND MODE UNTIL IT RECEIVES THE COMMAND FOR A NEW TYPE.

THE COMMAND IS TERMINATED BY THE ENABLE COMMAND (F4H).

M. SET/RESET STATUS INDICATORS (EDH)

THE KEYBOARD ACTIVATES AND DEACTIVATES THESE INDICATORS WHEN IT RECEIVES A VALID COMMAND CODE SEQUENCE FROM THE SYSTEM. WHEN THE KEYBOARD RECEIVES THE COMMAND BYTE (EDH) IT RESPONDS WITH "ACK", DISCONTINUES SCANNING, AND WAITS OR THE OPTION BYTE AS FOLLOWS:

BIT	INDICATOR
0	SCROLL LOCK INDICATOR
1	NUM LOCK INDICATOR
2	CAPS LOCK INDICATOR
3-4	RESERVED (MUST BE 0's)

A BIT SET TO "1" TURNS THE INDICATOR "ON", A "0" TURNS IT "OFF".

THE KEYBOARD RESPONDS TO THE OPTION BYTE WITH "ACK", SETS THE INDICATORS AND, IF THE KEYBOARD WAS PREVIOUSLY ENABLED, CONTINUES SCANNING.

IF ANOTHER COMMAND IS RECEIVED IN PLACE OF THE OPTION BYTE, EXECUTION OF THE "SET/RESET INDICATORS MODE" IS STOPPED, WITH NO CHANGE TO THE INDICATORS, AND THE NEW COMMAND IS PROCESSED.

THE INDICATORS DEFAULT TO THE "OFF" STATE AT "POWER-ON" AND ARE NOT AFFECTED BY THE "SET DEFAULT" AND "DEFAULT DISABLE" COMMANDS.

N. SET AUTOREPEAT RATE/DELAY (F3H)

THE KEYBOARD RESPONDS TO THE COMMAND WITH "ACK", STOPS SCANNING, AND WAITS FOR THE RATE/DELAY VALUE BYTE. BITS 6 AND 5 OF THIS BYTE INDICATE THE DELAY, AND BITS 4, 3, 2, 1, AND 0 (THE LEAST SIGNIFICANT BIT) INDICATE THE RATE. BIT 7 (THE MOST SIGNIFICANT BIT) IS ALWAYS "0". THE DELAY IS EQUAL TO 1 PLUS THE BINARY VALUE OF BITS 6 & 5, MULTIPLIED BY 250 mSEC $\pm$ 20%. THE PERIOD (INTERVAL FROM ONE AUTOREPEAT OUTPUT TO THE NEXT) IS DETERMINED BY THE FOLLOWING EQUATION:

$$\text{PERIOD} = (8 + A) \times (2^{B}) \times 0.00417 \text{ SECONDS.}$$

WHERE:

A - BINARY VALUE OF BITS 2, 1, AND 0
B - BINARY VALUE OF BITS 4 AND 3.

THE AUTOREPEAT RATE (MAKE CODES PER SECOND) IS : FOR EACH PERIOD AND ARE LISTED IN THE FOLLOWING TABLE.

BIT	AUTOREPEAT RATE	BIT	AUTOREPEAT RATE
00000	30.0	10000	7.5
00001	26.7	10001	6.7
00010	24.0	10010	6.0
00011	21.8	10011	5.5
00100	20.0	10100	5.0
00101	18.5	10101	4.6
00110	17.1	10110	4.3
00111	16.0	10111	4.0
01000	15.0	11000	3.7
01001	13.3	11001	3.3
01010	12.0	11010	3.0
01011	10.9	11011	2.7
01100	10.0	11100	2.5
01101	9.2	11101	2.3
01110	8.6	11110	2.1
01111	8.0	11111	2.0

THE DEFAULT VALUES AT POWER ON FOR THE SYSTEM KEYBOARD ARE AS FOLLOWS:

AUTOREPEAT RATE = 10.9 CHARACTERS PER SECOND ± 20%.

DELAY = 500 mSEC ± 20%.

THE KEYBOARD RESPONDS TO THE VALUE BYTE WITH "ACK", SETS THE RATE AND DELAY TO THE VALUES INDICATED, AND CONTINUES SCANNING, IF ENABLED.

THE EXECUTION OF THIS COMMAND STOPS WITHOUT CHANGE TO THE EXISTING RATE IF ANOTHER COMMAND IS RECEIVED INSTEAD OF THE RATE/DELAY VALUE BYTE AND THE NEW COMMAND IS PROCESSED.

VII. KEYBOARD COMMANDS

THESE COMMANDS MAY BE SENT TO THE SYSTEM ANY TIME THE KEYBOARD IS ENABLED. THEY ARE LISTED IN ALPHABETICAL ORDER AND HAVE A DIFFERENT MEANING WHEN SENT BY THE SYSTEM (SEE SYSTEM COMMANDS).

COMMANDS (KEYBOARD TO SYSTEM)

COMMAND	HEX CODE
ACK	FA
BAT COMPLETION	AA
BREAK CODE PREFIX	F0
ECHO	EE
KBD ID	SEE DESC. BELOW
KEY DETECTION ERROR	00 OR FF
OVERRUN	00 OR FF
RESEND	FE

A. ACKNOWLEDGE (FAH)

THE KEYBOARD SENDS "ACK" IN RESPONSE TOO ANY VALID COMMAND FROM THE SYSTEM EXCEPT "ECHO" AND "RESEND".

B. BAT COMPLETION CODE (AAH)

INDICATES TO THE SYSTEM THAT THE KEYBOARD BASIC ASSURANCE TEST (BAT) WAS SUCCESSFULLY COMPLETED. ANY OTHER CODE INDICATES A FAILURE OF THE KEYBOARD.

C. ECHO (EEH)

THE KEYBOARD SENDS THIS CODE IN RESPONSE TO AN ECHO COMMAND.

D. KEYBOARD ID

THE KEYBOARD ID CONSISTS OF 2 BYTES (SEE READ ID COMMAND UNDER SYSTEM COMMANDS). THE KEYBOARD RESPONDS TO THE READ ID WITH "ACK", DISCONTINUES SCANNING, AND SENDS THE TWO ID BYTES. THE LOW BYTE IS SENT FIRST FOLLOWED BY THE HIGH BYTE. FOLLOWING OUTPUT OF THE KEYBOARD ID, THE KEYBOARD BEGINS SCANNING.

E. KEY CODE

UNIQUE OUTPUT CODE GENERATED FOR EACH KEY POSITION OF THE SWITCH ARRAY. REFER TO "KEYBOARD SCAN CODES" FOR THE DEFINITION OF OUTPUT CODE PER POSITION.

F. KEY DETECTION ERROR (00H or FFH)

THE KEYBOARD SENDS A KEY DETECTION ERROR CHARACTER IF CONDITIONS IN THE KEYBOARD MAKE IT IMPOSSIBLE TO IDENTIFY A SWITCH CLOSURE. IF THE KEYBOARD IS USING SCAN CODE SET 1, THE CODE IS FFH. FOR SETS 2 AND 3, THE CODE IS 00H.

G. OVERRUN (00H or FFH)

THIS CODE REPLACES THE LAST CODE IN THE KEYBOARD BUFFER WHEN ITS CAPACITY HAS BEEN EXCEEDED. THE CODE IS SENT WHEN IT REACHES THE TOP OF THE BUFFER QUEUE. IF THE KEYBOARD IS USING SCAN CODE SET 1, THE CODE IS FFH, FOR SETS 2 AND 3, THE CODE IS 00H.

H. RESEND (FEH)

THE KEYBOARD ISSUES A "RESEND" COMMAND FOLLOWING RECEIPT OF AN INVALID INPUT OR ANY INPUT WITH INCORRECT PARITY.

I. DEFAULT CONDITIONS AFTER RESET (BOTH MODES)

THE FOLLOWING ARE THE DEFAULT CONDITIONS AFTER A HARDWARE OR SOFTWARE RESET:

1. AUTO REPEAT 10 CPS @ 500 mSEC INITIAL DELAY, CLICK DISABLED AND LEDs OFF.

2. CLICK (OPTIONAL ANNUNCIATOR IS NOT INSTALLED)

3. TWO KEY LOCKOUT - EXCEPT FOR KEYS 60, 81, 94, 100, 101, 103, AND 104, IF TWO KEYS ARE DEPRESSED, A THIRD KEY WILL NOT BE ACCEPTED UNTIL ONE OF THE TWO KEYS ARE RELEASED.

4. IF MORE THAN TWO KEYS ARE HELD DEPRESSED AFTER A VALID RESET, A PHANTOM KEY MAY BE DETECTED.

FIG 1. KEYBOARD INPUT (11-bit)

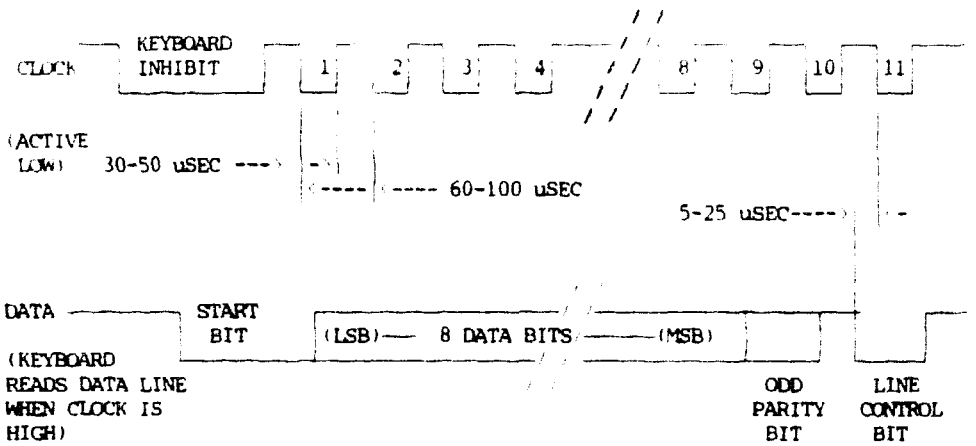


FIG 2. KEYBOARD OUTPUT (11-bit)

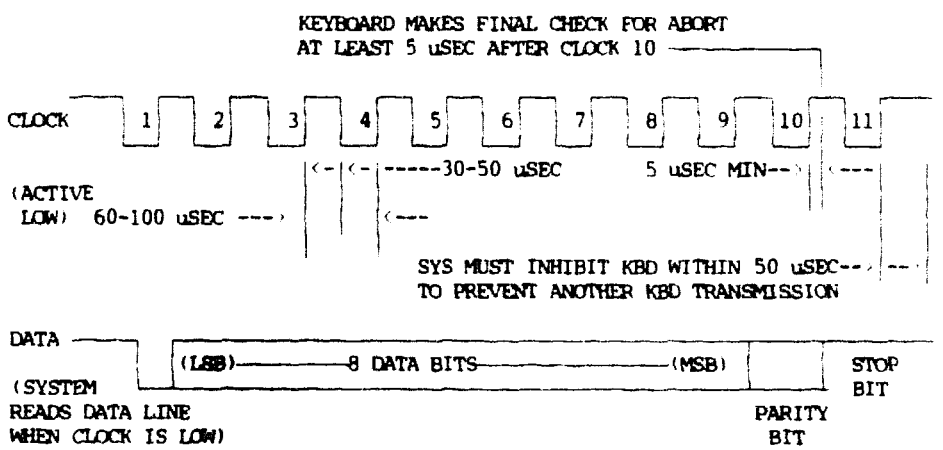
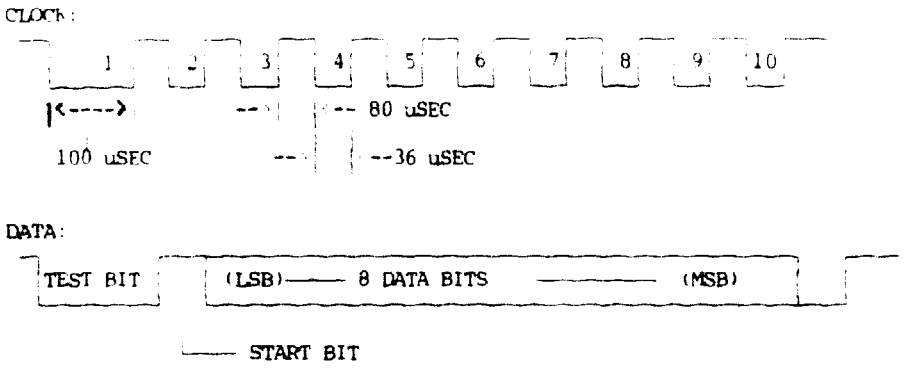


FIG 3. KEYBOARD OUTPUT (9-bit)



NOTE: ALL BIT TIMES ARE NOMINAL. TOLERANCES ARE +/- 5 uSEC.

IV. THE KEYBOARD USES THREE SETS OF SCAN CODES. THE FOLLOWING TABLE LISTS THESE CODES:

	CODE SETS			
Key No.	Set 1	Set 2	Set 3	MODE
1	01	76	08	M
2	3B	05	07	M
3	3C	06	0F	M
4	3D	04	17	M
5	3E	0C	1F	M
6	3F	03	27	M
7	40	0B	2F	M
8	41	83	37	M
9	42	0A	3F	M
10	43	01	47	M
11	44	09	4F	M
12	57	78	56	M
13	58	07	5E	M
14	(1) *	(2) *	57	M
15	46	7E	5F	M
16	(1) *	(2) *	62	M
17	29	0E	0E	AR
18	02	16	16	AR
19	03	1E	1E	AR
20	04	26	26	AR
21	05	25	25	AR
22	06	2E	2E	AR
23	07	36	36	AR
24	08	3D	3D	AR
25	09	3E	3E	AR
26	0A	46	46	AR
27	0B	45	45	AR
28	0C	4E	4E	AR
29	0D	55	55	AR
30	58	5D	5C	AR
31	0E	66	66	AR
32	(1) *	(2) *	67	M
33	(1) *	(2) *	6E	M
34	(1) *	(2) *	6F	M
35	45	77	76	M

Key No.	Set 1	Set 2	Set 3	Mode
36	(1) *	(2) *	77	M
37	37	7C	7E	M
38	4A	7B	84	M
39	0F	0D	0D	AR
40	10	15	15	AR
41	11	1D	1D	AR
42	12	24	24	AR
43	13	2D	2D	AR
44	14	2C	2C	AR
45	15	35	35	AR
46	16	3C	3C	AR
47	17	43	43	AR
48	18	44	44	AR
49	19	4D	4D	AR
50	1A	54	54	AR
51	1B	5B	5B	AR
52	2B	5D	5C	AR
53	(1) *	(2) *	64	AR
54	(1) *	(2) *	65	M
55	(1) *	(2) *	6D	M
56	47	6C	6C	M
57	48	75	75	M
58	49	7D	7D	M
59	4E	79	7C	AR
60	3A	58	14	M/B
61	1E	1C	1C	AR
62	1F	1B	1B	AR
63	20	23	23	AR
64	21	2B	2B	AR
65	22	34	34	AR
66	23	33	33	AR
67	24	3B	3B	AR
68	25	42	42	AR
69	26	4B	4B	AR
70	27	4C	4C	AR
71	28	52	52	AR
72	2B	5D	53	AR
73	1C	5A	5A	AR
74	59	67	09	M
75	5A	6E	0A	M

Key No.	Set 1	Set 2	Set 3	MODE
76	5B	6A	0B	M
77	4B	6B	6B	M
78	4C	73	73	M
79	4D	74	74	M
80	5D	65	7B	AR
81	2A	12	12	M/B
82	56	61	13	AR
83	2C	1A	1A	AR
84	2D	22	22	AR
85	2E	21	21	AR
86	2F	2A	2A	AR
87	30	32	32	AR
88	31	31	31	AR
89	32	3A	3A	AR
90	33	41	41	AR
91	34	49	49	AR
92	35	4A	4A	AR
93	57	62	51	AR
94	36	59	59	M/B
95	(1) *	(2) *	63	AR
96	4F	69	69	M
97	50	72	72	M
98	51	7A	7A	M
99	E01C	E05A	79	M
100	1D	14	11	M/B
101	38	11	19	M/B
102	39	29	29	AR
103	E038	E011	39	M
104	E01D	E014	58	M
105	(1) *	(2) *	61	AR
106	(1) *	(2) *	60	AR
107	(1) *	(2) *	6A	AR
108	5E	6D	02	M
109	52	70	70	M
110	53	71	71	M
111	5C	64	78	M

SET 1 BREAK CODE = MAKE CODE + 80H
SET 2 & SET 3 BREAK CODE = F0H PREFIX THEN MAKE CODE

* = (1) (2) SEE KEYS AFFECTED BY SHIFT, ALT & CTRL BELOW:

(1) Keys Affected by Shift, Alt & Ctrl (Set 1)

Key No.	Base Case or Shft + Num Lk (Make/Break)	Shift Case (See Note 1) (Make/Break)	Num Lock on (Make/Break)
32	E052/E0D2	E0AAE052/E0D2E02A	E02AE052/E0D2E0AA
53	E053/E0D3	E0AAE053/E0D3E02A	E02AE053/E0D3E0AA
105	E04B/E0CB	E0AAE04B/E0CBE02A	E02AE04B/E0CBE0AA
33	E047/E0C7	E0AAE047/E0C7E02A	E02AE047/E0C7E0AA
54	E04F/E0CF	E0AAE04F/E0CFE02A	E02AE04F/E0CFE0AA
95	E048/E0C8	E0AAE048/E0C8E02A	E02AE048/E0C8E0AA
106	E050/E0D0	E0AAE050/E0D0E02A	E02AE050/E0D0E0AA
34	E049/E0C9	E0AAE049/E0C9E02A	E02AE049/E0C9E0AA
55	E051/E0D1	E0AAE051/E0D1E02A	E02AE051/E0D1E0AA
107	E04D/E0CD	E0AAE04D/E0CDE02A	E02AE04D/E0CDE0AA
36	E035/E0B5	E0AAE035/E0B5E02A	

Note 1: If the left shift key is held down, the AA/2A shift make and break is sent with the other scan codes. If the right shift key is held down, B6/36 is sent. If both shift keys are down, both sets of codes are sent with the other scan code.

Key No.	Base Case (Make/Break)	Ctrl Case Shift Case (Make/Break)	Alt Case (Make/Break)
14	E02AE037/E0B7E0AA	E037/E0B7	54/D4

Key No.	Base Case (Make)	Ctrl Case (Make)
16	E11D45E19DC5	E046E0C6

Note: This key is not auto-repeat. All associated scan codes occur on the make of the key.

(1) Keys Affected by Shift, Alt & Ctrl (Set 2)

Key No.	Base Case or Shft + Num Lk (Make/Break)	Shift Case (See Note 1) (Make/Break)	Num Lock on (Make/Break)
32	E070/E0F070	E0F012E070/E0F070E012	E012E070/E0F070E0F012
53	E071/E0F071	E0F012E071/E0F071E012	E012E071/E0F071E0F012
105	E06B/E0F06B	E0F012E06B/E0F06BE012	E012E06B/E0F06BE0F012
33	E06C/E0F06C	E0F012E06C/E0F06CE012	E012E06C/E0F06CE0F012
54	E069/E0F069	E0F012E069/E0F069E012	E012E069/E0F069E0F012
95	E075/E0F075	E0F012E075/E0F075E012	E012E075/E0F075E0F012
106	E072/E0F072	E0F012E072/E0F072E012	E012E072/E0F072E0F012
34	E07D/E0F07D	E0F012E07D/E0F07DE012	E012E07D/E0F07DE0F012
55	E07A/E0F07A	E0F012E07A/E0F07AE012	E012E07A/E0F07AE0F012
107	E074/E0F074	E0F012E074/E0F074E012	E012E074/E0F074E0F012
36	E04A/E0F04A	E0F012E04A/E0F04AE012	

Note 1: If the left shift key is held down, the F0 12/12 shift make and break is sent with the other scan codes. If the right shift key is held down, F0 59/59 is sent. If both shift keys are down, both sets of codes are sent with the other scan code.

Key No.	Base Case (Make/Break)	Ctrl Case Shift Case (Make/Break)	Alt Case (Make/Break)
14	E012E07C/E0F07CE0F012	E07C/E0F07C	84/F084

Key No.	Base Case (Make)	Ctrl Case (Make)
16	E11477E1F014F077	

Note: This key is not auto-repeat. All associated scan codes occur on the make of the key.