
DECstation 320

DECstation 320
Technical Reference Manual

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DECstation 320 Technical Reference Manual

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Technical Reference Manual
Page Insertion Guide

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Also, a tagged divider for each section has been provided for insertion at this point.

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- Foldout Schematic page: Insert at the end of the Delta Power Supply section

Schematic	Switching Power Supply PK-200 EP

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Exploded View	Parts Ass'y Location 8790142
Schematic	8790142

- Foldout Timing Diagram: Insert at the end of the Section 4 SCSI Interface, in the Options section

SCSI Bus Timing Diagram	Figure 4-2

The *DECstation 320 Technical Reference Manual* describes the computer hardware components and their relationships to one another, as well as the BIOS (Basic Input Output Services).

The information in this manual is intended for hardware and software designers, engineers, programmers, and anyone who requires an understanding of the design and operation of the computer.

The *DECstation 320 Technical Reference Manual* is divided into two major sections, Hardware and Software. The hardware section provides information on system hardware architecture, including specifications, jumpers and switch settings, a theory of operation, schematics, and a devices section including timing diagrams. The hardware section is grouped into the following subsections:

Main Logic Board	Keyboard
Devices	Disk Drive
Power Supply	Options

The Software section contains information on system BIOS, scan codes, and other reference material needed for system assembly language programming. The software section is grouped into the following subsections:

A Quick Reference list of software interrupts
(for all device, I/O, and system status services)
Keyboard ASCII and scan codes
An MS-DOS memory map

The information in this manual is a supplement to and based on a working knowledge of the following literature:

The *DECstation 320 Installation and Operation Manual* (Packaged with the computer)

The Intel 80386 Programming Reference Manual. Intel order number 210498-005

The Intel 80386 Hardware Reference Manual. Intel order number 210760-002

80386 Data Sheet. Intel order number 210253-012

This Intel literature may be ordered directly from Intel at the following number: 1-800-549-4725

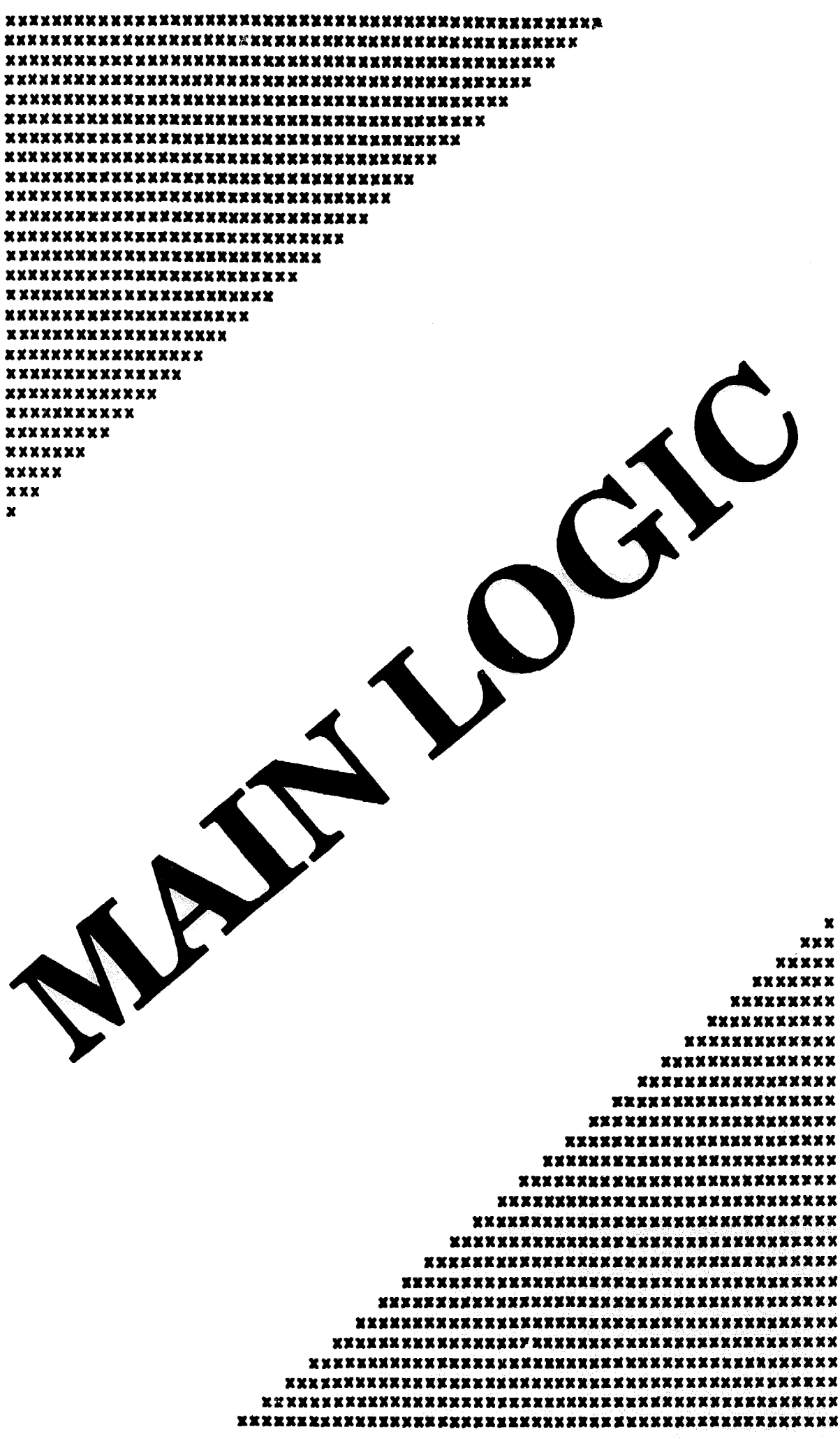

MAIN LOGIC

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Scope of Document

This document provides detailed specifications on the DECstation 320.

The DECstation 320 computer system is composed of four buses:

- **The 80386 Local Bus**—consists of the 80386 CPU, the 82C301 bus controller, and the optional Weitek Numeric Processor.
- **The 32-Bit Memory Bus**—consists of up to four banks of 32-bit access dynamic RAM (DRAM). Two banks are located on the main logic board which also has an expansion slot for an additional two banks. Each bank consists of either four 256 Kb x 9 DRAM modules or four 1 Mb x 9 DRAM modules with an access time of 100 ns.
- **The System I/O (AT) Bus**—contains the BIOS ROM devices, the floppy disk controller (FDC), and eight expansion slots (two IBM® PC-compatible and six AT-compatible) for optional devices, and the 80287 coprocessor.
- **The Peripheral Bus**—an extension of the system I/O bus; contains the direct memory access (DMA), interrupt, counter/timer, speaker, keyboard, and real-time clock (RTC) operations.

Each bus has different timing characteristics. For example, the 80386 bus operates at a clock rate of 20 MHz with either no wait state or one wait state when accessing 32-bit RAM, and the AT bus operates at 8 MHz with up to four wait states.

Introduction

Compatibility. The DECstation 320 is designed to be as compatible as possible with the existing IBM PC/AT™, in terms of both hardware and software.

Most operating systems and application programs that ran on the IBM AT will run on the DECstation 320.

Although 8- and 16-bit memory cards can be used on the AT bus, performance will be significantly increased compared to the 32-bit memory options.

Modular Design. The DECstation 320 is modular in design to allow maximum flexibility in system configuration. The computer consists of a main unit and a detachable keyboard with coiled cable. The main unit is supplied with one internal 3 1/2-inch, 1.44 Mb floppy disk drive. The standard types of monitors used with the DECstation 320 are the monochrome, RGB, and EGA monitors. Because these units are modular, they can be placed on top of the main unit or at any convenient location.

Memory. The DECstation 320 comes standard with 2 megabyte of 32-bit wide system RAM. This 32-bit wide System memory can be expanded to 2, 4, 8, 10 or 16 megabytes, the maximum RAM allowed by the system memory map.

Additional Features. Other features include a parallel printer port, a serial port, and a speaker for audio feedback.

Main Unit. The main unit is the heart of the DECstation 320. It houses the main logic assembly, the system power supply, optional hard disk unit, and the floppy disk drive.

The main logic assembly is a large board mounted on the floor of the main unit and connected to the keyboard, power supply, and disk drive by a series of cables.

The power supply is a 200 watt switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The floppy disk drive uses 3 1/2-inch, double-sided, double-density diskettes to read or write data. These are soft-sector diskettes. The disk drive assembly is installed in the main unit. The floppy disk stores approximately 1.44 megabytes (formatted) of data. All system programs, with the exception of the system startup sequence, are stored on disk.

Monitors. A monochrome, EGA, VGA, or RGB display can be used with the DECstation 320. The appropriate display adapter must be installed in the main unit.

Features

16 MHz, 32-bit 80386 processor with on-chip memory management and protection.

Standard 1 Mb, 0-wait state, 32-bit memory.

- Supports up to 8 megabytes of 32-bit wide memory
- Bus addressing supports PC (8-bit), AT (16-bit), and 32-bit data widths

Standard 1.44 Mb, 3 1/2-inch floppy disk drive.

- Selectable 1.44 Mb or 720 Kb format allows compatibility with the IBM PC/AT, or IBM PC
- Channel for additional internal floppy disk drive of 3 1/2-inch or 5 1/4-inch type

Channel for user-selectable hard disk drive.

Six IBM AT-compatible slots for standard peripherals and additional memory (16-bit) expansion.

Two IBM PC-compatible slots for standard peripherals and additional memory (8 bit) expansion.

One 32-bit memory upgrade slot.

- 2 Mb or 8 Mb for a total of 16 Mb
- 0 wait state (statistical)

True software compatibility with the IBM PC/AT in the single-user MS-DOS® (real) mode or the multi-user (protected) mode. Can support UNIX and MS-DOS concurrently in the Protected Mode.

Built-in real-time clock with CMOS RAM and battery backup.

Serial/parallel interface adapter included.

Enhanced IBM AT-compatible keyboard.

Support for optional Weitek 1167 math coprocessor.

200 watt power supply.

Physical Specifications

Width	19 in.
Height	6 in.
Depth	18 in.
Weight	47 lbs.

Switch Settings and Jumper Pin Configurations

Jumper	Function	As Shipped
E1-E2	Color/Monochrome Monitor installed = color not installed = monochrome	installed
E3-E4	80387 Coprocessor installed	not installed
E5-E6 and E6-E7	Floppy Disk Controller Select E5-E6 installed = primary FDC E6-E7 installed = secondary FDC	 installed not installed

Table 1. Switch Settings and Jumper Pin Configurations

Functional Description

The following sections of this document explain in detail the functions of the various devices found in the DECstation 320.

80386 Processor

General Overview

The 80386 processor is an advanced 32-bit microprocessor designed for applications needing very high performance. It is also optimized for multi-tasking operating systems.

The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes of virtual memory. Even though the processor will access up to four gigabytes of memory the implementation used in the DECstation 320 only supports up to 16 megabytes.

The integrated memory management and protection architecture includes address translation registers, advanced multi-tasking hardware, and a protection mechanism to support operating systems. The processor also allows the simultaneous running of multiple operating systems.

The 80386 consists of a central processing unit, a memory management unit, and a bus interface.

Central Processing Unit

The *central processing unit* consists of the *execution unit* and the *instruction unit.*

The execution unit contains the eight 32-bit general-purpose registers, which are used for both address calculation and data operations. In addition, it contains a 64-bit barrel shifter, which is used to speedshift, rotate, multiply, and divide data contained in the registers.

The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

Memory Management Unit (MMU)

The *memory management* unit consists of a *segmentation unit* and a *paging unit*.

Memory is organized into one or more variable length segments, each up to 4 gigabytes in size. A given region of the linear address space, a *segment*, has certain attributes associated with it. These attributes include its location, size, type, and protection characteristics. Each task on the 80386 can have a maximum of 16,381 segments of up to 4 gigabytes each, thus, due to the memory management organization of the processor, it provides 64 terabytes of virtual memory to each task. The segmentation unit provides four levels of protection for isolating applications and the operating system from each other. Even though the processor will address up to four gigabytes of memory, the DECstation 320 only supports up to 16 megabytes.

The 80386 has two modes of operation: Real Address Mode (Real Mode) and Protected Virtual Address Mode (Protected Mode).

In Real Mode, the 80386 operates as a very fast 8086 but with 32-bit extensions if desired. Real Mode is required primarily to set up the processor for Protected Mode operation.

Protected Mode provides access to the sophisticated memory management, paging, and privilege capabilities of the processor. Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics, thus allowing 8086 software to execute.

Bus Interface

Finally, to facilitate high-performance system hardware designs, the 80386 local bus offers address pipelining, dynamic data bus sizing, and direct byte enable signals for each byte of the data bus. These features are discussed in later sections of the this manual.

80387 Numeric Processor WTL1167 (Optional)

The optional 80387 Numeric Processor connects to the 80386 local bus through a 121-pin PGA socket designated U15. This IC provides a 32-bit data path to the CPU and performs 32- and 64-bit floating point operations on a variety of numeric data types. The 80387 effectively extends the register and instruction set of the 80386 based system for existing data types, as well as adding several new data types.

Clock Generation

The 82C301 (U14) provides three major system clocks:

- The processor clock, CLK2
- The BCLK for the AT bus state machine of the 82C301
- The AT bus clock, SYSCLK

The BCLK is a clock internal to the 82C301.

The clock generation circuitry uses two external clocks, CLK2IN and ATCLK1, as selectable clock sources. These are supplied by TTL oscillator (Y3). CLK2IN is a 40 MHz input signal and ATCLK1 is a 16 MHz input signal.

The clock input to the 80386 processor is CLK2, which is a 40 MHz signal. The clock signal provided to the AT bus is ATSCLK and is rated at 8 MHz and may be increased to 10 MHz by a mode speed option in software.

Command and Control Signals

Generation

The command and control signals necessary for system operation are generated by two devices: the 82C301 bus controller (U14) and the 82C306 control buffer (U13).

82C301 Bus Controller

This 84-pin PLCC device produces and synchronizes the CPU and system clocks and performs interfacing between the 80386 and the rest of the system control lines.

Reset Control

RESET1* is produced at power up/down or when the reset button on the front panel is depressed. When the RESET1* is asserted, the bus controller asserts RESET3 and RESET4 for a system reset. RESET3 is routed to the 80386 CPU and the Weitek coprocessor, and RESET4 is sent to the control buffer. For a warm restart not requiring an extensive reset, RESET2* can be asserted to generate RESET3 for resetting only the processor and coprocessor. RESET2* is generated by pressing the Ctrl, Alt, and Del keys on the keyboard simultaneously. RESET3 is also asserted when a CPU shutdown is detected. This differentiation is provided so that some register states can be maintained through the reset if so desired.

Bus Arbitration

General

The bus controller performs the synchronization and control required for communication between the local processor bus, the memory subsystem, and the system I/O (AT) bus. It controls all bus activities and handles the HRQ1, HRQ2, and REFREQ signals by generating a HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner.

Upon the CPU assertion of HLDA, the arbitration logic responds by asserting HLDA1 (for HRQ1), or HLDA2 (for HRQ2). The requesting DMA or master device has control of the bus until it de-asserts the HRQ1 signal to terminate the HLDA cycle. During the HLDA cycle, the bus controller generates both SMCMD* and AC0 through AC3 to control the buffer enable and directions for the address and data buffers. HRQ2 is disabled in the DECstation 320. Bus size conversions are not supported by the bus controller for these bus cycles and if necessary should be performed by the requesting device.

All CPU access cycles are started by the bus controller asserting the MALE* signal. The bus controller then samples the AF32* signal one SCLK clock cycle later. If AF32* is active, the cycle is assumed to be a local bus cycle and the bus controller terminates this cycle when it detects the READY* signal active. In response to an MALE*, if AF32* is detected inactive, the control is passed to the AT bus control portion of the bus controller. At the end of the bus access cycle, the AT bus control logic of the bus controller generates READY* to terminate the processor access cycle.

CPU Bus

Interface to the 80386 requires interpretation of the status lines upon assertion of the ADS* signal. It also requires synchronization and generation of a READY* response to the CPU upon completion of the requested operation.

By interpreting the CPU status lines and the ADS* signal, the bus controller generates control signals MALE* and SMCMD*. In response to each ADS* signal generated by the CPU, a MALE* signal is generated by the bus controller to indicate the start of a new CPU access cycle.

In a non-pipelined CPU cycle, MALE* is generated in response to the ADS* signal being asserted by the 80386. In a pipelined cycle, MALE* is generated when the assertion of the READY* signal is detected for the previous CPU cycle.

If the AF32* signal is not active one cycle after MALE* is asserted, control is passed to the AT bus control section of the bus controller. The bus controller then waits for READY* to become active to terminate the access cycle. The READY* signal can also be generated by the 82C302 (U27) page/interleave memory controller, which controls the system memory access.

SMCMD* indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles, SMCMD* is generated for all memory cycles by decoding the M/(IO)*, D/(C)* and W/(R)* signals. During non-CPU cycles, SMCMD* is active when XMEMR* or XMEMW* signals are active.

Bus Timeout

An optional feature allows generation of a *non-maskable interrupt* (NMI) if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32* is asserted in response to MALE* and READY* is not returned to the bus controller within 128 CLK2 cycles. A control bit in the 82C301 Bus Controller's Port B register enables this feature and will be explained later in this section.

AT Bus

The bus controller gains control of the AT bus when AF32* is detected inactive. It also performs the necessary synchronization of control and status signals between the AT bus and the processor. The bus controller supports 8-, 16-, or 32-bit transfers between the processor and 8-, 16-, or 32-bit memory or I/O devices located on the I/O bus.

An AT bus cycle is initiated by asserting the ALE signal that is decoded from the CPU status signals and is terminated by asserting READY*. On the trailing edge of ALE, the signals MCS16* and IOCS16* are sampled to determine the bus size conversion required. The bus controller then enters the command cycle. The bus controller provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide timing emulation of lower-speed I/O channels to maintain compatibility with AT or PC/XT I/O adapters and memory cards. The command cycle is terminated by detecting OWS* or IOCHRDY* active.

I/O Channel Speed Control

The bus controller AT bus logic can be programmed to insert wait states in units of ATSCLK and to delay the generation of the XIOR*, XIOW*, XMEMR*, and XMEMW* commands in one-half units of ATSCLK within the selected wait states. The command phase delay can be selectively defined for I/O cycles and for 8-, 16-, or 32-bit wide memory cycles by setting the corresponding fields in the Port B register location 05H. This location controls the I/O channel wait state generation for 8-, 16-, and 32-bit accesses.

Data Conversion

The bus controller performs data conversions for CPU accesses to devices not on the local bus when AF32* is not asserted. AT bus conversions are performed for the following types of transfers:

- 32-bit to 8-/16-bit
- 24-bit to 8-/16-bit
- 16-bit to 8-/16-bit

Larger transfers are broken into smaller AT bus reads or writes and the action codes A0-A3 to the control buffer are generated. Byte Addresses XA0-XA1 are generated to drive the lower two bits of the AT bus.

The bus controller responds to IOCS16*, MCS16*, IOCS32*, and MCS32* to determine what size of data the I/O channel needs. If none of the above signals is asserted, 8-bit transfers are assumed and the request is converted into two, three, or four I/O channel cycles, based on BE0-BE3. For either MCS16* or IOCS16*, the bus controller converts a 32-bit access into two 16-bit AT bus accesses.

The bus controller also supports 32-bit transfers between the processor, memory, and the I/O devices on the I/O channel. IOCS32* and MCS32* inputs allow a device to request a 32-bit transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32* and MCS32* override IOCS16* and MCS16*.

In performing these data conversions, the bus controller generates a 4-bit action code AC0-AC3 to control the buffers in the 82B305 data buffer. This is done for the alignment of data path and direction control between the D, MD, and SD data buses. The functional description for these codes is given in the section on "82B305 Data Buffers."

Port B Register

The bus controller contains an AT-compatible configuration register called the Port B register. The following table gives the bit definitions for it:

Port	Bit	Default	Type	Function
61H	7	0	Read Only	System Parity Check
	6	0	Read Only	I/O Channel Check
	5	0	Read Only	Timer 2 Out
	4	0 or 1	Read Only	Refresh Detect
	3	1	Read/Write	Enable I/O Channel Check
	2	1	Read/Write	Enable Parity Check
	1	0	Read/Write	Speaker Data
	0	0	Read/Write	Timer 2 Gate Speaker

Table 2. Bit Definitions for Port B Register

The bus controller can also be programmed to vary the number of wait states and command delays to the system bus as well as to change the bus clock speed. This is done by writing the address of the Index Register to the Index Register port (22H) and then writing or reading the desired value to or from the Data Register port (23H). Tables 3 - 5 provide the definitions of the Programmable Index Registers:

Note: Use a JMP$+2 instuction between I/O port accesses to allow bus settle time.

Index 04H Version/Processor Clock Select/NMI Source		
Bit(s)	**Function**	**Default(s)**
7,6	Version (0=initial version)	0,0
5	Reserved	0
4	Processor Clock Select 0=Use processor oscillator input (20 MHz) 1=Use AT bus state machine clock (SYSCLKx2) (8 MHz)	0
3	Enable/Disable power fail NMI 0=Disable 1=Enable	0
2	Enable/Disable READY timeout NMI 0=Disable 1=Enable	0
1	Enable/Disable power fail warning pin 0=Disable 1=Enable	0
0	READY timeout has/has not occurred 0=Ready timeout has occurred 1=Ready timeout has not occurred	0

Table 3. Index 04H Bit Definitions

Index 05H	**Command Delay**	
The value for each of the command delay fields is as follows: 0 = 0-cycle delay 1 = 1-cycle delay 2 = 2-cycle delay 3 = 3-cycle delay		
Bit(s)	**Function**	**Default(s)**
7,6	AT bus 32-bit memory command delay	0,0
5,4	AT bus 16-bit memory command delay	0,0
3,2	AT bus 8-bit memory command delay	0,1
1,0	AT bus I/O cycle command delay	0,1

Table 4. Index 05H Bit Definitions

Index 06H	Wait State/Bus Clock Source	
Bit(s)	**Function**	**Default(s)**
7,6	Wait states per 32-bit transfer 0 = 3-cycle delay 1 = 2-cycle delay 2 = 1-cycle delay 3 = 0-cycle delay	0,1
5,4	Wait states per 16-bit transfer 0 = 3-cycle delay 1 = 2-cycle delay 2 = 1-cycle delay 3 = 0-cycle delay	0,1
3,2	Wait states per 8-bit transfer 0 = 5-cycle delay 1 = 4-cycle delay 2 = 3-cycle delay 3 = 2-cycle delay	0,1
1,0	Bus clock source select 0 = Use processor clock/3 for AT bus state machine (6.67 MHz) 1 = Use processor clock/2 for AT bus state machine (10 MHz) 2 = Reserved 3 = Use ATCLK input pin for AT bus state machine (8 MHz)	0,1

Table 5. Index 06H Bit Definitions

82A306 Control Buffer

The control buffer contains the circuitry for decode and generation of the AF32* signal, parity generation, parity checking, byte enable latching of data for the memory cycle, and color reference signal generation.

14 MHz Oscillator and Divider

The color reference oscillator is provided by the bus controller IC (U13), thus eliminating the 8224 device normally used in AT-compatible systems. A *divide by 12* counter is also included to generate the OSC/12 (1.19 MHz) signal used on the main logic board. The raw clock is supplied by crystal Y2.

AF32* Generation

The AF32* signal generated by the 82A306 is not used in the DECstation 320 system.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located in the control buffer. An additional input (FBE*) is provided to force all byte enables active during certain memory operations.

Parity Checking and Generation

The control buffer provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH0-PPH3 and PPL0-PPL3, which are generated on the two (nibble wide) 82A305 data buffers (U23, U24).

For a memory read access, read parity bits PPH0-PPH3 and PPL0-PPL3 are checked against the parity bits MP0-MP3 read from memory. Parity bits PPH0-PPH3, PPL0-PPL3, and MP0-MP3 are latched by CAS* and PCHK* so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes that are not valid. The OR'ed byte-wise parity error is then latched as the output LPAR* if PEN* input is asserted.

During a memory write access, write parity for each byte is generated from PPH0-PPH3 and PPL0-PPL3 and can be gated onto the memory parity bus MP0-MP3 if the control buffer is enabled by the WPE* signal controlling the tri-state drivers.

Bus Drivers

24mA bus drivers are provided for some of the control signals on the I/O channel. These signals include SYSCLK, OSC, OSC/12, RESETDRV, SBHE*, BALE, IOR*, IOW*, MEMR*, MEMW*, SMEMR*, SMEMW*, and OUT1*. The fuctionality for these signals is covered under "I/O Decode" and "Memory Control and Refresh."

Memory Control and Refresh

82C302 Memory Controller

Memory Configuration

The memory control functions in this system utilize Page Mode Access DRAMs. Memory is organized as 36-bit banks (32 bits for data and 4 bits for parity) using four 9-bit SIMM boards per bank. The system will support up to 16 Mb of 32-bit DRAMs using 1 Mb x 9 modules.

The minimum configuration is a single bank operating in Non-Interleaved Mode.

The memory controller is designed such that the memory can be upgraded from one to two banks, making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair. However, each pair of banks can use different DRAM types. One or both banks of smaller DRAM types can later be upgraded to banks of larger DRAMs.

The following table shows the available configurations:

Number of Banks	Number/Size of SIMMs	Total Memory
1	4 - 256 Kb x 9	1 Mb
1	4 - 1 Mb x 9	4 Mb
2	8 - 256 Kb x 9	2 Mb
2	8 - 1 Mb x 9	8 Mb
4	16 - 256 Kb x 9	4 Mb
4	8 - 256 Kb x 9	
	8 - 1 Mb x 9	10 Mb
4	16 - 1 Mb x 9	16 Mb

Table 6. Available Memory Configurations

Page-Interleaved Operation

The memory controller uses a page-interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses stored in the other. If accesses are sequential (or at least made to alternating even and odd addresses) the RAS precharge time of one set might overlap the access time of the second set. Typically the hit rate (the fraction of times that the required bank is available) is 50%. This is especially true since operand accesses can be interspersed with instruction fetches.

Page Mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256 Kb x 1 DRAM) that are subsequently selected using the column address. Once a row address has been made, higher-speed random access can be made to any bit within the row.

Page Mode access and cycle times are typically half those of the normal access and cycle times. During Page Mode operation any access to the currently active RAS page would occur in the page access rather than the normal access time. Any subsequent access could be to anywhere in the same page without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving.

Memory Access and Arbitration

The memory controller controls the DRAM memory access from three sources: the CPU, the DMA, and the refresh request. These accesses are arbitrated based on the inputs of HLDA1* and REF*.

CPU Access

The CPU-initiated accesses are decoded according to the memory map defined in the Configuration Registers. These registers are at 08H to 0FH and are covered later in this section. These are the only accesses that use the Page Mode operation of the DRAMs.

The memory controller maintains four page registers, in which it stores the page addresses of the most recently accessed DRAM pages of the two-way interleaved banks. These four registers are called Active Page Registers. Accesses to the active pages are called *hits* and are faster because the DRAM is operated in the Page Mode with the RAS signal staying asserted.

The memory controller supports memory configurations with either one, two, or four banks. Because one Active Page Register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration, only one Active Page Register is in use. For each Active Page Register in use, the corresponding RAS* stays asserted after the previous access. If an access does not hit any active pages, a *miss* cycle, the normal DRAM access cycle is entered by first de-asserting the RAS* associated with the bank accessed.

RAS and CAS Generation

The memory controller is based on 2 Kb page-interleaved organization. The following table shows the address lines used for the different organizations:

For Non-Interleaved Operation (One Bank Only)

DRAM Type	Row	Column
256 Kb DRAMs	A11-A19	A2-A10
1 Mb DRAMs	A12-A21	A2-A11

For Interleaved Memory (Two or Four Banks)

DRAM Type	Row	Column
256 Kb DRAMs	A12-A20	A2-A10
1 Mb DRAMs	A12-A21	A22, A2-A10

Table 7. Address Lines for Available Memory Configurations

In interleaved memory cases, Bit A11 determines which one of the even page banks or odd page banks is accessed. For configurations using only 256 Kb DRAMs, A11 and A21 are used to control RAS0*-RAS3*. For those using only 1 Mb DRAMs, A11 and A23 are used. For those using both 256 Kb and 1 Mb DRAMs, the 1 Mb DRAMs must occupy the first two banks and the 256 Kb DRAMs must occupy the second two banks. This constraint is there to ensure that there will not be a hole in the address space without actual DRAMs.

RAS Timeout

When using DRAM Page Mode, you must observe the maximum RAS pulse width. For most DRAMs, this is 10 microseconds. Using the OSC/12 (1.19 MHz) clock generated by the control buffer timers are maintained within the memory controller for each bank to assure data integrity . RAS is de-asserted for each bank when its counter times out at about 10 microsecond intervals. The Memory Configuration Register bit 13H Bit 7 can be programmed to set the desired RAS time-out interval for each bank. See Table 13, later in this section, for details.

Refresh

To reduce power supply noise cause by surges during RAS transitions, RAS pulses to each bank are automatically staggered by one CLK2 cycle. Because all RAS's could be active for Page Mode operation, a refresh cycle requires that all RAS's be first de-asserted then asserted with the correct refresh address.

Direct-Memory Access

Direct-memory accesses are initiated by asserting the signal HLDA1. The XMEMR* and XMEMW* signals determine whether the access is a read or write memory access. The bytes accessed are controlled externally with the BE0*-BE3* signals generated by the bus controller. The memory controller makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers.

DRAM Access Logic

The DRAM control logic generates the necessary RAS, CAS, and DWE signals for all DRAM accesses. CPU, DMA, and refresh access cycles use DA8-DA9, XDA0-XDA7, and bank select signals BA0-BA1. (Note that in the current version of the memory controller, the signals BA0-BA1 default to zero.) The memory controller control logic provides the signal MDEN* to control the buffer chips. MDEN* enables data buffers for the MD bus for non-refresh DRAM cycles.

Note: "Default Configuration" refers to IC power up. The BIOS will reprogram these values.

Memory Mapping Logic

The memory controller Configuration Registers, located at Port 22H Index 08H-13H define what is a valid memory access and what is a ROM memory access, according to the local bus addresses. Registers 08H and 09H determine how ROM areas (as defined by an IBM AT) between the 768Kb to 1Mb address range are accessed.

For valid local memory accesses, the memory controller asserts the AF32* signal to indicate that it has control of the local bus and also asserts the READY* signal at the end of the access cycle. If an access is a ROM access, the memory controller asserts ROMCS* to provide controls for the ROMs. In this case, the READY* signal must be provided to the CPU and memory controller by the bus controller.

Clock, Reset, and Miscellaneous Logic

The RESET4 signal causes all internal registers to be reset to their default values. Configuration Registers not specified with default values are not reinitialized and might not retain their old values. The memory controller control logic generates the PCHK* and PEN* signals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

The memory controller contains Index Registers used to configure the memory. These are accessed like the registers in the bus controller. Write the index address to Port 22H and then the programming value out to the Data Port 23H. XDEN* is asserted for these accesses to control the buffer connecting the XD and XDA buses. The Data Port can also be read.

Memory Configuration Registers

The Configuration Registers 08H to 0FH are used to control how the CPU memory accesses are defined. They define all addresses as ROM accesses, DRAM accesses, other local CPU bus accesses, or I/O channel accesses. These provisions are made because the low 1 megabyte is occupied by both DRAMs and ROMs and also devices on the AT bus. For ROM accesses, the memory controller generates the ROMCS* signal to control the ROM access. For DRAM access, the memory controller generates the necessary DRAM controls to the system memory under its control. It generates AF32* for all other local CPU bus accesses, and it does not control the I/O channel accesses.

The bus controller (U14) provides three 256 Kb areas where the ROMs can be located. The functions of these areas are as follows:

Area	Location	Function
Low ROM	Just below the 1 megabyte address	8086-compatible operation
Middle ROM	Below the 16 megabyte address	80286-compatible operation
High ROM	Below the 4 gigabyte address	80386 operation

Table 8. Functions of ROM Areas

On system reset, the default Configuration Register setting causes accesses to these three ROM areas to generate ROMCS*. The high ROM area is always recognized by the memory controller as BIOS ROM access area. The other two ROM areas can be mapped to be either ROM or RAM access.

After reset, Register 08H Bits 3 and 4, (See Table 9), can be programmed to map the entire middle ROM area to DRAM with write protection if desired.

Register 08H Bit 2 determines whether the bus controller recognizes the addresses generated beyond 16 megabytes as local CPU bus cycles.

Register 08H Bit 1 is used to enable Registers 0AH-0FH, which control the low megabyte DRAM (40000H-FFFFFH) address mapping for 256 Kb to 1Mb addresses in 16 Kb blocks. This bit defaults upon reset so that only the 0-256 Kb areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed.

Register 08H Bit 0 defaults to single-bank memory configuration upon reset. Therefore it must be programmed to enable page/interleaved operation.

Register 09H controls the address mapping and write protection for the low ROM area (C0000H-FFFFFH) in 64 Kb blocks. (See Table 10.) Registers 0AH-0FH define whether each 16 Kb address range is a DRAM block in the system memory or on the I/O channel. (See Table 11.)

DRAM Array Configuration and Timing

The Configuration Registers 10H-13H provide the DRAM type definition and starting address for each pair of banks, Banks 0 and 1 and Banks 2 and 3.

Register 10H Bits 6 and 7 and Register 12H Bits 6 and 7 define whether the DRAMs are enabled, and if so, whether the system uses 256 Kb DRAMs or 1 Mb DRAMs. (See Table 12.) These bits default to 256 Kb DRAMs upon reset.

Register 10H Bits 0-5 and Register 12H Bits 0-5 define the Address Bits 20-25 of the starting address of the pairs of banks. (See Table 12.) Some of these banks might not be valid because the memory banks must start at some predefined boundaries. For 256 Kb DRAMs, all six bits (20-25) are valid if only a single bank is enabled. The banks starting address can be on any 1 megabyte boundary. Otherwise, only Bits 21-25 are valid starting address bits on 2 Mb boundaries. For 1 Mb DRAMs, only Bits 23-25 are valid, forcing the banks starting address to be on 8 Mb boundaries.

Register 11H Bit 7 and Register 13H Bit 7 define the RAS precharge time required when a page miss occurs so that DRAMs of different speeds can be supported for each pair of banks. (See Table 13.)

Register 11H Bit 6 and Register 13H Bit 6 define the wait state to be inserted to meet the DRAM speed. (See Table 13.) These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions about the DRAM speed and the memory configuration.

Tables 9-15 describe the functions of the memory controller's programmable registers:

Identification Register (08H)		
Bit(s)	**Function**	**Default Value**
7	Controller type	0
6-5	Version 0 = initial	0,0
4	Read/Write or Read Only of 256 Kb RAM at 16128K 00FC000H 0 = read/write 1 = read only	0
3	Disable/Enable BIOS ROM below 16 Mb 0 = disable 1 = enable	0
2	Assert/Do not assert AF32* for addresses above 16 Mb 0 = do not assert 1 = assert	0
1	Use/Ignore memory configuration Registers 0AH-0FH 0 = ignore 1 = use	1
0	Disable/Enable interleave 0 = disable (use single bank) 1 = enable	0(*)

* 0 for one bank of 32-bit memory (1 megabyte)
  1 for two banks of 32-bit memory (2 megabytes or more)

Table 9. Register 08H

RAM/ROM Boot Area Configuration Register (09H)		
Bit(s)	**Function**	**Default Value**
7-4	Disable/Enable writing to RAM located in BIOS 0 = read/write 1 = read only	0
	Bit 7 (RAM at 768K C0000-CFFFF)	0,1*
	Bit 6 (RAM at 832K D0000-DFFFF)	0,1*
	Bit 5 (RAM at 896K E0000-EFFFFH)	0,1*
	Bit 4 (RAM at 960K F0000-FFFFFH)	0,1*
3-0	Disable/Enable substituting BIOS ROM below 1 megabyte with RAM at the same address 0 = disable 1 = enable	1
	Bit 3 (ROM at 768K C0000-CFFFF)	0,0*
	Bit 2 (ROM at 832K C0000-DFFFF)	0,0*
	Bit 1 (ROM at 896K E0000-EFFFFH)	0,0*
	Bit 0 (ROM at 960K F0000-FFFFFH)	1,0*

* Default values change after ROM is initialized (ROM code is moved into DRAM.) The first value is the default before initialization. The second is the default after initialization.

Table 10. Register 09H

Selective Enabling/Disabling of 16 Kb Blocks of RAM (Registers 0AH,0BH, 0CH, 0DH, 0EH, and 0FH)

0 = System board controls address
1 = Address is on the I/O channel

Register	Block (Address Map)	Default Value
0AH	040000-05FFFFH	00H
0BH	060000-07FFFFH	00H
0CH	080000-08FFFFH	00H
0DH	0A0000-0BFFFFH	FFH*
0EH	0C0000-0DFFFFH	FFH*
0FH	0E0000-0FFFFFH	FFH*

* Default depends on options in I/O channel and use of expansion memory.

Table 11. Registers 0AH-0FH

Bank Type/Starting Address (10H for Banks 0/1, 12H for Banks 2/3)		
Bit(s)	**Function**	**Default Value**
7-6	Bank enabled/disabled 0 = bank disabled 1 = bank enabled with 256 Kb words (default) 2 = bank enabled with 1Mb words 3 = reserved	40H for 10H; varies for 12H*
5-0	Starting address bits 25-20 256 Kb DRAMs 1 Mb per bank (first bank only) 25-21 256 Kb DRAMs 1 Mb per bank (two banks required) 25-23 1 Mb DRAMs 4 Mb per bank (two banks required)	

* Index 12H default equals 00 if there are no Banks 2/3. It equals 42H for Banks 2/3 if 256 Kb DRAMs are used.

Table 12. Registers 10H and 12H

Bank Timing (11H for Banks 0/1, 13H for Banks 2/3)		
Bit(s)	**Function**	**Default Value**
		00H, 00H
7	RAS precharge time for a page miss 0 = 3 CLK2 times (93 ns) 1 = 5 CLK2 times (155 ns)	
6	Access wait states 0 = 0 wait states 1 = 1 wait state	
5-0	Reserved	

Table 13. Registers 11H and 13H

Error Source/Address (MSBs) (Register 28H)		
Bit(s)	**Function**	**Default Value**
7	Enable/Disable parity check 0 = enable 1 = disable	0
6-2	Not Used	
1-0	High parity address bits (25,24) (read only)	

Table 14. Register 28H

Parity Error Address (LSBs) (Register 29H)		
Bit(s)	**Function**	**Default Value**
7-0	Error address bits (23-16) (read only)	

Table 15. Register 29H

Memory Expansion

The main logic board contains sockets for eight SIMM boards (Banks 0 and 1) of DRAMs. Using 1 Mb x 9 SIMMs, this gives 8 megabytes of on-board memory. If more memory is desired, a 32-bit memory expansion card is available that contains eight more SIMM boards (Banks 2 and 3). Because of the interleaved nature of the memory, both Banks 2 and 3 must be used with this card. Using this option can expand the total system memory to a total of 16 megabytes. This card is plugged in the Number 1 expansion slot. It is incompatible with standard AT-type option cards.

Address Buffers

82A303 High Address Buffer (U20)

Address Decode

The address decode circuit provides as outputs the signals LIOCS*, LMEGCS*, L64MEG*, and HIROM*. These signals are active if the address accesses satisfy the conditions defined in Table 16. The signal decodes for LIOCS* and LMEGCS* are controlled by HLDA1 and are latched onto the trailing edge of MALE*. The L64MEG* and HIROM* signals are simply decoded from the address signals.

Signal	Decode Condition
LIOCS*	A12-A15 = 00H
LMEGCS*	A20-A31 = 00H
L64MEG*	A26-A31 = 00H
HIROM*	A26-A31 = 3FH

Table 16. Address Access Conditions

Address Bus Interfaces

The 82A303 interconnects the local X and system address buses. Bidirectional drivers connect each bus and the internal buses. These drivers have 24 mA current drivers for direct connection to the system address bus. Table 17 shows how the drivers are configured between the buses for each type of active bus request. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

For all CPU-sourced accesses, the addresses are latched on the trailing edge of MALE*.

Active Signal	Source Bus	Target Bus
HLDA1	XA	SA, A, MA
MASTER*	SA	XA, A, MA
REF*	—	SA driven low
ATEN	A	XA, SA, MA
Default	A	MA

Table 17. Bus Direction Request Types

27-Bit Extensions

The standard AT implementation supports only 24-bit addresses. The system architecture allows for address extension on the SA and XA buses to 27 bits (128 Mb). This is done by grounding the enable pin XBHE for the XA bus and the enable pin SBHE for the SA bus. Internal pullups are provided so that if the enable pins are left unconnected Bits 24-27 of the respective bus are forced low.

82A304 Low Address Buffer (U21)

Address Decode

The signals IO2XCS*, 8042CS*, PORTBCS*, NMICS*, 287CS*, and AS provide the lower address decodes for the corresponding devices after being qualified by the LIOCS* signal generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT I/O addresses and is shown in Table 18. For applications that require these devices to be relocated, the EXDEC signal can be tied low to ignore the LIOCS* qualification and the MA10-MA11 address bits.

Signal	Address Decoded
IO2XCS*	022H, 023H
8042CS*	060H, 064H
PORTBCS*	061H
NMICS*	070H
287CS*	0E0H to 0FFH

Table 18. Address Decode

Address Bus Interfaces

The 82A304 interfaces between bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER*, REF*, and ATEN* signals to drive the signals from the source to the target buses as defined in Table 19 for each active signal. When REF* is asserted, the refresh counter is gated to the SA bus as the refresh row address and is incremented. When none of the listed signals is active, the default configuration is such that the A bus drives the MA bus for memory accesses by the CPU.

The SA00-SA11 signals are 24 mA address buffers for direct interface to the AT bus.

Active Signal	Source Bus	Target Bus
HLDA1	XA	SA, MA, A
MASTER*	SA	XA, MA, A
REF*	Counter	SA
ATEN*	A2-A11	SA2-SA11, XA2-XA11, MA4-MA11
	XA0-XA1	SA0-SA1
default	A	MA

Table 19. Bus Direction Request Types

Data Buffers and Conversion Logic

82B305 Data Buffers (U23, U24)

The data buffers interface between the local, memory, and system (I/O channel) data buses and provide data alignment and size conversion for AT I/O channel operations. It is designed as a nibble slice to reduce pin count. Two of the devices are incorporated into the system design and are used to interface all buses.

Bus Controls

The data buffers control the bus buffers according to the signals HLDA1, ATEN*, MDEN*, LDEN*, SDIR, MRD*, and AC0-AC3. The first group of signals (HLDA1, ATEN*, MDEN*, and LDEN*) determine which buses are connected and the second group of signals (SDIR, MRD*, and AC0-AC3) determines the direction of the buffers' drivers.

All drivers are active for the active buses, and external bus controls are required if selected data bits need to be controlled. For the DRAM interface, the LBE0*-LBE3* signals must be used to ensure that only the valid data bytes are written to the DRAMs during a write cycle. Table 20 outlines bus connections for different bus cycles.

Bus Cycles	From Bus	To Bus	Direction Control
HLDA1 = 0	D	MD	MRD* =1
ATEN* = 1	MD	D	MRD* =0
HLDA1 = 0	D	SD	SDIR =1
ATEN* = 0	SD	D	SDIR =0
HLDA1 = 1	SD	MD,D	SDIR =0
			MRD* =1
	MD	SD	SDIR =1
			MRD* =0
	D	SD	SDIR =1
			MRD* =1
			LDEN* =0

Table 20. Bus Control Definitions

Data Conversion

The data buffers provide the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action code signals AC0-AC3 are used to control how the bus bits are connected between the I/O channel SD bus and the CPU local Bus D or the system memory MD bus. The action code signals are provided by the 82C301 bus controller for CPU-to-AT bus access cycles and are qualified by the ACEN signal. The meanings of the action code signals are given in Table 21.

AC0-AC3	From Bus	To Bus
0	MD,D Bits 0-15	SD Bits 0-15
1	MD,D Bits 8-15	SD Bits 8-15
		SD Bits 0-7
2	MD,D Bits 16-31	SD Bits 0-15
3	MD,D Bits 24-31	SD Bits 8-15
		SD Bits 0-7
4	MD,D Bits 0-31	SD Bits 0-31
5	SD Bits 0-7	MD,D Bits 0-7
6	SD Bits 0-7	MD,D Bits 8-15
7	SD Bits 0-7	MD,D Bits 16-23
8	SD Bits 0-7	MD,D Bits 24-31
9	SD Bits 0-15	MD,D Bits 0-15
A	SD Bits 0-15	MD,D Bits 16-31
B	Reserved	
C	SD Bits 0-31	MD,D Bits 0-31
D	Reserved	
E	Reserved	
F	Reserved	

Table 21. Action Code Definitions

System I/O (AT) Bus

The DECstation 320 system I/O (AT) bus is 100% compatible with the IBM AT bus. It has an open-bus structure that allows multiple microprocessors to share system resources. A total of eight expansion slots are available (six AT- and two PC type). Some features of this bus are:

- 24-bit memory addressing
- 8- or 16-bit data accesses
- I/O addressing range of 100 to 3FF hex
- Interrupt and DMA support
- I/O wait state generation

ROM Subsystem

The on-board ROM consists of two EPROM modules, each capable of holding up to 32 kilobytes of data, or 64 kilobytes total. One module contains the even address BIOS code. The other contains the odd address code.

I/O Decode

82C206 Integrated Peripherals Controller (IPC)

The 82C206 (U8) is an LSI implementation of the standard peripherals required to implement an IBM AT system board. This device contains the equivalent of:

- Two 8237A DMA controllers
- A 74LS612 mapper
- Two 8259A interrupt controllers
- An 8254 counter/timer
- An MC146818 real-time clock with RAM

The IPC provides all the standard peripherals required for a system board implementation, except the keyboard interface controller.

DMA Controllers. The two DMA controllers are connected in such a way as to provide four channels of DMA (DMA1) for 8-bit transfers and three channels of DMA (DMA2) for 16-bit transfers. (The first 16-bit DMA channel is used for cascading.) The BIOS programs the DMA controllers at power up as follows:

Master Clear issued to both controllers
All eight channels are first set to–
    Single mode select
    Verify transfer
    Autoinitialization disabled
    Address increment select
Then channel 4 is set to cascade mode and enabled.

Mapper. Included as part of the DMA subsystem is the Page Register (DMAPAGE) device, which is used to supplement the DMA and drive the upper address lines when required.

Interrupt Controllers. The IPC provides 16 channels of interrupt, partitioned into two cascaded controllers (INTC1 and INTC2) with eight inputs each. Three of the sixteen channels are connected internally to various devices. The remaining 13 interrupt channels are user-definable. The BIOS programs the interrupt controllers at power up as follows:

Slave Controller - First Interrupt at 70h
Call address interval = 4 bytes
Slave ID = 2
8086/8088 Mode
Normal EOI
Non-buffered mode
Not special fully nested mode
Cascade mode
Edge triggered mode

Master Controller - First interrupt at 08h
Call address interval = 4 bytes
Slave on IRQ2
8086/8088 mode
Normal EOI
Non-buffered mode
Not special fully nested mode
Cascade mode
Edge triggered mode

The Pre-unmasked IRQs at boot time are:

IRQ0	Timer Tick Clock
IRQ1	Keyboard
IRQ2	Cascade for Slave
IRQ6	Floppy Disk
IRQ9	Software redirected to INT 0Ah for old IRQ2
IRQ14	Hard Disk (If Present)

The three internally connected channels are:

- Channel 0 - Counter/Timer Counter 0 Interrupt
- Channel 2 - Cascade to INTC2 (Slave Interrupt Controller)
- Channel 8 - Real-Time Clock Interrupt

Counter/Timer. The counter/timer (CTC) subsystem contains three independent counters: Counters 0, 1, and 2. All three counters are driven from a clock input pin (TMRCLK) that is independent from the other clock inputs to the device.

Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as timekeeping and task-switching.

Counter 1 can be programmed to generate pulses or square waves for use by external devices.

Counter 2 is a full-function counter/timer that has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or a gated rate/pulse generator.

Real-Time Clock. The real-time clock (RTC) subsystem contains a clock/calendar to maintain the real time and date. In addition, it contains 114 bytes of RAM. To keep the clock/calendar and RAM active when the system is turned off, you must connect the device to an external battery. The DECstation 320 uses a lithium battery attached to the drive tower for this purpose.

Control of Subsystems

Interconnection and control of all the major subsystems is accomplished via a top-level control section. For discussion purposes, this control section is divided into two subsections:

- **Clock and Wait State Control Section** – controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device.
- **Top-Level Decoder** – accommodates the 200-plus registers in the IPC and maintains I/O decode compatibility with the IBM AT. The top-level decoder generates enables to the various subsystems. This subsystem also handles control and direction of the XD0-XD7 data buffers.

Top-Level Decoder

The IPC top-level decoder provides eight separate enables to various internal subsystems of the device. The following is a truth table for the top-level decoder:

ACK*	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Selected Device
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	1	071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPG
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	Disabled	
X	1	X	X	X	X	X	X	X	X	X	Disabled	
X	X	1	X	X	X	X	X	X	X	X	Disabled	

Table 22. Truth Table for Top-Level Decoder

The enabling of the IPC XD0-XD7 output buffers is also controlled by the top level decoder. The output buffers are enabled whenever an enable is generated to an internal subsystem and the XIOR* signal is asserted.

The decoder is enabled by three signals: ACK*, XA9, and XA8. To enable any internal device, ACK* must be "1" and both XA8 and XA9 must be "0."

The decode scheme employed in the IPC is designed to comply with the IBM AT requirements. If you wish to take advantage of the areas that are unused by inserting additional peripherals in the I/O map, you can do so. The IPC does not respond to the unused address spaces established by the top-level decoder. The extra peripherals can be tied directly to the XD0-XD7 data lines because the IPC output buffers are not enabled unless an internal subsystem is enabled.

Clock and Wait State Control

The clock and wait state control subsystem performs three functions: control of the DMA command length, control of the CPU read or write cycle length, and selection of the DMA clock rate. All these functions are user-selectable by writing to the Configuration Register located at Address 23H.

Writing and reading this register is accomplished by first writing a 01H to Location 22H to select the IPC Configuration Register and then performing either a read or write to Location 23H. The following is a layout of Configuration Register 23H Index 01H. Explanation of the individual bits follows.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0 – When the higher-speed CPUs are accessing the IPC, the cycle can be extended by programming up to four wait states into the Configuration Register. This causes the IPC to assert a not ready condition (LOW) on the signal IOCHRDY whenever a valid decode from the top-level decoder is detected and either signal XIOR* or signal XIOW* is asserted. IOCHRDY will remain low for the number of wait states programmed into Bits 6 and 7 of the Configuration Register.

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 23. Configuration Register Bits 7 and 6

Wait states are in increments of one SCLK cycle and are not affected by the DMA clock divider.

16W1-16W0 – Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles, using Bits 4 and 5. This allows you to tailor the DMA cycle more closely to the application.

16W1	16W0	16-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 24. Configuration Register Bits 5 and 4

8W1-8W0 – Wait states can be inserted in 8-bit DMA cycles by programming Bits 2 and 3 in the Configuration Register.

8W1	8W0	8-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 25. Configuration Register Bits 3 and 2

Further control of the cycle length is available through the use of the IOCHRDY pin on the IPC. During DMA, this pin is used as an input to the wait state generation logic to extend the cycle if necessary. To extend the cycle, the peripheral drives the input low (0). The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

EMR – The EMR bit, Bit 1, enables the extended DMA read function. Normally the assertion of DMAMEMR* is delayed one clock cycle later than XIOR*, (I/O bus read), in the IBM AT implementation. This might not be desirable in some systems. Proramming a "1" into Bit 1 starts DMAMEMR* at the same time as XIOR*.

CLK – The CLK bit, Bit 0, allows you to insert a divider between the DMA controller subsystems and the SCLK input pin or to connect the two directly. When Bit 0 contains a "0," the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in Bit 0 bypasses the divider and causes the IPC to use the SCLK input directly. Whenever the state of Bit 0 is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

Configuration Register Defaults

The Configuration Register contents are pre-loaded by reset to an initial value of 0C0H. This value establishes a default that is IBM AT-compatible. The BIOS then programs a value of 040H upon initialization and corresponds to:

Read/Write Cycles	2 wait states
16-Bit DMA Transfers	1 wait state
8-Bit DMA Transfers	1 wait state

DMAMEMR* is delayed one clock cycle later than XIOR*. DMA clock is equal to SCLK/2.

Description of DMA Controller Functions

As previously stated, the equivalent of two 8237A DMA controllers is implemented in the IPC. Each controller is a four-channel DMA device that generates the memory addresses and control signal necessary to transfer information between a peripheral device and memory directly. This allows high-speed information transfer with little CPU intervention.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection of the two DMA devices, thereby maintaining IBM AT compatibility.

DMA cycle length control is provided internally in the IPC, allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers, which can extend command signals or insert wait states.

Each DMA channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA subsystem to transfer blocks of as many as 65536 words. The register associated with each counter allows the channel to reinitialize without re-programming.

From this point on, the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise specified.

DMA Operation

During normal operation of the IPC, the DMA subsystem will be in one of three conditions:

- Idle
- Program
- Active

In the *idle* condition, the DMA controller will be executing cycles of only one state. The idle state S1 is the default condition, and the DMA controller remains in this condition unless the device is initialized and one of the DMA requests becomes active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active, the device enters the **active** condition and issues a hold request to the system. Once in the active condition, the IPC generates the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or memory-to-memory transfer.

I/O-to-memory and memory-to-I/O transfers take place in one cycle. Memory-to-memory transfers require two cycles.

During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device so the transfer is completed in one cycle. Memory-to-memory transfers, on the other hand, require the DMA subsystem to store data from the read operation in an internal register. The contents of this register are then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In a memory-to-I/O transfer, the IPC asserts both DMAMEMR* (DMA memory read) and XIOW* (I/O bus write), allowing data to be transferred directly to the requesting device from memory. Note that the IPC does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data can be varied by programming the DMA subsystem or, optionally extended by the peripheral device. During an active cycle, the DMA subsystem will sequence through a series of states. Each state is one DMA clock cycle long, and the number of states in a cycle varies depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0-S4. (See "Active Condition," later in this section, for further explanation of these states.)

Idle Condition

When no device is requesting service, the DMA subsystem is in an idle condition. During this time, the IPC will sample the DREQ input pins every clock cycle. The internal select from the top-level decoder and HLDA are also sampled at the same time to determine whether the CPU is attempting to access the internal registers. When either of the above situations occurs, the DMA subsystem exits the idle condition. Note that the program condition has priority over the active condition because a CPU cycle has already started.

Program Condition

The program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top-level decoder described previously. During this time, Address Lines XA0-XA3 become inputs if DMA1 is selected. If DMA2 is selected, XA1-XA4 become inputs. Note that when DMA2 is selected XA0 is ignored. The XA0-XA4 inputs are used to select the DMA controller registers that are to be read or written. The DMA controller register assignments are shown in Tables 26 and 27.

Because of the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the Count and Address Registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the Word Count or Address Registers in the DMA subsystem. This internal flip-flop is cleared by a reset or a Master Clear command and can be set or cleared by the CPU issuing the appropriate command.

DMA Controller #1				
Add.	**XIOR***	**XIOW***	**Flip Flop**	**Operation**
000h	0	1	0	Read CH0 Current Address low byte
000h	0	1	1	Read CH0 Current Address high byte
000h	1	0	0	Write CH0 Base & Current Address low byte
000h	1	0	1	Write CH0 Base & Current Address high byte
001h	0	1	0	Read CH0 Current Word Count low byte
001h	0	1	1	Read CH0 Current Word Count high byte
001h	1	0	0	Write CH0 Base & Current Word Count low byte
001h	1	0	1	Write CH0 Base & Current Word Count high byte
002h	0	1	0	Read CH1 Current Address low byte
002h	0	1	1	Read CH1 Current Address high byte
002h	1	0	0	Write CH1 Base & Current Address low byte
002h	1	0	1	Write CH1 Base & Current Address high byte
003h	0	1	0	Read CH1 Current Word Count low byte
003h	0	1	1	Read CH1 Current Word Count high byte
003h	1	0	0	Write CH1 Base & Current Word Count low byte
003h	1	0	1	Write CH1 Base & Current Word Count high byte
004h	0	1	0	Read CH2 Current Address low byte
004h	0	1	1	Read CH2 Current Address high byte
004h	1	0	0	Write CH2 Base & Current Address low byte
004h	1	0	1	Write CH2 Base & Current Address high byte
005h	0	1	0	Read CH2 Current Word Count low byte
005h	0	1	1	Read CH2 Current Word Count high byte
005h	1	0	0	Write CH2 Base & Current Word count low byte
005h	1	0	1	Write CH2 Base & Current Word count high byte
006h	0	1	0	Read CH3 Current Address low byte
006h	0	1	1	Read CH3 Current Address high byte
006h	1	0	0	Write CH3 Base & Current Address low byte
006h	1	0	1	Write CH3 Base & Current Address high byte

DMA Controller #1 Continued				
Add.	**XIOR***	**XIOW***	**Flip Flop**	**Operation**
007h	0	1	0	Read CH3 Current Word Count low byte
007h	0	1	1	Read CH3 Current Word Count high byte
007h	1	0	0	Write CH3 Base & Current Word Count low byte
007h	1	0	1	Write CH3 Base & Current Word Count high byte
008h	0	1	X	Read Status Register
008h	1	0	X	Write Command Register
009h	0	1	X	Read DMA Request Register
009h	1	0	X	Write DMA Request Register
00Ah	0	1	X	Read Command Register
00Ah	1	0	X	Write single-bit DMA Request Mask Register
00Bh	0	1	X	Read Mode Register
00Bh	1	0	X	Write Mode Register
00Ch	0	1	X	Set byte pointer flip-flop
00Ch	1	0	X	Clear byte pointer flip-flop
00Dh	0	1	X	Read Temporary Register
00Dh	1	0	X	Master clear
00Eh	0	1	X	Clear Mode Register counter
00Eh	1	0	X	Clear all DMA Request Mask Register bits
00Fh	0	1	X	Read all DMA Request Mask Register bits
00Fh	1	0	X	Write all DMA Request Mask Register bits

Table 26. DMA Controller #1 Register Assignments

DMA Controller #2				
Add.	**XIOR***	**XIOW***	**Flip-Flop**	**Oeration**
0C0h	0	1	0	Read CH4 Current Address low byte
0C0h	0	1	1	Read CH4 Current Address high byte
0C0h	1	0	0	Write CH4 Base & Current Address low byte
0C0h	1	0	1	Write CH4 Base & Current Address high byte
0C2h	0	1	0	Read CH4 Current Word Count low byte
0C2h	0	1	1	Read CH4 Current Word Count high byte
0C2h	1	0	0	Write CH4 Base & Current Word Count low byte
0C2h	1	0	1	Write CH4 Base & Current Word Count high byte
0C4h	0	1	0	Read CH5 Current Address low byte
0C4h	0	1	1	Read CH5 Current Address high byte
0C4h	1	0	0	Write CH5 Base & Current Address low byte
0C4h	1	0	1	Write CH5 Base & Current Address high byte
0C6h	0	1	0	Read CH5 Current Word Count low byte
0C6h	0	1	1	Read CH5 Current Word Count high byte
0C6h	1	0	0	Write CH5 Base & Current Word Count byte
0C6h	1	0	1	Write CH5 Base & Current Word Count byte
0C8h	0	1	0	Read CH6 Current Address low byte
0C8h	0	1	1	Read CH6 Current Address high byte
0C8h	1	0	0	Write CH6 Base & Current Address low byte
0C8h	1	0	1	Write CH6 Base & Current Address high byte
0CAh	0	1	0	Read CH6 Current Word Count low byte
0CAh	0	1	1	Read CH6 Current Word Count high byte
0CAh	1	0	0	Write CH6 Base & Current Word Count low byte
0CAh	1	0	1	Write CH6 Base & Current Word Count high byte
0CCh	0	1	0	Read CH7 Current Address low byte
0CCh	0	1	1	Read CH7 Current Address high byte
0CCh	1	0	0	Write CH7 Base & Current Address low byte
0CCh	1	0	1	Write CH7 Base & Current Address high byte

DMA Controller #2				
Add.	**XIOR***	**XIOW***	**Flip-Flop**	**Oeration**
0CEh	0	1	0	Read CH7 Current Word Count low byte
0CEh	0	1	1	Read CH7 Current Word Count high byte
0CEh	1	0	0	Write CH7 Base & Current Word Count low byte
0CEh	1	0	1	Write CH7 Base & Current Word Count high byte
0D0h	0	1	X	Read Status Register
0D0h	1	0	X	Write Command Register
0D2h	0	1	X	Read DMA Request Register
0D2h	1	0	X	Write DMA Request Register
0D4h	0	1	X	Read Command Register
0D4h	1	0	X	Write single-bit DMA Request Mask Register
0D6h	0	1	X	Read Mode Register
0D6h	1	0	X	Write Mode Register
0D8h	0	1	X	Set byte pointer flip-flop
0D8h	1	0	X	Clear byte pointer flip-flop
0DAh	0	1	X	Read Temporary Register
0DAh	0	1	X	Master clear
0DCh	0	1	X	Clear Mode Register counter
0DCh	1	0	X	Clear all DMA Request Mask Register bits
0DEh	0	1	X	Read all DMA Request Mask Register bits
0DEh	1	0	X	Write all DMA Request Mask Register bits

Table 27. DMA Controller #2 Register Assignments

In the program condition, the DMA subsystem supports several special commands for controlling the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select, and XIOW* or XIOR* signals. The special commands are: Master Clear, Clear Mask Register, Clear Mode Register Counter, and Set and Clear Byte Pointer Flip-Flop.

The IPC will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and the HLDA signal are mutually exclusive. Erratic operation of the IPC can occur if a request for service occurs on an unmasked channel that is being programmed. To prevent the IPC from attempting to service a device with a channel that is partially programmed, the channel should be masked or the DMA subsystem disabled.

Active Condition

The IPC DMA subsystem enters the active condition whenever a software request occurs or whenever a DMA request on an unmasked channel occurs. In either case the device must not be in the program condition. The IPC then begins a DMA transfer cycle.

In a read cycle, for example, after receiving a DREQ signal, the IPC issues an HRQ signal to the system. Until an HLDA signal is returned, the DMA subsystem remains in an idle condition. On the next clock cycle, the DMA subsystem exits the idle condition and enters state S0.

During S0, the device resolves priority and issues the DACK signal on the highest-priority channel requesting service. The DMA subsystem then proceeds to state S1 where the multiplexed addresses are output and latched.

State S2 is then entered, at which time the IPC asserts DMAMEMR*. The device then moves into S3, where the XIOW* command signal is asserted. The DMA subsystem remains in S3 until the wait state counter decrements to zero and the IOCHRDY signal is true. Note that at least one additional S3 occurs unless compressed timing is selected.

Once a ready condition is detected, the DMA subsystem enters S4, where both commands are de-asserted. In Burst Mode and Demand Mode, discussed later, subsequent cycles begin in S2 unless the intermediate addresses require updating. In these subsequent cycles, the lower addresses are changed in S2.

The DMA subsystem can be programmed on a channel-by-channel basis to operate in one of four modes:

- Single Transfer Mode
- Block Transfer Mode
- Demand Transfer Mode
- Cascade Mode

Single Transfer Mode

Single Transfer Mode directs the DMA subsystem to execute only one transfer cycle at a time. The DREQ signal must be held active until the DACK signal becomes active. If the DREQ signal is held active throughout the cycle, the IPC de-asserts the HRQ signal and releases the bus once the transfer is complete. After the HLDA signal becomes inactive, the IPC again asserts the HRQ signal and executes another cycle on the same channel unless a request from a higher-priority channel has been received. In the Single Transfer Mode, the CPU is assured of being allowed to execute at least one bus cycle between transfers.

Following each transfer, the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000h to FFFFh, the terminal count bit in the Status Register is set and a T/C (Terminal Count) signal is generated. If the autoinitialization option has been enabled, the channel reinitializes itself. If not, the DMA subsystem sets the DMA request bit mask and suspends transferring on the channel.

Block Transfer Mode

When Block Transfer Mode is selected, the IPC begins transfers in response to either a DREQ signal or a software request and continues until the terminal count (FFFFh) is reached. At that time, the T/C signal is pulsed and the Status Register terminal count bit is set. In Block Transfer Mode, the DREQ signal need only be held active until the DACK signal is asserted. Autoinitialization is optional in this mode also.

Demand Transfer Mode

In Demand Transfer Mode, the DMA subsystem begins transfers in response to the assertion of the DREQ signal and continues until either the terminal count is reached or the DREQ signal becomes inactive.

Demand Transfer Mode is normally used for peripherals that have limited buffering ability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. Then, the peripheral can re-establish service by again asserting the DREQ signal. During idle periods between transfers, the CPU is released to operate and can monitor the operation by reading intermediate values from the Base Address, Current Address, Base Word Count, and Current Word Count Registers. Once the DREQ signal is de-asserted, higher-priority channels are allowed to intervene. Reaching terminal count will result in the generation of a T/C signal pulse, the setting of a terminal count bit in the Status Register, and autoinitialization (if enabled).

Cascade Mode

Cascade Mode is used to interconnect multiple DMA controllers, thus extending the number of DMA channels while preserving the priority chain.

In Cascade Mode, the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master receives an HLDA signal from the CPU in response to a DREQ signal caused by the HRQ signal from a slave DMA controller, the master DMA controller ignores all inputs except the HLDA signal from the CPU and the DREQ signal on the active channel. This prevents conflicts between the DMA devices.

Channel 0 of DMA2 is internally connected to DMA1 for Cascade Mode. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascading is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device that is actually generating the HRQ signal to the system. (This is normally the first-level device.) Then, proceed to the second-level devices. Reset causes the DACK signal outputs to become active low and places them in the inactive state.

To allow the internal cascade between DMA1 and DMA2 to function correctly, do not modify the active low state of the DACK signal. The IPC has an inverter between the DACK0 signal of DMA2 and the HLDA signal of DMA1, and the first-level device's DMA request mask bits will prevent second-level cascaded devices from generating unwanted hold requests during the initialization process.

DMA Transfers

Four types of transfers are provided in the IPC DMA subsystem:

- **Read Transfers** – move data from memory to an I/O device by generating the memory address and asserting the DMAMEMR* and XIOW* signals during the same cycle.
- **Write Transfers** – move data from an I/O device to memory by generating the memory address and asserting DMAMEMW* and XIOR* signals.
- **Memory to Memory Transfers** – move block of memory from one location to another. DMA Channels 0 and 1 may be used as memory to memory channels by setting Bit 0 in the Command register. Once programmed the process can be started by either a software or external request to Channel 0 of the DMA controller. Channel 0 provides the source block address during the read portion of the cycle and Channel 1 provides the address for the write portion of the cycle. During the read cycle, a byte of data is latched into the internal temporary register of the IPC. The contents are then output to the XD0 - XD7 data lines during the write portion of the cycle and written to memory. Channel 0 may also be programmed to maintain the same source address on every cycle by setting Bit 1 in the Command register.

- **Verify Transfers** – useful for diagnostics. In these pseudo-transfers, the DMA subsystem will operate as if it is performing a read or write transfer by generating the HRQ signal, addresses, and the DACK signal but will do so without asserting a command signal. Because no transfer actually takes place, the IOCHRDY signal is ignored during *verify transfer* cycles.

Autoinitialization

Each of the four DMA channel Mode Registers contains a bit that causes the channel to reinitialize after reaching terminal count. During this process, referred to as *autoinitialization*, the Base Address and Base Word Count Registers, which were originally written by the CPU, are relocated into the Current Address and Current Word Count Registers. Both the Base and Current Registers are loaded during a CPU write cycle.

The Base Registers remain unchanged during DMA active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the Request Mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers, the Word Count Registers of both Channels 0 and 1 must be programmed with the same starting value for full autoinitialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 reloads the starting address and word count and continues transferring data from the beginning of the source block. If Channel 1 reaches terminal count first, it reloads the current registers, and Channel 0 remains uninitialized.

DREQ Priority

The IPC supports three schemes for establishing DREQ priority. These are *fixed priority*, *specific rotation*, and *automatic rotation*. The default is fixed priority, which assigns priority based on channel position. In this method, Channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels, in order, with Channel 3 receiving the lowest priority.

When multiple requests occur at the same time, the IPC issues an HRQ signal but does not freeze the priority logic until the HLDA signal is returned. Once the HLDA signal becomes active, the priority logic is frozen and the DACK signal is asserted on the highest requesting channel. Priority is not re-evaluated until the HLDA signal is deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on Data Lines XD0-XD7. These addresses are externally latched by U2 and U3, (74ALS373), and used to drive the system address bus.

Because DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a 1-bit skew occurs in the intermediate address fields. DMA1 will therefore output Addresses A8-A15 on the data bus at this time, whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

Eight-Bit Cycles. During 8-bit DMA cycles, in which DMA1 is active, the IPC outputs the lower 8 bits of address on XA0-XA7. The intermediate 8 bits of address are output on XD0-XD7, and the ADSTB8 signal is asserted for one DMA clock cycle. The falling edge of the ADSTB8 signal is used to latch the intermediate addresses A8-A15. An enable signal, AEN8, is used to control the output drivers of the external latch (U2). A16-A23 are also generated at this time from a DMA Page Register in the IPC. Note that A16 is output on the XA16 pin of the device.

Sixteen-Bit Cycles. During 16-bit cycles, in which DMA2 is active, the IPC must output the lower 8 bits of the addresses on XA1-XA8. The intermediate addresses (A9-A16) are output on XD0-XD7. Control for a separate latch (U3) is provided by signals ADSTB16 and AEN16. The DMA Page Register now generates A17-A23. During 16-bit DMA transfers, XA0 and XA16 remain inactive.

DMA Page Register. The DMA Page Register is a set of sixteen 8-bit registers in the IPC that are used to generate the high order addresses during DMA cycles. Only eight of the registers are actually used. The remaining eight are included to maintain IBM AT compatibility. With the exception of Channel 0 of DMA2 (which is used for internal cascading to DMA1), each DMA channel has a register associated with it. Assignment of each register is shown in the following table, along with the register's read/write addresses.

Address	Register Function
080h	Unused
081h	8-bit DMA Channel 2 (DACK2)
082h	8-bit DMA Channel 3 (DACK3)
083h	8-bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-bit DMA Channel 0 (DACK 0)
088h	Unused
089h	16-bit DMA Channel 2 (DACK6)
08Ah	16-bit DMA Channel 3 (DACK7)
08Bh	16-bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh Cycle

Table 28. DMA Address Extension Register Map

During demand and block transfers, the IPC generates multiple sequential transfers. For most of these transfers, the information in the external address latches remains the same, eliminating the need to be relatched. Because the need to update the latches occurs only when a carry or borrow from the lower 8 bits of the address counter exists, the IPC updates the latch contents only when necessary. Therefore, the IPC executes S1 cycles only when necessary, resulting in an overall through-put improvement.

Compressed Timing

The DMA subsystem in the IPC can be programmed to transfer a word in as few as three DMA clock cycles. The normal DMA cycle consists of three states: S2, S3, and S4. (This assumes Demand or Block Transfer Mode.) Normal transfers require four DMA clock cycles because S3 is executed twice because of the one wait state insertion.

In systems capable of supporting higher through-put, the IPC can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed, and the cycle terminates in S4. If compressed timing is selected, the T/C signal will be output in S2, and S1 cycles will be executed as necessary to update the address latch.

Compressed timing is not allowed for memory-to-memory transfers.

Description of Registers

Current Address Register

Each DMA channel has a 16-bit Current Address Register that holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If autoinitialization is selected, the register is reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrementing by setting the Address Hold bit in the Command Register.

Current Word Count Register

Each DMA channel also has a Current Word Count Register, which determines the number of transfers to perform. The actual number of transfers performed is one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFh. When this roll-over occurs, the IPC generates the T/C signal. Then, it either suspends operation on that channel and sets the appropriate Request Mask bit or it autoinitializes and continues.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write-only register that is loaded by the CPU when writing to the Current Address Register.

The purpose of the Base Address Register is to store the initial value of the Current Address Register for autoinitialization. The contents of the Base Address Register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitiaization bit is set.

Base Word Count Register

The Base Word Count Register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. The Base Word Count Register is loaded into the Current Word Count Register during auto-initialization.

Command Register

The Command Register controls the overall operation of the DMA subsystem. This register can be read or written by the CPU and is cleared by either a reset or a Master Clear command. The format and explanation of this register are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK – Bit 7 determines the DACK signal level. Programming a 1 in this bit position makes the DACK signal an active high signal.

DRQ – Bit 6 determines the DREQ signal active level. Writing a 1 in this bit position causes the DREQ signal to become active low.

EW – Extended write is enabled by writing a 1 to Bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP – Writing a 1 to Bit 4 causes the IPC to use a rotating priority scheme for honoring DMA requests. The default condition (0) is fixed priority.

CT – Writing a 1 to Bit 3 enables compressed timing. The default (0) condition causes the DMA to operate with normal timing.

CD – Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). Disabling is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occurring.

AH – Writing a 1 to Bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M – Writing a 1 in Bit 0 enables Channels 0 and 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address.

Bits 0 and 1 of the Write Mode Register determine which channel's Mode Register is written. The remaining six bits control the mode of the selected channel.

Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, Bits 0 and 1 will both be a logical 1. The definitions of the Mode Register bits are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

M1-M0 – Mode selection for each channel is accomplished by Bits 6 and 7. The following table shows the definitions.

M1	M0	Mode
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

Table 29. Definition of Mode Selection Bits

DEC – Determines the direction of the address counter. A 1 in Bit 5 decrements the address after each transfer.

AI – Writing a 1 in Bit 4 enables the autoinitialization function.

TT1-TT0 – Bits 2 and 3 control the type of transfer which is to be performed. The following table gives the definitions:

TT1	TT0	Type
0	1	Verify transfer
0	1	Write transfer
1	0	Read transfer
1	1	Illegal

Table 30. Mode Register
Bits 2 and 3 (Transfer Type)

CS1-CS0 – Bits 0 and 1 are the Channel Select bits. They determine which channel's Mode Register will be written. Read back of a Mode Register will result in Bits 0 and 1 being 1's. The following table explains the configuration of Bits 0 and 1.

CS1	CS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 31. Mode Register
Bits 0 and 1 (Channel Select)

Request Register

The Request Register is a 4-bit register used to generate software requests. (DMA service can be requested either externally or under software control.)

Request Register bits can be set or reset independently by the CPU. The request mask has no effect on software-generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4-7 are read as 1's. All four request bits are cleared to zero by reset. The following table gives an explanation of the Request Register:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

RB – Writing a 1 to Bit 2 sets the Request bit. Bits 0 and 1 select the bit (channel) to be manipulated.

RS1-RS0 – Bits 0 and 1 determine which channel's Mode Register will be written. Read back of the Mode Register will result in Bits 0 and 1 both being 1's. The following is a table of channel selection:

RS1	RS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 32. Request Register Write Operations

The format for a Request Register read operation is as follows.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RC1	RC0

RC3-RC0 – During a Request Register read, the state of the Request bit associated with each channel is returned in Bits 0-3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The Request Mask Register is a set of four bits that are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

MB – Bit 2 sets or resets the Request Mask bit for the channel selected by Bits 0 and 1 (MS0 and MS1). Writing a 1 to Bit 2 sets the mask, inhibiting external requests.

MS1-MS0 – Bits 0 and 1 select the specific mask bit to be set or reset. The following table explains the bit configurations:

MS1	MS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 33. Request Mask Register Bits 0 and 1 (Mask Bit Selection)

Alternatively, all four mask bits (Bits 0-3) can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

MB3-MB0 – Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a reset or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached if autoinitialize is disabled. The entire register can be cleared, enabling all four channels, by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine whether a channel has reached terminal count and whether an external service request is pending.

Bits 0-3 of this register are cleared by a reset, a Master Clear command, or each time a status read takes place. Bits 4-7 are cleared by a reset, a Master Clear command, or the pending request being de-asserted. Bits 4-7 are not affected by the state of the Mask Register bits. The channel number corresponds to the bit position.

The Status Register is a read-only register. It conforms to the following format:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

Special Commands

Five special commands are provided to make the task of programming the device easier.

These commands are activated as a result of a specific address and assertion of an XIOR* or XIOW* signal. Information on the data lines is ignored by the IPC whenever an XIOW* signal activated command is issued; thus, data returned on XIOR* signal activated commands is invalid.

Clear Byte Pointer Flip-Flop – initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence. This command is normally executed prior to reading or writing an Address or Word Count Register.

Set Byte Pointer Flip-Flop – allows the CPU to adjust the pointer to the high byte of an Address or Word Count Register.

Master Clear - has the same effect as a hardware reset (clears the Command Register, Status Register, Request Register, Temporary Register, Mode Register counter, and byte pointer flip-flop; sets the Request Mask Register). Immediately following a Master Clear or a reset, the DMA will be in the idle condition.

Clear Request Mask Register - enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter - clears the additional counter, which is used to allow access to the four Mode Registers while only using one address. After clearing the counter, you can read all four Mode Registers by doing successive reads to the Read Mode Register address. The registers are read in order from Channel 0 to Channel 3.

Interrupt Controller

Overview

Two interrupt controllers, INTC1 and INTC2, are included in the IPC. Each of the controllers is equivalent to an 8259A device operating in iAPX86 Mode.

The two devices are connected and must be programmed to operate in Cascade Mode for proper operation of all 16 interrupt channels.

INTC1 is located at Addresses 020h-021h and is configured for master operation in Cascade Mode. INTC2 is a slave device and is located at Addresses 0A0h-0A1h.

The interrupt request output signal from INTC2 (INT) is internally connected to the Interrupt Request Input Channel 2 (IR2) of INTC1. The address decoding and cascade interconnection matches that of the IBM AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the counter/timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the real-time clock is connected to Channel 0 (IR0) of INTC2.

Unless otherwise noted, the following descriptions of the interrupt subsystems pertain to both INTC1 and INTC2. Wherever register addresses are used, the address for the INTC1 register is listed first and the address for the INTC2 register follows, in parentheses. Example: 020h (0A0h).

Controller Operation

The Interrupt Request Register (IRR) is used to store requests from all the channels that are requesting service. The IRR bits are labeled using the channel names IR7-IR0.

The In-Service Register (ISR) contains all the channels that are currently being serviced. The ISR bits are labeled IS7-IS0, corresponding to IR7-IR0.

The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels.

The interrupt controller's priority resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register.

During interrupt acknowledge (INTA) cycles, a master controller outputs a code to the slave device. This code is compared in the cascade buffer/comparator with a 3-bit ID code previously written. If a match occurs in the slave controller, the controller generates an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during INTA cycles.

Interrupt Sequence

The IPC allows the CPU to perform an indirect jump to a service routine in response to a interrupt request for service from a peripheral device. The indirect jump is based on a vector provided by the IPC on the second of two CPU-generated INTA cycles. (The first INTA cycle is used for resolving priority, and the second cycle is for transferring the vector to the CPU.)

The following events occur during an interrupt sequence:

1. One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding Interrupt Request Register bit(s).
2. The interrupt controller resolves priority (based on the state of the IRR, IMR, and ISR registers) and asserts the INTR signal (if appropriate).
3. The CPU accepts the interrupt and responds with the INTA cycle.
4. During the first INTA cycle, the highest-priority ISR bit is set and the corresponding IRR bit is reset. The internal cascade address is generated, and the XD7-XD0 outputs remain tri-stated.
5. The CPU executes a second INTA cycle, during which the IPC drives an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is:

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

Table 34. Interrupt Vector Byte

Note that V7-V3 are programmable by writing to Initialization Control Word 2. This will be covered later in the section.

6. At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End of Interrupt Mode is selected. (This mode is covered later in this section.) Otherwise, the ISR must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If there is no interrupt request at the beginning of the first INTA cycle, INTC1 issues an interrupt level 7 during the second INTA cycle.

The following table defines the interrupt request sources:

Controller	Channel No.	Interrupt Request Source
INTC1	IR0	IRQ0 - Counter/Timer Out0
INTC1	IR1	IRQ1 - Keyboard
INTC1	IR2	IRQ2 - INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 - Serial Port 2
INTC1	IR4	IRQ4 - Serial Port 1
INTC1	IR5	IRQ5 - Parallel Port 2
INTC1	IR6	IRQ6 - Diskette Controller
INTC1	IR7	IRQ7 - Parallel Port 1
INTC2	IR0	IRQ8 - Real-Time Clock IRQ
INTC2	IR1	IRQ9 - Software Redirected to IRQ2
INTC2	IR2	IRQ10 - Reserved
INTC2	IR3	IRQ11 - Reserved
INTC2	IR4	IRQ12 - Reserved
INTC2	IR5	IRQ13 - Coprocessor Interrupt
INTC2	IR6	IRQ14 - Hard Disk Controller
INTC2	IR7	IRQ15 - Reserved

Table 35. Interrupt Request Sources

End Of Interrupt

An EOI is defined as a condition that causes an In Service Register bit to be reset. To define the ISR bit to reset, you can either use a CPU command (for a specific EOI) or you can instruct the priority resolver to clear the highest-priority ISR bit (for a non-specific EOI).

In modes that do not alter the fully nested structure, a non-specific EOI is sufficient. The IPC can determine the correct ISR bit to reset because the highest-priority ISR bit is necessarily the last level acknowledged and serviced.

In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine.

An ISR bit that is masked, in Special Mask Mode by an Interrupt Mask Register bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 the lowest, and priority assignment is fixed (Fixed Priority Mode).

Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming the Operational Command Word 2 (OCW2) Register.

Fixed Priority Mode

Fixed Priority Mode is the default condition. It exists unless rotation, either manual or automatic, is enabled or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown below:

Priority:	Lowest							Highest
Interrupt:	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, the following events occur:

1. Priority is resolved.
2. The vector of the highest-priority request is placed on the bus.
3. The In Service Register bit for that channel is set. This ISR bit remains set until an EOI is issued to that channel.

As long as the ISR bit is set, all interrupts of equal or lower priority are inhibited. A higher-priority interrupt that occurs during an interrupt service routine will be acknowledged only if the CPU has internally re-enabled interrupts.

Specific Rotation Mode

Specific rotation allows the system software to re-assign priority levels by issuing a command that redefines the highest-priority channel. The following is an example of specific rotation when a command is issued with Channel 5 selected.

Before Rotation

Priority:	Lowest							Highest
Interrupt:	7	6	5	4	3	2	1	0

After Rotation

Priority:	Lowest							Highest
Interrupt:	5	4	3	2	1	0	7	6

Automatic Rotation Mode

In applications in which a number of equal-priority peripherals are requesting interrupts, you can use automatic rotation to equalize the priority assignment. In Automatic Rotation Mode, a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller are serviced at least once in eight interrupt requests to the CPU from the controller.

Automatic rotation will occur, if enabled, as a result of an EOI (automatic or CPU-generated). The following is an example of automatic rotation in which IR4 is the highest-priority request being serviced.

Before Rotation

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

Priority:	Lowest							Highest
Interrupt:	7	6	5	4	3	2	1	0

After Rotation (IR4 Service Completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

Priority:	Lowest							Highest
Interrupt:	4	3	2	1	0	7	6	5

Programming the Interrupt Controller

Two types of commands are used to control the IPC interrupt controllers: *initialization command words* (ICWs) and *operational command words* (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of four bytes to each interrupt controller. The initialization sequence is started by writing the first initialization command word (ICW1) to Address 020h (0A0h) with a 1 on Bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1. Resets the Initialization Command Word Counter to 0.
2. Latches ICW1 to the device.
3. Selects Fixed Priority Mode.
4. Assigns IR7 the highest priority.
5. Clears the Interrupt Mask Register.
6. Sets the Slave Mode address to 7.
7. Disables Special Mask Mode.
8. Selects the Interrupt Request Register for status read operations.

The next three I/O writes to Address 021h (0A1h) will load ICW2-ICW4. (All four bytes must be written for the controller to be properly initialized.) The initialization sequence can be terminated at any point by writing to Address 020h (0A0h) with a 0 in Data Bit 4. Note that this will allow OCW2 or OCW3 to be written.

Registers ICW1-ICW4 are write-only registers in the following formats:

ICW1 – Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

SI – Bit 4 indicates to the interrupt controller that an initialization sequence is starting. This bit must be a 1 to write ICW1.

LTM – Bit 3 selects level or edge-triggered inputs to the IRR. If a 1 is written to LTM, a high level on the IRR input will generate an interrupt request. To generate the proper interrupt vector, the interrupt request must be active until the first INTA cycle is started. (An IR7 vector is generated if the IRR input is de-asserted early.) The interrupt request must be removed prior to EOI to prevent a second interrupt from occurring.

SM – Bit 1 selects between Single Mode and Cascade Mode. Single Mode is used when only one interrupt controller (INTC1) is used. Therefore, it is not recommended for the interrupt controller.

Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 allows INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest-priority interrupt request pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both controllers to operate.

ICW2 – Address 021h (0A1h)

ms							blsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

V7-V3 – These bits are the upper five bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the priority resolver during INTA. (See Table 34, earlier in the section.) INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1 - Address 021h

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

S7-S0 - These bits determine which interrupt requests have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04h for INTC2 to function.

ICW3 Format for INTC2 - Address 0A1h

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	ID2	ID1	ID0

ID2-ID0 - These bits determine which Slave Mode address the controller will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02h for Cascade Mode operation. Note that Bits 3-7 should be 0.

ICW4 - Address 021h (0A1h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

EMI - Bit 4 will enable multiple interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts when Cascade Mode and Fixed Priority Mode are both selected, without INTC2 being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and to check its In-Service Register for zero when exiting an interrupt service routine. If a zero value exists, a non-specific EOI command should be sent to INTC1. If not, no command is issued.

AEOI - Auto EOI (AEOI) is enabled when ICW4 is written with a 0 in Bit 1. The interrupt controller performs a non-specific EOI on the trailing edge of the second INTA cycle. Do not use AEOI in a device with fully nested interrupts unless the device is a cascade master.

Operational Command Words

Operational command words (OCWs) allow the IPC interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has three operational command words that can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at Address 021h (0A1h). It can be written any time the controller is not in Initialization Mode. OCW2 and OCW3 are located at Address 020h (0A0h). Writing to Address 020h (0A0h) with a 0 in Bit 4 places the controller in Operational Mode and loads OCW2 (if Data Bit 3 = 0) or OCW3 (if Data Bit 3 = 1). The following format descriptions are for OCW1-OCW3. These registers are read/write registers.

OCW1 – Address 021h (0A1h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

M7-M0 – Bits 0-7 control the state of the Interrupt Mask Register. Each interrupt request can be masked by writing a 1 in the appropriate bit position. (M0 controls IR0, M1 controls IR1, M2 controls IR2, and so on.) Setting an IMR bit has no affect on lower-priority requests. All IMR bits are cleared by writing ICW1.

OCW2 – Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

R – Bit 7, in conjunction with Bits 5 (EOI) and 6 (SL), selects operational function. Writing a 1 in Bit 7 selects one of the rotation functions. The following table shows the R selections:

R	SL	EOI	Function
1	0	0	Rotate on Auto EOI enable*
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on Specific EOI

Table 36. R Selections

*This function is disabled by writing a 0 to all three bit positions.

SL – Bit 6, in conjunction with Bits 7 and Bit 5, selects operational function. Writing a 1 in Bit 6 causes a specific or immediate function to occur. All specific commands require Bits 2-0 (L2-L0) to be valid except for no operation. The following table shows the SL selections:

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI Command
1	1	0	Specific Rotate Command
1	1	1	Rotate on Specific EOI

Table 37. SL Selections

EOI – Bit 5, in conjunction with Bits 6 and 7, selects operational function. Writing a 1 in Bit 5 causes a function related to EOI to occur. The following table shows the EOI selections.

R	SL	EOI	Function
0	0	1	Non-specific EOI command
0	1	1	Specific EOI command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on Specific EOI

Table 38. EOI Selections

SI – Writing a 0 in Bit 4 takes the interrupt controller out of Initialization Mode and allows OCW2 and OCW3 to be written.

2/3 – If the I/O write places a 0 in Bit 4 (SI), writing a 0 in Bit 3 (2/3) selects OCW2. Writing a 1 selects OCW3.

L2-L0 – These three bits are internally decoded to select the interrupt channel to be affected by the specific command. L2-L0 must be valid during three of the four specific cycles shown in Table 37. Following is a table that defines the L2-L0 selections:

L2	L1	L0	Interrupt
0	0	0	IR0
0	0	1	IR1
0	1	0	IR2
0	1	1	IR3
1	0	0	IR4
1	0	1	IR5
1	1	0	IR6
1	1	1	IR7

L2-L0 Definitions

OCW3 – Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

ESMM – Writing a 1 in Bit 6 enables the Set/Reset Special Mask Mode function, controlled by Bit 5 (SMM). ESMM allows the other functions on OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM – Writing a 1 to both Bits 5 and 6 enables the Special Mask Mode. Writing a 1 to Bit 6 and a 0 to Bit 5 disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts. Writing a 0 enables interrupts on the associated channel by causing the priority resolver to ignore the condition of the ISR.

SI – Same as for OCW2.

2/3 – Same as for OCW2.

PM – Writing a 1 to Bit 2 of OCW3 enables Polled Mode, causing the IPC to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle has Bit 7 set if an interrupt is pending. If Bit 7 of the byte is set, the level of the highest pending request is encoded on Bits 2-0. The Interrupt Request Register remains frozen until the read cycle is completed, at which time the PM bit is reset.

RR – When Bit 1 is 1, reading the status port at Address 020h (0A0h) causes the contents of the Interrupt Request Register or In Service Register (determined by Bit 0) to be placed on XD0-XD7. Asserting Bit 2 (PM) forces RR reset.

RIS – Bit 0 selects between the IRR and the ISR registers during status read operations if Bit 1 (RR) is 1.

Counter/Timer

The counter/timer circuit (CTC) in the IPC contains three 16-bit counters (Counters 0-3) that can be programmed to count in binary or binary coded decimal (BCD.) Each counter operates independently of the others and can be programmed as a timer or a counter.

All three counters are driven from a common set of control logic. The control logic decodes control information written to the CTC and provides the control necessary to load, read, configure, and control each counter.

Counter 2 can be operated in any of the following six modes:

Mode 0 - Interrupt on Terminal Count
Mode 1 - Hardware-Retriggerable One-Shot
Mode 2 - Rate Generator
Mode 3 - Square Wave Generator
Mode 4 - Software-Triggered Strobe
Mode 5 - Hardware-Retriggerable Strobe

Counters 0 and 1 can be programmed for all six modes. However, the usefulness of Modes 1 and 5 is limited because of the lack of an external hardware trigger signal.

All three counters are driven from a common clock input pin (TMRCLK) that is independent from other clock inputs to the IPC. Counter 0's output (Out0) is connected to IR0 of INTC1 and can be used as an interrupt to the system for keeping time and task switching. Counter 1 can be programmed to generate pulses or square waves for use by external devices. Counter 2 is a full-function counter/timer. It can be used as an interval timer, a counter, or a gated rate/pulse generator.

Counter Description

Each counter contains the following:

- A Control Register.
- A Status Register.
- A 16-bit counting element (CE).
- A pair of 8-bit counter input latches (CIL,CIH).
- A pair of 8-bit counter output latches (COL,COH).
- A clock input for loading and decrementing the CE.
- A mode-defined GATE input for controlling the counter. (Only Gate 2 is accessible.)
- An OUT signal. (OUT0 is not externally accessible.)

The OUT signal's state and function is controlled by the Counter Mode and the condition of the CE. (See "Mode Definitions," at the end of this section.)

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The Control Register stores the mode and command information used to control the counter. This register can be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043h). The remaining bits in the byte contain the mode, the type of command, and the count format information.

The Status Register allows the software to monitor counter condition and read back the contents of the Control Register.

The CE is a loadable 16-bit synchronous down counter. It is loaded or decremented on the falling edge of the TMRCLK signal. It contains the maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3, the CE will be reloaded when it reaches 0. In all other modes, it will wrap around to FFFF in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the counter input latches, the latches are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the counter output latches. COL and COH are transparent latches that can be read while transparent or latched. (See "Latch Counter Command," later in this section.)

Programming the CTC

After power-up, the condition of the CTC Control Registers, the Counter Registers, the CE, and the output of all counters is undefined. Each counter must be programmed before it can be used. This is either done by the BIOS or by the software application.

Counters are programmed by writing a control word and then an initial count. The Control Register of a counter is written by writing to the Control Word address. The Control Register is a write-only location. The following table shows the addresses and format of the control words and the Control Word Register.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

Address	Function
040h	Counter 0 Read/Write
041h	Counter 1 Read/Write
042h	Counter 2 Read/Write
043h	Control Register Write Only

Table 39. Control Word Addresses

Control Word (043h)

F3-F0 – Bits 7-4 determine the command to be performed. The following table lists the available commands.

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (See "Counter LatchCommand")
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (See "Counter LatchCommand")
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (See "Counter LatchCommand")
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read Back Command (See "Read BackCommand")

Table 40. Counter Commands

M2-M0 – Bits 3-1 determine the counter's mode during a Read/Write Counter command or select the counter during a Read Back command. (See the specific commands, later in this section.) Bits 3-1 become "don't care" during Latch Counter commands.

BCD – Bit 0 selects the binary coded decimal counting format during Read/Write Counter commands. During a Read Back command, this bit must be a 0.

Read/Write Counter Command

When writing to a counter, observe the following conventions:

- Write each counter's control word before writing the initial count.
- When writing the initial count, follow the format specified in the control word (for example, least significant byte only or least significant byte, then most significant byte).

Providing the programming format is observed, a new initial count can be written into the counter at any time after programming without rewriting the control word.

During Read/Write Counter commands, M2-M0 are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Selct Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Table 41. Mode Select

Latch Counter Command

When a Latch Counter command is issued, the counter's output latches (COL,COH) latch the current state of the CE. COL and COH remain latched until read by the CPU or until the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE can be read directly.

It is possible to issue Latch Counter commands to multiple counters before reading the first counter to which a command was issued. However, multiple Latch Counter commands issued to the **same** counter without reading the counter will cause all but the first command to be ignored.

Read Back Command

The Read Back command allows you to check the count value, mode, and state of the OUT signal, and the Null Count Flag of the selected counter(s). The format for the Read Back command is as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	LC	LS	C2	C1	C0	0

LC – Writing a 0 in Bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS – Writing a 0 in Bit 4 causes the selected counter(s) to latch the current condition of its Control Register, null count, and output into the Status Register. The next read of the counter causes the contents of the Status Register to be read. (See "Status Read," later in the section.)

C2-C0 – Writing a 1 in Bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for Bits 2 and 1, except that they enable Counters 1 and 0, respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS=LC=0, status is returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter cause the count to be returned.

Status Byte

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT – Bit 7 contains the state of the counter's OUT signal.

NC – Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0 whenever the counter is loaded from the Counter Input Registers.

F1-F0 – Bits 5 and 4 contain the F1 and F0 command bits that were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte, or both must be transferred during counter read/write operations.

M2-M1 – Bits 2 amd 1 reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD - Bit 0 indicates that the CE is operating in BCD format.

Counter Operation

Because of the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be used as the example in describing counter operation. However, the descriptions of Modes 0, 2, 3 and 4 are relevant to all three counters.

The following terms are defined for describing CTC operation:

- TMRCLK Pulse – A rising edge followed by a falling edge of the IPC TMRCLK input.
- Trigger – The rising edge of the GATE2 input signal.
- Counter Load – The transfer of the 16-bit value in CIL and CIH to the CE.
- Initialized – A control word is written and the counter input latches are loaded.

Counter 2 operates in one of the modes that are described in the following sections.

Mode 0: Interrupt on Terminal Count

Writing the control word causes the OUT2 signal to go low and to remain low until the CE reaches 0. At that time, the signal goes back high and remains high until a new count or control word is written. Counting is enabled when the GATE2 signal is at a logical "1". Disabling the count has no effect on the OUT2 signal.

The CE is loaded with the first TMRCLK pulse after the control word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written. This TMRCLK pulse does not decrement the count. Therefore, for an initial count of *n*, the OUT2 signal does not go high until *n* + 1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and causes counting to continue from the new count.

If an initial count is written with the GATE2 signal equal to 0, the CE is still loaded on the next TMRCLK pulse. In this case, however, counting does not begin until the GATE2 signal equals 1. The OUT2 signal, therefore, goes high *n* TMRCLK pulses after the GATE2 signal equals 1.

Mode 1: Hardware-Retriggerable One-Shot

Writing the control word causes the OUT2 signal to go high initially. Once initialized, the counter is armed and a trigger causes the OUT2 signal to go low on the next TMRCLK pulse. The OUT2 signal then remains low until the counter reaches 0. An initial count of *n* results in a one-shot pulse that is *n* TMRCLK cycles long.

Any subsequent triggers that occur while the OUT2 signal is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH does not affect the current one-shot unless the counter is retriggered.

Mode 2: Rate Generator

Mode 2 functions as a divide-by-*n* counter, with OUT2 as the carry. Writing the control word during initialization sets the OUT2 signal high.

When the initial count decrements to 1, the OUT2 signal goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high and reloads the CE. Then, the process is repeated. In Mode 2, the counter continues counting (if the GATE2 signal equals 1) and generates an OUT2 pulse every *n* TMRCLK cycles. A count of 1 is illegal in Mode 2.

When the GATE2 signal goes to 0, it disables counting and forces OUT2 high immediately. A trigger reloads the CE on the next TMRCLK pulse. Thus, GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect counter operation unless a trigger is received. Otherwise, the new count is loaded at the end of the current counting cycle.

Mode 3: Square Wave Generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an event count, the duty cycle of OUT2 will be 50%. For odd count values, OUT2 is high one TMRCLK cycle longer than it is low.

Mode 4: Software-Triggered Strobe

Writing the control word causes the OUT2 signal to go high initially. Expiration of the initial count causes the OUT2 signal to go low for one TMRCLK cycle. GATE2=0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. It begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, $n + 1$ cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be retriggered by software.

Mode 5: Hardware-Triggered Strobe

Writing the control word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2=0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Because loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, $n + 1$ TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter retriggerable.

GATE2 Definition

In Modes 0, 2, 3, and 4, GATE2 is level-sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3, and 5, the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop, the output of which is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge- and level-sensitive.

The following table describes each channel's control and output. (Note: Channel 1 is programmed as a rate generator to produce a 15-micro-secord period signal used for refresh request.)

Channel	Signal Name	Description
0		System Timer
0	Gate 0	Tied active
0	Clk In 0	1.190 MHz Oscillator
0	Clk Out 0	IRQ0
1		Refresh Request Generator
1	Gate 1	Tied active
1	Clk In 1	1.190 MHz Oscillator
1	Clk Out 1	REFREQ
2		Speaker Tone Generation
2	Gate 2	Controlled by Bit 0 of Port 061H
2	Clk In 2	1.190 MHz Oscillator
2	Clk Out 2	Used to drive speaker

Table 42. Channel Control and Output

Real-Time Clock

This section of the IPC combines a complete time-of-day clock with alarm, 100-year calendar, programmable period interrupt, and 114 bytes of low power static RAM. This section of the device can operate in a battery-powered mode to protect the contents stored in the SRAM and keep the clock functioning.

Register Access

Reading and writing to the 128 locations in the real-time clock is accomplished by first writing the index address out to 070H and then writing the desired data out to 071H. The index addresses for the real-time clock locations are:

Index	Function
00H	Seconds
01H	Seconds alarm
02H	Minutes
03H	Minutes alarm
04H	Hours
05H	Hours alarm
06H	Day of week
07H	Date of month
08H	Month
09H	Year
0AH	Register A
0BH	Register B
0CH	Register C
0DH	Register D
0EH	Diagnostic status byte
0FH	Shutdown status byte
10H	Diskette drive type byte (Drives A and B)
11H	Reserved
12H	Hard disk type byte (Drives C and D) types 1-14
13H	Reserved
14H	Equipment byte
15H	Low base memory byte
16H	High base memory byte
17H	Low expansion memory byte
18H	High expansion memory byte
19H	Disk C extended byte
1AH	Disk D extended byte
1BH-2BH	Reserved
2CH	Bit 0 = swap disk bit
2DH	Reserved
2EH-2FH	2-byte CMOS checksum
30H	Low expansin memory byte
31H	High expansion memory byte
32H	Date century byte
33H	Information flags (set during power on)
34H-7FH	Reserved

Table 43. Index Addresses for the Real-Time Clock Locations

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real-time clock. Initialization of the time, calendar, and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal format.

Before initialization of the internal registers can be performed, the SET bit in Register B should be set to a 1 to prevent real-time clock updates from occurring. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the real-time clock will perform clock/calendar updates at a 1Hz rate.

The 24/12 in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization, the 24/12 bit cannot be changed without reinitializing the hour locations. In 12-hour format, the high order bit of the hour's byte in both the time and alarm bytes will indicate p.m. when it is a "1."

During updates, which occur once per second, the 10 bytes of time, calendar, and alarm information are unavailable to be read or written by the CPU for 2ms. Information read while the real-time clock is performing an update will be undefined. The "Update Cycle" section shows how to avoid update cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, you need only program the time that the interrupt is to occur into the three alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1," which turns that byte into a "don't care" byte. For instance, an interrupt can be generated every hour by programming C0h into Register 5, or it can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from Index Addresses 0Eh-7Fh are not affected by the real-time clock. These bytes are accessible during the update cycle and can be used for anything. In the DECstation 320, these locations are used for nonvolatile configuration storage and calibration parameters because this device is normally battery-powered when the system is turned off.

Control and Status Registers

The IPC contains four registers (A-D) used to control the operation and monitor the status of the real-time clock. These registers are located at Index Addresses 0Ah-0Dh and are accessible by the CPU at all times.

Register A (0Ah)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Except for UIP, Register A is a read/write register.

UIP – Bit 7 is the Update In Progress flag. It is a status bit used to indicate that an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP goes active (high) 244 μs prior to the start of an update cycle and remains active for an additional 2 ms while the update is taking place. The UIP bit is read-only and is not affected by reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV0-DV2 - Bits 4-6 are used to control the divider/prescaler on the real-time clock. While the IPC can operate at frequencies higher than 32.768 KHz, this is not recommended for battery-powered operation because of the increased power consumption at these higher frequencies. The following table gives the settings for DV0-DV2:

DV2	DV1	DV0	OSC1 Frequency	Mode
0	1	0	32.768 KHz	Operate
1	1	X	Reset Divider	

Table 44. Bits 6, 5, and 4 of Register A

RS0-RS3 - Bits 0-3 control the periodic interrupt rate. The periodic interrupt is derived from the divider/prescaler in the real-time clock and is separate from the alarm interrupt. Both the alarm and the periodic interrupts, however, do use the same interrupt channel in the interrupt controller. Use of the periodic interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the real-time clock can be programmed:

Rate Selection				Time Base
RS3	RS2	RS1	RS0	32.768 KHz
0	0	0	0	None
0	0	0	1	3.90526 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 μs
0	1	0	0	244.141 μs
0	1	0	1	488.281 μs
0	1	1	0	976.562 μs
0	1	1	1	1.935125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

Table 45. Interrupt Rates for Real-Time Clock

Register B (0Bh)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	DM	24/12	DSE

Register B is a read/write register.

SET – Writing a "0" to Bit 7 enables the update cycle and allows the real-time clock to function normally. When Bit 7 is set to a "1," the update cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET* input signal.

PIE – Bit 6 is the Periodic Interrupt Enable bit. It controls the generation of interrupts based on the value programmed into the RS0-RS3 bits (Bits 0-3) of Register A. This allows you to disable this function without affecting the programmed rate. Writing a "1" to Bit 6 enables the generation of periodic interrupts. Bit 6 is cleared to "0" by RESET*.

AIE – The generation of alarm interrupts is enabled by setting Bit 5 to a "1". Once this bit is enabled, the real-time clock generates an alarm whenever a match occurs between the programmed alarm and clock information. Programming the "don't care" condition into one or more of the Alarm Registers enables the generation of periodic interrupts at rates of 1 second or greater. Bit 5 is cleared by the RESET* signal.

UIE – This read/write bit is used to update the update-end flag bit in Register C. This causes the proper IRQ to be asserted. The RESET* pin going low or the SET bit going high resets the UIE bit.

DM – This bit determines whether the time and calendar updates are to use binary or BCD format. This bit is written or read by the processor program, but not modified by any internal functions or RESET*. A 1 signifies binary data while a 0 specifies BCD data.

24/12 – The 24/12 control bit, Bit 1, is used to establish the format of both hours and hours alarm bytes. If this bit is a "1," the real-time clock interprets and updates the information in these two bytes using the 24-hour mode. This bit can be read or written by the CPU. It is not affected by RESET*.

DSE – The real-time clock can be instructed to handle daylight-saving time changes by setting Bit 0 to a "1." This enables two exceptions to the normal timekeeping sequence to occur. Setting Bit 1 to a "0" disables the execution of these two exceptions. PSRSTB* has no affect on Bit 1.

Register C (0Ch)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

Register C is a read-only register.

IRQF – Bit 7, the Interrupt Request Flag bit, is set to a "1" when any condition that can cause an interrupt is true and the interrupt enable for that condition is true. The condition that causes this bit to be set also generates an interrupt. The logic expression for this flag is as follows:

IRQF = PF & PIE or
AF & AIE or
UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB* signal. Writing to this register has no affect on the contents.

PF – Bit 6, the Periodic Interrupt flag, is set to a "1" when a transition, which is selected by RS0 - RS3 (Bits 0-3 of Register A), occurs in the divider chain. Bit 6 will become active, independent of the condition of the PIE control bit. The PF bit then generates an interrupt and sets IRQF if PIE is a "1".

AF – A "1" appears in Bit 5, the AF bit, whenever a match has occurred between the Time Registers and the Alarm Registers during an update cycle. This flag is also independent of its enable (AIE) and generates an interrupt if AIE is true.

UF – See "Update Cycle," later in this section.

Register D (0Dh)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Register D is a read-only register.

VRT – Bit 7, the Valid RAM and Time bit, indicates the condition of the contents of the real-time clock. This bit is cleared to a "0" whenever the PS input signal is low. This pin is normally derived from the power supply that supplies power (Vcc) to the device. It allows you to determine whether the registers have been initialized since power was applied to the device. PSRSTB* has no affect on this bit. This signal can only be set by reading Register D. All unused register bits are "0" when read. They are not writable.

Update Cycle

During normal operation, the real-time clock will perform an update cycle once every second. The performance of an update cycle depends on the divider bits DV0-DV2 not being cleared and the SET bit in Register B being cleared. The function of the update cycle is to increment the Clock/Calendar Registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt is issued if the alarm and interrupt control bits are enabled.

During an update, the lower ten registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the real-time clock and the CPU, a flag is provided in Register A to alert you of a pending update cycle.

This Update In Process (UIP) bit, Bit 7, is asserted 244 μs before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete, the UIP bit is cleared and the Update Flag (UF) bit in Register C is set. CPU access is always allowed to Registers A through D during update cycles.

Two methods of reading and writing to the real-time clock are recommended. Both enable you to avoid contention between the CPU and the real-time clock for access to the time and date information:

- The first method is to read Register A, determine the state of the UIP bit and--if it is "0"--perform the read or write operation. For this method to work successfully, the entire read or write operation including any interrupt service routines that might occur must not require more than 244 μs to complete (from the beginning of the read of Register A to the completion of the last read or write to the Clock/Calendar Registers).
- The second method of accessing the lower ten registers is to read Register C once, disregard the contents, and then continue reading this register until the UF bit is a "1". The UF bit becomes true immediately after an update is completed. You then have until the start of the next update cycle to complete a read or write operation.

Power-Up/Down

Most applications require the real-time clock to remain active whenever the system power is turned off. To accomplish this, an alternate source of power is provided by connecting a battery to the Vcc supply pin of the device. A circuit is provided to switch from system power to batter power in such a way as to eliminate power drain on the battery when the entire IPC is active.

A pin is provided on the device to protect the contents of the real-time clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper system operation. To prevent noise on the inactive pins, the PWRGD signal input disables all unnecessary inputs while the system is powered down. PWRGD remains inactive to allow the remainder of the device to operate properly when power is applied to the system.

One pin (PSRSTB) is provided to initialize the device whenever power is applied to the IPC. The PSRSTB pin does not alter the RAM or clock/calendar contents, but it does initialize the necessary Control Register bits. Assertion of the PSRSTB signal disables the generation of interrupts and sets a flag indicating that the contents of the device might not be valid.

Floppy Disk Controller

General Overview

The floppy disk controller resides on the main logic board and is located on the system data bus (SD0-SD15). It is a Western Digital WD37C65 integrated system. It supports two 3 1/2-inch, high-capacity (1.44 Mb) drives through an internal, daisy-chained flat cable.

The controller supports data rates of 250 Kb/s, 300 Kb/s, or 500 Kb/s. High- and low-capacity 5 1/4-inch floppy disk drives can be used on the same internal controller. The FDC interface uses the DMA (DRQ2-DACK2*) and interrupt request (IRQ6) controls from the system bus. The on-board controller can be strapped to either the primary (3F2-3F7 hex) or the secondary (372-377 hex) FDC port address. The control signals can be disabled through software, allowing two devices to share the same DMA and IRQ channels.

Host Interface

The host interface is the host microprocessor peripheral bus. This bus is composed of eight control signals and eight data lines. In either the Special or PC/AT Mode, IRQ and DMA requests are tri-stated and qualified by DMA enable, internally provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS TTL loads. Inputs, except the data bus, are Schmidt Trigger receivers.

During the command or result phase, the Main Status Register must be read by the CPU before each byte of information is written into or read from the Data Register. After each byte is written into or read from the Data Register, the CPU should wait 12 μs before reading the Main Status Register.

Bits D6 and D7 in the Main Status Register must be "0" and "1," respectively, before each byte of the command word can be written into the FDC. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the FDC.

During the result phase, Bits D6 and D7 in the Main Status Register must both be "1's" before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the FDC is required only in the command and result phases, not during the execution phase.

During the execution phase, the Main Status Register need not be read. If the FDC is in the Non-DMA Mode, the receipt of each data byte from the FDD is indicated by an interrupt signal on Pin 16 (IRQ). The generation of a read signal (RD*) or write signal (WR*) clears the interrupt and outputs the data onto the data bus. If the CPU cannot handle interrupts quickly enough, it might poll the Main Status Register and Bit D7 (RQM) functions as the interrupt signal. If a write command is in process, the WR* signal performs the reset to the interrupt signal.

Note that in the Non-DMA Mode, it is necessary to examine the Main Status Register to determine the cause of the interrupt. It might be a data interrupt or a command interrupt, either normal or abnormal. If the FDC is in the DMA Mode, no interrupt signals are generated during the execution phase. The FDC generates DMA requests when each byte of data is available. The DMA controller responds to these requests with both the DACK* and RD* signal. When the DACK* signal goes low, the DMA Request (DMA) signal is cleared. If a write command has been issued, a WR* signal appears instead of the RD* signal. After the execution phase has been completed, the terminal count has occurred, or the EOT sector has been read or written, an interrupt occurs (IRQ). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically cleared.

The RD* or WR* signals should be asserted while the DACK* is true. The CS* signal is used in conjunction with the RD* and WR* signals as a gating function during programmed I/O operations. CS* has no effect during DMA operations. It is very important to note that in the result phase all bytes must be read. The Read Data command, for example, has several bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The FDC will not accept a new command until all seven bytes have been read. Other commands might require fewer bytes to be read during the result phase.

The FDC contains five status registers. The Main Status Register, mentioned previously, can be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during a result phase and can be read only after completing a command. The particular command that has been executed determines how many status registers are read.

The bytes of data that are sent to the FDC to form the command phase, and those that are read from the FDC in the result phase, must occur in the order shown in the appropriate table (49-63) in the "Commands" section. The command code must be sent first and the other bytes sent in the prescribed sequence.

No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the FDC, the execution phase automatically starts. Similarly, when the last byte of data is read out of the result phase, the command ends automatically and the FDC is ready for a new command.

Control Register (3F7h Primary, 377h Secondary)

The Control Register provides support logic that latches the two lsb's of the data bus upon receiving the Load Control Register (LDCR*) and Write (WR*) signals. These bits are used to select the desired data rate, which in turn controls the internal clock generation.

Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the clock or crystal. The frequency must be 64 times the MFM data rate, up to a maximum frequency of 16 MHz. This implies a maximum data rate of 250 Kb/s unless the Control Register is used. Bits 0 and 1 are used to set the transfer rate, Bits 3-7 are reserved. Table 46 presents the Control Register.

CR1 Bit 0	CR0 Bit 1	DRV Type	Data Rate	Comments	RPM Out
0	0	X	500 Kb/s	MFM	1
0	0	X	250 Kb/s	FM	1
0	1	0	250 Kb/s	MFM	0
0	1	1	300 Kb/s	MFM	0
1	0	X	250 Kb/s	MFM, RST Default	1
1	0	X	125 Kb/s	FM,RST Default	1
1	1	X	125 Kb/s	FM	0

Table 46. Control Register

Note: Drive type 0 = dual speed, 1 = single speed. Same for RPM bit returned. 0 = dual speed, 1 = single speed.

Main Status Register (3F4h Primary, 374h Secondary)

The Main Status Register is an 8-bit register that contains the status of the FDC. It can be accessed at any time. Only the Master Status Register can be used to facilitate the transfer of data between the processor and FDC.

Bits 6 (DIO) and Bit 7 (RQM) in the Main Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD* or WR* signal during a command or result phase and DIO and RQM getting set is 12 μs if the 500 Kb/s MFM data rate is selected. The maximum time from the trailing edge of the last RD* in the result phase to CB (FDC Busy) going low is 12 μs. The locations and functions of the bits in the Main Status Register are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

RQM – When Bit 7 is "1," the Data Register is ready to send data to or receive data from the processor.

DIO – Bit 6 indicates the direction of data transfer between the FDC and the Data Register. A "1" indicates that the transfer is from the register to the processor. A "0" indicates that the transfer is from the processor to the register.

EXM – Bit 5 is set only during the execution phase of Non-DMA Mode. When this bit goes low, it indicates that the execution phase has ended and the result phase has started.

CB – A "1" in Bit 4 indicates that a read or write command is in progress. The FDC will not accept any other command.

D3B – A "1" in Bit 3 indicates that Drive 3 is in the Seek Mode and the FDC will not accept read or write commands.

D2B – A "1" in Bit 2 indicates that Drive 2 is in the Seek Mode and the FDC will not accept read or write commands.

D1B – A "1" in Bit 1 indicates that Drive 1 is in the Seek Mode and the FDC will not accept read or write commands.

D0B – A "1" in Bit 0 indicates that Drive 0 is in the Seek Mode and the FDC will not accept read or write commands.

Status Register 0

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IC1	IC2	SE	EC	NR	HS	US1	US0

IC1-IC2 – Bits 6 and 7 are Interrupt Code bits. The following table shows their functions:

IC1	IC2	Meaning
0	0	Normal termination of command
0	1	Abnormal termination of command
1	0	Invalid command issued
1	1	Abnormal termination of command because of FDD ready signal changing state

Table 47. Bits 7 and 6 of Status Register 0

SE – When the FDC completes the SEEK command, the Seek End bit, Bit 5, is set to a "1."

EC – Bit 4, the Equipment Check bit, is set if a fault signal is received from the FDD or if the Track 0 signal fails to occur after 255 step pulses (Recalibrate command).

NR – Drive ready is always presumed true. Therefore, the Not Ready bit, Bit 3, will always be a "0."

HS – Bit 2, the Head Select bit, is used to indicate the state of the head at interrupt.

US1-US0 – Bits 0 and 1 are the Unit Select bits. They are used to indicate the drive unit number at the time of interrupt.

US0	US1	Drive Number
0	0	0
0	1	1

Unit Select Bit Table

Status Register 1

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
EN	X	DE	OR	X	ND	NW	MA

EN – Bit 7, the End of Cylinder bit, is set when the FDC tries to access a sector beyond the final sector of a cylinder.

b6 – Always 0

DE – The Data Error bit, Bit 5, is set if the FDC detects a CRC error in either the ID field or the data field.

OR – Bit 4, the Overrun bit, is set if the FDC is not serviced by the host system during data transfers within a certain time interval.

b3 – Always 0

ND – Bit 3, the No Data bit, is set:

- During the execution of a Read Data, Write Deleted Data, or Scan command if the FDC cannot find the sector specified in the Internal Data Register (IDR)
- During the execution of a Read ID command if the FDC cannot read the ID field without generating an error
- During a Read a Track command if the starting sector cannot be found

NW – The Not Writable bit, Bit 1, is set if the FDC detects a WP* (Write Protect) signal from the FDD during a Write Data, Write Deleted Data, or Format a Track command.

MA – Bit 0 is the Missing Address Mark bit. It is set if the FDC cannot detect the ID address mark after twice encountering the index hole. At the same time, the MD (Missing Address Mark in Data Field) bit in Status Register 2 is set.

Status Register 2

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	CM	DD	WC	SH	SN	BC	MD

b7 – Not used. Bit 7 is always 0.

CM – Bit 6 is the Control Mark bit. It is set during the execution of the Read Data or Scan command if the FDC encounters a sector that contains a Deleted Data Address Mark.

DD – Bit 5, the Data Error bit, is set if the FDC detects a CRC error in the data field.

WC – Bit 4 is the Wrong Cylinder bit. It is set if the contents of the cylinder on the medium are different from that stored in the IDR.

SH – The Scan Equal bit, Bit 3, is set during execution of the Scan command if the condition Equal is satisfied.

SN – Bit 2, the Scan Not bit, is set during the execution of the Scan command if the FDC cannot find a sector on the cylinder that meets the condition.

BC – Bit 1 is the Bad Cylinder bit. It is set when the contents of the cylinder on the medium are different from those stored in the IDR and the contents of the cylinder are FF.

MD – Bit 0 is the Missing Address Mark in Data Field bit. It is set when data is read from the medium and the FDC cannot find an Data Address Mark or Deleted Data Address Mark.

Status Register 3

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	WP*	RY	T0	WP*	HS	US1	US0

b7 - Not used. Bit 7 is always 0.

WP* – Bit 6, the Write Protect bit, is set when write protect status is received from the FDD.

RY – The Ready bit, Bit 5, is always set to logical "1".

T0 – Bit 4 is the Track 0 bit. It is set when the Track 0 signal is received from the FDD.

WP* – Bit 3, the Write Protect bit, is set when write protect status is received from the FDD.

HS – Bit 2 is used to indicate the status of the side select signal from the FDD.

US1 – Bit 1 is used to indicate the status of the unit select signal from the FDD.

US0 – Bit 0 is used to indicate the status of the unit select signal from the FDD.

Data Register (3F5h Primary, 375h Secondary)

The 8-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read from, or written to, the Data Register to program or obtain the results after a particular command.

Operations Register (3F2h Primary, 372h Secondary)

The Operations Register provides support logic that latches the data bus upon receiving the LDOR* and WR* signals. The Operations Register replaces the typical latched port used in floppy subsystems to control disk drive spindle motors and to select the desired disk drive. The following table represents the Operations Register.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
MS	X	MOEN2	MOEN1	DMAEN	SRST*	X	DSEL

b7 – Bit 7 is the Mode Select bit. During a soft reset condition, this bit can be used to select between Special Mode and AT Mode.

b6 – Not used.

MOEN2 – Bit 5 is the Motor On Enable bit, which is the inverted output of MO2*. This bit is only active in AT Mode.

MOEN1 – Bit 4 is the Motor On Enable bit, which is the inverted output of MO1*. This bit is active only in AT Mode.

DMAEN – Bit 3 is the DMA Enable bit, which is active in both the Special and PC/AT Modes. This bit qualifies the DMA and IRQ outputs as well as the DACK* input.

SRST* – Bit 3 indicates a soft reset when it is low.

b1 - Not used.

DSEL – Bit 0 is the Drive Select bit. If it is low and MOEN1="1," then DS1 is active. If it is high and MOEN2="1," then DS2 is active. Bit 0 is only used in AT Mode

Base, Special, and AT Modes

Base Mode

After a hardware reset, the RST signal active, the FDC will be held in soft reset, SRST* signal active, with the normally driven signals and the DMA request and IRQ request outputs tri-stated. Base Mode can be initiated at this time by a chip access by the host. Although the access can be any read or write, it is strongly suggested that the first access be a read of the Main Status Register.

Once Base Mode is entered, the soft reset is released, and IRQ and DMA are driven. Base Mode prohibits the use of the Operations Register. Therefore, there can be no qualifying by the DMAEN signal and no soft resets. The drive select output signals, DS1 to DS4, offer a 1 of 4 decoding of the unit select bits resident in the command structure. The RWC* signal represents *reduced write current* and indicates when write precompensation is necessary.

Special Mode

Special Mode allows the use of the Operations Register for the DMAEN signal as a qualifier to do a software driven device reset (SRST*). To enter Special Mode, the Operations Register is loaded with 1 X 0 0 X 0 X X, setting Mode Select to "1," which disables MOEN1 and MOEN2 and also causes SRST* to be active. Then, a read of the Control Register address, LDCR* and RD*, sets the device into Special Mode. The DS1 through DS4 signals, as well as the RWC* signal, are again offered in this mode.

AT Mode

For AT compatibility, users will write to the Operations Register, LDOR* and WR*. This action, performed after a hardware reset. or in the Base Mode, initiates AT Mode.

AT Mode can also be entered from Special Mode by loading the Operations Register with 0 X 0 0 X 0 X X, setting Mode S to a logical "0," disabling MOEN1 and MOEN2, and causing SRST* to be active. Then, a read of the Control Register address sets the device in AT Mode.

The DS* outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. The RWC* pin is now RPM* so that users with two-speed drives can reduce spindle speed from a nominal 369 RPM to 300 RPM when active low or reduce write current when a slower data rate is selected for a given drive.

Polling Routine

After any reset, either RST or SRST*, US0 and US1 go into a polling routine. In between commands (and in between step pulses in the SEEK command), the FDC polls all four FDDs, looking for a change in the ready line from any of the drives.

Because the drive is always presumed ready, an interrupt is generated only following a reset. This occurs because a reset forces not ready status, which then promptly becomes ready. In Special or AT Mode, if DMAEN is not valid prior to 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus.

The polling of the ready line by the FDC occurs continuously between commands. Each drive is polled every 1.024 ms except during read/write commands.

Device Resets

The FDC supports both hardware reset (RST) pin 19, and software reset (SRST*), through the use of the Operations Register.

The RST pin causes a device reset for the active duration, RST causes a default to Base Mode, and default selects 250 Kb/s MFM (or 125 Kb/s FM code dependent) as the data rate (16 MHz input clock).

SRST* resets the microcontroller as does the RST but does not affect the current data rate selection or the mode.

Both RST and SRST*, when active, disable the high current driver outputs to the FDD.

Data Separator

The **data separator**, built in the WD37C65 FDC, is a WD92C32 Phase Lock Loop Floppy Disk Data Separator (DPLL). It is designed address high-performance error rates on floppy disk drives and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance.

Write Precompensation

The FDC maintains the standard first-level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz clock, CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle and is equal to one-half the WCLK period.

When the PCVAL signal is active, all data is precompensated by + or - 125 ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If the PCVAL signal is not active, and if a track inside number 28 is accessed, then + or - 187 ns precompensation is generated. When the non-standard data rate using CLK2 is chosen, the MFM precompensation is always two clock cycles. For 9.6 MHz, this is + or - 208 ns. In this case, the PCVAL signal is disabled.

Clock Generation

This logical block internal to the WD37C65 FDC provides all the clocks needed by the FDC: the *sampling clock* (SCLK), the *write clock* (WCLK), and the *master clock* (MCLK).

SCLK drives the data separator used during data recovery. This clock frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency of 2 times the selected data rate.

MCLK is used by the microsequencer. MCLK and MCLK* clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate. The following table presents the clock data rates:

Data Rate	Code	SCLK	MCLK	WCLK
500 Kb/s	MFM	16 MHz	4.0 MHz	1.0 MHz
250 Kb/s	FM	8 MHz	4.0 MHz	500 KHz
250 Kb/s	MFM	8 MHz	2.0 MHz	500 KHz
125 Kb/s	FM	4 MHz	2.0 MHz	250 KHz
300 Kb/s	MFM	9.6 MHz	2.4 MHz	600 KHz

Table 48. Clock Data Rates

Commands

The FDC is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The result after the execution of the command can also be a multibyte transfer back to the processor.

Command operation consists of three phases:

- Command Phase – The FDC receives all information required to perform a particular operation from the processor.
- Execution Phase – The FDC performs the operation as instructed.
- Result Phase – After completion of the operation, status and other housekeeping information are made available to the processor.

Tables 49-63 provide details about the FDC commands.

Command Symbol Description

Symbol	Name	Description
A0	Address Line 0	Controls selection of Main Status Register (A0=0) or Data Register (A0=1)
C	Cylinder Number	Current selected cylinder number
D	Data	Data pattern to be written into a sector
D7-D0	Data bus	8 bit data bus D0=lsb, D7=msb
DTL	Data Length	When N is 0, DTL stands for the data length to be written into a sector
EOT	End of Track	Final sector number on a cylinder. During read or write operations the FDC will stop data transfer after it reaches a sector number equal to EOT.
GPL	Gap Length	Gap 3 length. During a format command it determines the size of Gap 3.
H	Head Address	Head number, 0 or 1, as specified in the ID field.
HLT	Head Load Time	Head Load Time of FDD from 2-254 ms in increments of 2 ms.
HS	Head Select	Selected head number 0 or 1.
HUT	Head Unload Time	Head unload time after a read or write operation from 16-240 ms in 16 ms increments.
MF	FM or MFM	If low, FM mode is selected, if high, MFM mode is selected.

Command Symbol Legend

Symbol	Name	Description
MT	Multitrack	If MT is high, a multitrack operation is performed.
N	Number	Number of data bytes written in a sector.
NCN	New Cylinder Number	The new cylinder number that will be reached after a seek operation.
ND	Non DMA Mode	The operation is performed in the non-DMA mode.
PCN	Present Cylinder Number	The cylinder number at the end of the Sense Interrupt Status command.
R	Record	Sector number which will be read or written
R/W	Read/Write	Read or Write signal.
SC	Sector	Number of sectors per cylinder
SK	Skip	Skip Deleted Data Address k.
SRT	Step Rate Time	Stepping rate for the FDD 1-16 ms in1 ms increments.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Stands for one of the four status registers where information is stored after a command is executed.
STP		During scan operations if STP = 1 then contiguous sectors are compared with the data sent, if STP = 2 then alternate sectors are compared.

Command Symbol Legend

Read Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	0	0	1	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W	Cylinder number								Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W	Head address								
	W	Sector number								
	W	Number of bytes								
	W	Final sector number								
	W	Gap length								
	W	Data length								
Execution										Data transfer between FDD (Floppy Disk Drive) and system.
Results	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	Cylinder number								Sector ID information after command execution.
	R	Head address								
	R	Sector number								
	R	Number of bytes								

Table 49. Read Data Command

Read Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	0	1	1	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 50. Read Deleted Data Command

Write Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	0	0	0	1	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W	Cylinder number								Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W	Head address								
	W	Sector number								
	W	Number of bytes								
	W	Final sector number								
	W	Gap length								
	W	Data length								
Execution										Data transfer between FDD and system.
Results	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	Cylinder number								Sector ID information after command execution.
	R	Head address								
	R	Sector number								
	R	Number of bytes								

Table 51. Write Data Command

Write Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	0	0	1	0	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W	Cylinder number								Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W	Head address								
	W	Sector number								
	W	Number of bytes								
	W	Final sector number								
	W	Gap length								
	W	Data length								
Execution										Data transfer between FDD and system.
Results	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	Cylinder number								Sector ID information after command execution.
	R	Head address								
	R	Sector number								
	R	Number of bytes								

Table 52. Write Deleted Data Command

Read a Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	SK	0	0	0	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system. FDD reads all data fields from index hole to EOT.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 53. Read a Track Command

Read ID

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	0	0	1	0	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
Execution										The first correct ID information on the cylinder is stored in the Data Register.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 54. Read ID Command

Format a Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	0	0	1	1	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Number of bytes							Bytes per sector.
	W		Number of sectors							Sectors per track.
	W		Gap length							Gap 3.
	W		DT							Filler byte.
Execution										FDC formats the entire track.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 55. Format a Track Command

Scan Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	0	0	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		STP							1 = compare contiguous sectors; 2 = compare alternate sectors.
Execution										Data compared between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 56. Scan Equal Command

Scan Low or Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	1	0	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		STP							1 = compare contiguous sectors; 2 = compare alternate sectors.
Execution										Data compared between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 57. Scan Low or Equal Command

Scan High or Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	1	1	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		STP							1 = compare contiguous sectors; 2 = compare alternate sectors
Execution										Data compared between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 58. Scan High or Equal Command

Recalibrate

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	1	1	Command codes.
	W	X	X	X	X	X	0	US1	US0	
Execution										Heads retract to Track 0.

Table 59. Recalibrate Command

Sense Interrupt Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	0	0	0	Command codes.
Results	R		ST0							Status information about the FDC at the end of a SEEK operation.
	R		Present cylinder							

Table 60. Sense Interrupt Status Command

Specify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	0	1	1	Command codes.
	W	Step rate time, head unload time								
	W	Head load time, Non-DMA Mode								

Table 61. Specify Command

Sense Drive Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
Results	R	ST3								Status information about FDC.

Table 62. Sense Drive Status Command

Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	1	1	1	Command codes.
	W	X	X	X	X	X	0	US1	US0	
	W	New cylinder number								
Execution										Heads positioned to the proper cylinder.

Table 63. Seek Command

Serial/Parallel Interface

The serial/parallel card (standard) is compatible with the IBM AT. The serial portion of the card supports the EIA RS-232C interface standard through a 9-pin male D-shell connector located on the rear of the unit for external chassis access.

The UART, a National Semiconductor NS16450, used on this card is fully programmable and supports asynchronous communications with 5, 6, 7, or 8 character bits; 1, 1.5, or 2 stop bits; with or without parity. The baud-rate generator supports operation from 50 to 9600 baud. A prioritized interrupt scheme controls transmit, receive, error, line status, and data set interrupts.

The Serial portion of the adapter is accessible through Interrupt IR4 for COM1 and IR3 for COM2. The serial port is addressable through I/O port 3F8h-3FFh for COM1 and 2F8h-2FFh for COM2. For a detailed set of instructions and programming information, refer to the NS16450 in the Devices section.

The parallel portion of the board is accessible through Interrupt IR7 for LPT1 and IR5 for LPT2. The following is a table of addresses that can be used in programming the parallel port. The first address is for the primary port and the second is for the secondary port.

0378h (37Ch)Printer - Data Latch

Bit	Description
0	Bit 0 - LSB
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

0379h (37Dh)Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	"0" = Error
4	"1" = Printer Select
5	"1" = Out of Paper
6	"0" = Acknowledge
7	"0" = Busy

Address	Description
037Ah (037Eh)	Printer - Control Latch

Bit	Description
0	"1" = Strobe
1	"1" = Auto FD XT
2	"0" = Initialize
3	"1" = Select Printer
4	"1" = Enable Interrupt
5	Not Used
6	Not Used
7	Not Used

037Bh	Not Used

Keyboard Control

The keyboard controller (U1) is a single-chip microcomputer (Intel 8042) that is programmed to be IBM AT compatible.

The controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer, I/O address 060h. The controller will interrupt the CPU on interrupt line IR1 when data is available to be read.

Data is sent to the keyboard by writing to the controller's input buffer, I/O address 064h for issuing a command, and 060h for data. (Status Register bits inform the CPU of any error encountered in receiving the data.) The byte of data is serialized and sent to the keyboard, with odd parity bits automatically inserted. The keyboard acknowledges all data transmissions, and the acknowledgment separates each byte transmitted.

The keyboard sends serial format data to the controller, using an 11-bit frame. (Data sent is synchronized by a keyboard-supplied clock.) The first bit is a start bit. It is followed by 8 data bits, an odd parity bit, and a stop bit. At the end of a transmission, the controller disables the interface until the system accepts the data byte.

For a received byte of data with a parity error, a resend command is sent to the keyboard.

Whenever the controller is unable to receive the data correctly, FF hex is placed in its output buffer, and the parity bit in the Status Register is set to 1.

The controller will also time a byte of data from the keyboard, and if the byte transmission does not end within 2 milliseconds, FF hex is placed in the controller's output buffer, and the receive time-out bit in the Status Register is set. (No retries will be attempted on a receive time-out error).

For scan codes received from the keyboard, the controller converts these codes to system scan codes before they are put into the controller's output buffer.

Data is sent to the keyboard in the same serial format used to receive data from the keyboard. If the keyboard does not start clocking the data out of the controller within 15 milliseconds, or if it completes that clocking within 2 milliseconds, FE hex is placed in the controller's output buffer, and the transmit time-out error bit is set in the Status Register.

If the response contains a parity error, FE hex is placed in the controller's output buffer, and the transmit time-out and parity error bits are set in the Status Register. The controller is programmed to a set time limit for the keyboard to respond. If 25 milliseconds are exceeded, the controller places FE hex in its output buffer and sets the transmit and receive time-out error bits in the Status Register. (No retry is made by the controller for any transmission error.)

The controller also senses the status of the display type jumper E1-E2.

Status Register Bit Definitions

Bit 0, Output Buffer Full – When this bit is a 0 it indicates that the output buffer is empty. A 1 indicates that there is data in the output buffer but the system has not yet read the data. When the system does read the data this bit is returned to a 0.

Bit 1, Input Buffer Full – A 0 in this position means the input buffer at I/O address 60h or 64h is empty. A 1 indicates that data has been written into the buffer but the controller (8042) has not read it yet. When the data is read by the controller this bit returns to a 0.

Bit 2, System Flag – This bit may be set to 0 or 1 by writing to the flag bit in the controller's command byte. It is set to 0 on power up reset.

Bit 3, Command/Data – The input buffer may be addressed as I/O address 60h or 64h. Address 60h is defined as a data port while address 64h is a command port. Writing to address 64h sets this bit to a 1, and writing to address 60h sets it to 0. The controller uses this bit to determine if the byte in the input buffer is a data or command byte.

Bit 4, Inhibit Switch – This bit is updated when data is placed in the output buffer. It reflects the state of the keyboard inhibit switch. A 0 in this bit means the keyboard is inhibited.

Bit 5, Transmit Time Out – A 1 in this bit indicates that a transmit by the keyboard controller was not properly completed. This bit works in conjunction with Bits 6 and 7. If the transmit byte was not clocked out in the specified time limit, this will be the only bit set. If the transmit byte was clocked out and a response was not sent within the specified time limit, this bit and the receive time out bits is set. If the transmit byte was sent and a response was received with a parity error, this bit and the parity error bit is set.

Bit 6, Response Time Out – A 1 indicates that a transmission was started by the keyboard but did not finish within the programmed time limit.

Bit 7, Parity Error – A 0 indicates the last byte received from the keyboard had odd parity. A 1 indicates the last byte received had even parity. The keyboard should send data with odd parity.

Keyboard Controller Command Set
(I/O Address 64h)

20 – Read Keyboard Controller's Command Byte — The controller sends the current command byte to the output buffer.

60 – Write Keyboard Controller's Command Byte — The next byte of data written to I/O address 60h is put in the controller's command byte. Bit definitions for the command byte are as follows:

Bit 7– Reserved. Should be a 0.

Bit 6 – IBM Personal Computer Compatibility Mode.
Writing a 1 to this bit causes the controller to convert the scan codes it receives to those used by the IBM Personal Computer.

Bit 5 – IBM Personal Computer Mode.
Writing a 1 to this bit programs the keyboard to support the IBM Personal Computer keyboard interface. The controller will not check parity or convert scan codes.

Bit 4 – Disable Keyboard.
Writing a 1 to this bit disables the keyboard interface by driving the clock line low. Data is not sent or received.

Bit 3 – Inhibit Override.
A 1 in this bit disables the keyboard inhibit function.

Bit 2 – System Flag.
The value written to this bit is put in the system flag bit of the status register.

Bit 1 – Reserved. Should be written to a 0.

Bit 0 - Enable Output Buffer Full Interrupt.
Writing a 1 to this bit causes the controller to generate an interrupt when it places data into the output buffer.

A4 - Test Password. This command checks if there is a password currently installed in the 8042. The test result is placed in the output buffer (I/O Address 060h). A hex FA means the password is installed. A F1 means no password is installed.

A5 - Load Security. This command starts the load password procedure. Following this command the 8042 will input from the data port until a null (0) is detected, which terminates the password entry.

A6 - Enable Security. This command enables the 8042 security feature. This command is only valid when a password pattern is currently loaded into the 8042.

A7 - Disable Auxiliary Device Interface. This command sets Bit 5 of the 8042 command byte. This disables the auxiliary device and data is not sent or received.

A8 - Enable Auxiliary Device Interface. This command clears Bit 5 of the 8042 command byte. This releases the auxiliary device interface.

A9 - Interface Test. This command causes the 8042 to test the auxiliary device clock and data lines. The test result is placed in the output buffer (I/O Address 060h). The test results are as follows:

- 00 - No Error
- 01 - Auxiliary device clock line stuck low
- 02 - Auxiliary device clock line stuck high
- 03 - Auxiliary device data line stuck low
- 04 - Auxiliary device data line stuck high

AA - Self Test. Causes the controller to perform internal diagnostics. 55h is placed in the output buffer if no errors are encountered.

AB - Interface Test. Causes the controller to test the clock and data lines. The result is placed in the output buffer as follows:

- 00 - No error detected
- 01 - Clock line stuck low
- 02 - Clock line stuck high
- 03 - Data line stuck low
- 04 - Data line stuck high

AC – Diagnostic Dump. Sends 16 bytes of the controller's RAM, current state of the input port, current state of the output port, and the controller's program status word to the system. All items are sent in scan code format.

AD – Disable Keyboard Feature. This sets Bit 4 of the controller's command byte. This disables keyboard interfacing by driving the clock line low. Data will not be sent or received.

AE – Enable Keyboard Interface. This command clears Bit 4 of the command byte. This releases the keyboard interface.

C0 – Read Input Port. Tells the controller to read the input port and place the data in the output buffer. This command should be used only if the output buffer is empty.

C1 – Poll Input Port Low. Port 1 Bits 0-3, in Status Bits 4-7.

C2 – Poll Input Port High. Port 1 Bits 4-7, in Status Bits 4-7.

D0 – Read Output Port. Causes the controller to read the output port and place the contents in the output buffer. This command should only be used if the output buffer is empty.

D1 – Write Output Port. The next byte of data written to I/O address 60h is placed in the output port. Note that Bit 0 of the controller's output port is connected to system reset and should not be written low.

E0 – Read Test Inputs. This causes the controller to read it's T0 and T1 inputs. The data is placed in the output buffer with data bit 0 representing T0 and data bit 1 representing T1.

F0-FF – Pulse Output. Port Bits 0-3 of the controllers output port may be pulsed low for approximately 6 μsec. Bits 0-3 of this command indicate which bits are to be pulsed. A 0 causes the bit to be pulsed, and a 1 causes the bit not to be pulsed. Note that Bit 0 of the controller's output port is connected to system reset and should not be written low.

Interface Requirements

System I/O (AT) Bus

This section identifies the I/O interface requirements for both the PC-compatible and AT-compatible option cards. There are eight expansion slots in the DECstation 320. Two are PC-type slots. Each of these has a 62-position connector. The other six are AT-type slots, each of which has one 62-position connector and one 36-position connector. The last slot is a for a 32-bit memory expansion option. System board power consumption is rated at 3.5 Amps for the +5V supply and 45 mA for the +12V supply, including the FDC. This allows an effective 16.3A available for the +5V and 6.5A total for the +12V on the system I/O bus and disk drive power connectors.

PC Interface Compatiblity

The following pin assignments are used on the 62-position connector found on both the AT- and the PC-type option slots:

Pin	Signal Name	Pin	Signal Name
A1	IOCHCHK*	B1	Ground
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5 V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5 V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12 V
A8	SD1	B8	0WS*
A9	SD0	B9	+12 V
A10	IOCHRDY	B10	Ground
A11	AEN	B11	SMEMW*
A12	SA19	B12	SMEMR*
A13	SA18	B13	IOW*
A14	SA17	B14	IOR*
A15	SA16	B15	DACK3*
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1*
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH*
A20	SA11	B20	SYSCLK*
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2*
A27	SA4	B27	T/C
A28	SA3	B28	BALE
A29	SA2	B29	+5 V
A30	SA1	B30	OSC
A31	SA0	B31	Ground

Table 64. Pin Assignments for 62-Position Connector

PC Bus Pin Definitions

The following signal descriptions for the System I/O Bus are for PC and AT bus-compatible option cards. Note that all signal lines are TTL compatible levels and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

CLK (B20). CLK is the System clock. It has a 50% duty cycle and is used only for sychronization with the CPU. It is not intended for uses requiring a fixed frequency. It is an 8 MHz signal.

SA0 through SA19 (A12-A31). These lines are 20 address bits used to address memory and I/O devices within the DECstation 320. They are gated on the system bus when the BALE signal is high and are latched on the falling edge of the BALE signal. Generation of these signals is accomplished by the CPU or a DMA controller. SA0-SA19 are active high.

BALE (B28). BALE is a Buffered Address Latch Enable generated by the CPU Bus Controller. It is used to latch valid addresses from the CPU, and can be used by an I/O board to indicate a valid CPU address, in conjunction with AEN. BALE is pulled to a high state during DMA cycles, which include Refresh cycles. BALE is active high.

AEN (A11). AEN is an Address Enable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus, the READ command lines, and the WRITE command lines. AEN is active high.

SD0 through SD7 (A2-A9). These signals are the data bus bits 0 through 7 from the CPU to memory and I/O devices on the bus. SD0 is the least significant bit (lsb), and SD7 is the most significant bit (msb).

RESETDRV (B2). RESETDRV is used to reset or initialize the expansion logic during power-up time, line voltage outage, or when the Reset switch on the front panel is pressed. BRESET is active high.

IOCHCHK* (A1). This signal indicates an uncorrectable system error when active. The IOCHCHK* signal provides the system board with parity information about memory or devices on the bus. IOCHCHK* is active low.

IOCHRDY (A10). This signal is used to lengthen I/O or memory cycles when driven low by the active device. (This signal should not be held low more than 15 microseconds.) Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command. See the timing diagram for setup times. IOCHRDY is active high (Ready condition).

IRQ9 and IRQ3 through IRQ7 (B4, B21-B25). These signals are used to tell the CPU that an I/O device needs attention. The Interrupt Requests are prioritized with IRQ2 having the highest priority and IRQ7 the lowest. An Interrupt Request is generated when any IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IOR* (B14). IOR* is a read signal that instructs an I/O device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOR* is active low.

IOW* (B13). IOW* is a write signal that instructs an I/O device to read, or latch, the data from the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOW* is active low.

SMEMR* (B12). SMEMR* is a read signal that instructs a memory device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMR* is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMR* is active low.

SMEMW* (B11). SMEMW* is a write signal that instructs a memory device to read, or latch, the data from the data bus **(SD0-SD7)**. This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMW* is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMW* is active low.

DRQ1, DRQ2, and DRQ3 (B18, B6, B16). These lines are asynchronous DMA requests by peripheral devices to gain DMA service. They are prioritized with DRQ1 having the highest priority, DRQ2 next, and DRQ3 lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform only 8-bit transfers. All DRQ lines are active high.

DACK1*, DACK2*, and DACK3* (B17, B26, B15). These lines are DMA acknowledge signals used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. All DACK signals are active low.

REFRESH* (B19). This signal is used to indicate a refresh cycle that can be used by a memory board to refresh Dynamic memory. REFRESH* is active low and generated every 15 μsec.

T/C (B27). T/C is a signal that provides a pulse when the terminal count for any DMA channel is reached. T/C is active high.

OSC (B30). OSC is an oscillator signal that is a high-speed clock with a 70 nanosecond period (14.31818 megahertz). It has a 50% duty cycle.

AT Interface Compatibility

The following pin assignments are used on the 36-position connector found only on the AT-type slots.

Pin†	Signal Name	Pin††	Signal Name
C1†	SBHE	D1††	MEMCS16*
C2	SA23	D2	IOCS16*
C3	SA22	D3	IRQ10
C4	SA21	D4	IRQ11
C5	SA20	D5	IRQ12
C6	SA19	D6	IRQ15
C7	SA18	D7	IRQ14
C8	SA17	D8	DACK0*
C9	MEMR*	D9	DRQ0
C10	MEMW*	D10	DACK5*
C11	SD08	D11	DRQ5
C12	SD09	D12	DACK6*
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7*
C15	SD12	D15	DRQ7
C16	SD13	D16	+5 V
C17	SD14	D17	MASTER*
C18	SD15	D18	Ground

Table 65. Pin Assignments for 36-Position Connector

† **Note:** Pin No.s that begin with a **C** on the PCB are labeled **A** on the schematic.

†† **Note**: Pin No.s that begin with a **D** on the PCB are labeled **B** on the schematic.

AT Bus Pin Definitions

SBHE (C1). Bus High Enable indicates a transfer on the upper eight bits of the data bus, SD8-SD15. Sixteen bit devices use this signal to condition the data bus buffers tied to SD8-SD15. SBHE is active high.

SA17-SA23 (C2 through C8). These signals are used to address memory and I/O devices in the system. These signals are valid when BALE is high. These signals are not latched during microprocessor cycles, therefore they do not stay valid for the entire cycle. They generate decodes for 1 wait state memory cycles. These decodes should be latched by the I/O adapters on the falling edge of BALE. These signals may also be driven by other DMA controllers or microprocessors that reside on the bus. SA17-SA23 are active high.

MEMR* (C9). This signal, along with SMEMR*, is used to instruct memory devices to drive data onto the data bus and is active on all memory read cycles. MEMR* may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMR*, it must have address lines valid on the bus for at least one system clock period before asserting MEMR*. MEMR* is active low.

MEMW* (C9). This signal, along with SMEMW*, is used to instruct memory devices store data present on the data bus and is active on all memory write cycles. MEMW* may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMW*, it must have address lines valid on the bus for at least one system clock period before asserting MEMW*. MEMW* is active low.

SD8-SD15 (C11 through C18). These are the upper eight bus bits for the memory and I/O devices. 16 bit devices will use SD0-SD7 of the PC bus and SD8-SD15 if the AT bus.

MEMCS16* (D1). This signal is used to tell the system board if the present data transfer is a 16-bit N wait state memory cycle where N is determined by the 82C301. The default is 2. It is decoded from the SA17-SA23 lines. MEMCS16* is active low.

IOCS16* (D2). This signal is used to tell the system board if the present data transfer is a 16-bit N wait state I/O cycle where N is determined by the 82C301. The default is 2. IOCS16* is active low.

IRQ10-IRQ12, IRQ14-IRQ15 (D3 through D7). Interrupt Requests IRQ10-IRQ14 are used to signal the microprocessor that an I/O device needs attention. An interrupt request is generated by raising an IRQ line high. The line must be held high until the microprocessor acknowledges the request. IRQ13 is reserved for the system board.

DRQ0, DRQ5-DRQ7 (D9, D11, D13, D15). DMA request 0 and DMA request 5 through 7 are asynchronous channel requests used by peripheral devices on the I/O bus to gain DMA service. A request is generated by bringing the DRQ line high, and the line must be held high until a DMA Acknowledge line goes active. DRQ0 will perform 8-bit transfers, and DRQ5-DRQ7 will perform 16-bit transfers. These signals are active high.

DACK0*, DACK5* - DACK7* (D8, D10, D12, D14). These lines are used to acknowledge DRQ0 and DRQ5-DRQ7. These signals are active low.

+5V (D16). Bus connector power.

MASTER* (D17). This signal is used with the DRQ lines to gain control of the system. A processor or DMA controller on the I/O bus can issue a DRQ to a DMA channel and receive a DACK. In response to the DACK, the processor or DMA controller can pull the MASTER* signal low, thus allowing it to control the system data, address, and control lines. After MASTER* is low, the I/O device must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. Warning, if this signal is held low for more than 15 microseconds, system memory may be lost due to lack of refresh.

GROUND (D18). Ground for I/O bus.

Memory Expansion Bus

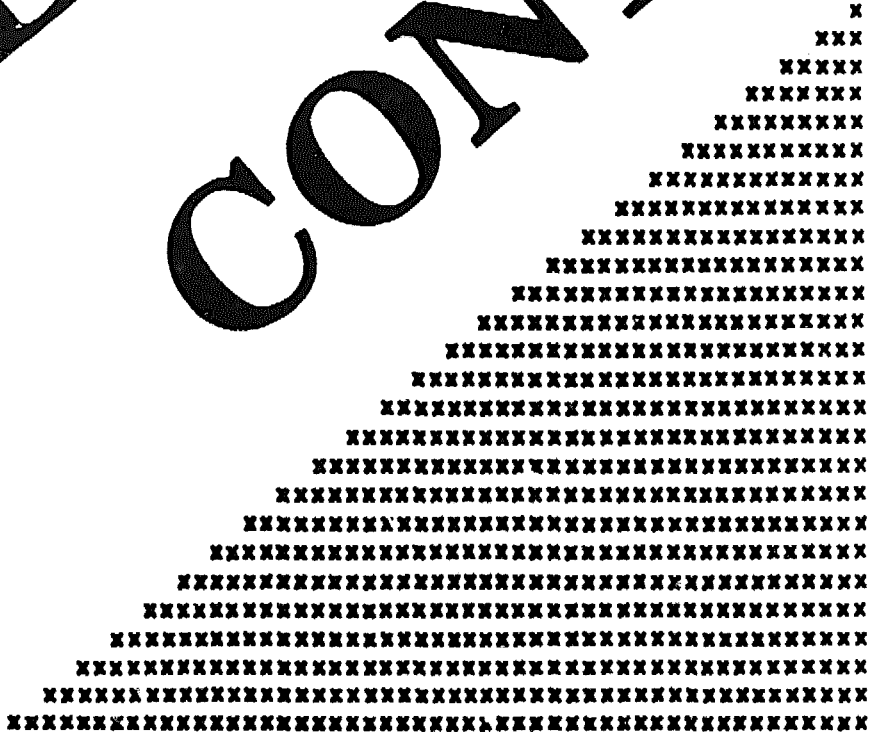
The *memory expansion bus* (MEB) is located in Slot #1 of the card cage. It is designed to support one 32-bit memory card with either 2 or 8 megabytes of 100 nS DRAM. The memory expansion bus is presented to two 36-pin card edge connectors with the following signal description:

Pin	Signal Name	Pin	Signal Name
A1	+5 V	B1	+5 V
A2	Ground	B2	Ground
A3	MD00	B3	MD01
A4	MD02	B4	MD03
A5	MD04	B5	MD05
A6	MD06	B6	MD07
A7	MD08	B7	MD09
A8	MD10	B8	MD11
A9	MD12	B9	MD13
A10	MD14	B10	MD15
A11	MD16	B11	MD17
A12	MD18	B12	MD19
A13	MD20	B13	MD21
A14	MD22	B14	MD23
A15	MD24	B15	MD25
A16	MD26	B16	MD27
A17	MD28	B17	MD29
A18	MD30	B18	MD31
C1	+5 V	D1	+5 V
C2	Ground	D2	Ground
C3	+5 V	D3	+5 V
C4	Ground	D4	Ground
C5	MA0	D5	MA1
C6	MA2	D6	MA3
C7	MA4	D7	MA5
C8	MA6	D8	MA7
C9	MA8	D9	MA9
C10	Ground	D10	+5 V
C11	+5 V	D11	DWE*
C12	RAS2*	D12	CAS2*
C13	RAS3*	D13	CAS3*
C14	LBE0*	D14	MP0
C15	LBE1*	D15	MP1
C16	LBE2*	D16	MP2
C17	LBE3*	D17	MP3
C18	+5 V	D18	Ground

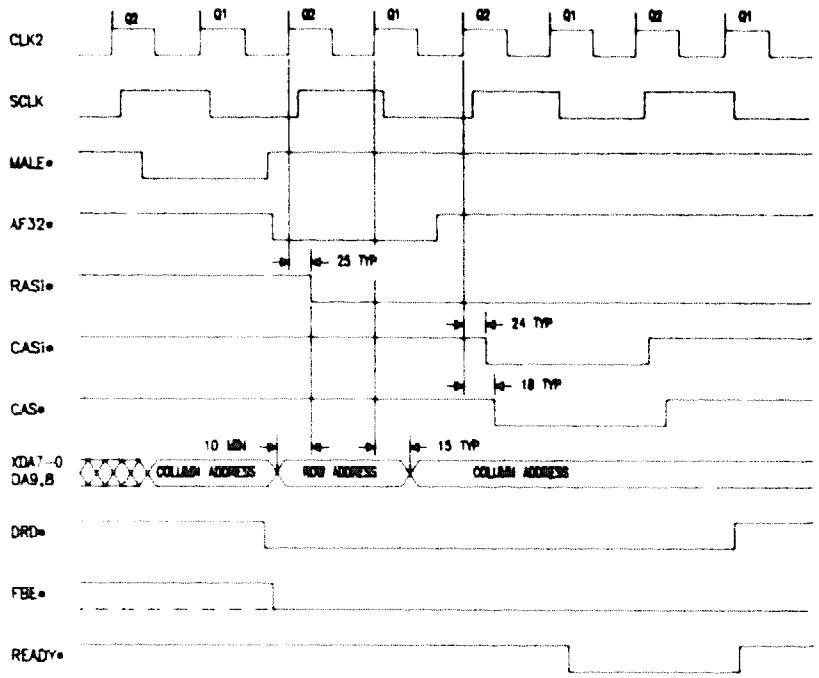
Table 66. Signal Description for 36-Pin Memory Card Edge



MAIN LOGIC CONT'D

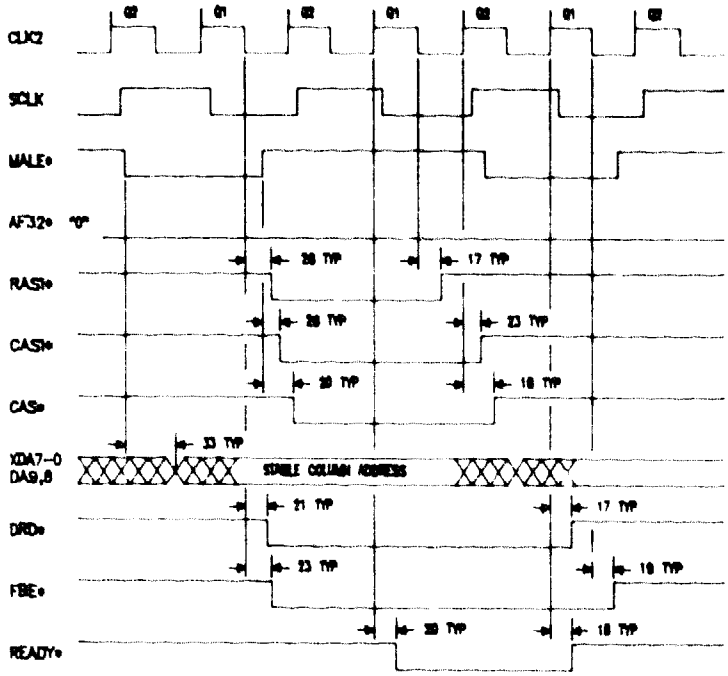


82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ CYCLE WITH RAS BEING INACTIVE



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82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ HIT, 0 WAIT STATE

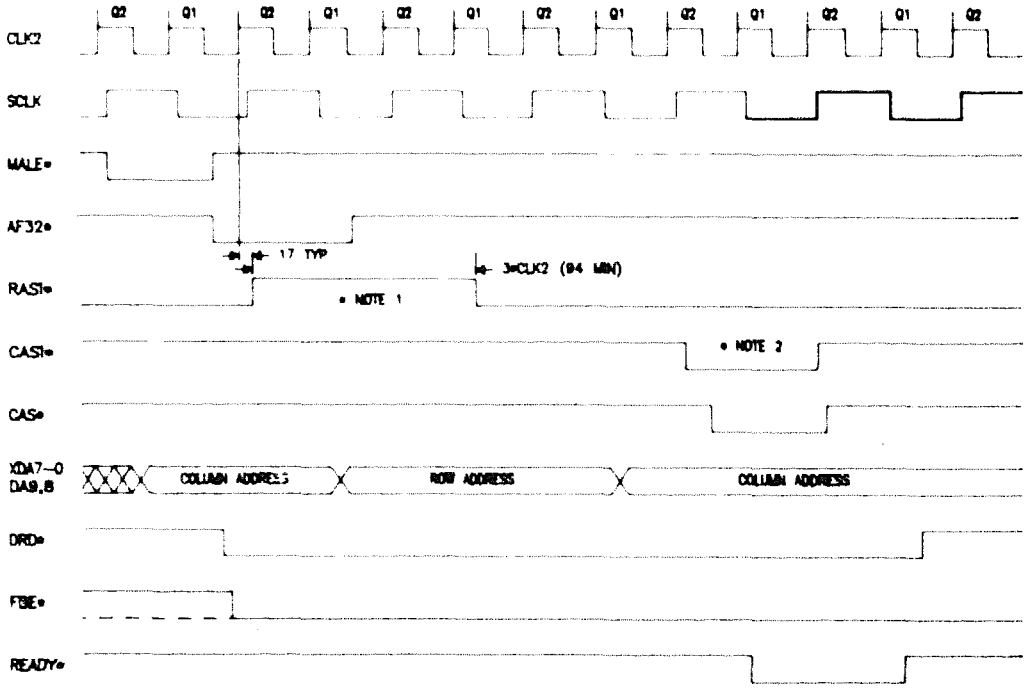


SCHEMATIC -
TANDY 4000
TIMING DIAGRAM

TANDY

1 OF

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ MISS CYCLE

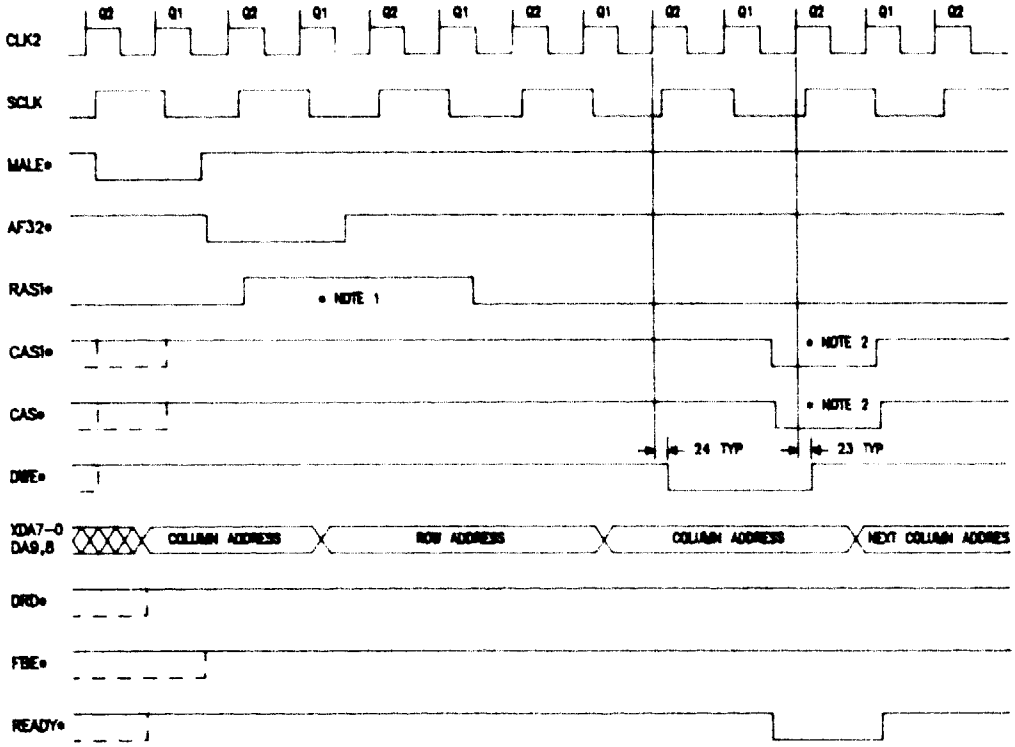


NOTES

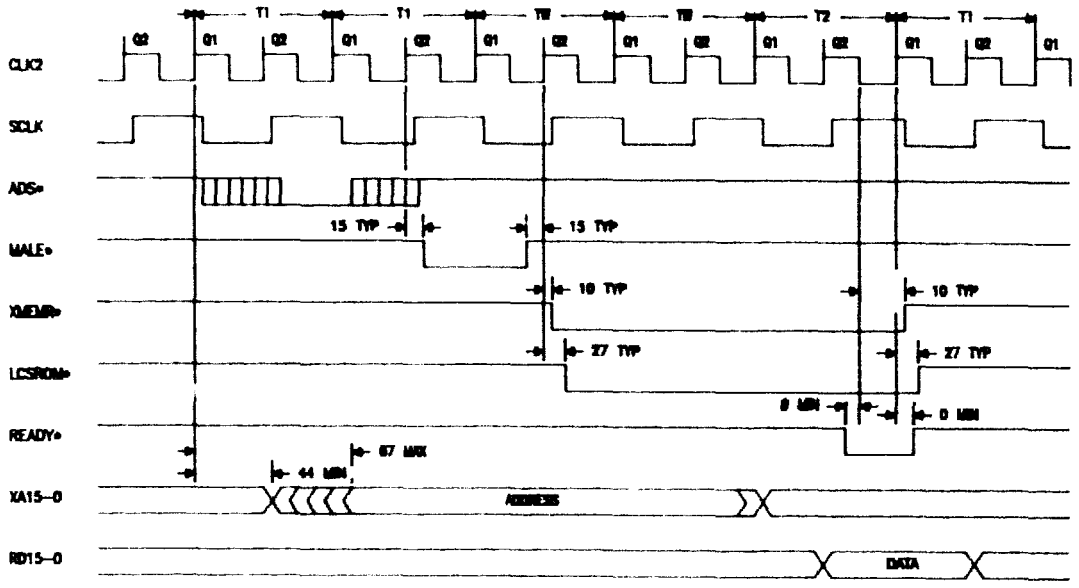
1. RAS* PRECHARGE TIME WILL BE INCREAS BY 2 CLK2 CYCLES IF BIT 7 OF REGISTER 11 (OR 13) IS PROGRAMMED TO "1".
2. CAS1* & CAS* PULSE WIDTHS WILL BE INCREASED BY 2 CLK2 CYCLES IF BIT 6 OF REGISTER 11 (OR 13) IS PROGRAMMED TO "1".

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82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
WRITE MISS CYCLE



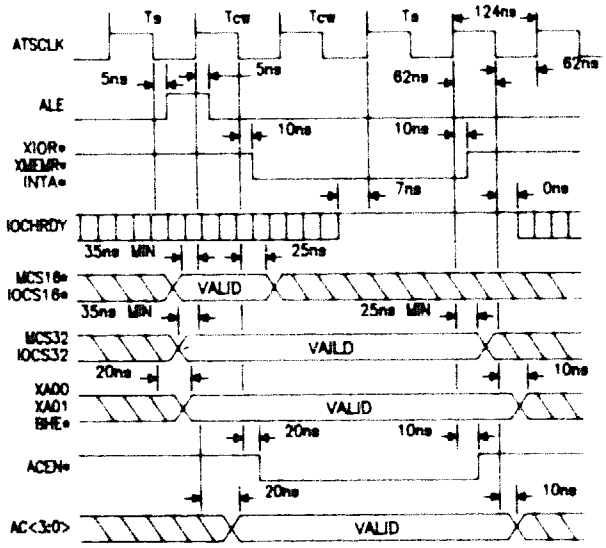
ROM READ CYCLE

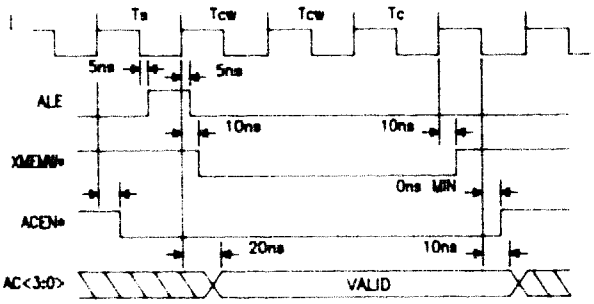


NOTES

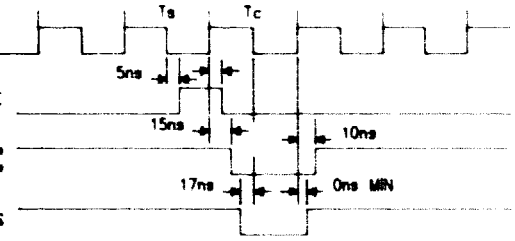
1. ALL UNITS IN NANOSECONDS.

82C301 I/O TIMING DIAGRAMS





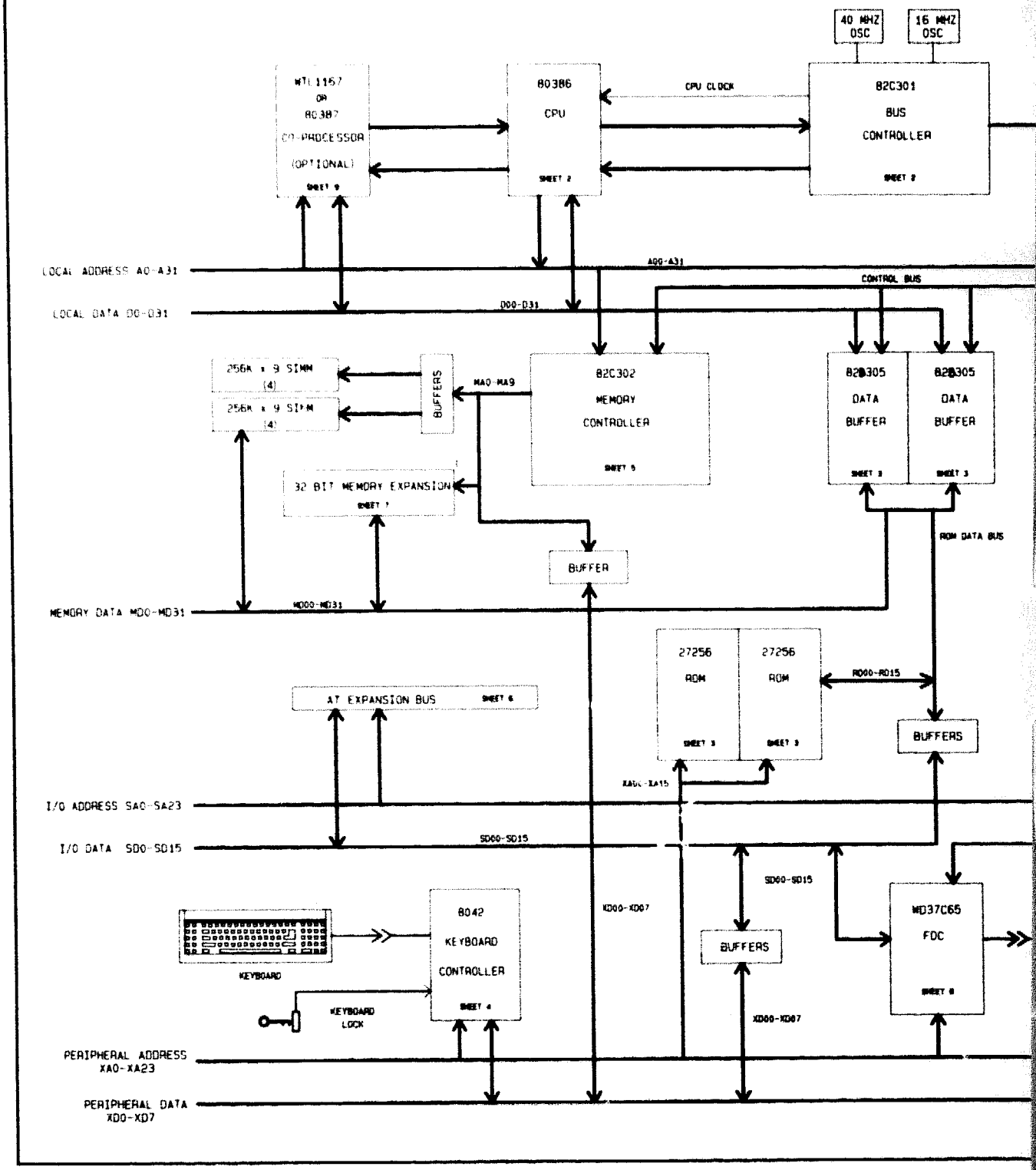
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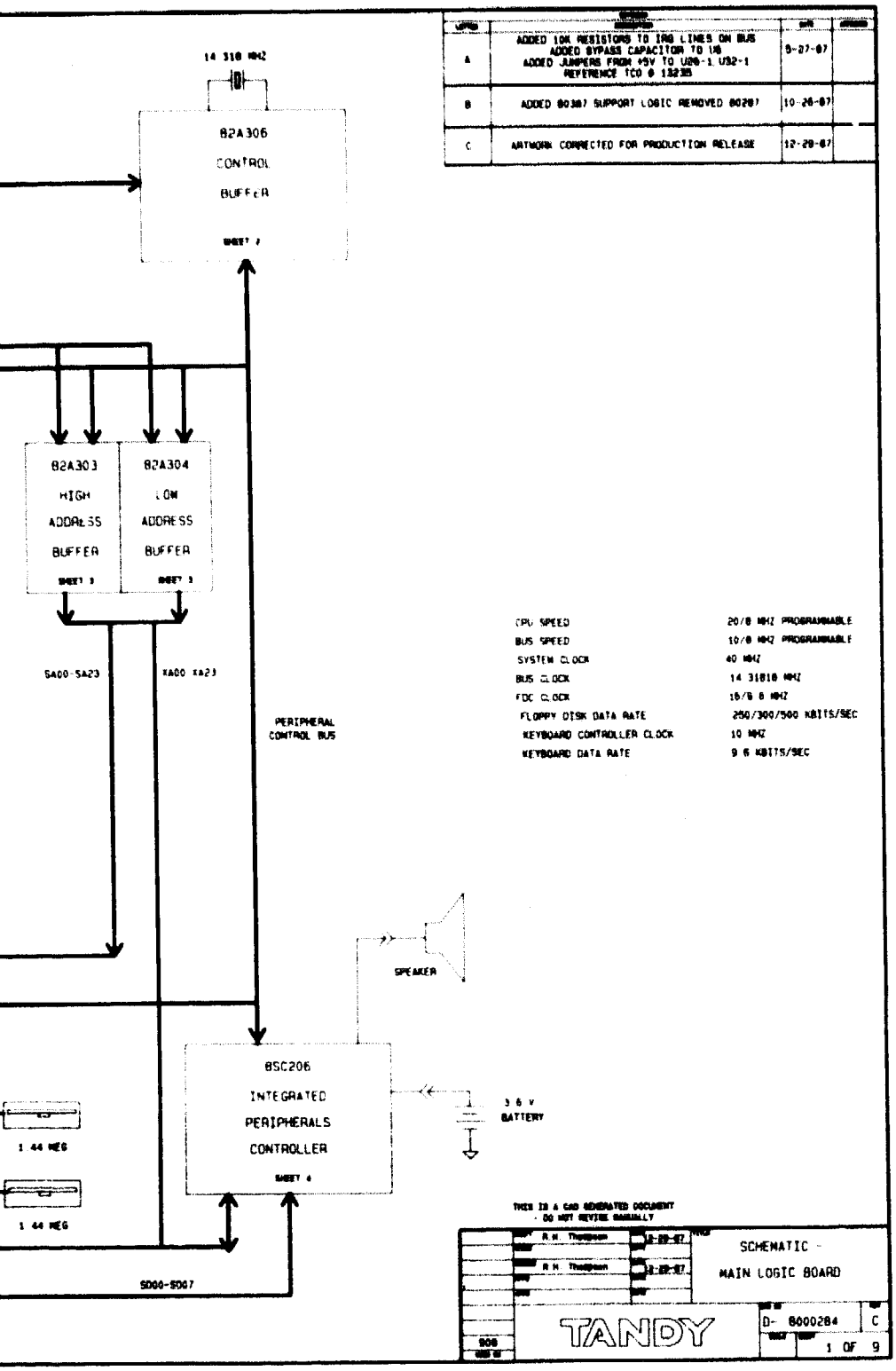
TANDY

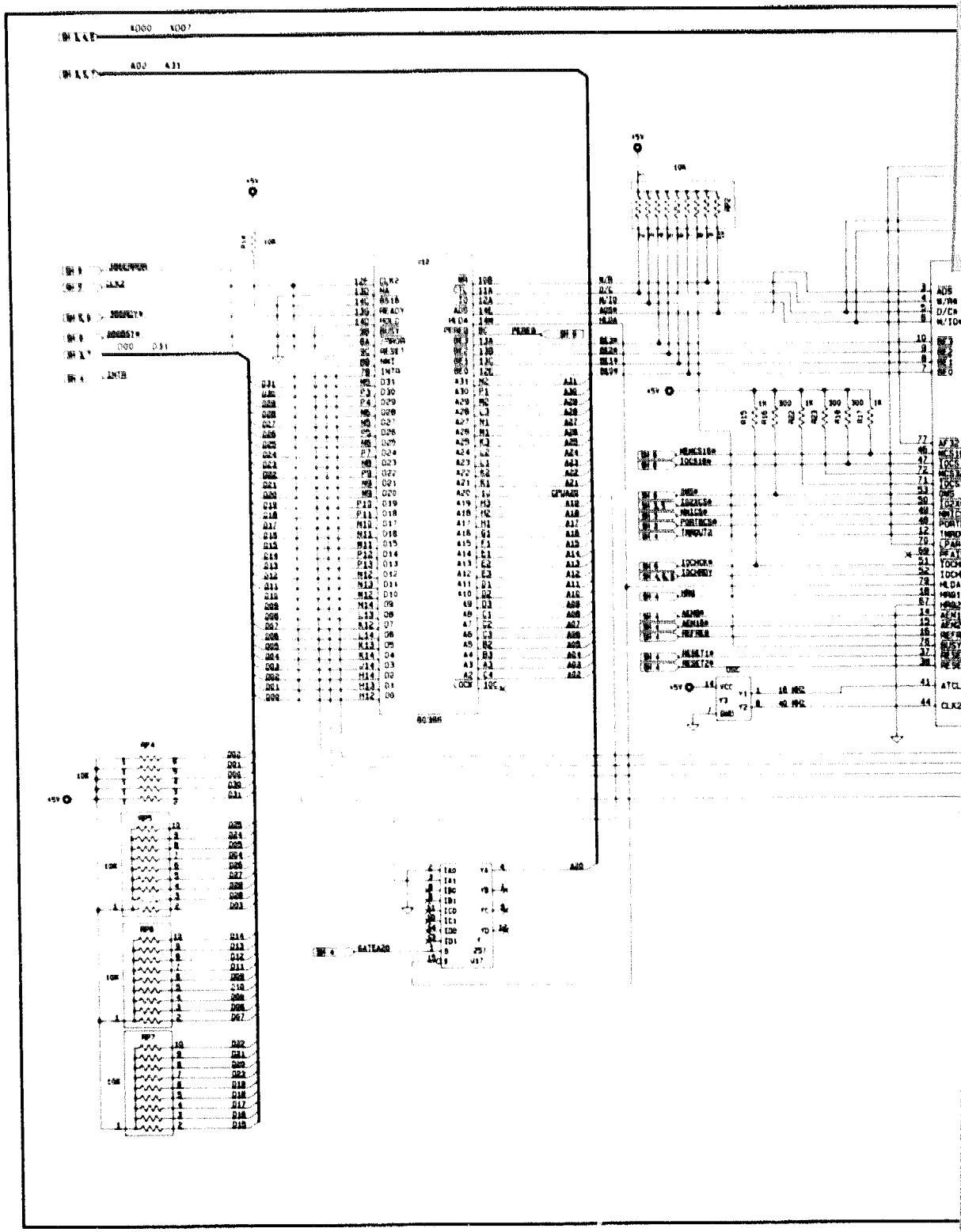
D

1 OF

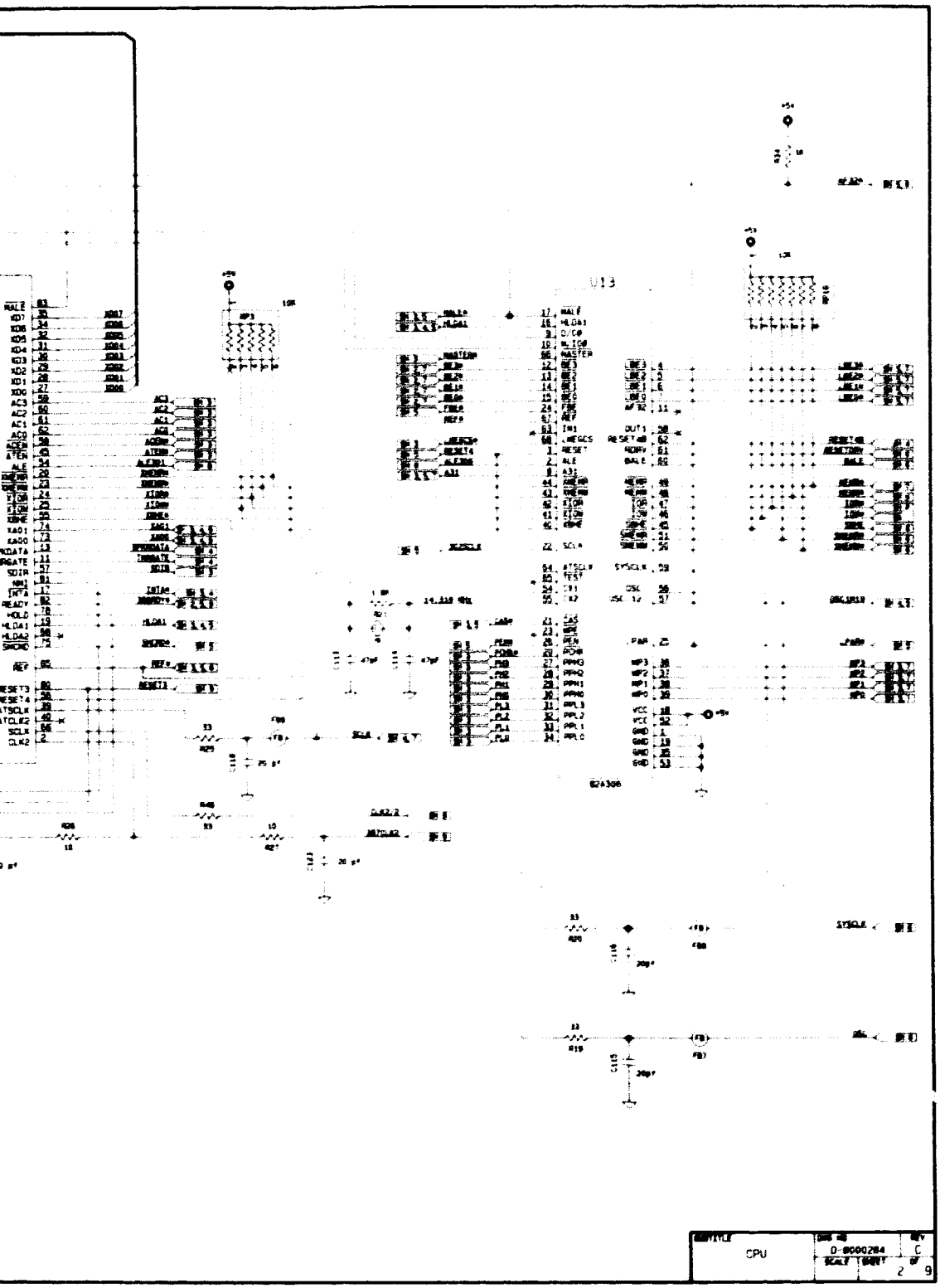


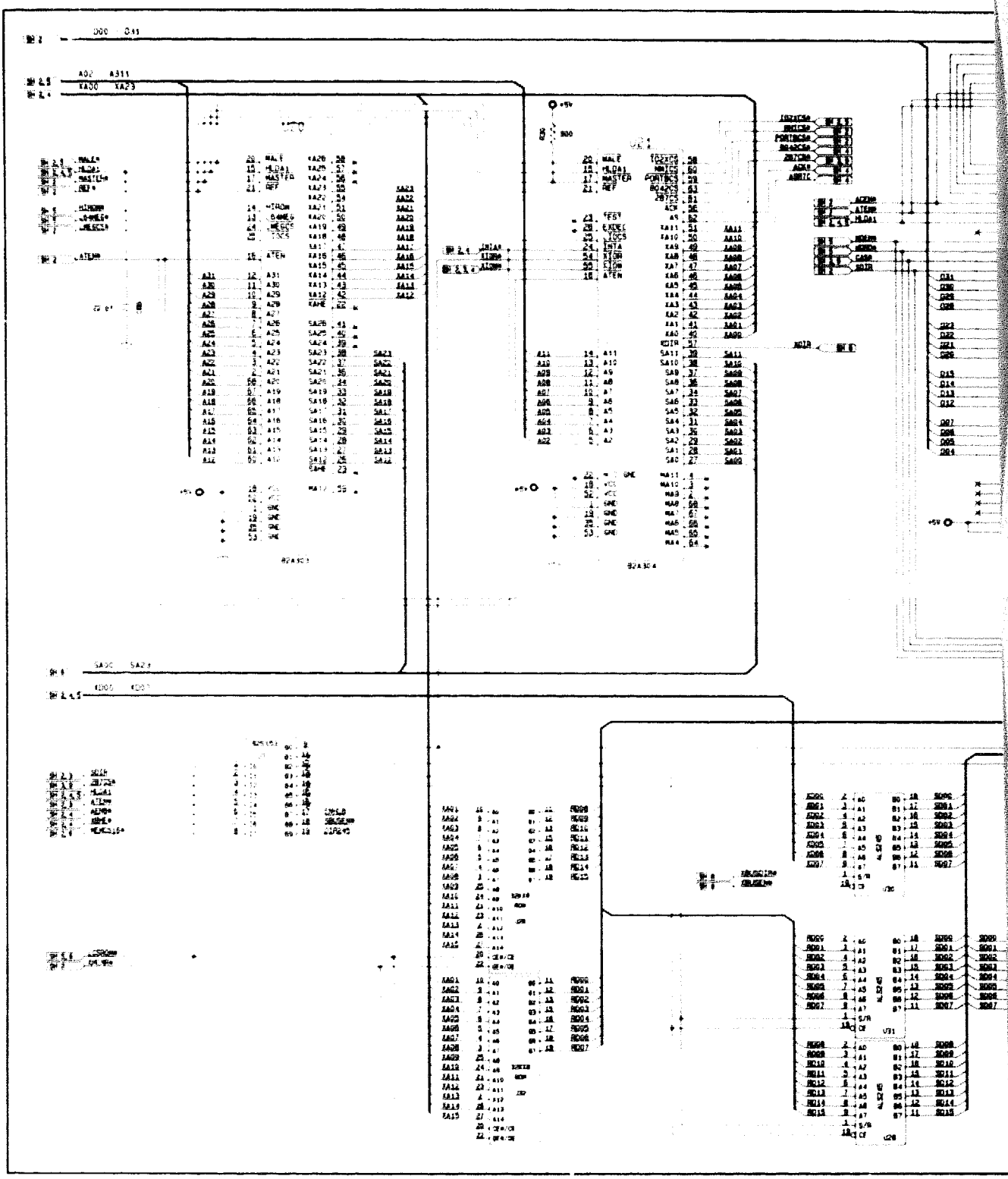
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14.318 MHZ
82A306
CONTROL
BUFFER
82A303
HIGH
ADDRESS
BUFFER
82A304
LOW
ADDRESS
BUFFER
SA00-SA23
XA00 XA23
PERIPHERAL
CONTROL BUS
SPEAKER
82C206
INTEGRATED
PERIPHERALS
CONTROLLER
3.6 V
BATTERY
1.44 MEG
1.44 MEG
SD00-SD07
CPU SPEED 20/8 MHZ PROGRAMMABLE
BUS SPEED 10/8 MHZ PROGRAMMABLE
SYSTEM CLOCK 40 MHZ
BUS CLOCK 14.31818 MHZ
FDC CLOCK 16/8.8 MHZ
FLOPPY DISK DATA RATE 250/300/500 KBITS/SEC
KEYBOARD CONTROLLER CLOCK 10 MHZ
KEYBOARD DATA RATE 9.6 KBITS/SEC
A ADDED 10K RESISTORS TO IRQ LINES ON BUS
ADDED BYPASS CAPACITOR TO IRQ
ADDED JUMPERS FROM +5V TO U80-1, U32-1
REFERENCE TCO # 13235
9-27-87
B ADDED 80387 SUPPORT LOGIC REMOVED 80287
10-26-87
C ARTWORK CORRECTED FOR PRODUCTION RELEASE
12-29-87
THIS IS A CAD GENERATED DOCUMENT
- DO NOT REVISE MANUALLY
R.H. Thompson 12-29-87
R.H. Thompson 12-29-87
SCHEMATIC -
MAIN LOGIC BOARD
TANDY
D- 8000284 C
1 OF 9

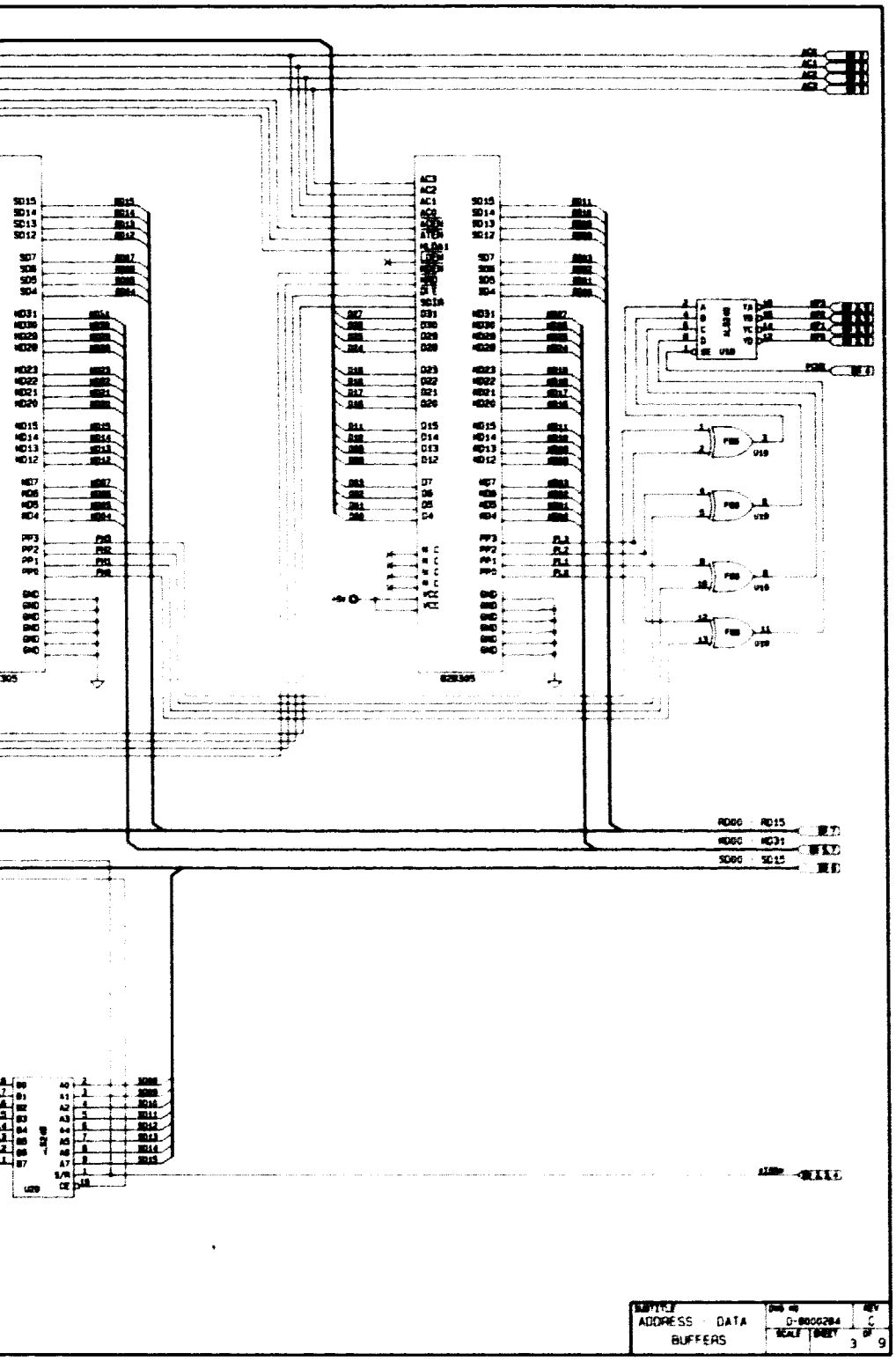


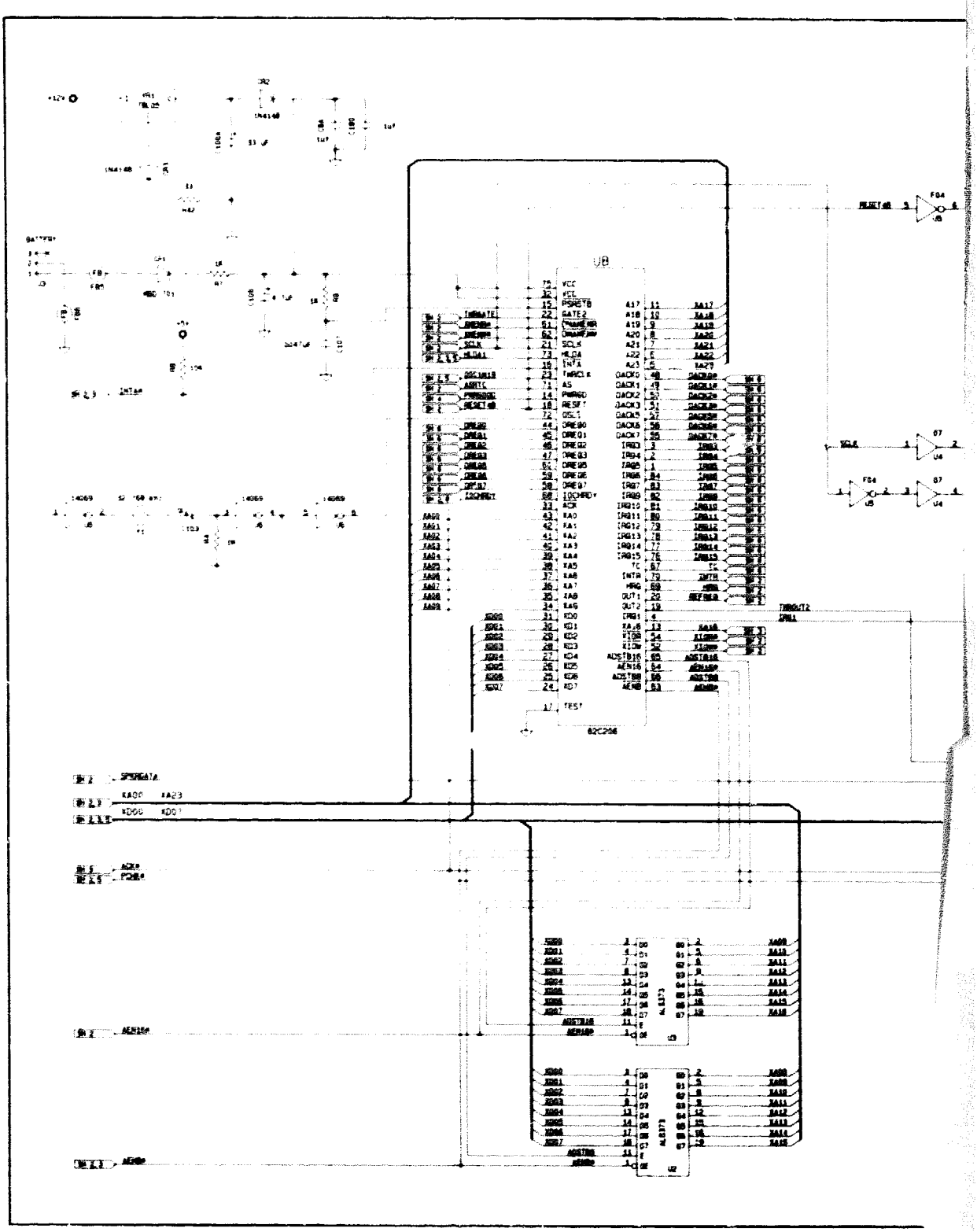
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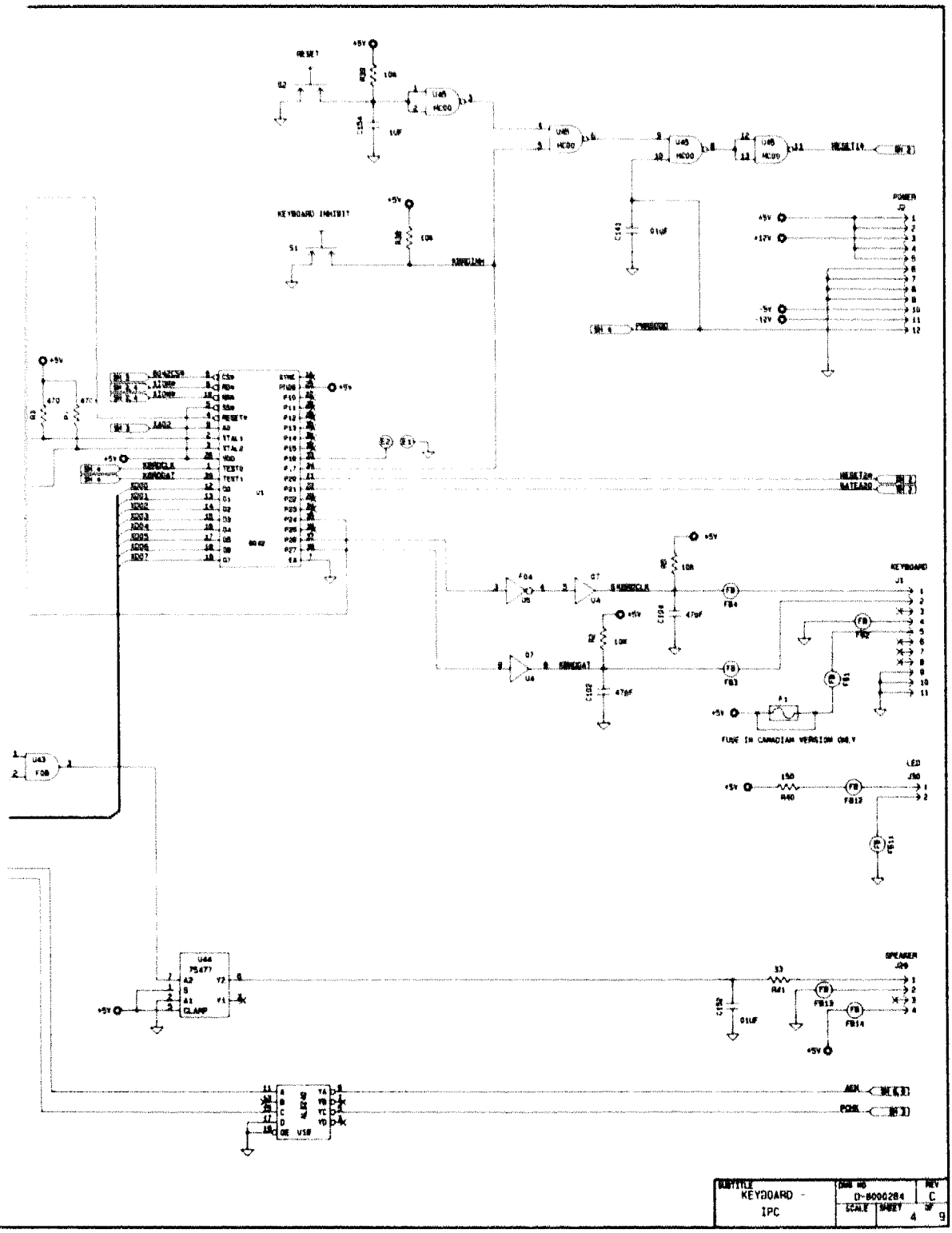


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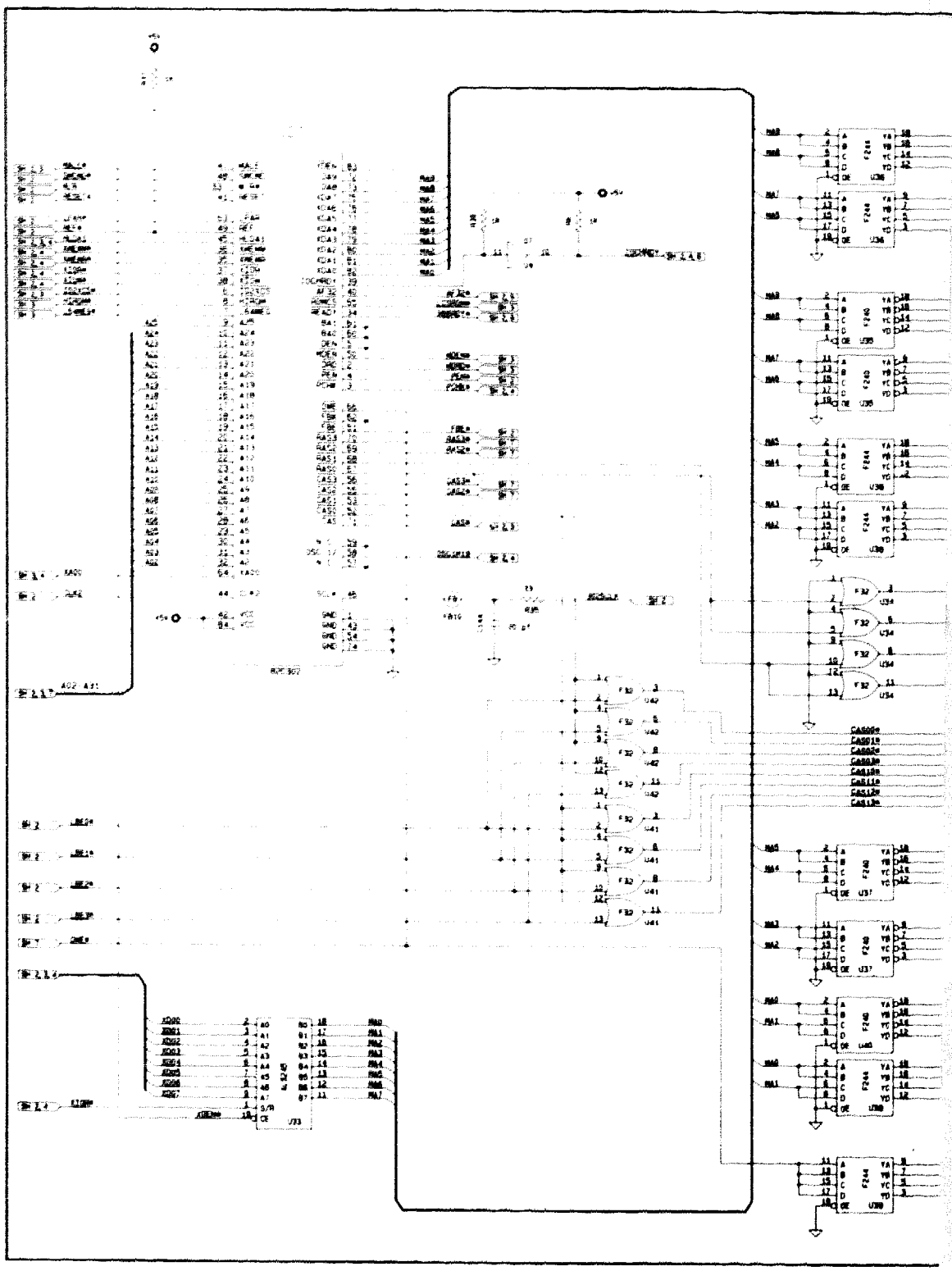

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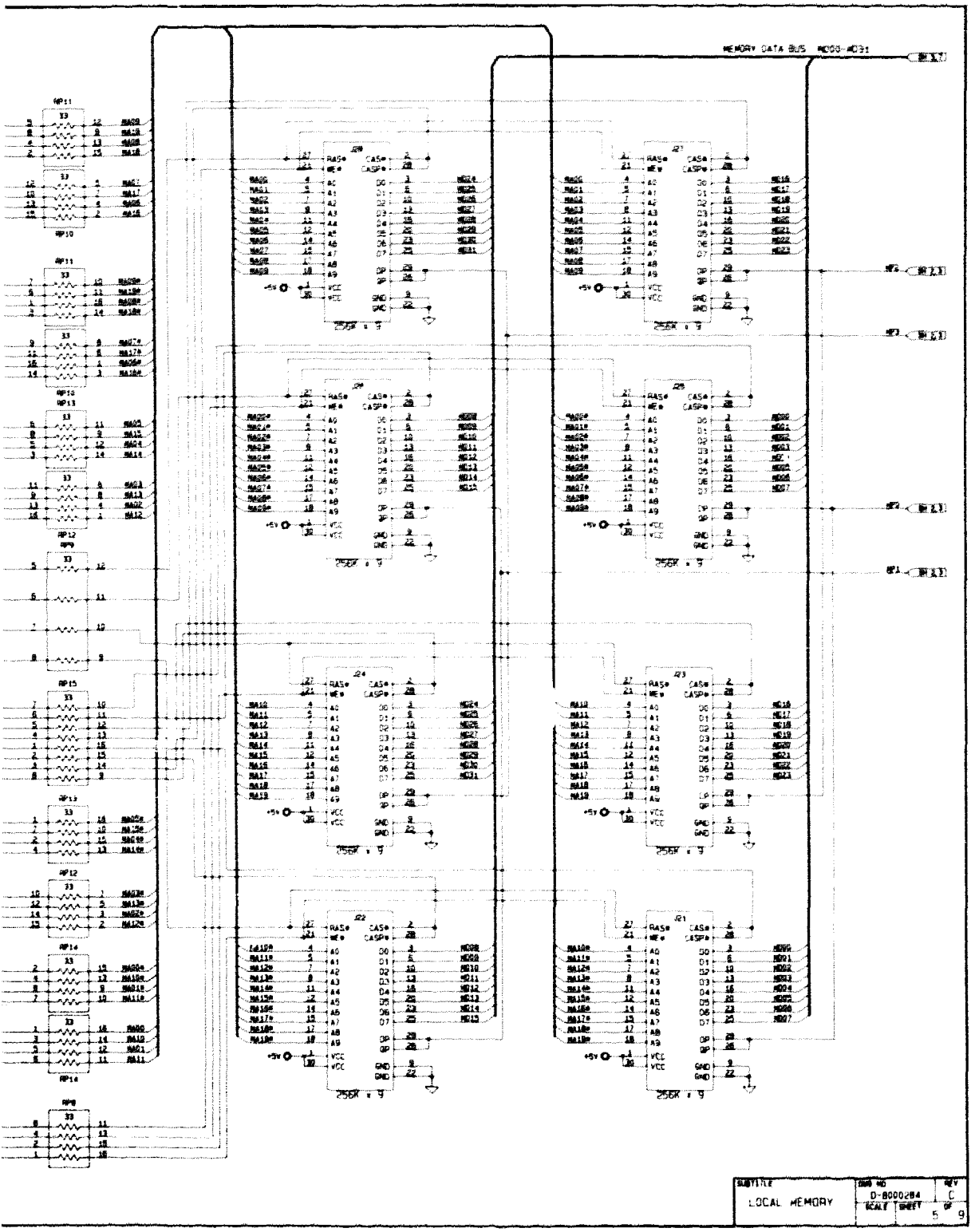
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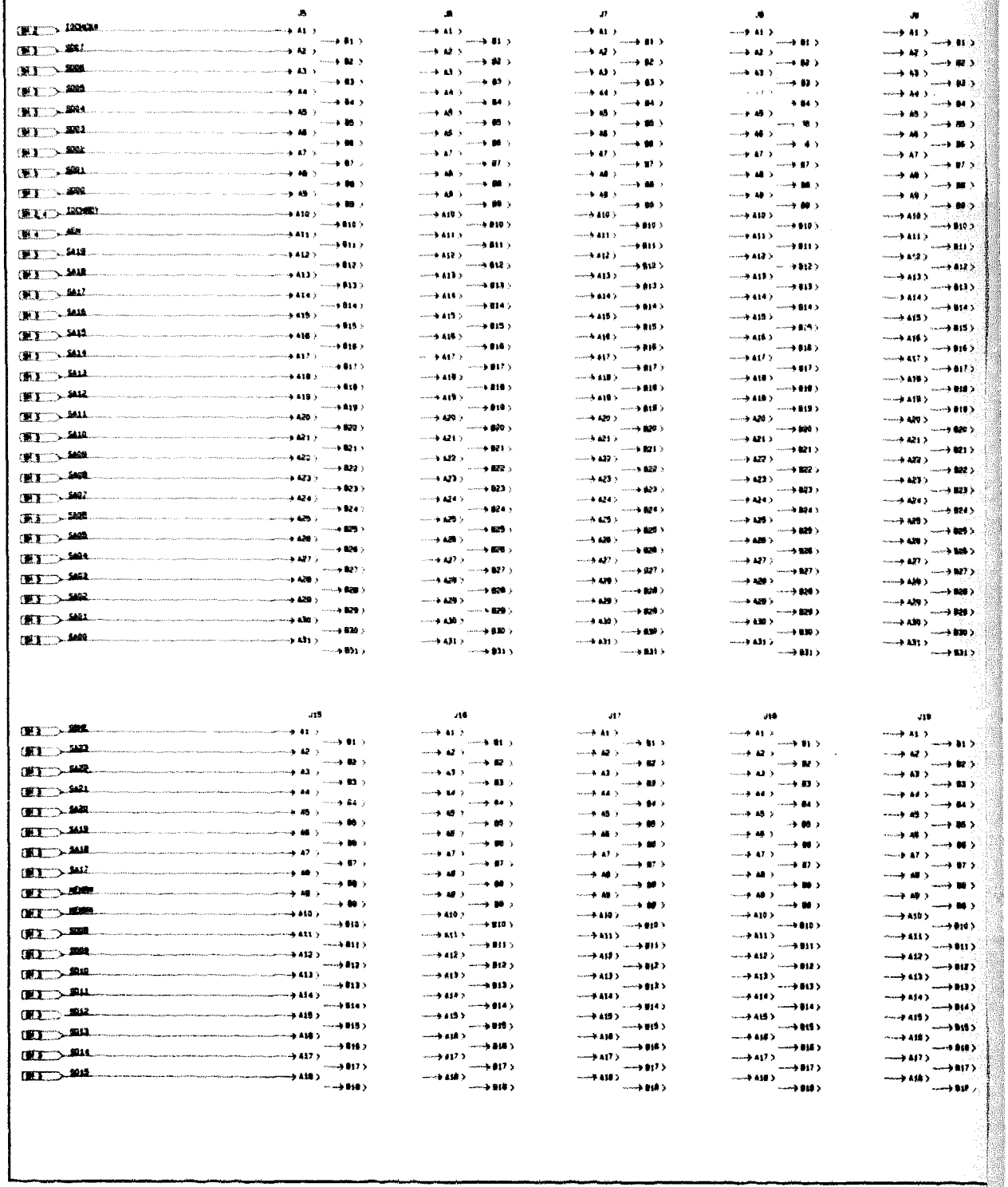
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KEYBOARD - IPC	0-8000284	C
	SCALE	SHEET 4 OF 9



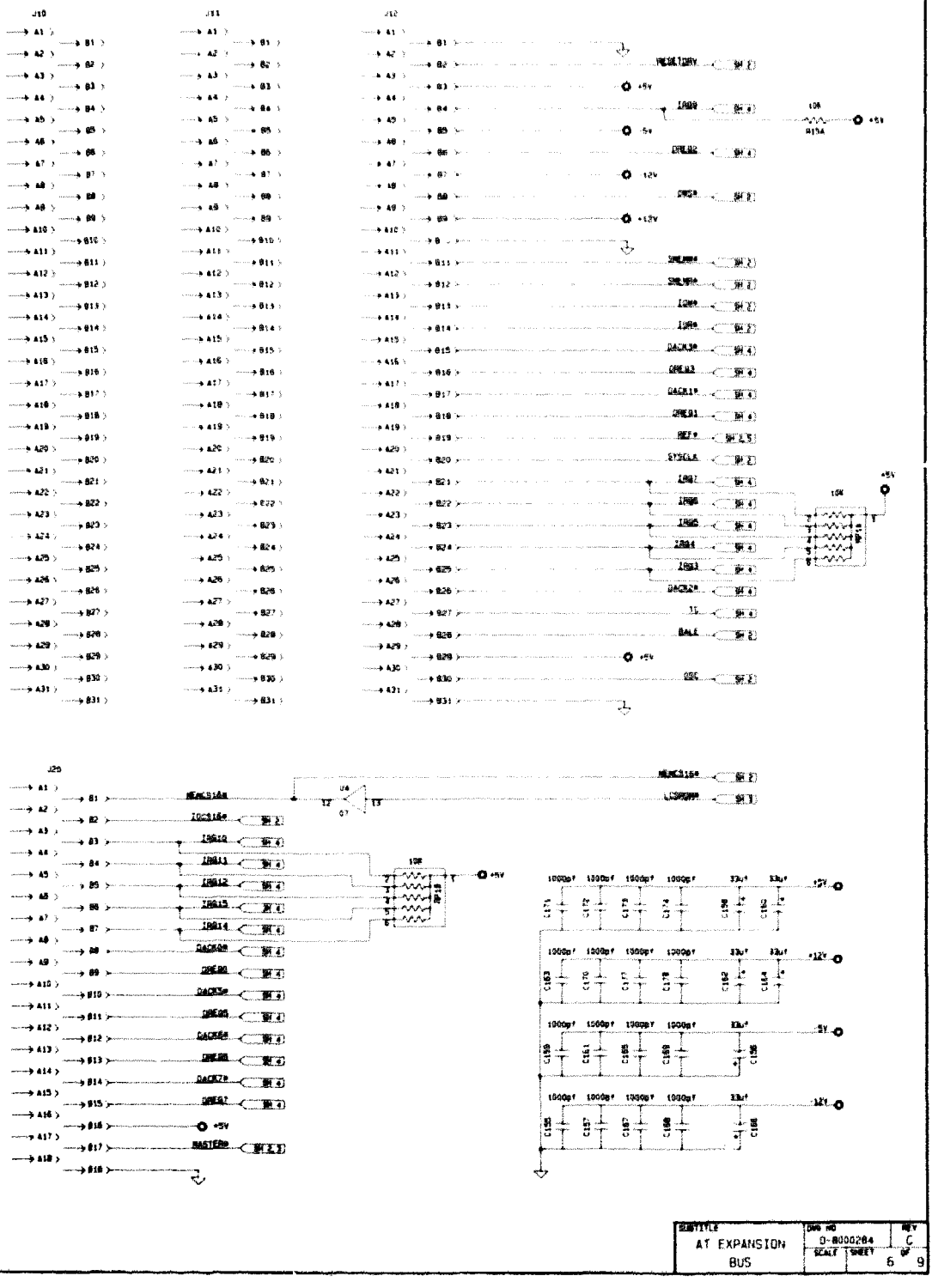
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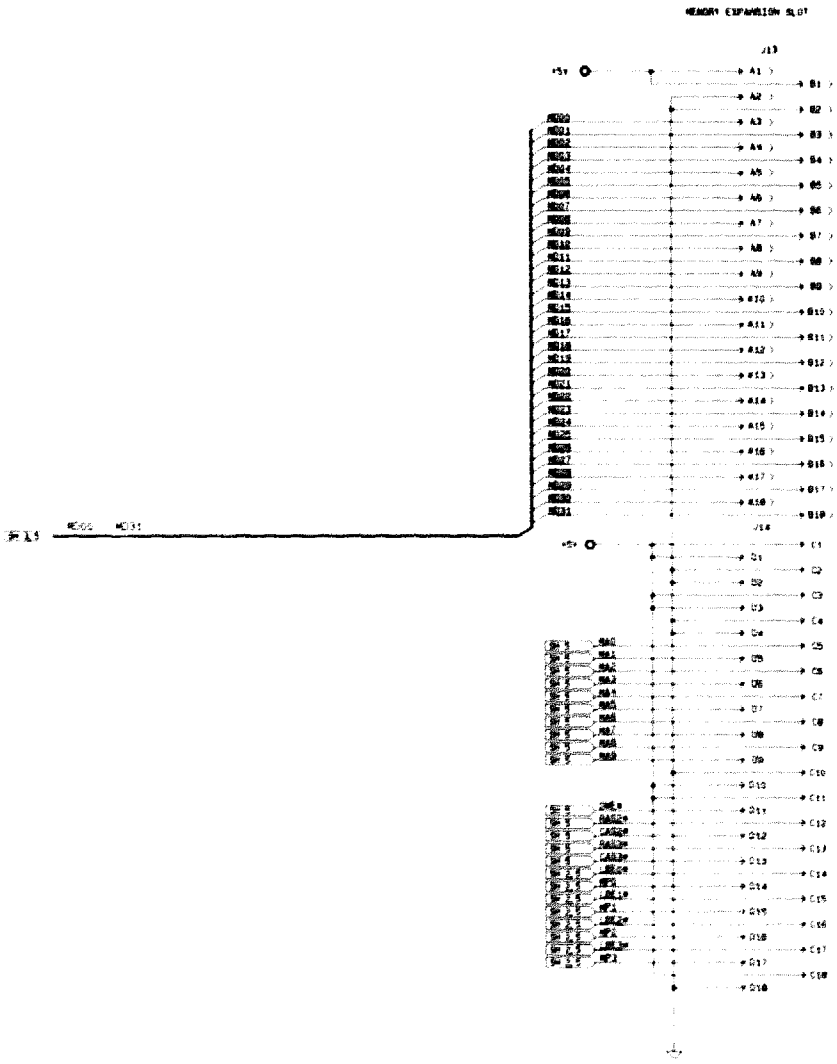
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LOCAL MEMORY	D-8000284	C
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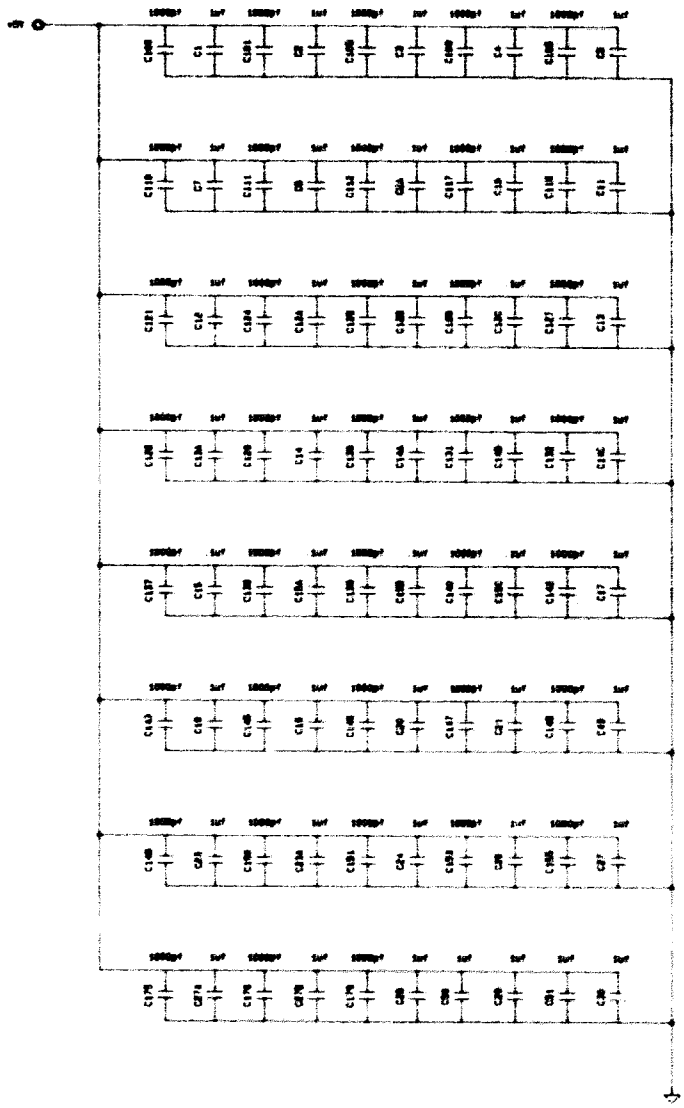
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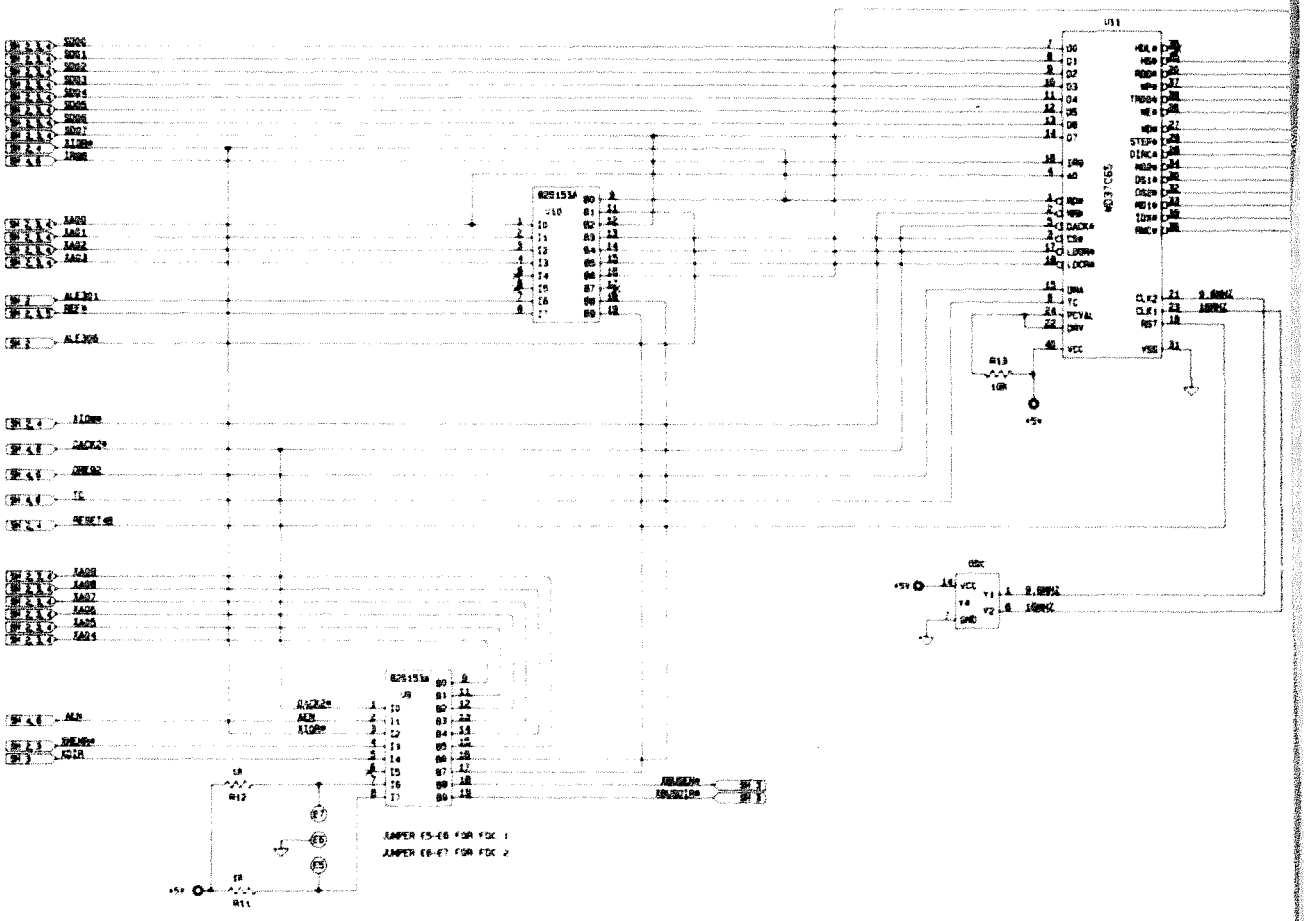
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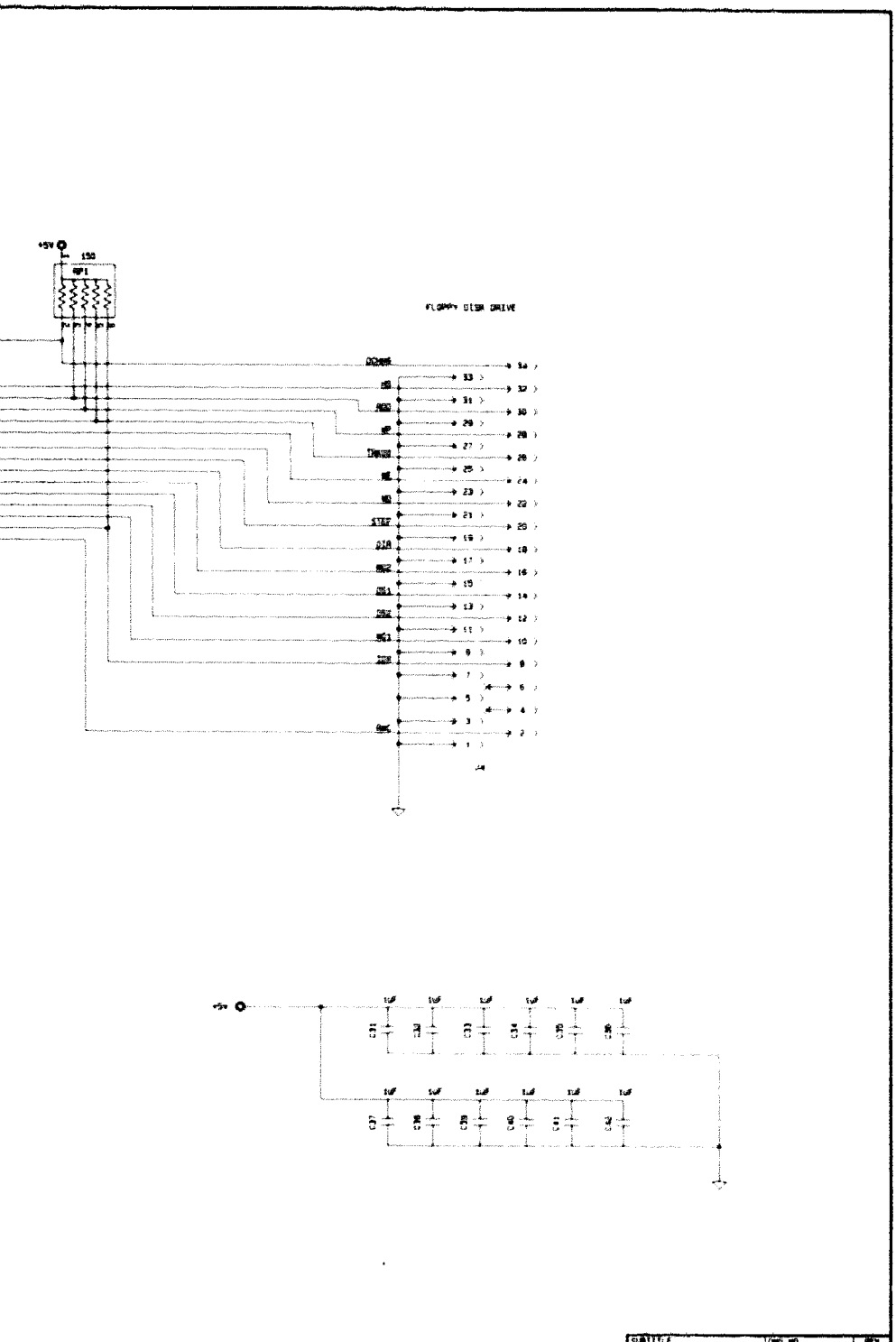


EXPANSION MEMORY BUS	D-0000284	C
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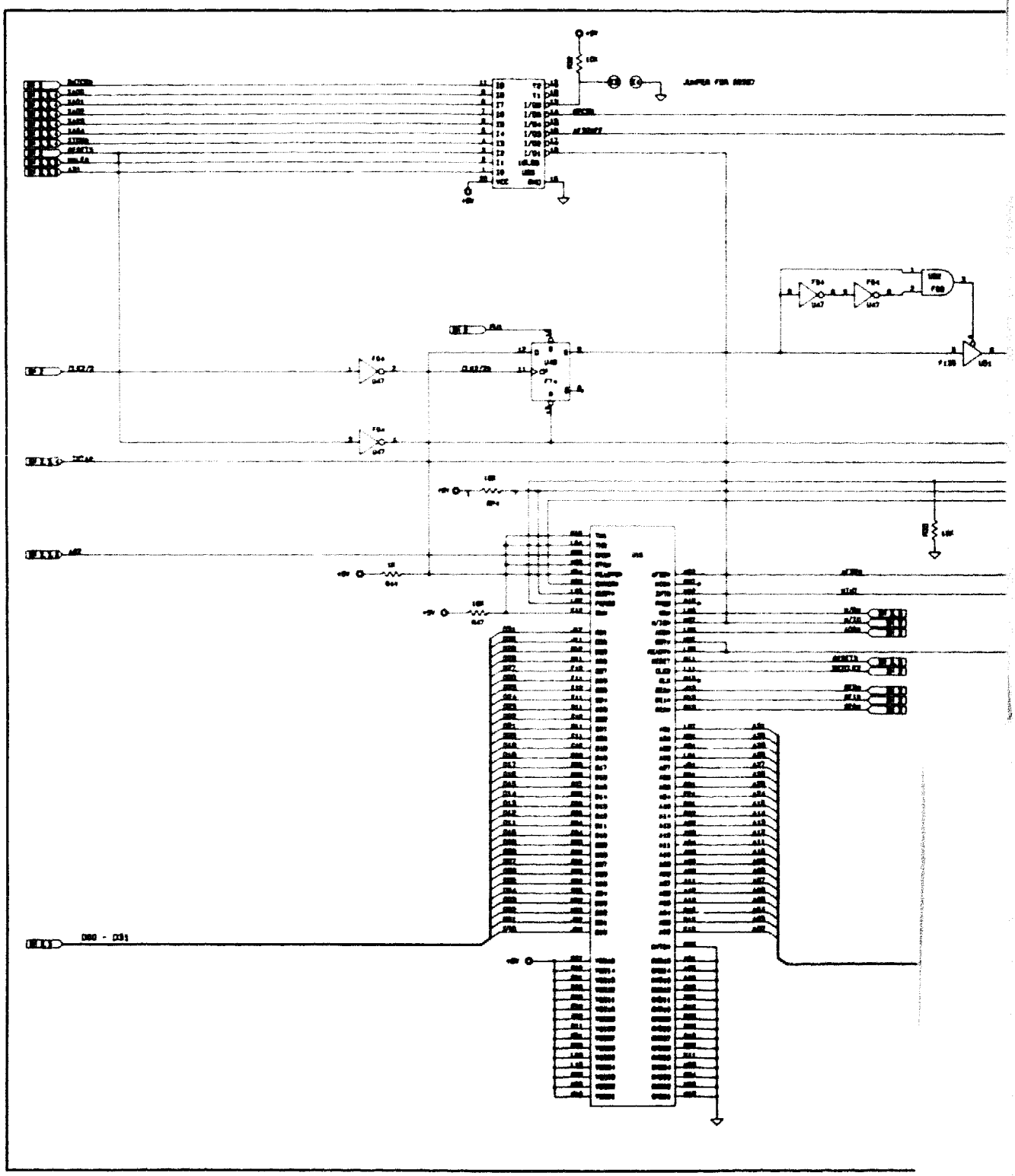


JUMPER E5-E6 FOR FDC 1
JUMPER E6-E7 FOR FDC 2

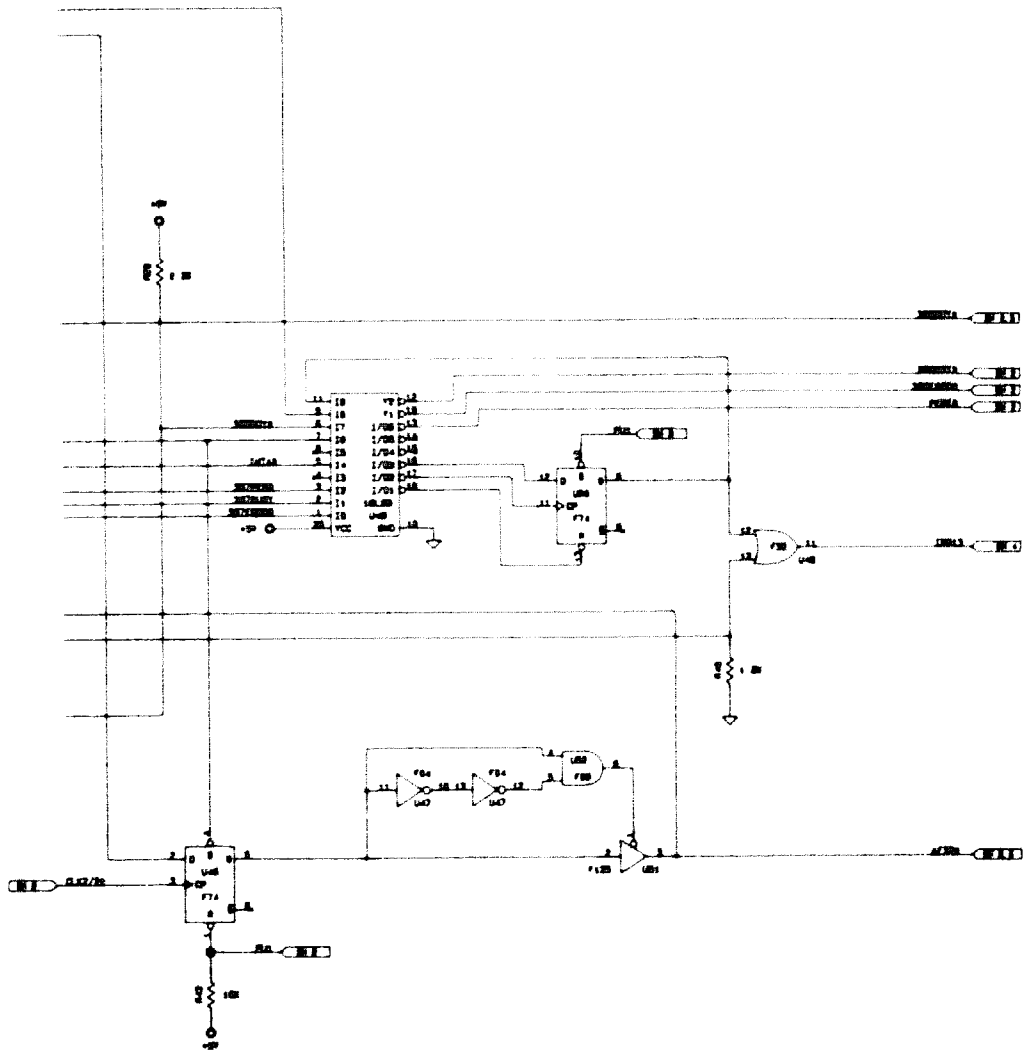
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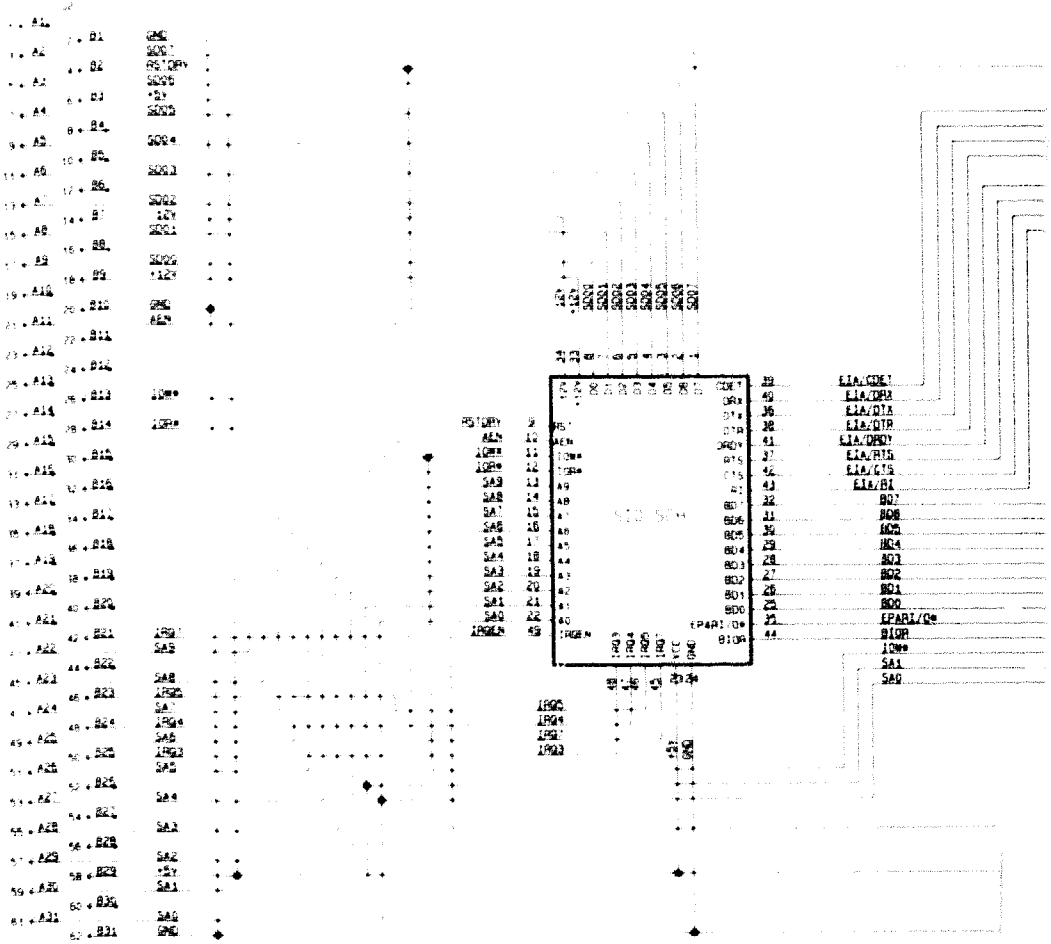


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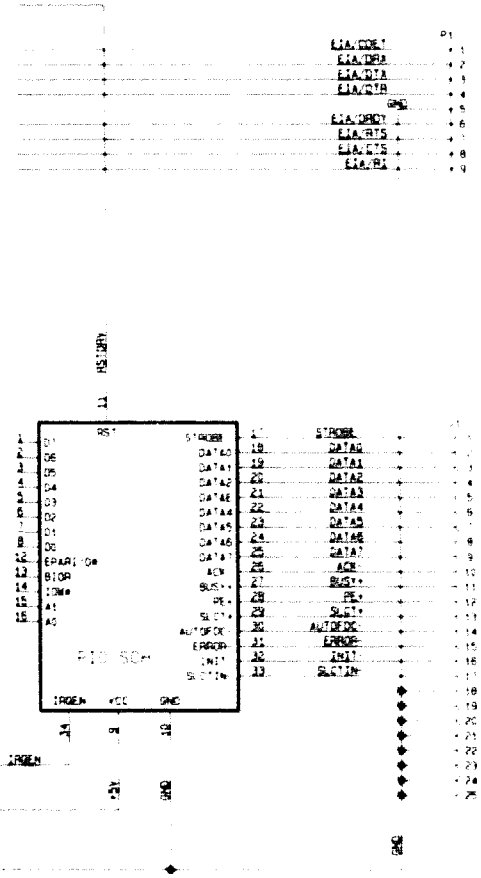
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CO-PROCESSOR INTERFACE	D-8000304	C
	SCALE	SHEET 9 OF 9

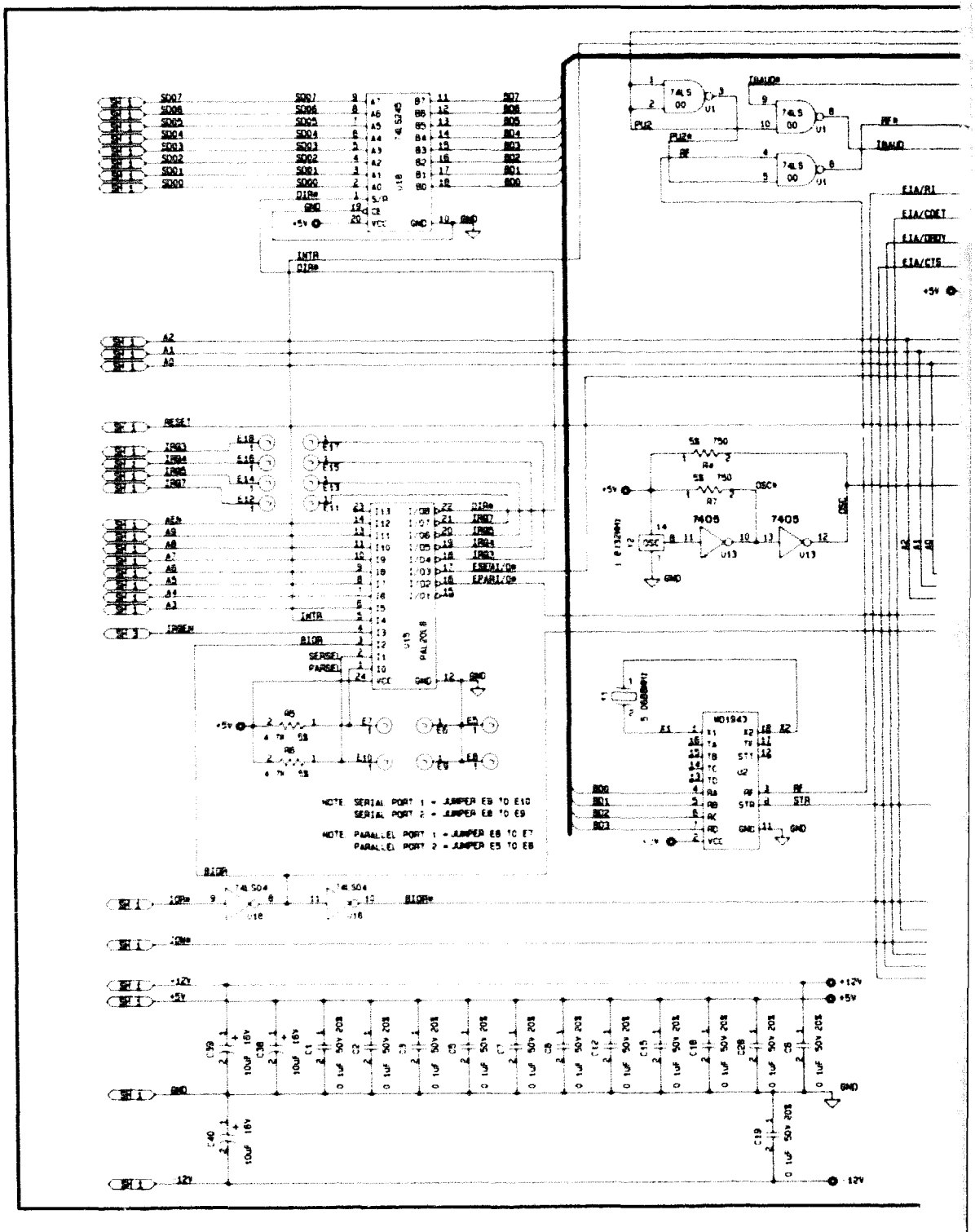


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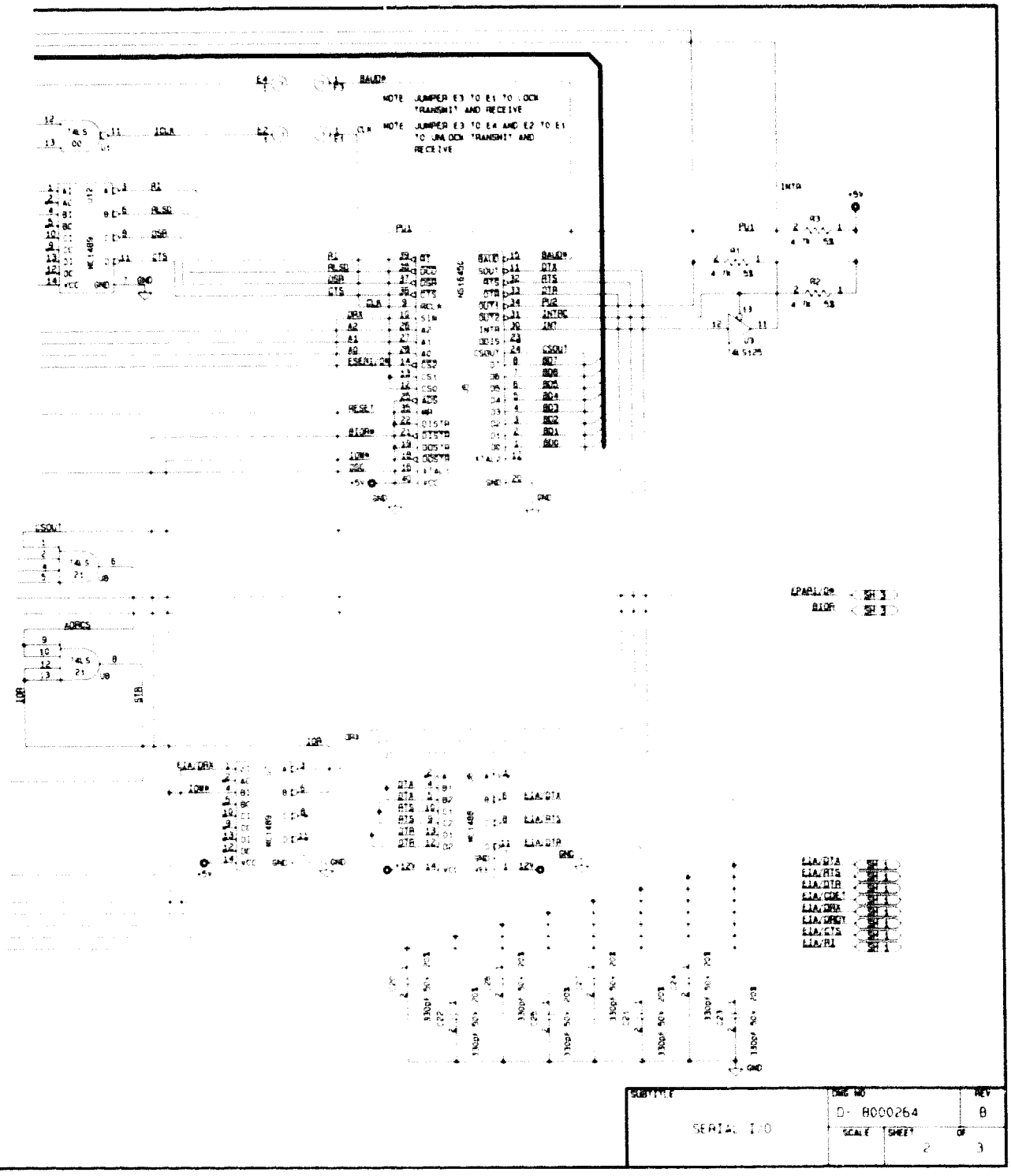
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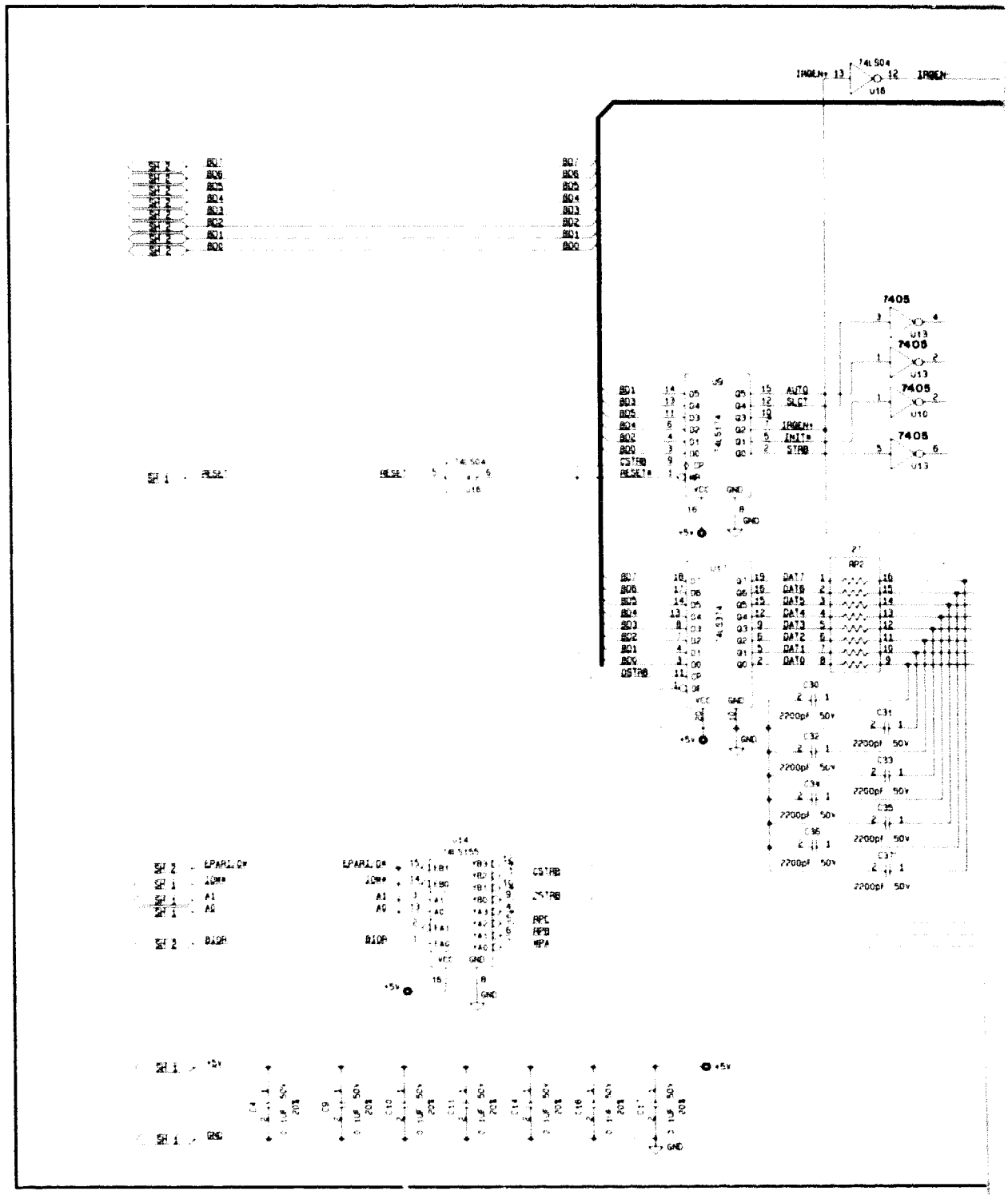


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629	TANDY		DWG NO 0- 8000264
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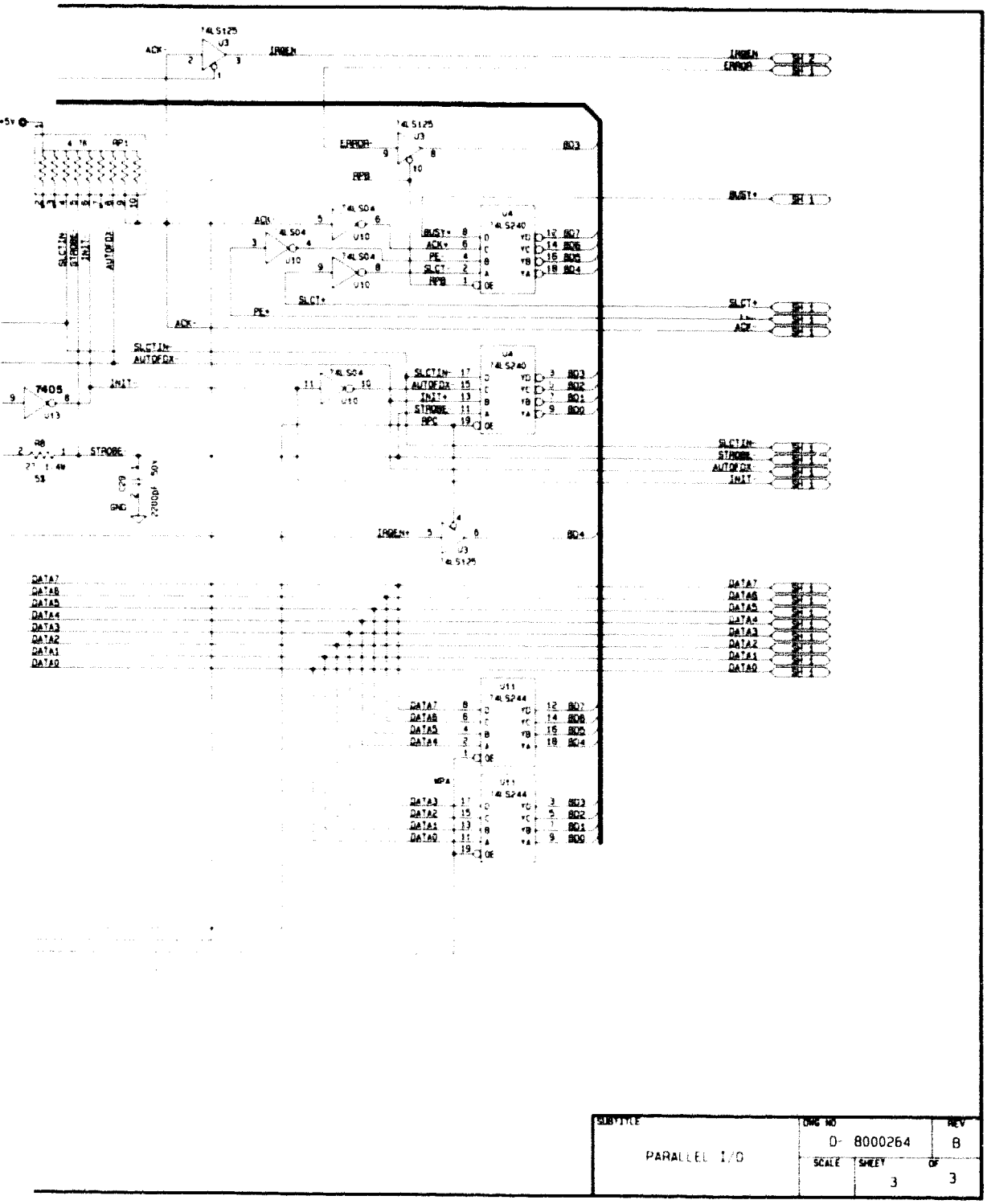


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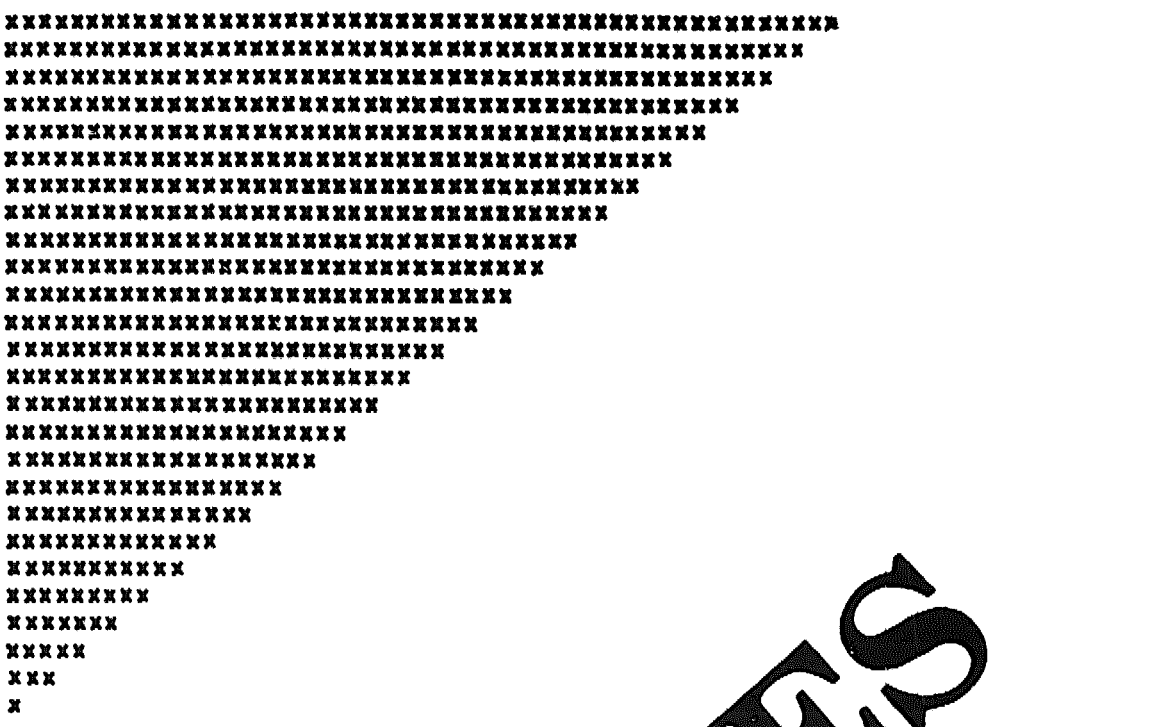

NOTE JUMPER E3 TO E1 TO LOCK TRANSMIT AND RECEIVE
NOTE JUMPER E3 TO E4 AND E2 TO E1 TO UNLOCK TRANSMIT AND RECEIVE
BAUD9
INTR
+5V
GND
PU1
RI
RLSD
DSR
CTS
DCD
DTR
RTS
BAUD9
SOUT
INTR
CSOUT
ESERIAL_IRQ
RESET
BIOR
IOW
IOR
SIR
ADRCS
LPARALOR
BIOR
LIA/DTA
LIA/RTS
LIA/DTR
LIA/CDET
LIA/DRX
LIA/DRDY
LIA/CTS
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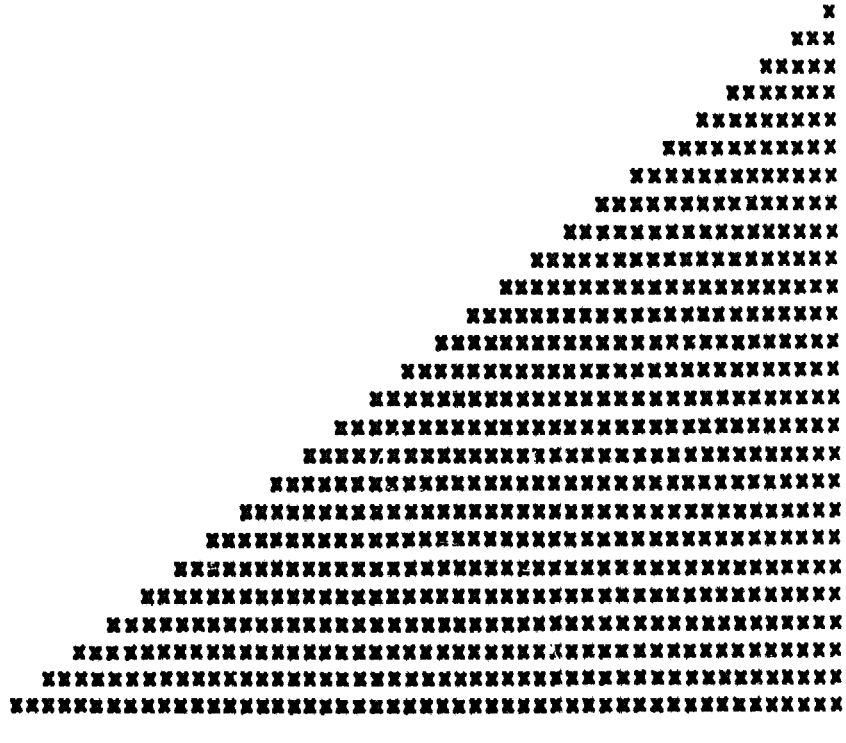
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SUBTITLE	DWG NO	REV
PARALLEL I/O	D- 8000264	B
	SCALE	SHEET 3 OF 3



DEVICES



82C206
INTEGRATED PERIPHERALS CONTROLLER

- **100% Compatible to IBM™ PC AT**
- **Fully compatible to Intel™'s 8237 DMA controller, 8259 Interrupt controller, 8254 Timer/Counter, and Motorola™'s 146818 Real Time Clock**
- **Offers 7 DMA channels, 13 Interrupt request channels, 2 Timer/Counter channels, and a Real Time Clock**
- **Reduced recovery time (120 ns) between control**
- **114 bytes of CMOS RAM memory**
- **8 MHz DMA clock with programmable internal divider for 4 MHz operation**
- **Programmable wait states for the DMA cycle**
- **16 Mbytes DMA address space**
- **Single chip 84-pin CMOS implementation**

The 82C206 Integrated Peripheral Controller incorporates two 8237 DMA controllers, two 8259 Interrupt controllers, one 8254 Timer Counter, one MC146818 Real Time Clock, 74LS612 memory mapper, in addition to several other TTL SSI interface logic chips to offer a single chip integration of all the peripherals attached to the peripheral bus (X-Bus) in the IBM™ PC AT™. While offering a complete compatibility to the IBM PC AT architecture, the chip offers enhanced features and improved speed performance. These include an additional 64 bytes of user RAM for the Real Time Clock, and drastically reduced recovery specifications for the 8237, 8259 and 8254. Variable wait state option is provided for the DMA cycles. Programmable delays are provided for the CPU access to the internal registers of the chip. The chip also provides an option to select 8 or 4 MHz system clock.

The 82C206, along with the CS8220 PC AT Compatible CHIPSet, provides a highly integrated high performance solution for a PC AT compatible implementation.

The 82C206 is implemented using advanced CMOS technology and is packaged in an 84-pin PLCC.

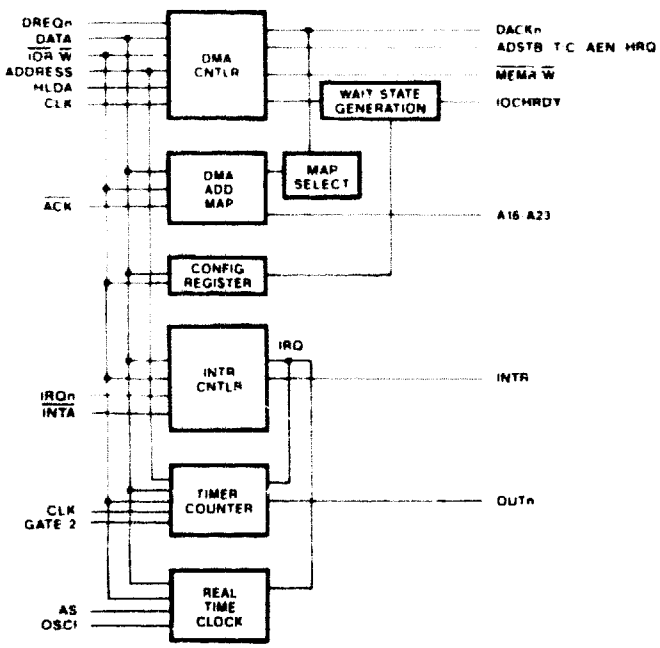
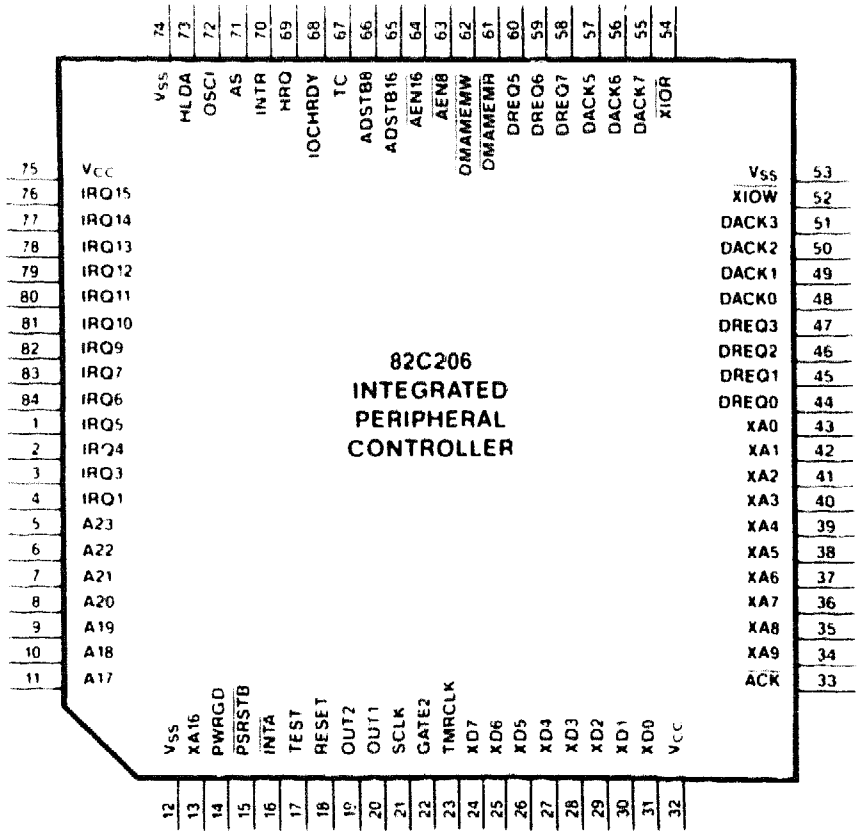


Figure 1. 82C206 Integrated Peripheral Controller Block Diagram

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82C206
INTEGRATED
PERIPHERAL
CONTROLLER
74 VSS
73 HLDA
72 OSCI
71 AS
70 INTR
69 HRQ
68 IOCHRDY
67 TC
66 ADSTB8
65 ADSTB16
64 AEN16
63 AEN8
62 DMAMEMW
61 DMAMEMR
60 DREQ5
59 DREQ6
58 DREQ7
57 DACK5
56 DACK6
55 DACK7
54 XIOR
75 VCC
76 IRQ15
77 IRQ14
78 IRQ13
79 IRQ12
80 IRQ11
81 IRQ10
82 IRQ9
83 IRQ7
84 IRQ6
1 IRQ5
2 IRQ4
3 IRQ3
4 IRQ1
5 A23
6 A22
7 A21
8 A20
9 A19
10 A18
11 A17
12 VSS
13 XA16
14 PWRGD
15 PSRSTB
16 INTA
17 TEST
18 RESET
19 OUT2
20 OUT1
21 SCLK
22 GATE2
23 TMRCLK
24 XD7
25 XD6
26 XD5
27 XD4
28 XD3
29 XD2
30 XD1
31 XD0
32 VCC
53 VSS
52 XIOW
51 DACK3
50 DACK2
49 DACK1
48 DACK0
47 DREQ3
46 DREQ2
45 DREQ1
44 DREQ0
43 XA0
42 XA1
41 XA2
40 XA3
39 XA4
38 XA5
37 XA6
36 XA7
35 XA8
34 XA9
33 ACK

82C206 Pin Description

Pin No.	Name	Type	Function
24-31	XD7-XD0	I/O	DATA BUS The Data Bus lines are 3-state bi-directional lines connected to the system data bus (XD bus in a PC/AT design) The outputs are enabled in the program condition during the I/O Read to output the contents of the DMA controller registers (Address register, Status register, the Temporary register or a Word Count register), the three Interrupt Controller registers (Interrupt Request register, In Service register and the Interrupt Mask register), the Timer/Counters registers (namely the contents of these counters or states of the counters), the Real Time Clocks internal registers and page registers of memory mapper During an I/O write cycle, the outputs are disabled and the CPU can program the DMA Controller registers, the Interrupt Controller registers, the Timer/Counters registers, the DMA Page register and the Real Time Clock registers and internal RAM During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB8 or ADSTB16. During memory-to-memory operations, data from the memory comes into the DMA Controller on the data bus during read from the memory. In the write to memory transfer, the data bus outputs place the data into the new memory location During the interrupt sequence, the interrupt controllers output the interrupt vector byte on the data bus Data bus XD7-XD0 also acts as the multiplexed address/data bus for the Real Time Clock

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
35-43 34	XA8-XA0 XA9	I/O I	ADDRESS BUS. This is the system address bus used to address various registers of the 82C206. It is tied to the external bus (XA bus) in a PC/AT compatible design. During a non-DMA cycle, A3-A0 act as inputs and are used by the CPU to address the registers of the DMA Controller corresponding to DMA channels 0-3 and A4-A1 address the registers of the DMA Controller corresponding to DMA channels 5-7. In the active DMA cycle, A7-A0 are outputs and carry address information for DMA channels 0-3. Correspondingly, A8-A1 are address outputs for 16 bit DMA channels 5-7. During program condition, A9-A0 are used to address configuration register and the internal registers of DMA Controller, INT Controller, Timer, RTC and Memory Mapper.
18	RESET	I	RESET. Reset is active high input which affects the following registers. DMA Controllers: Clears the Command, Status, DMA Request, Temporary register, First/Last flip-flop, sets the Mask register. Following reset, the DMA controller is in an idle state. INTERRUPT Controllers: Clears the edge sense circuit, the interrupt mask register, all ICW4 functions, IRQ0 is assigned highest priority, slave address is set to 7, special mask mode is disabled and status read is set to IRR.
54	XIOR	I/O	I/O READ. I/O Read is a bidirectional active low three-state line. In an idle cycle (non DMA, non-interrupt), it is an input control signal used by the CPU to read the 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to access data from a peripheral during a DMA write transfer.
52	XIOW	I/O	I/O WRITE. I/O Write is a bidirectional active low three-state signal. In an idle cycle (non-DMA, non-interrupt) it is an input control signal used by the CPU to load information to the 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to load data to the peripheral during a DMA Read transfer.
61	DMAMEMR	O	DMA MEMORY READ. DMAMEMR is an active low three-state output used to access data from the selected memory location during DMA Read or memory-to-memory transfer.

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
62	DMAMEMW	O	DMA MEMORY WRITE. DMAMEMW is an active low three-state output used to write data to the selected memory location during DMA write or a memory-to-memory transfer. In a PC/AT compatible design, this signal is connected to XMEMW.
21	SCLK	I	CLOCK INPUT. The Clock Input is used to generate the timing signals which control DMA operations. This input may be driven from DC to 10 MHz. The Clock may be stopped in either state for standby operation. The internal clock used for DMAC is either the SCLK or SCLK/2 depending on the setting of DMA CLOCK SELECT bit in the configuration register.
68	IOCHRDY	I/O	I/O CHANNEL READY. In the input mode, a low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA Clock cycle will elapse before internal DMA Ready goes up. This signal is used to extend memory read and write pulses for the DMA controllers to accommodate slow memories or I/O devices. IOCHRDY must satisfy set-up and hold times with respect to DMACLK in order to work reliably. In the output mode, this pin is an open drain output and provides an active low output whenever any 82C206 register is addressed for read or write. This output will remain low for a programmed number of DMACLK cycles (as configured by bits 6 and 7 of 82C206 configuration register) and then goes high, if pulled up by an external register. IOCHRDY provides a means of introducing a programmed number of wait-states (as counted by DMACLK cycles) for I/O read/write cycles to 82C206. In a PC/AT architecture based design this pin should be wire-ored to PC/AT's IOCHRDY signal.
73	HLDA	I	HOLD ACKNOWLEDGE. The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
44-47 60-58	DREQ0-DREQ3 DREQ5-DREQ7	I	DMA REQUEST. The DMA Request (DREQ) are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O and 8 or 16-bit system memory. DREQ5-DREQ7 support 16-bit data transfers between 16-bit peripheral and 16-bit system memory. DREQ4 is not available as it is used to cascade DREQ0-DREQ3.
67	TC	O	TERMINAL COUNT. Terminal Count (TC) is an active high signal. Information concerning the completion of DMA services is available at the TC output pin. A pulse is generated by the DMA Controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs. When a TC pulse occurs, the DMA Controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
69	HRQ	O	HOLD REQUEST. The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA Controller issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the DMA Controller always controls the busses, HRQ may be tied to HLDA. This will result in one SO state before the transfer.
48-51 57-55	DACK0-DACK3 DACK5-DACK7	O	DMA ACKNOWLEDGE. DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to be active low.
66	ADSTB8	O	ADDRESS STROBE. This is an active high signal used to control latching of the upper address byte (A8-A15) for 8-bit peripherals. It will drive directly the strobe input of external transparent octal latches. During block operations, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB8 is active for DMA channels 0-3.
64	AEN16	0	ADDRESS ENABLE for 16-BIT DMA TRANSFERS. This signal enables the 8-bit latch containing the upper 8 address bits (A9-A16) on to system address bus. It is inactive when external bus master controls the system bus (MASTER=0). This signal is active low.
65	ADSTB16	O	ADDRESS STROBE for 16-BIT TRANSFERS (channels 5-7). This is an active high signal used to control latching of the upper address byte A9-A16 for 16-bit DMA transfers. Its function is just like ADSTB8.
63	AEN8	O	ADDRESS ENABLE for 8-BIT DMA TRANSFERS. This signal is the output enable for the 8-bit latch containing upper 8 address bits (A8-A15). It enables A8-A15 system address bus. It is inactive when external bus master controls the system bus (MASTER=0). This signal is active low.

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
33	ACK (MSE)	I	MODULE SELECT ENABLE. When high, it enables the chip select function on one of the modules (DMA Controller, INT Controler, TIMER, RTC, DMA Page register or the Configuration register) for the programming function, i.e. CPU read or write of the command, status or other register of various modules of the 82C206. When low, the 82C206 is essentially disconnected from the system bus. The 82C206 at this time could be performing an active DMA or an interrupt cycle. In a PC/AT compatible design, this pin is tied to ACK signal.
11-5 13	A23-A17 XA16	O O	DMA PAGE REGISTER ADDRESS. XA16 and A17-A23 are 3-state output pins. XA16 is the least significant bit of the DMA page register and is used for DMA transfers for 8-bit peripherals only (channel 0-3). XA16 is not used for DMA transfers to 16-bit peripherals (channel 5-7) as XA9-XA16 is provided by demultiplexing the data bus. A17-A23 are the upper 7 bits of the DMA page register.
76-82 83, 84 1-3 4	IRQ15-IRQ9 IRQ7, IRQ6 IRQ5-IRQ3 IRQ1	I I	INTERRUPT REQUESTS. Asynchronous inputs. An interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge triggered mode) or just a high level on an IRQ input (level triggered mode).
16	INTA	I	INTERRUPT ACKNOWLEDGE. This pin is used to enable the interrupt controllers interrupt vector data on to the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
70	INTR	O	INTERRUPT. This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, and is usually connected to the CPU's interrupt pin.
23	TMRCLK	I	TIMER CLOCK. Clock input for Counter 0, Counter 1 and Counter 2.
22	GATE2	I	GATE 2. Gate input for Counter 2. In a PC/AT compatible design, the Counter 2 is used for tone generation for speaker. In this design, the GATE 2 input is driven by Bit 0 of I/O Port 61H (called TIM2GATE SPK).
20	OUT1	O	OUT 1. Output of Timer 1. In a PC/AT compatible design, Timer 1 is programmed as a rate generation to produce 15 μsec period signal used for interrupt request for refresh cycles.
19	OUT 2	O	OUT 2. Output of Timer 2. In a PC/AT compatible design, OUT 2 is used to drive the speaker.

82C206 Pin Description (Continued)

Pin No.	Name	Type	Function
71	AS	I	ADDRESS STROBE Address strobe is a positive pulse whose falling edge latches the address from the XD bus
72	OSCI	I	OSCILLATOR INPUT The time base for the time functions is connected to this pin External square waves of 32 768 KHz may be connected to this input
15	PSRSTB	I	This input is used to establish the condition of the control registers when power is applied to the device In a PC/AT compatible design, this pin should be tied to the battery back-up circuit. When PSRSTB and TEST are both low, the following occurs (a) Periodic Interrupt Enable (PIE) bit is cleared to zero (b) Alarm Interrupt Enable (AIE) bit is cleared to zero (c) Update ended Interrupt Enable (UIE) bit is cleared to zero (d) Update ended Interrupt Flag (UF) bit is cleared to zero (e) Interrupt Request status Flag (IRQF) is cleared to zero (f) Periodic Interrupt Flag (PF) bit is cleared to zero (g) The part is not accessible (h) Alarm interrupt Flag (AF) bit is cleared to zero (i) Square Wave output enable bit is cleared to zero
14	PWRGD	I	PWRGOOD The Power Good pin must be high for bus cycles in which the CPU accesses the RTC When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor
17	TEST	I	TEST Test is an active high input It initializes various internal registers so that the test program starts in a known state It should be tied low for normal operation.
32, 75	V_{CC}	—	Power Supply
12, 53, 74	V_{SS}	—	Ground

82C206—INTEGRATED PERIPHERALS CONTROLLER

The 82C206 is a LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and a MC146818 Real Time Clock with RAM. The 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Figure 1 illustrates the subsystems contained within the 82C206.

Two DMA Controllers are provided and connected in such a way as to provide the user with four channels of DMA (DMA1) for 8-bit transfers and three channels of DMA (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen channels of interrupt are provided in the 82C206. These channels are partitioned into two cascaded controllers (INTC1,INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. The three internally connected channels are as follows:

Channel 0 — Counter/Timer Counter 0 Interrupt
Channel 2 — Cascade to Slave Interrupt Controller (INTC2)
Channel 8 — Real Time Clock Interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the users specific system requirements.

A Counter/Timer (CTC) subsystem is provided which contains three independent counters. All three counters are driven from a clock input pin which is independent from the other clock inputs to the device. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the 82C206 for maintaining the time and date. This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all of these major subsystems a top level control section is employed which is divided into subsystems for purposes of discussion.

The first section is the Clock and Wait State Control section. This subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device. The last subsystem is the Top Level Decode.

In order to accommodate over 200 registers in the 82C206 and maintain I/O decode compatibility with the IBM PC/AT, a multilevel decode scheme is employed. The Top Level Decode subsystem performs the function of generating enables to the various subsystems. Control and direction of the XD0-XD7 data bus buffers are also handled by this subsystem.

Each of these subsystems will now be described separately.

Top Level Decode

The 82C206 Top Level Decode provides 8 separate enables to various subsystems of the device. Figure 2 contains a truth table for the Top Level Decoder. The enabling of the 82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem *and* the $\overline{\text{XIOR}}$ signal is asserted.

ACK	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	ADDRESS RANGE(Hex)	SELECTED DEVICE
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	1	071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	DISABLED	
X	1	X	X	X	X	X	X	X	X	X	DISABLED	
X	X	1	X	X	X	X	X	X	X	X	DISABLED	

Figure 2. 82C206 Internal Decode

The decoder is enabled by three signals. These three signals are ACK, XA9 and XA8. To enable any internal device ACK must be "1" and both XA9 and XA8 must be "0".

The decode scheme employed in the 82C206 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the 82C206 will not respond to the unused address spaces established by the Top Level Decoder. The extra peripherals may be tied directly to the XD0-XD7 data lines since the 82C206 output buffers are not enabled unless an internal subsystem is enabled.

Clock and Wait State Control

The Clock and Wait State Control subsystem performs four functions: control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023H.

Writing and reading this register is accomplished by first writing a 01H to location 022H to select the 82C206 Configuration Register, and then performing either a read or write to location 023H.

Configuration Register (023H) (Index 01H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0—When the higher speed CPU's are accessing the 82C206, the cycle can be extended by programming up to four wait states into the Configuration Register. This will cause the 82C206 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the Top Level Decoder is detected and either XIOR or XIOW is asserted. IOCHRDY will remain low for the number of wait states programmed into the Configuration Register bits 6 and 7.

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Wait states are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

16W1-16W0—Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

16W1	16W0	16-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

8W1-8W0—Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the Configuration Register.

8W1	8W0	8-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Further control of the cycle length is available through the use of the IOCHRDY pin on the 82C206. During DMA this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low (0) by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

EMR—This bit enables the extended DMAMEMR function. Normally the assertion of DMAMEMR is delayed one clock cycle later than XIOR in the IBM PC/AT implementation. This may not be desirable in some systems. A "1" programmed into this bit position will start DMAMEMR at the same time as XIOR.

CLK—This bit allows the user to insert a divider between the DMA Controller subsystems and the SCLK input pin, or connect the two directly. When this bit position contains a "0", the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in this position bypasses the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

The Configuration Register contents are preloaded by RESET to an initial value of 0C0 hex. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles —4 wait states

16-bit DMA transfers —1 wait state

8-bit DMA transfers —1 wait state

DMAMEMR delayed 1 DMA clock cycle later than XIOR

DMA clock is equal to SCLK/2

DMA FUNCTIONAL DESCRIPTION

The equivalent of two 8237A DMA Controllers is implemented in the 82C206. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfer with little CPU intervention.

The two DMA Controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 privides the cascade interconnection of the two DMA devices, thereby maintaining IBM PC/AT compatibility.

DMA cycle length control is provided internally in the 82C206 allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers which can extend command signals or insert wait states.

Each DMA Channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA to transfer blocks as large as 65536 words. The register associated with each counter allows the channel to reinitialize without reprogramming.

From this point on the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise noted

DMA Operation

During normal operation of the 82C206, the DMA subsystem will be in either the Idle condition, the Program condition or the Active condition. In the Idle condition the DMA controller will be executing cycles consisting of only one state. The idle state SI is the default condition and the DMA will remain in this condition unless the device has been initialized and one of the DMA requests is active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active the device enters the Active condition and issues a hold request to the system. Once in the Active condition the 82C206 will generate the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In the case of a memory-to-I/O transfer, the 82C206 will assert both DMAMEMR and XIOW allowing data to be transfered directly to the requesting device from memory. Note that 82C206 does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data may be varied by programing the DMA or, optionally extended by the peripheral device. During an Active cycle the DMA will sequence through a series of states. Each state will be one DMA clock cycle in length and the number of states in a cycle will vary depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0-S4 and will be explained in detail in the section entitled Active Condition.

Idle Condition

When no device is requesting service the DMA is in an Idle condition which maintains the state machine in the SI state. During this time the 82C206 will sample the DREQ input pins every clock cycle. The internal select from the top level decoder and HLDA are also sampled at the same time to determine if the CPU is attempting to access the internal registers. When either of the above two situations occurs, the DMA will exit the Idle condition. Note that the Program condition has priorit over the Active condition since a CPU cycle has already started.

Program Condition

The Program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top level decode described previously. During this time address lines XA0-XA3 become inputs if DMA1 is selected, or XA1-XA4 become inputs if DMA2 is selected. Note, when DMA2 is selected XA0 is ignored. These address inputs are used to select the DMA controller registers which are to be read or written. Figure 3 lists the register address assignment. Due to the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop will be cleared by hardware RESET or a Master Clear command and may be set or cleared by the CPU issuing the appropriate command.

Special commands are supported by the DMA subsystem in the Program condition to control the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select and XIOW or

ADDRESS		OPERATION			
DMA1	DMA2	XIOR	XIOW	Flip-Flop	Register Function
000h	0C0h	0	1	0	Read Channel 0 Current Address Low Byte
		0	1	1	Read Channel 0 Current Address High Byte
		1	0	0	Write Channel 0 Base and Current Address Low Byte
		1	0	1	Write Channel 0 Base and Current Address High Byte
001h	0C2h	0	1	0	Read Channel 0 Current Word Count Low Byte
		0	1	1	Read Channel 0 Current Word Count High Byte
		1	0	0	Write Channel 0 Base and Current Word Count Low Byte
		1	0	1	Write Channel 0 Base and Current Word Count High Byte
002h	0C4h	0	1	0	Read Channel 1 Current Address Low Byte
		0	1	1	Read Channel 1 Current Address High Byte
		1	0	0	Write Channel 1 Base and Current Address Low Byte
		1	0	1	Write Channel 1 Base and Current Address High Byte
003h	0C6h	0	1	0	Read Channel 1 Current Word Count Low Byte
		0	1	1	Read Channel 1 Current Word Count High Byte
		1	0	0	Write Channel 1 Base and Current Word Count Low Byte
		1	0	1	Write Channel 1 Base and Current Word Count High Byte
004h	0C8h	0	1	0	Read Channel 2 Current Address Low Byte
		0	1	1	Read Channel 2 Current Address High Byte
		1	0	0	Write Channel 2 Base and Current Address Low Byte
		1	0	1	Write Channel 2 Base and Current Address High Byte
005h	0CAh	0	1	0	Read Channel 2 Current Word Count Low Byte
		0	1	1	Read Channel 2 Current Word Count High Byte
		1	0	0	Write Channel 2 Base and Current Word Count Low Byte
		1	0	1	Write Channel 2 Base and Current Word Count High Byte
006h	0CCh	0	1	0	Read Channel 3 Current Address Low Byte
		0	1	1	Read Channel 3 Current Address High Byte
		1	0	0	Write Channel 3 Base and Current Address Low Byte
		1	0	1	Write Channel 3 Base and Current Address High Byte
007h	0CEh	0	1	0	Read Channel 3 Current Word Count Low Byte
		0	1	1	Read Channel 3 Current Word Count High Byte
		1	0	0	Write Channel 3 Base and Current Word Count Low Byte
		1	0	1	Write Channel 3 Base and Current Word Count High Byte
008h	0D0h	0	1	X	Read Status Register
		1	0	X	Write Command Register
009h	0D2h	0	1	X	Read DMA Request Register
		1	0	X	Write DMA Request Register
00Ah	0D4h	0	1	X	Read Command Register
		1	0	X	Write Single Bit DMA Request Mask Register
00Bh	0D6h	0	1	X	Read Mode Register
		1	0		Write Mode Register
00Ch	0D8h	0	1	X	Set Byte Pointer Flip-Flop
		1	0	X	Clear Byte Pointer Flip-Flop
00Dh	0DAh	0	1	X	Read Temporary Register
		1	0	X	Master Clear
00Eh	0DCh	0	1	X	Clear Mode Register Counter
		1	0	X	Clear All DMA Request Mask Register Bits
00Fh	0DEh	0	1	X	Read All DMA Request Mask Register Bits
		1	0	X	Write All DMA Request Mask Register Bits

Figure 3. DMA Registers

XIOR. These commands are Master Clear, Clear Mask Register, Clear Mode Register Counter, Set and Clear Byte Pointer Flip-Flop.

The 82C206 will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and HLDA are mutually exclusive. Erratic operation of the 82C206 can occur if a request for service occurs on an unmasked channel which is being programmed. The channel should be masked or the DMA disabled to prevent the 82C206 from attempting to service a device with a channel which is partially programmed.

Active Condition

The 82C206 DMA subsystem enters the Active condition whenever a software request occurs or a DMA request on an unmasked channel occurs and the device is not in the Program condition. The 82C206 will then begin a DMA transfer cycle.

In a read cycle for example, after receiving a DREQ, the 82C206 will issue a HRQ to the system. Until a HLDA is returned the DMA will remain in an idle condition. On the next clock cycle the DMA will exit Idle and enter state S0. During S0 the device will resolve priority and issue DACK on the highest priority channel requesting service. The DMA will then proceed to state S1 where the multiplexed addresses are output and latched. State S2 is then entered, at which time the 82C206 will assert DMAMEMR. The device then transitions into S3 where the XIOW command is asserted. The 82C206 DMA will then remain in S3 until the Wait State Counter has decremented to zero *and* IOCHRDY is true. Note that at least one additional S3 will occur unless Compressed Timing is selected. Once a ready condition is detected, the DMA will enter S4 where both commands are deasserted. In Burst Mode and Demand Mode (discussed below), subsequent cycles will begin in S2 unless the intermediate addresses require updating. In these subsequent cycles the lower addresses are changed in S2.

The DMA can be programmed on a channel by channel basis to operate in one of four modes. The four modes are listed below.

Single Transfer Mode—This mode directs the DMA to execute only one transfer cycle at a time. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the cycle, the 82C206 will deassert HRQ and release the bus once the transfer is complete. After HLDA has gone inactive the 82C206 will again assert HRQ and execute another cycle on the same channel unless a request from a higher priority channel has been received. In this mode the CPU is ensured of being allowed to execute at least one bus cycle between transfers.

Following each transfer the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000h to FFFFh the terminal count bit in the status register is set and a T/C pulse is generated. If the autoinitialization option has been enabled, the channel will reinitialize itself. If Autoinitialize is not selected the DMA will set the DMA request bit mask and suspend transfering on that channel.

Block Transfer Mode—When Block Transfer Mode is selected, the 82C206 will begin transfers in response to either a DREQ or a software request and will continue until a terminal count (FFFFh) is reached, at which time T/C is pulsed and the status register terminal count bit is set. In this mode DREQ need only be held active until DACK is asserted. Autoinitialization is optional in this mode also.

Demand Transfer Mode—In Demand Transfer mode the DMA will begin transfers in response to the assertion of DREQ and will continue until either terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering ability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count regis-

ters Once DREQ has been deasserted, higher priority channels are allowed to intervene Reaching terminal count will result in the generation of a T/C pulse, the setting of the terminal count bit in the status register and autoinitialization (if enabled)

Cascade Mode—This mode is used to interconnect more than one DMA controller to extend the number of DMA channels while preserving the priority chain In Cascade mode the master DMA controller does not generate address or control signals The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices Once the master has received a HLDA from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller will ignore all inputs except HLDA from the CPU and DREQ on the active channel This prevents conflicts between the DMA devices

Figure 4 shows the cascade interconnection for two levels of DMA devices Note that Channel 0 of DMA2 is internally connected for Cascade mode to DMA1 Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascade is not limited to two levels of DMA controllers

When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device) and then proceed to the second level devices RESET causes the DACK outputs to become active low and are placed in the inactive state To allow the internal cascade between DMA1 and DMA2 to function correctly, the active low state of DACK should not be modified This is because the 82C206 has an inverter between DACK0 of DMA2 and HLDA of DMA1 The first level device's DMA request mask bits will prevent second level cascaded devices from generating unwanted hold requests during the initialization process

DMA Transfers

Four types of transfer modes are provided in the 82C206 DMA subsystem These transfer types are

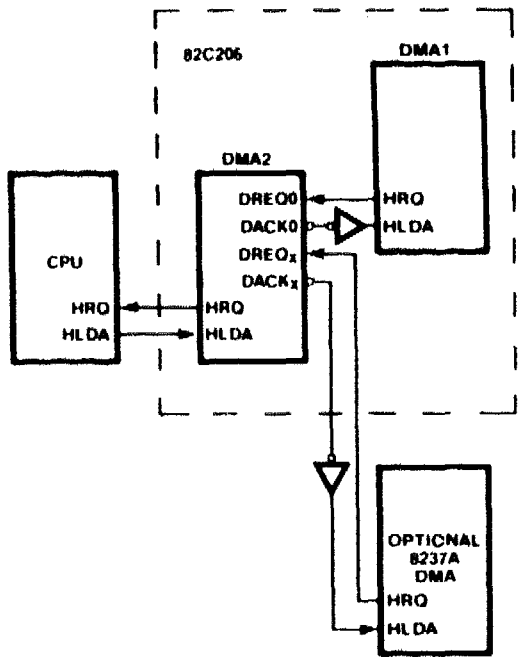


Figure 4. Cascade Mode Interconnect

Read Transfer—Read transfers move data from memory to an I/O device, by generating the memory address and asserting DMAMEMR and XIOW during the same cycle

Write Transfer—Write transfers move data from an I/O device to memory by generating the memory address and asserting XIOR and DMAMEMW

Memory-to-Memory Transfer—The memory-to-memory transfer is used to move a block of memory from one location in memory to another DMA channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting a bit in the Command Register Once programmed to perform a memory-to-memory transfer the process can be started by generating either a software or an external request to channel 0. Once the transfer is initiated, Channel 0 provides the address for the source block during the memory read portion of the cycle. Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is

latched in the internal Temporary Register of the 82C206. The contents of this register are then output on the XD0-7 data lines during the write portion of the cycle and subsequently written to memory. Channel 0 may be programmed to maintain the same source address on every cycle. This allows the CPU to initalize large blocks of memory with the same value. The 82C206 will continue performing transfer cycles until Channel 1 reaches terminal count.

Verify Transfer—The verify transfer is a pseudo-transfer which is useful for diagnostics. In this type of transfer the DMA will operate as if it is performing a Read or Write Transfer by generating HRQ, addresses and DACK but will do so without asserting a command signal. Since no transfer actually takes place IOCHRDY is ignored during Verify transfer cycles.

Autoinitialization

Each of the four DMA channel Mode Registers contains a bit which will cause the channel to reinitialize after reaching terminal count. During this process, referred to as Autoinitialization, the Base Address and Base Word Count Registers, which were originally written by the CPU, are reloaded into the Current Address and Current Word Count Registers (both the base and current registers are loaded during a CPU write cycle). The base registers remain unchanged during DMA Active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the request mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers the Word Count Registers of both Channel 0 and Channel 1 must be programmed with the same starting value for full autoinitialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 will reload the starting address and word count and continue transferring data from the beginning of the source block. Should Channel 1 reach terminal count first, it will reload the current registers and Channel 0 will remain uninitialized.

DREQ Priority

The 82C206 supports two schemes for establishing DREQ priority. The first is fixed priority which assigns priority based on channel position. In this method Channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels in order with Channel 3 receiving the lowest priority.

The second type of priority assignment is rotating priority. In this scheme the ordering of priority from Channel 0 to Channel 3 is maintained but the actual assignment of priority changes. The channel most recently serviced will be assigned the lowest priority and, since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in Figure 5.

In instances where multiple requests occur at the same time the 82C206 will issue a HRQ but will not freeze the priority logic until HLDA is returned. Once HDLA becomes active the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority will not be re-evaluated until HLDA has been deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during Active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on data lines XD0-XD7. These addresses should be externally latched and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a one bit skew occurs in the intermediate address fields. DMA1 will therefore output addresses A8-A15 on the data bus at this time whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

During 8-bit DMA cycles, in which DMA1 is active, the 82C206 will output the lower 8-bits

First Arbitration	Second Arbitration	Third Arbitration	Priority
Channel 0	[Channel 2] · Cycle Grant	[Channel 3] · Cycle Grant	Highest
[Channel 1] · Cycle Grant	[Channel 3]	Channel 0	
Channel 2	Channel 0	Channel 1	
Channel 3	Channel 1	Channel 2	Lowest

[Channel X] Requested Channel

Figure 5. Rotating Priority Scheme

of address on XA0-XA7. The intermediate 8-bits of address will be output on XD0-XD7 and ADSTB8 will be asserted for one DMA clock cycle. The falling edge of ADSTB8 is used to latch the intermediate addresses A8-A15. An enable signal, AEN8, is used to control the output drivers of the external latch. A16-A23 are also generated at this time from a DMA Page Register in the 82C206. Note that A16 is output on the XA16 pin of the device.

16-bit DMA cycles from DMA2 require the 82C206 to output the lower 8-bits of the address on XA1-XA8. The intermediate addresses A9-A16 are output on XD0-XD7. Control for a separate latch is provided by signals ADSTB16 and AEN16. The DMA Page Register now generates A17-A23. During 16-bit DMA transfers XA0 and XA16 remain inactive.

The DMA Page Register is a set of 16 8-bit registers in the 82C206 which are used to generate the high order addresses during DMA cycles. Only 8 of the registers are actually used but all 16 were included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it with the exception of Channel 0 of DMA2 which is used for internal cascading to DMA1. Assignment of each of these registers is shown in Figure 6 along with its Read/Write address.

Address	Register Function
080h	Unused
081h	8-bit DMA Channel 2 (DACK2)
082h	8-bit DMA Channel 3 (DACK3)
083h	8-bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-bit DMA Channel 0 (DACK0)
088h	Unused
089h	16-bit DMA Channel 2 (DACK6)
08Ah	16-bit DMA Channel 3 (DACK7)
08Bh	16-bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh Cycle

Figure 6.
DMA Address Extension Register Map

During Demand and Block Transfers, the 82C206 generates multiple sequential transfers. For most of these transfers the informa-

tion in the external address latches will remain the same, eliminating the need to be relatched. Since the need to update the latches occurs only when a carry or borrow from the lower 8-bits of the Address Counter exists, the 82C206 will only update the latch contents when necessary. The 82C206 will therefore, only execute S1 cycles when necessary, resulting in an overall through-put improvement.

Compressed Timing

The DMA subsystem in the 82C206 can be programmed to transfer a word in as few as 3 DMA clock cycles. The normal DMA cycle consists of three states: S2, S3, and S4 (this assumes Demand or Block Transfer Mode). Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the 1 wait state insertion. In systems capable of supporting higher through-put, the 82C206 can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If Compressed Timing is selected, T/C will be output in S2 and S1 cycles will be executed as necessary to update the address latch. Note that Compressed Timing is not allowed for memory-to-memory transfers.

Register Description

Current Address Register

Each DMA channel has a 16-bit Current Address Register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If Autoinitialization is selected, this register will be reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrementing by setting the Address Hold Bit in the Command Register.

Current Word Count Register

Each channel has a Current Word Count Register which determines the number of transfers to perform. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFh. When this roll-over occurs the 82C206 will generate T/C and either suspend operation on that channel and set the appropriate Request Mask Bit or Autoinitialize and continue.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write only register which is loaded by the CPU when writing to the Current Address Register. The purpose of this register is to store the initial value of the Current Address Register for Autoinitialization. The contents of this register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitialize Bit is set.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write only register which is loaded by writing to the Current Word Count Register. This register is loaded into the Current Word Count Register during Autoinitialization.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a Master Clear command.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK—DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

DRQ—DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

EW—Extended Write is enabled by writing a 1 to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP—Writing a 1 to bit 4 causes the 82C206 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

CT—Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

CD—Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occuring.

AH—Writing a 1 to bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M—A 1 in the bit 0 position enables Channel 0 and Channel 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of the Write Mode Register command determine which channel's Mode Register gets written. The remaining six bits control the mode of the selected channel. Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bits 0 and 1 will both be 1.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

(Read/Write Register)

M1-M0—Mode selection for each channel is accomplished by bits 6 and 7.

M1	M0	MODE
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

DEC—Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.

AI—The Autoinitialization function is enabled by writing a 1 in bit 4 of the Mode Register.

TT1-TT0—Bits 2 and 3 control the type of transfer which is to be performed.

TT1	TT0	TYPE
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Illegal

CS1-CS0—Channel Select bits 1 and 0 determine which channel's Mode Register will be written. Read back of a mode register will result in bits 1 and 0 both being ones.

CS1	CS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Request Register

This is a four bit register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or

reset independently by the CPU. The Request Mask has no effect on software generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

(Write Operation)

RB—The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

RS1-RS0—Channel Select 0 and 1 determine which channel's Mode Register will be written. Read back of the mode register will result in bits 0 and 1 both being ones.

RS1	RS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Format for the Request Register read operation is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RC1	RC0

(Read Operation)

RC3-RC0—During a Request Register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The Request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

(Set/Reset Operation)

MB—Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask, inhibiting external requests.

MS1-MS0—These two bits select the specific mask bit which is to be set or reset.

MS1	MS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Alternatively all four mask bits can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

(Read/Write Operation)

MB3-MB0—Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached, if Autoinitialize is disabled. The entire register can be cleared,

enabling all four channels, by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bits 0-3 of this register are cleared by RESET, Master Clear or each time a Status Read takes place. Bits 4-7 are cleared by RESET, Master Clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the Mask Register Bits. The channel number corresponds to the bit position.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

(Read Only Register)

Temporary Register

The Temporary Register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD0-XD7. During the second cycle of the transfer, the data in the Temporary Register is output on the XD0-XD7 pins. Data from the last memory-to-memory transfer will remain in the register unless a RESET or Master Clear occurs.

Special Commands

Five Special Commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a XIOR or XIOW. Information on the data lines is ignored by the 82C206 whenever an XIOW activated command is issued, thus data returned on XIOR activated commands is invalid.

Clear Byte Pointer Flip-Flop—This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

Set Byte Pointer Flip-Flop—Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear—This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set. Immediately following Master Clear or RESET, the DMA will be in the Idle Condition.

Clear Request Mask Register—This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter—In order to allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

INTERRUPT CONTROLLER FUNCTIONAL DESCRIPTION

The programmable interrupt controllers in the 82C206 function as a system wide interrupt manager in an iAPX86 system. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided,which can be reconfigured at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system environment.

Overview

Two interrupt controllers, INTC1 and INTC2, are included in the 82C206. Each of the interrupt controllers is equivalent to an 8259A device operating in iAPX86 Mode. The two devices are interconnected and must be programmed to operate in Cascade Mode (see Figure 7) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for Master operation (defined below) in Cascade Mode. INTC2 is a Slave device (defined below) and is located at 0A0H-0A1H. The Interrupt Request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IR2) of INTC1. The address decoding and Cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the Real Time Clock is connected to Channel 0 (IR0) of INTC2. Figure 8 lists the 16 interrupt channels and their interrupt request source.

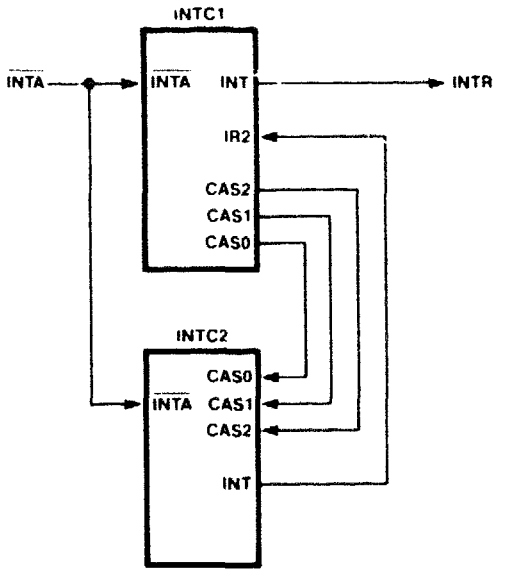


Figure 7. Internal Cascade Interconnect

Description of the Interrupt Subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example 020H (0A0H).

Controller Operation

Figure 9 is a block diagram of the major elements in the interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request Register bits are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/Comparator with a three bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge (INTA) cycles.

Interrupt Sequence

The 82C206 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the 82C206 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows.

1—One or more of the interrupt requests

Controller Number	Channel Name	Interrupt Request Source
INTC1	IR0	Counter/Timer Out0
INTC1	IR1	IRQ1 Input Pin
INTC1	IR2	INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 Input Pin
INTC1	IR4	IRQ4 Input Pin
INTC1	IR5	IRQ5 Input Pin
INTC1	IR6	IRQ6 Input Pin
INTC1	IR7	IRQ7 Input Pin
INTC2	IR0	Real Time Clock IRQ
INTC2	IR1	IRQ9 Input Pin
INTC2	IR2	IRQ10 Input Pin
INTC2	IR3	IRQ11 Input Pin
INTC2	IR4	IRQ12 Input Pin
INTC2	IR5	IRQ13 Input Pin
INTC2	IR6	IRQ14 Input Pin
INTC2	IR7	IRQ15 Input Pin

Figure 8. Interrupt Request Source

(IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2—The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3—The CPU accepts the interrupt and responds with an INTA cycle.

4—During the first INTA cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal Cascade address is generated and the XD7-XD0 outputs remain tri-stated.

5—The CPU will execute a second INTA cycle, during which the 82C206 will drive an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is shown in Figure 12. Note that V7-V3 in Figure 12 are programmable by writing to Initialization Control Word 2 (see Initialization Command Words section below).

6—At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End Of Interrupt mode is selected (see End Of Interrupt section below). Otherwise, the ISR bit must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If no interrupt request is present at the beginning of the first INTA cycle (i.e., a spurious interrupt) INTC1 will issue an interrupt level 7 vector during the second INTA cycle.

End Of Interrupt

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the Priority Resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

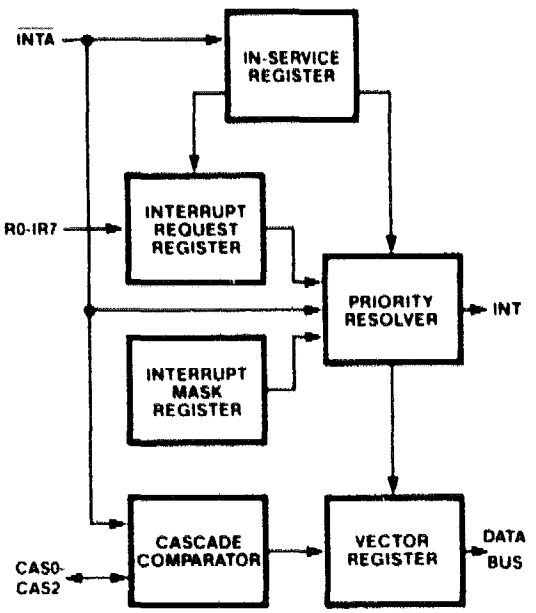


Figure 9. Interrupt Controller Block Diagram

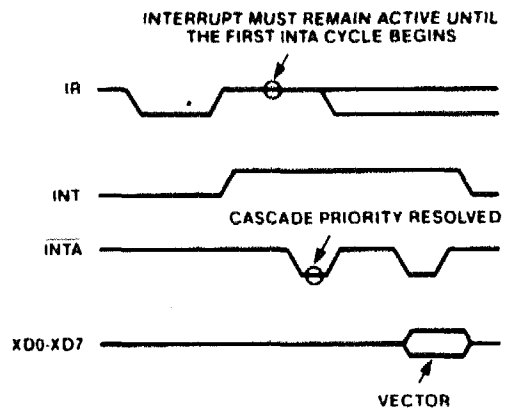


Figure 10. Interrupt Sequence

The 82C206 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by a IMR bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2)

Fixed Priority Mode—This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

	Lowest						Highest
Priority Status	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine, will only be acknowledged if the CPU has internally re-enabled interrupts.

Specific Rotation Mode—Specific Rotation allows the system software to re-assign priority levels by issuing a command which redefines the highest priority channel.

Before Rotation

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

(Specific Rotation command issued with Channel 5 specified)

After Rotation

	Lowest							Highest
Priority Status	5	4	3	2	1	0	7	6

Automatic Rotation Mode—In applications where a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur if enabled, due to the occurrance of EOI (automatic or CPU generated).

Before Rotation (IR4 is highest priority request being serviced)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

After Rotation (IR4 service completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

	Lowest							Highest
Priority Status	4	3	2	1	0	7	6	5

Programming The Interrupt Controller

Two types of commands are used to control the 82C206 interrupt controllers, Initialization Command Words (ICWs) and Operational Command Words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1—The Initialization Command Word Counter is reset to zero.
2—ICW1 is latched into the device
3—Fixed Priority Mode is selected
4—IR7 is assigned the highest priority
5—The Interrupt Mask Register is cleared
6—The Slave Mode Address is set to 7
7—Special Mask Mode is disabled
8—The IRR is selected for Status Read operations

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See Figure 11 for a flow chart of the initialization sequence. The initialization sequence can be terminated

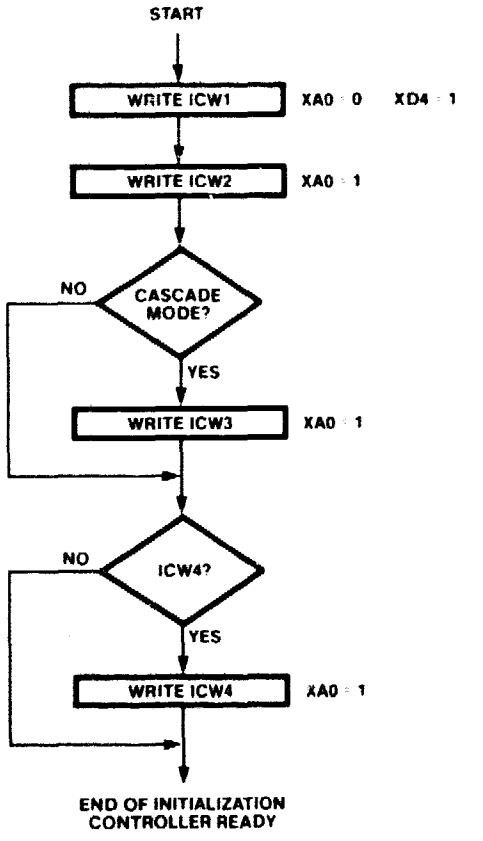


Figure 11. Initialization Sequence

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR7	V7	V6	V5	V4	V3	1	1	0
IR7	V7	V6	V5	V4	V3	1	0	1
IR7	V7	V6	V5	V4	V3	0	1	1
IR7	V7	V6	V5	V4	V3	0	1	0
IR7	V7	V6	V5	V4	V3	0	0	1
IR7	V7	V6	V5	V4	V3	0	0	0

Figure 12. Interrupt Vector Byte

at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

ICW1—Address 020H (0A0H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

(Write Only Register)

SI—Bit 4 indicates to the interrupt controller that an Initialization Sequence is starting and must be a 1 to write ICW1.

LTM—Bit 3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a 'high' level on the IRR input will generate an interrupt request. The IR must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is deasserted early) and the IR must be removed prior to EOI to prevent a second interrupt from occuring.

SM—Bit 1 selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.

ICW2—Address 021H (0A1H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

(Write Only Register)

V7-V3—These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during INTA (see Figure 12). INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1—Address 021H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

(Write Only Register)

S7-S0—Select which IR inputs have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

ICW3 Format for INTC2—Address 0A1H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	ID2	ID1	ID0

(Write Only Register)

ID2-ID0—Determine the Slave Mode address the controller will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02H for Cascade Mode operation. Note, b7-b3 should be zero.

ICW4—Address 021H (0A1H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	

(Write Only Register)

EMI—Bit 4 will Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its In-Service Register for zero, when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

AEOI—Auto End Of Interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

Operational Command Words

Operational Command Words (OCWs) allow the 82C206 interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021h (0A1h) and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2,OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1—Address 021H (0A1H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

(Read/Write Register)

M7-M0—These bits control the state of the Interrupt Mask Register. Each Interrupt Request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2—Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

(Write Only Register)

R—This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

R	SL	EOI	Function
1	0	0	Rotate on auto EOI enable*
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

***This function is disabled by writing a zero to all three bit positions.**

SL—This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI Command
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

EOI—This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

R	SL	EOI	Function
0	0	1	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on specific EOI

SI—Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3—If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L2-L0—These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. L2-L0 must be valid during three of the four specific cycles (see SL above).

OCW3—Address 020H (0A0H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

(Write Only Register)

ESMM—Writing a 1 in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM—If ESMM and SMM both are written with a 1 the Special Mask Mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

SI—See SI above.

2/3—See 2/3 above.

PM—Polled Mode is enabled by writing a 1 to bit 2 of OCW3, causing the 82C206 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

RR—When the RR bit (bit 1) is 1, reading the Status Port at address 020h (0A0h) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR reset.

RIS—This bit selects between the IRR and the ISR during Status Read operations if RR = 1.

COUNTER/TIMER FUNCTIONAL DESCRIPTION

The Counter/Timer (CTC) in the 82C206 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains 3 16-bit counters (Counter 0-3) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters shown in Figure 13 are controlled from a common set of control logic. The Control Logic decodes control in-

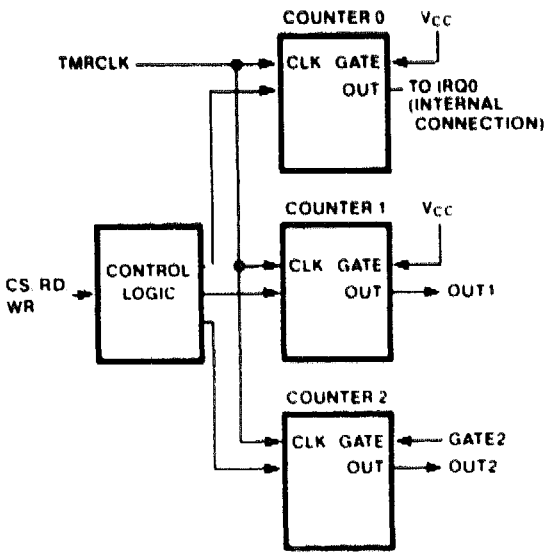


Figure 13. Counter/Timer Block Diagram

formation written to the CTC and provides the controls necessary to load, read, configure and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

Mode 0	Interrupt on terminal count
Mode 1	Hardware retriggerable one-shot
Mode 2	Rate generator
Mode 3	Square wave generator
Mode 4	Software triggered strobe
Mode 5	Hardware retriggerable strobe

All three counters in the CTC are driven from a common clock input pin (TMRCLK) which is independent from other clock inputs to the 82C206. Counter 0's output (Out0) is connected to IR0 of INTC1 (see Interrupt Controller Functional Description) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third counter (Counter 2) is a full function Counter/Timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator.

Counter Description

Each counter in the CTC contains a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL,CIH),and a pair of 8-bit Counter Output Latches (COL,COH). Each counter also has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The OUT signal's state and function are controlled by the Counter Mode and condition of the CE (see Mode Definitions).

The Control Register stores the mode and command information used to control the counter. The Control Register may be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043h). The remaining bits in the byte contain the mode, the type of command, and count format information.

The Status register allows the software to monitor counter condition and read back the contents of the Control Register.

The Counting Element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFF in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the Counter Input Latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the Counter Output Latches. COL and COH are transparent latches which can be read while transparent or latched (see Latch Counter Command).

Programming The CTC

After power-up the condition of CTC Control Registers, counter registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written by writing to the Control Word address (see Figure 14). The Control Word is a write only location.

Control Word—(043H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

(Write Only Register)

F3-F0—Bits 7-4 determine the command to be performed.

M2-M0—Bits 3-1 determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command) or select the counter during a Read-Back Command (see Read-Back Command). Bits 3-1 become "don't care" during Latch Counter Commands.

Address	Function
040h	Counter 0 Read/Write
041h	Counter 1 Read/Write
042h	Counter 2 Read/Write
043h	Control Register Write Only

Figure 14. Counter/Timer Address Map

BCD—Bit 0 selects binary coded decimal counting format during Read/Write Counter Commands. Note, during Read-Back Command this bit must be 0.

Read/Write Counter Command

When writing to a counter, two conventions must be observed.

1—Each counters Control Word must be written before the initial count is written.

2—Writing the initial count must follow the

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (see Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (see Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (see Counter Latch Command)2
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read-Back Command (see Counter Read-Back Command)

MSB = most significant byte
LSB = least significant byte

format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the Control Word providing the programmed format is observed.

During Read/Write Counter Commands M3-M0 are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

When a Latch Counter Command is issued, the counter's output latches (COL,COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple Latch Counter Commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read-Back Command

The Read-Back Command allows the user to check the count value, Mode, and state of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	LC	LS	C2	C1	C0	0

LC—Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS—Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of it's Control Register, Null Count and Output into the Status Register. The next read of the Counter will result in the contents of the Status Register being read (see Status Read).

C2-C0—Writing a 1 in bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS, LC = 0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

Status Byte

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT—Bit 7 contains the state of the OUT signal of the counter.

NC—Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0.

whenever the counter is loaded from the counter input registers

F1-F0—Bits 5-4 contain the F1 and F0 Command bits which were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

M2-M1—These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD—Bit 0 indicates the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be used as the example in describing counter operation, but the description of Mode 0, 2, 3 and 4 is relevant to all counters.

The following terms are defined for describing CTC operation:

TMRCLK pulse—A rising edge followed by a falling edge of the 82C206 TMRCLK input.

trigger—The rising edge of the GATE2 input.

counter load—The transfer of the 16-bit value in CIL and CIH to the CE.

initialized—A Control Word written and the Counter Input Latches loaded.

Counter 2 operates in one of the following modes:

Mode 0—Interrupt on terminal count.

Writing the Control Word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or Control Word is written. Counting is enabled when GATE2 = 1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the Control Word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see Write Operations). This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2 = 1. OUT2 therefore goes high N TMRCLK pulses after GATE2 = 1.

Mode 1—Hardware retriggerable one-shot

Writing the Control Word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

Mode 2—Rate generator

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2 = 1) and will generate an OUT2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in Mode 2.

GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not

affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3—Square wave generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low = (N-1)/2.

Mode 4—Software triggered strobe

Writing the Control Word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5—Hardware triggered strobe

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

Mode	Condition		
	Low	Rising	High
0	Disables Counting	—	Enables Counting
1	—	a) Initiates Counting b) Resets Out Pin	—
2	a) Disables Counting b) Forces Out Pin High	Initates Counting	Enables Counting
3	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
4	Disables Counting	—	Enables Counting
5	—	Initiates Counting	—

Figure 15. Gate Pin Function

GATE2

In Modes 0, 2, 3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3 and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flop-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive.

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

This section of the 82C206 combines a complete time-of-day clock with alarm, one hundred year calendar, a programmable periodic interrupt, and 114 bytes of low power static RAM. Provisions are made to enable the device to operate in a low power (battery powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

Register Access

Reading and writing to the 128 locations in the Real Time Clock is accomplished by first placing the Index Address of the location you wish to access on the data input pins XD0-XD6 and then strobing the AS input pin. The address will then be latched into the Index Address Register on the falling edge of AS. The Index Address Register is then used as a pointer to the specific byte in the Real Time Clock, which may be read or written to by asserting XIOR or XIOW with with an address on the XA9-XA0 inputs of 071H.

Since AS will most likely be generated by an I/O operation which will result in the assertion of XIOW, it is recommended that an address of 070H be applied to the XA9-XA0 inputs during this time. This will prevent the modification of other registers in the 82C206.

Address Map

Figure 16 illustrates the internal register/RAM organization of the Real Time Clock portion of the 82C206. The 128 addressable locations in the Real Time Clock are divided into 10 bytes which normally contain the time, calendar, and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except Registers C, D, Bit 7 of Register A and Bit 7 of the Seconds Byte which is always 0.

Index	Function
00	SECONDS
01	SECONDS ALARM
02	MINUTES
03	MINUTES ALARM
04	HOURS
05	HOURS ALARM
06	DAY OF WEEK
07	DATE OF MONTH
08	MONTH
09	YEAR
0A	REGISTER A
0B	REGISTER B
0C	REFISTER C
0D	REGISTER D
0E	USER RAM
0F	USER RAM
7E	USER RAM
7F	USER RAM

Figure 16. Address Map for Real Time Clock

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the Real Time Clock. Initalization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initalization of the internal registers can be performed, the SET bit in Register B should be set to a "1" to prevent Real Time Clock updates from occuring. The CPU then initalizes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initalized and enabled, the Real Time Clock will perform Clock/Calendar updates at a 1 Hz rate.

Index Register Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm	00-59
4	Hours (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours (24 hour mode)	00-23
5	Hours Alarm (12 hour mode)	01-12 (AM) 81-92 (PM)
	Hours Alarm (24 hour mode)	00-23
6	Day of Week	01-07
7	Day of Month	01-31
8	Month	01-12
9	Year	00-99

Figure 17. Time, Calendar, Alarm Data Format

Figure 17 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initalization the 24/12 bit cannot be changed without reinitalizing the hour locations. In 12 hour format the high order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2ms. These 10 locations cannot be written during this time. Information read while the Real Time Clock is performing an update will be undefined. The Update Cycle section shows how to avoid Update Cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into Register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from Index Address 0EH to 7FH are not affected by the Real Time Clock. These bytes are accessable during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery powered when the system in turned off.

Control and Status Registers

The 82C206 contains four registers used to control the operation and monitor the status of the Real Time Clock. These registers are located at Index Address 0AH-0DH and are accessable by the CPU at all times.

REGISTER A (0AH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/Write register except UIP)

UIP—Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. The UIP bit is read only and is not affected by Reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV2-DV0—These three bits are used to control the Divider/Prescaler on the Real Time Clock. While the 82C206 can operate at frequencies higher than 32.768 Khz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

DV2	DV1	DV0	OSCI Freq.	Mode
0	0	0	4.194304MHz	Operate
0	0	1	1.048576MHz	Operate
0	1	0	32.768KHz	Operate
1	1	X	Reset Divider	

Divider Options

RS3-RS0—These four bits control the Periodic Interrupt rate. The Periodic interrupt is derived from the Divider/Prescaler in the Real Time Clock and is separate from the Alarm Interrupt. Both the alarm and periodic interrupts do however, use the same interrupt channel in the Interrupt Controller. Use of the Periodic Interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the Real Time Clock can be programmed.

Rate Selection				Time Base	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 μs	3.90526 ms
0	0	1	0	61.035 μs	78125 ms
0	0	1	1	122.070 μs	122.070 μs
0	1	0	0	244.141 μs	244.141 μs
0	1	0	1	488.281 μs	488.281 μs
0	1	1	0	976.562 μs	976.562 μs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Periodic Interrupt Rate

REGISTER B (0BH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	024/12	DSE	

(Read/Write Register)

SET—Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET input pin.

PIE—The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by Reset.

AIE—The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by Reset.

24/12—The 24/12 control bit is used to establish the format of both the Hours and Hours Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by Reset.

DSE—The Real Time Clock can be instructed to handle daylight savings time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur. On the last Sunday in April AM. Setting this bit to a "0" disables the execution of these two exceptions. PSRSTB has no affect on this bit.

REGISTER C (0CH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

(Read only register)

IRQF—The Interrupt Request Flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB/ input pin. Writing to this register has no affect on the contents.

PF—The Periodic Interrupt Flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt a nd set IRQF if PIE is a "1".

AF—A "1" appears in the AF bit whenever a match has occured between the time registers and alarm registers during an update cycle. This flag is also independent of it's enable (AIE) and will generate an interrupt if AIE is true.

REGISTER D (0DH)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

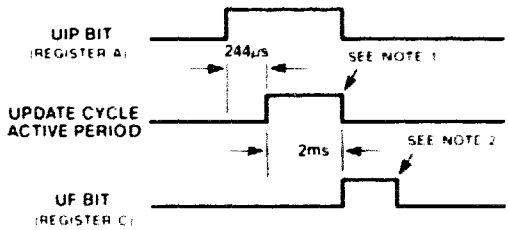
(Read only register)

VRT—The Valid RAM and Time Bit indicates the condition of the contents of the Real Time Clock. This bit is cleared to a "0" whenever the PS input pin is LOW. This pin

is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initalized since power was applied to the device PSRSTB has no affect on this bit and it can only be set by reading Register D All unused register bits will be "0" when read and are not writable

Update Cycle

During normal operation the Real Time Clock will perform an update cycle once every second The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in Register B cleared The function of the update cycle is to increment the clock/calendar registers and compare them to the Alarm Registers If a match occurs between the two sets of registers, an alarm is issued and an interrupt will be issued if the alarm and interrupt control bits are enabled



NOTE:
1 REGISTERS 0-9 ARE UNAVAILABLE TO BE READ OR WRITTEN DURING THIS TIME
2 UF BIT CLEARED BY CPU READ OF REGISTER C

Figure 18. Update Cycle

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU This is done to prevent the possible corruption of data in the registers or the reading of incorrect data To avoid contention problems between the Real Time Clock and the CPU, a flag is provided in Register A to alert the user of an impending update cycle This Update In Process Bit (UIP) is asserted 244μs before the actual start of the cycle and is maintained until the cycle is complete Once the cycle is complete the UIP bit will be cleared and the Update Flag (UF) in Register C will be set Figure 18 illustrates the update cycle CPU access is always allowed to Registers A through D during update cycles

Two methods for reading and writing to the Real Time Clock are recommended Both of these methods will allow the user to avoid contention between the CPU and the Real Time Clock for access to the time and date information

The first method is to read Register A, determine the state of the UIP bit and if it is "0" perform the read or write operation For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244μs to complete from the beginning of the read of Register A to the completion of the last read or write operation to the Clock Calendar Registers

The second method of accessing the lower 10 registers is to read Register C once and disregard the contents Then subsequently continue reading this register until the UF bit is a "1" This bit will become true immediately after an update has been completed The user then has until the start of the next update cycle to complete a read or write operation

Power-Up/Down

Most applications will require the Real Time Clock to remain active whenever the system power is turned off To accomplish this the user must provide an alternate source of power to the 82C206 This alternate source of power is normally provided by connecting a battery to the Vcc supply pin of the device A means should be provided to switch from the system power supply to the battery A circuit such as the one shown in Figure 19 may be used to eliminate power drain on the battery when the entire 82C206 is active The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain

The user should also ensure that the Vin maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.

A pin is provided on the device to protect the contents of the Real Time Clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased Icc. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initalize the device whenever power is applied to the 82C206. This pin (PSRSTB) will not alter the RAM or Clock/Calendar contents but it will initalize the necessary control register bits. (See Pin Description for a list of the control register bits affected by PSRSTB) Assertion of PSRSTB disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the PSRSTB input is also shown in Figure 19.

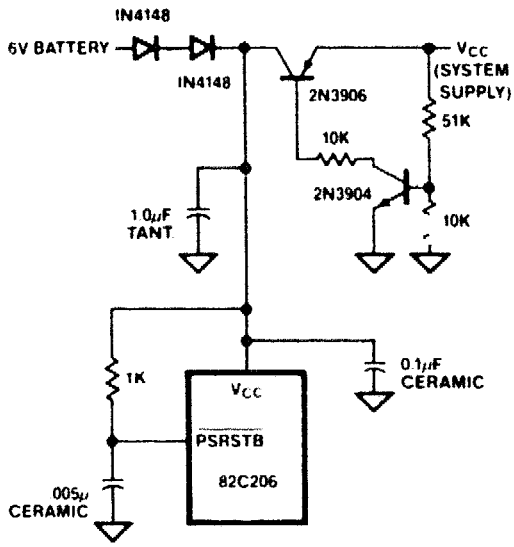


Figure 19. Power Conversion and Reset Circuitry

82C206 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device may occur of Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C206 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

DC Characteristics (T_A = 0-70° C, V_{CC} = 5 ± 5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2.0 mA
I_{OL}	Input Current	-10	10	μA	V_{IN} = V_{CC} to 0V
I_{OL}	Output Leakage Current	-10	10	μA	V_{OU} = V_{CC} to 0.45
I_{CC}	V_{CC} Supply Current		30	mA	CLK Freq = 8 MHz
I_{CCSB}	V_{CC} Standby Supply Current		10	μA	CLK Freq = DC

Capacitance (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	FC = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins
C_{OUT}	Output Capacitance		20	pF	Returned to V_{SS}

AC Characteristics (T_A = 0-70°C, V_{CC} = 5V ± 5%)

Symbol	Parameter	6 MHz Min.	6 MHz Max.	8 MHz Min.	8 MHz Max.	Units
t1	Address Setup to Command Active	25		25		nsec
t2	Command Active Period	250		200		nsec
t3	Address Hold Time from Command Inactive	0		0		nsec
t4	Data Valid Delay	200		160		nsec
t5	Data Hold Time from XIOR Inactive	10		10		nsec
t6	XD0-XD7 Active from XIOR	5	40	5	40	nsec
t7	Data Setup to XIOW Inactive	200		160		nsec
t8	Data Hold Time from XIOW Inactive	0		0		nsec
t9	Command Recovery Time	150		120		nsec
t10	Interrupt Request width (Low)	120		100		nsec
t11	Interrupt Request width (High)	250		200		nsec
t12	INT Output Delay		400		300	nsec
t20	Real Time Clock Cycle Time		500		500	nsec
t21	AS Pulse Width	200		160		nsec
t22	Data Valid Setup to AS Inactive	200		160		nsec
t23	Data Hold Time from AS Inactive	0		0		nsec
t24	OSCI Period	500		500		nsec
t25	OSCI High Time	200		200		nsec
t26	OSCI Low Time	200		200		nsec
t27	PSRSTB High Delay from V_{CC}	5		5		μsec
t28	PSRSTB Low Pulse Width	5		5		μsec
t29	VRT Bit Valid Delay		2		2	μsec
t40	TMRCLK Period	200	DC	125	DC	nsec
t41	TMRCLK Low Time	80		50		nsec
t42	TMRCLK High Time	80		50		nsec
t43	GATE2 Setup to TMRCLK	80		50		nsec
t44	GATE2 Hold Time from TMRCLK	80		50		nsec
t45	GATE2 Low Time	80		50		nsec
t46	GATE2 High Time	80		50		nsec
t47	OUT2 Delay from TMRCLK		200		120	nsec
t48	OUT2 Delay from GATE2		200		120	nsec

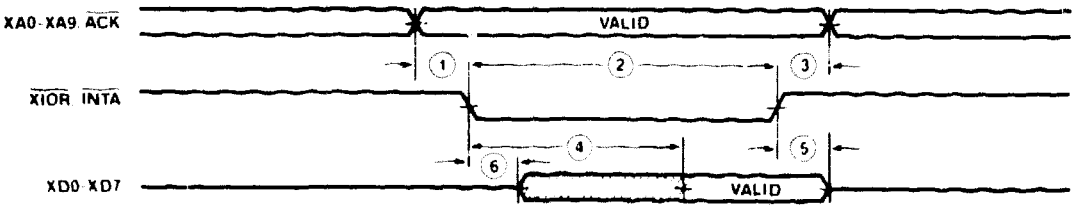
AC Characteristics (T_A = 0-70°C, V_{CC} = 5V + 5%) (Continued)

Symbol	Parameter	6 MHz Min.	6 MHz Max.	8 MHz Min.	8 MHz Max.	Units
t50	SCLK Period (1 X SCLK)	186		125		nsec
t50A	SCLK Period (2 X SCLK)	93		62		nsec
t51	SCLK Low Time (1 X SCLK)	75		43		nsec
t51A	SCLK Low Time (2 X SCLK)	32		22		nsec
t52	SCLK High Time (1 X SCLK)	82		55		nsec
t52A	SCLK High Time (2 X SCLK)	40		27		nsec
t53	DREQx Setup to SCLK	0		0		nsec
t54	HRQ Valid From SCLK		120		75	nsec
t55	HLDA Setup to SCLK	75		45		nsec
t56	AENx Valid Delay from SCLK		175		105	nsec
t57	AENx Invalid Delay from SCLK	TBD	130	TBD	80	nsec
t58	ADSTBx Valid Delay from SCLK		80		50	nsec
t59	ADSTBx Invalid Delay from SCLK		120		120	nsec
t60	XD0-XD7 Active Delay from SCLK		110		60	nsec
t61	XD0-XD7 Valid Setup to ADSTBx Low	80		65		nsec
t62	XD0-XD7 Hold Time from ADSTBx Low	25		25		nsec
t63	XD0-XD7 Tristate Delay from SCLK		170		135	nsec
t64	Address Valid Delay from SCLK		110		60	nsec
t65	Address Hold Time from DMAMEMR High	66		50		nsec
t66	Address Tristate Delay from SCLK		90		55	nsec
t67	DACKx Delay from SCLK		170		105	nsec
t68	Command Enable Delay from SCLK		150		90	nsec
t69	Command Active Delay from SCLK		190		120	nsec
t70	Write Cmnd Inactive Delay from SCLK		130		80	nsec
t71	Address Hold Time from Write High	116		75		nsec
t72	Command Tristate Delay from SCLK		120		75	nsec

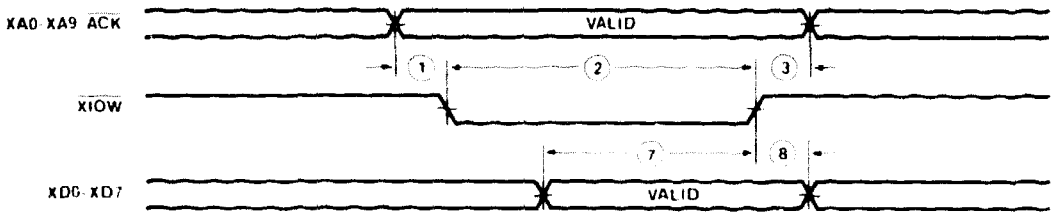
AC Characteristics (T_A = 0-70°C, V_{CC} = 5V + 5%) (Continued)

Symbol	Parameter	6 MHz Min.	6 MHz Max.	8 MHz Min.	8 MHz Max.	Units
t73	Read Cmnd Inactive Delay from SCLK		190		115	nsec
t74	TC Delay from SCLK		100		60	nsec
t75	XD0-XD7 Setup to Read Cmnd Inactive	155		90		nsec
t76	XD0-XD7 Hold from Read Cmnd Inactive	0		0		nsec
t77	XD0-XD7 Valid Delay from SCLK		190		120	nsec
t78	XD0-XD7 Hold from Write Inactive	15		15		nsec
t79	IOCHRDY Input Setup to SCLK	50		35		nsec
t80	IOCHRDY Input Hold Time from SCLK	35		20		nsec

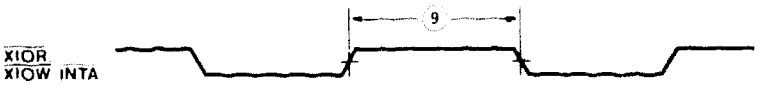
82C206 TIMING DIAGRAMS



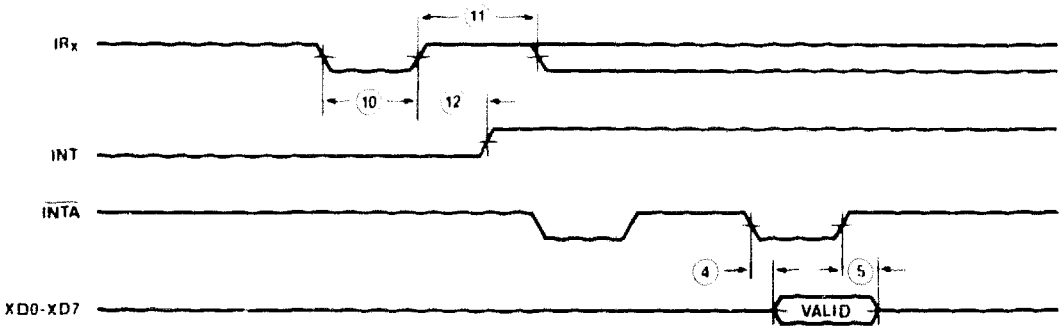
PERIPHERAL READ INTA CYCLE



PERIPHERAL WRITE CYCLE



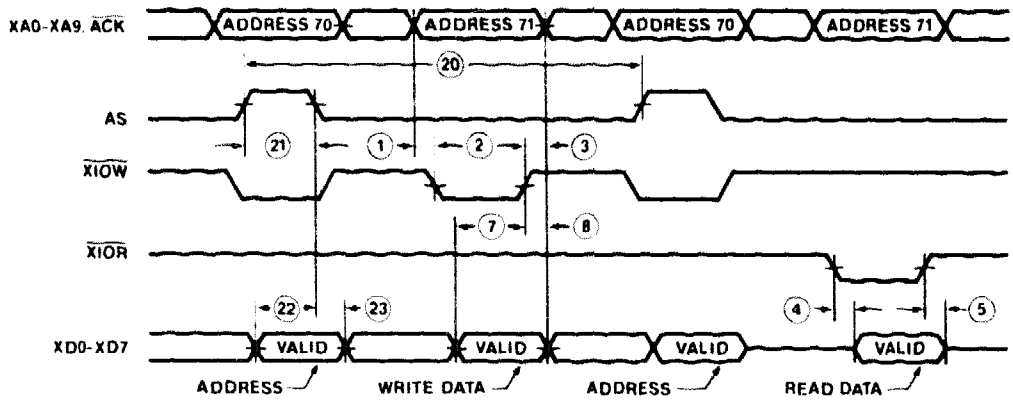
COMMAND RECOVERY



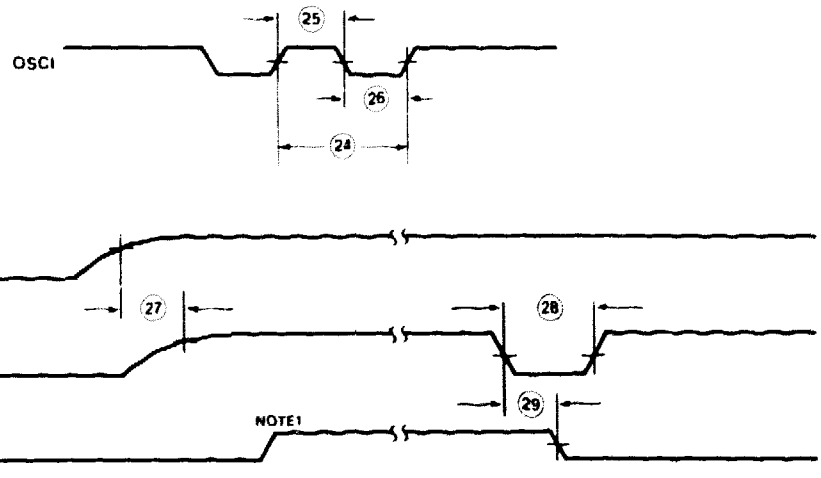
82C206 TIMING DIAGRAMS



IOCHRDY OUTPUT

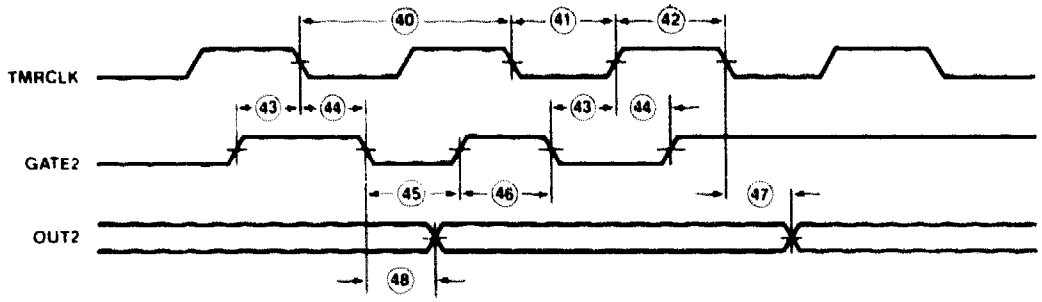


REAL TIME CLOCK ACCESS CYCLE

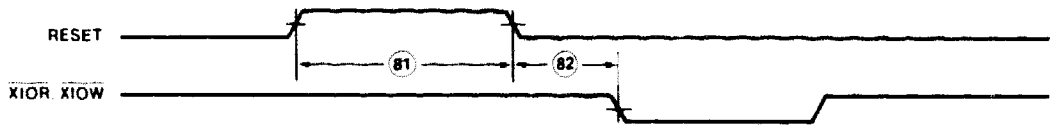


REAL TIME CLOCK POWFR-UP SEQUENCE

82C206 TIMING DIAGRAMS

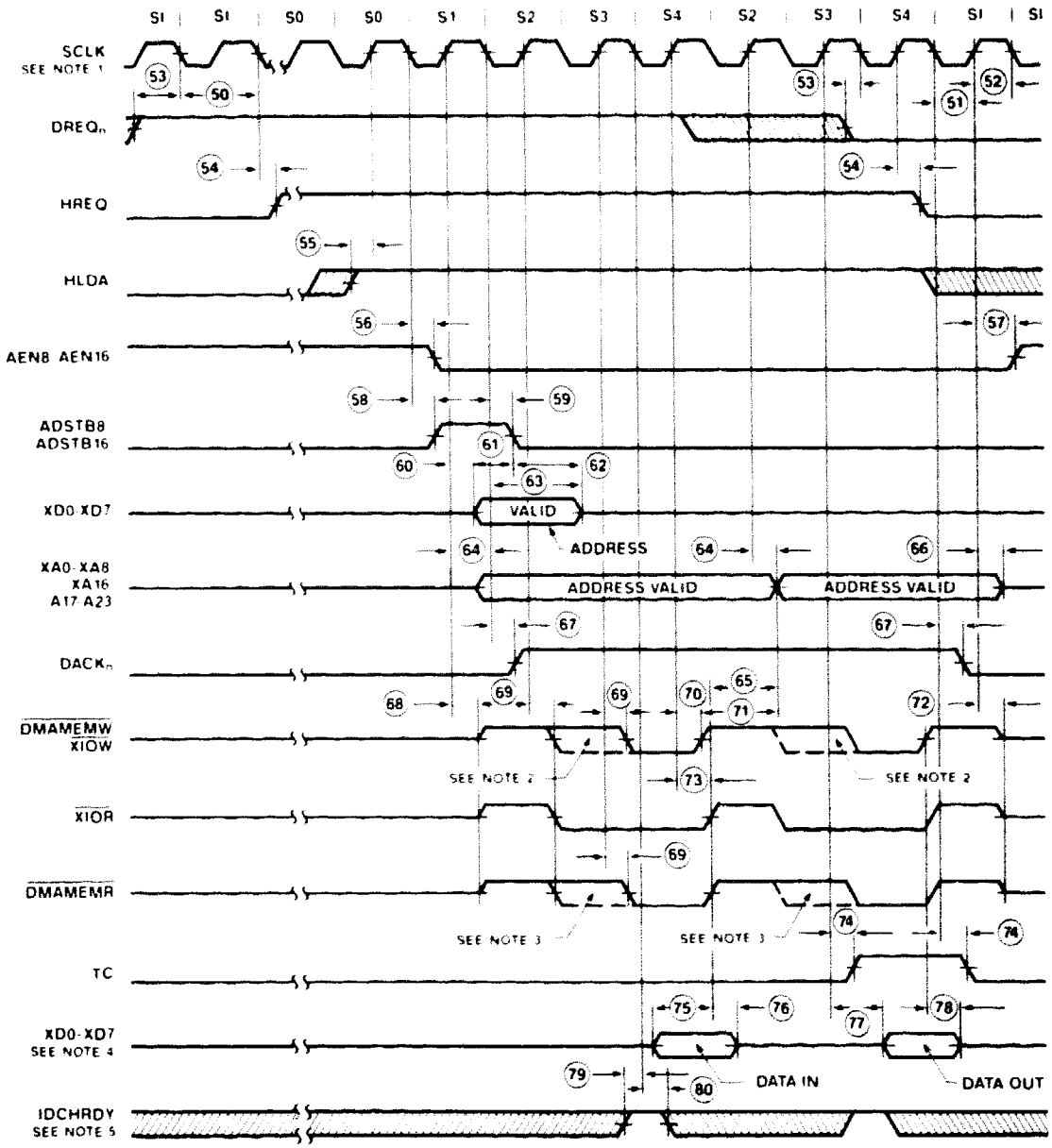


COUNTER/TIMER PARAMETERS



DMA RESET

82C206 TIMING DIAGRAMS



NOTES:

1. All timings referenced to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input.
2. Extended Write mode selected.
3. Extended Read mode selected.
4. Data Bus during memory to Memory Transfer.
5. IOCHRDY Input Timing.

Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON OFF

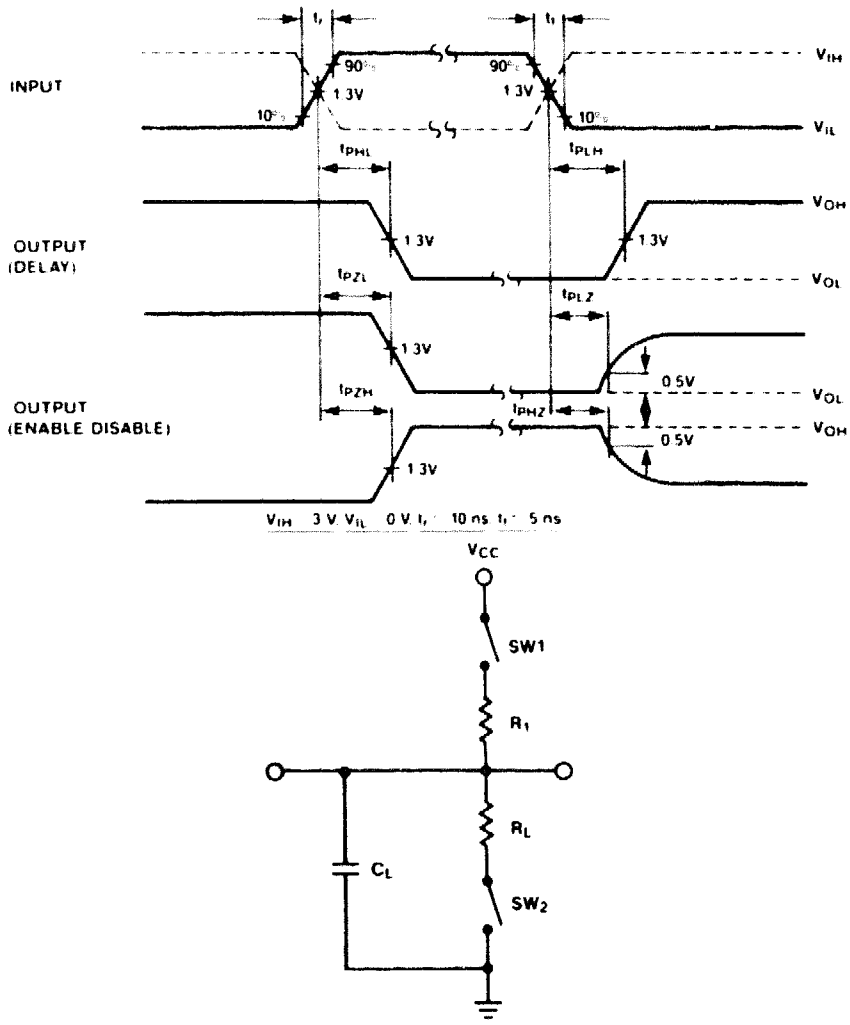
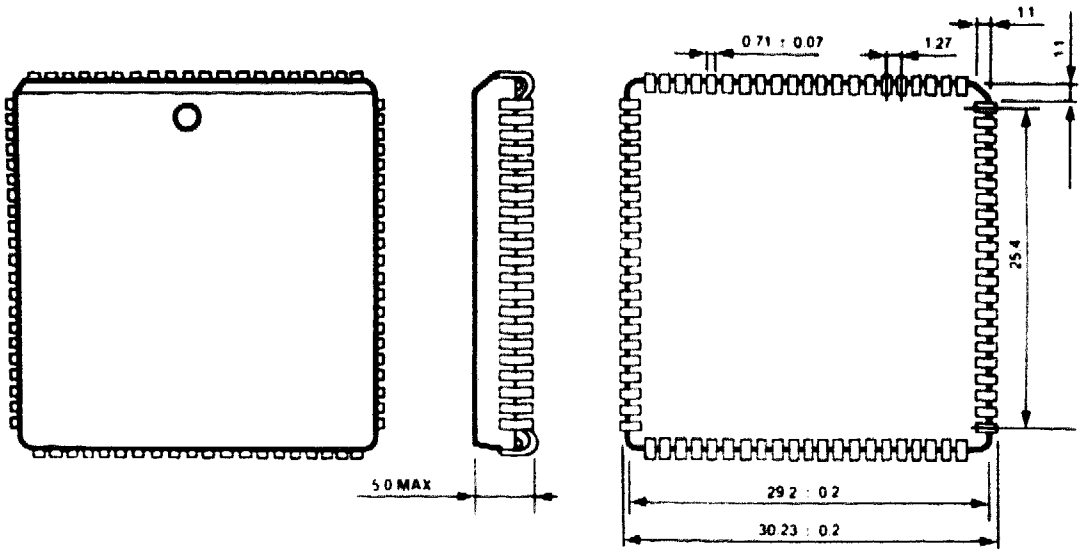


Figure 10. Load Circuit and AC Characteristics Measurement Waveform

84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)



Ordering Information

Order Number	Package Type	Operating Range
P82C206	PLCC-84	C (Note 1)

NOTE:
1 PLCC-84 Plastic Leaded Chip Carrier 84-Pin Package
C = Commercial Range, 0-70°C, ±5% Supply Voltage

CHIPS

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82C301, 82C302, 82A303, 82A304, 82A305, 82A306
CS8230: AT/386 CHIPSet™

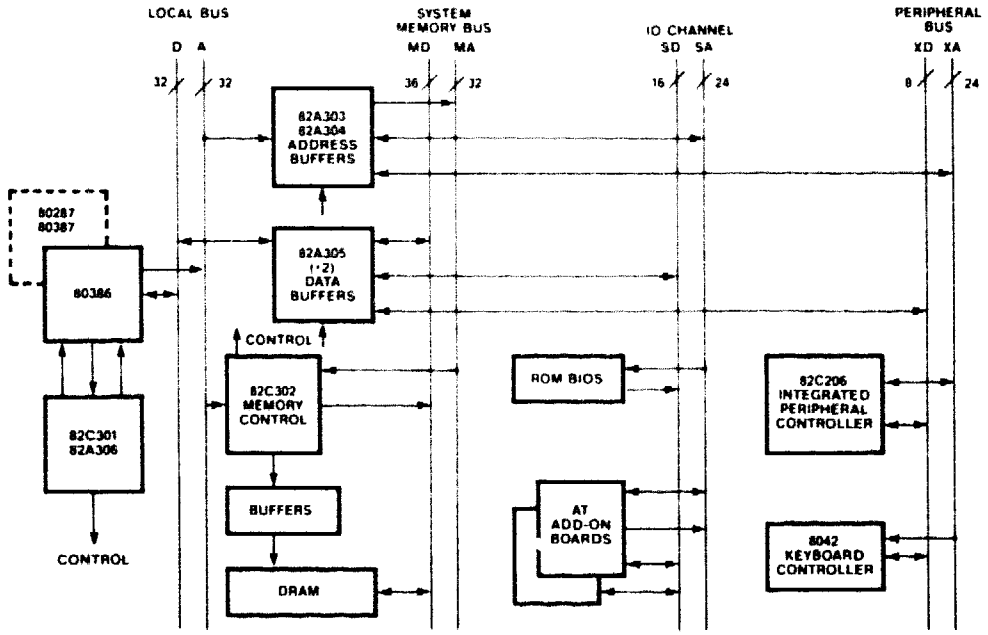
- **100% IBM™ PC AT compatible**
- **Flexible architecture allows usage in any iAPX 386™ design**
- **Operates in Page mode with Interleave memory subsystem**
- **16 MHz zero wait operation**
- **Independent clock to support correct AT bus timing**
- **1MB to 16MB of DRAM memory support**
- **A complete PC AT requires only 40 IC's plus memory**

The CS8230 AT/386 CHIPSet™ is a seven chip VLSI implementation of most of the system logic to control an iAPX 386 based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIP's 82C206 Integrated Peripherals Controller provides a complete PC AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet™ consists of one 82C301 Bus Controller, one 82C302 Page/Interleave MemoryController, one each of 82A303 and 82A304 Address Bus Interfaces, two 82A305 Data Bus Interfaces, and a 82A306 Control Signal Buffer.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram below. The 82C301 and 82A306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock, and allows for dynamic selection of the processor clock between the 16 MHz clock and the AT bus clock. The



AT/386 System Block Diagram

82A306 provides buffers for bus control signals in addition to other miscellaneous logic functions

The 82C302 Page/Interleave Memory Controller provides an interleaved memory subsystem design with page mode operation It supports 1 MB to 16 MB of DRAMs with combinations of 256Kbit and 1Mbit DRAMs The processor can operate at 16 MHz with zero wait state memory accesses by using 100 nsec DRAMs

The 82A303 and 82A304 interface between all address buses generate RAS/CAS addresses for the system memory and the addresses needed for proper data path conversion Two 82A305 are used to interface between the local system memory and AT data buses In addition to having high current drive they also perform the conversion necessary between the different sized data paths

System Overview

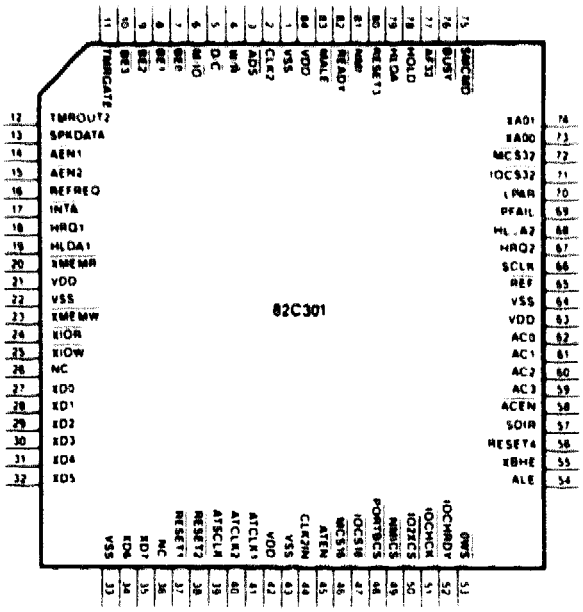
The CS 8230 is designed for use in 80386-based systems and provides complete support for the IBM PC AT bus. There are four buses supported by the CS 8230 as shown in the AT/386 system block diagram: CPU local bus (A and D), system memory bus (MA and MD), IO Channel bus (SA and SD), and X bus (XA and XD). The system memory bus is used to interface to DRAM's controlled by the 82C302. The IO channel bus refers to the bus supporting the AT bus adapters which could be either a 8 bit devices or 16 bit devices. The X bus refers to the peripheral bus to which the DMA controllers and timers are attached in an IBM PC AT. The X bus has only an 8-bit data path. The term "AT bus" is used to refer to the IO channel bus and X bus. Provisions are also made for user extension of the IO channel to 32 bit bus.

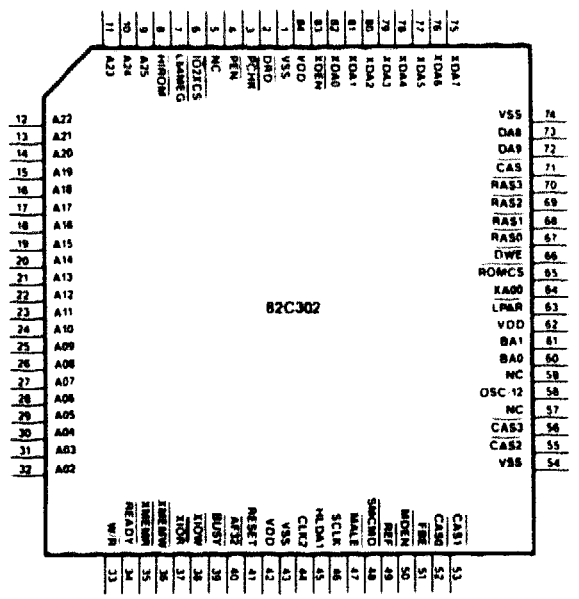
Notation and Glossary

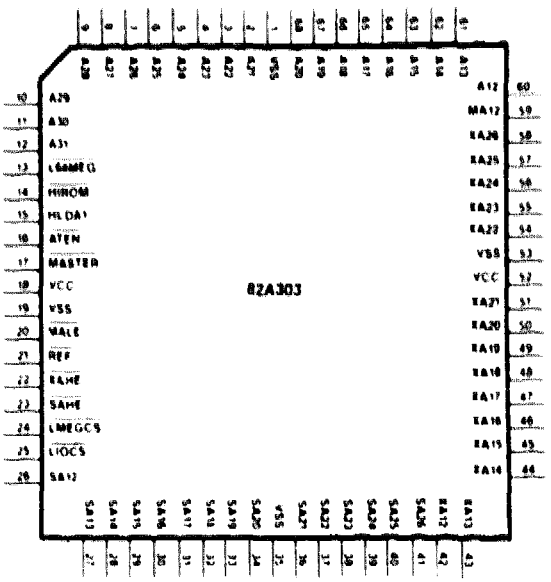
The following notations are used to refer to the configuration and diagnostic registers internal to the 82C301 and 82C302.

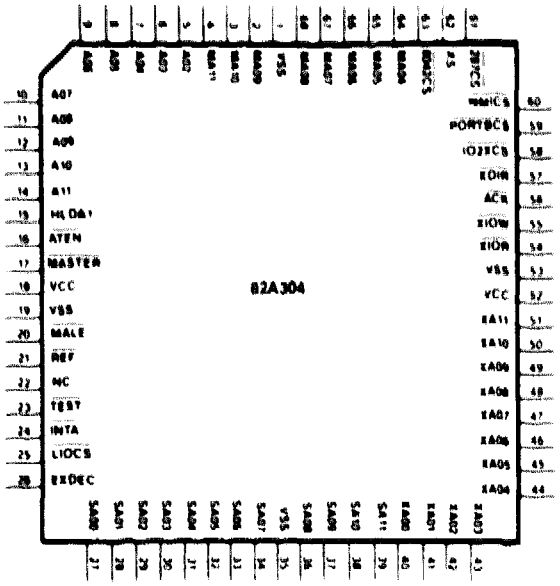
REGnH denotes the internal register with the index n in hexadecimal notation.

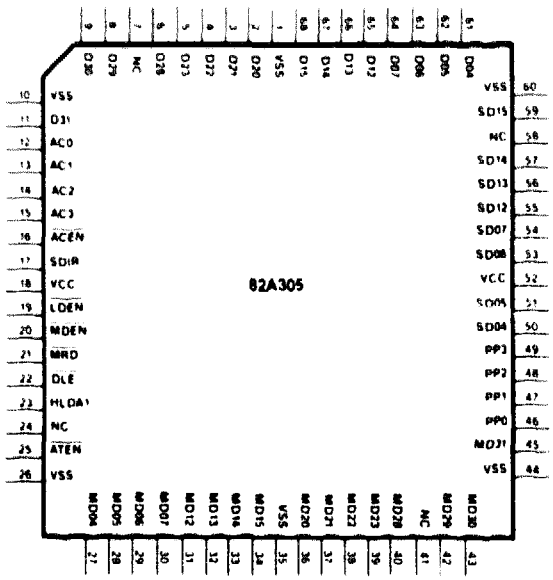
REGnH<x:y> denotes the bit field from bits y to x of the internal register with the index n in hexadecimal notation.

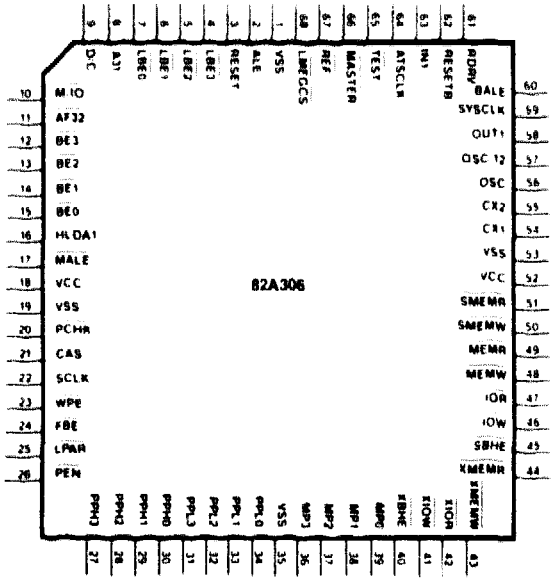

82C301
TIMRGATE2
TIMROUT2
SPKDATA
AEN1
AEN2
REFREQ
INTA
HRQ1
HLDA1
XMEMR
VDD
VSS
XMEMW
XIOR
XIOW
NC
XD0
XD1
XD2
XD3
XD4
XD5
SDCMD
BUSY
HOLD
HLDA
RESET1
CLK2
ADS
DIC
M/IO
REF
BE1
BE2
BE3
TIMRGATE1
XA01
XA00
MCS32
IOCS32
LPWR
PFAIL
HLDA2
HRQ2
SCLK
REF
VSS
VDD
AC0
AC1
AC2
AC3
ACEN
SOIR
RESET4
XBHE
ALE
IOCHRDY
OWS
IOCHCK
IOZCS
MRDCS
PORTBCS
IOCS16
MCS16
ATEN
CLK2N
VSS
VDD
ATCLK1
ATCLK2
ATSCLK
RESET2
RESET3
NC
XD7
XD6
XD5
VSS


82C302
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A09
A08
A07
A06
A05
A04
A03
A02
XDA1
XDA6
XDA5
XDA4
XDA3
XDA2
XDA1
XDA0
XDEN
VSS
VDD
DRD
PCHR
REN
NC
IOZCS
LMEG
HIMEM
A25
A24
A23
VSS
DA8
DA9
CAS
RAS3
RAS2
RAS1
RAS0
DWE
ROMCS
XA00
LPWR
VDD
BA1
BA0
NC
OSC-12
NC
CAS3
CAS2
VSS
CAS1
CAS0
FRE
MDEN
REF
SDCMD
SCLK
HLDA1
CLK2
VSS
VDD
RESET
XFER
BUSY
XIOW
XIOR
XMEMW
XMEMR
READY
W/R


82A303
A29
A30
A31
LGAMEG
HIROM
HLDA1
ATEN
MASTER
VCC
VSS
MALE
REF
BAHE
SAHE
LMEGCS
LIOCS
SA12
A12
MA17
EA26
EA25
EA24
EA23
EA22
VSS
VCC
EA21
EA20
EA19
EA18
EA17
EA16
EA15
EA14
EA13


82A304
A07
A08
A09
A10
A11
HLDA1
ATEN
MASTER
VCC
VSS
MALE
REF
NC
TEST
INTA
LIOCS
EXDEC
A12
A13
A14
A15
A16
A17
A18
A19
VSS
VCC
EA11
EA10
EA09
EA08
EA07
EA06
EA05
EA04
EA03


82A305
VSS
D31
AC0
AC1
AC2
AC3
ACEN
SDIR
VCC
LDEN
MDEN
MRD
DLE
HLDA1
NC
ATEN
VSS
VSS
SD15
NC
SD14
SD13
SD12
SD07
SD08
VCC
SD05
SD04
PP3
PP2
PP1
PP0
MD31
VSS


82A306
M IO
AF32
BE3
BE2
BE1
BE0
HLDA1
MALE
VCC
VSS
PCHR
CAS
SCLK
WPE
FBE
LPAR
PEN
BALE
SYSCLK
OUT1
OSC 12
OSC
CX2
CX1
VSS
VCC
SMEMR
SMEMW
MEMR
MEMW
IOR
IOW
SBHE
XMEMR
XIOR

82C301 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks			
44	CLK2IN	I	CLOCK 2 INPUT from a packaged TTL crystal oscillator having twice the rated frequency of the processor.
2	CLK2	O	CLK2 output to the Clock 2 input of 80386 and the memory controller. This clock output is derived from CLK2IN and has a 50% duty cycle. The clock can also be programmed to be the same as the BCLK.
66	SCLK	O	SCLK is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock and CLK2.
41	ATCLK1	I	BUS CLOCK INPUT source from Crystal or Oscillator. This clock input is used for the AT Bus operation and is required only if the AT bus state machine clock (BCLK) will not be derived from the CLK2 input. This signal should be tied LO if not used.
40	ATCLK2	O	BUS CLOCK CRYSTAL OUTPUT is connected to the crystal oscillator circuit if a packaged oscillator is not used. A series resistor should be used to reduce the amplitude of the resonant circuit. It should be left unconnected if a packaged TTL oscillator is used.
39	ATSCLK	O	AT SYSTEM CLOCK is buffered to drive the clock signal SYSCLK on the AT bus I/O channel. It is half the frequency of BCLK and should have a nominal value in the range of 6 to 8 MHz for maintaining correct AT I/O bus timing with IBM PC AT.
Control			
37	$\overline{\text{RESET1}}$	I	Active LO. $\overline{\text{RESET1}}$ is connected to the power good signal generated by the PWRGOOD from the power supply. When LOW it will activate RESET3 and RESET4 for resetting the system.
38	$\overline{\text{RESET2}}$	I	Active LO. $\overline{\text{RESET2}}$ (8042RC) is an active LOW signal generated from the keyboard controller 8042 for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3 signal.
56	RESET4	O	Active HI. RESET4 is the System Reset used to reset the AT Bus, 82C206 IPC, 8042 keyboard controller 82C302 or 82C312 memory controller. RESET4 is synchronized with the processor clock.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
CPU Interface			
80	RESET3	O	Active HI. RESET3 is the reset to the 80386 when RESET1 or RESET2 is active. This is also activated when shutdown condition in the CPU is detected.
82	READY	I/O	Active LO. READY is driven LO during AT bus cycles indicating that the current CPU bus cycle is to be completed. It is also asserted if 'Time Out' condition is detected. During all other cycles it is an input to 82C301. Ready is an open collector output requiring an external pull up resistor. It connects to the 80386 READY pin.
3	ADS	I	Active LO. ADDRESS STATUS input connected to the 80386 ADS pin.
4	W/R	I/O	READ/WRITE STATUS input from the 80386 W/R signal. It indicates a write bus cycle if it is HI and a read cycle if it is LO.
5	D/C	I	DATA/CONTROL STATUS input from the 80386 D/C signal.
6	M/IO	I	MEMORY/IO STATUS input from the 80386 M/IO signal.
78	HOLD	O	Active HI. HOLD REQUEST output to the 80386 HOLD input pin. This signal is used to request the CPU to relinquish the bus cycles to another requesting master such as HRQ1, HRQ2 and REFREQ.
79	HLDA	I	Active HI. HOLD ACKNOWLEDGE input connected to processor HLDA signal. When the signal is HIGH it indicates that the processor has relinquished the system bus in response to the HOLD request.
10-7	BE<3:0>	B	Active LO. BYTE ENABLE signals input from the 80386 BE<3:0> during a CPU cycle. BE3 controls the most significant while BE0 controls the least significant byte. BE<3:0> are generated by 82C301 during DMA cycles based on the status signals XA0, XA1 and XBHE.
81	NMI	O	Active HI. NON-MASKABLE INTERRUPT connects to the 80386 NMI pin and is generated by 82C301 to cause an NMI.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Decodes			
48	PORTBCS	I	Active LO PORT B CHIP SELECT is the address decode input from the 82A304 as enable for the Port B register at address 061H
49	NMICS	I	Active LO NMI CHIP SELECT is the address decode input from the 82A304 as enable for the NMI enable bit at address 070H
50	IO2XCS	I	Active LO IO2X CHIP SELECT is the address decode input from the 82A304 as chip select for the IO registers at 022H and 023H used to access the 82C301 internal configuration registers
53	0WS	I	Active LO ZERO WAIT STATE acknowledge input from the IO channel When active it causes immediate termination of the current AT bus memory or IO cycle
IO Channel Interface			
52	IOCHRDY	I	Active HI IO CHANNEL READY input from the AT bus When LOW it indicates a 'not ready' condition and forces the insertion of wait states in I/O or memory accesses When HIGH it will allow the completion of the current memory or I/O access
51	IOCHCK	I	Active LO IO CHANNEL CHECK input from the AT bus which causes an NMI to be generated if enabled It is used to signal an Error condition from a device residing on the AT bus
70	LPAR	I	Active LO PARITY ERROR input from local memory system which causes an NMI to be geneated if enabled
69	PFAIL	I	Active LO POWER FAIL WARNING signal input from the power supply
54	ALE	O	Active HI ADDRESS LATCH ENABLE to AT bus This signal controls the address latches used to hold the address during a bus cycle The signal should be buffered to drive the AT bus
DMA Interface			
19	HLDA1	O	Active HI HOLD ACKNOWLEDGE 1 is active when a bus cycle is granted in response to HRQ1
68	HLDA2	O	Active HI HOLD ACKNOWLEDGE 2 is active when a bus cycle is granted in response to HRQ2

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
18	HRQ1	I	Active HI HOLD REQUEST 1 is active when a DMA/ Master is requesting a bus cycle. For an AT compatible architecture it should be connected to the HOLD REQUEST signal from DMA1 and DMA2.
67	HRQ2	I	Active HI HOLD REQUEST 2 is active when a DMA/ Master is requesting a bus cycle. This should be grounded if not used.
14	AEN1	I	Active LO ADDRESS ENABLE for 8 bit DMA transfers.
15	AEN2	I	Active LO ADDRESS ENABLE for 16 bit DMA transfers.
Control Strobes			
46	MCS16	I	Active LO MCS16 When active causes 16 bit memory accesses on IO channel.
72	MCS32	I	Active LO MCS32 when active causes 32 bit memory accesses on IO channel.
47	IOCS16	I	Active LO IOCS16 when active causes 16 bit IO accesses on IO channel.
71	IOCS32	I	Active LO IOCS32 when active causes 32 bit IO accesses on IO channel.
75	SMCMD	O	Active LO SYSTEM MEMORY COMMAND when active indicates the current access cycle is a memory cycle.
Refresh			
16	REFREQ	I	Active HI REFresh REQuest when active initiates a DRAM refresh sequence be initiated. This signal is obtained from the timer controller, 8254, in a PC AT implementation.
65	REF	I/O	Active LO REFresh is an open drain signal. It initiates a refresh cycle for the DRAMs. As an input it can be used to force a refresh cycle from an I/O device. An external pull up is required.
X Bus Interface			
20	XMEMR	I/O	Active LO X BUS MEMORY READ is a control strobe directing memory to place data on the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	XMEMW	I/O	Active LO X BUS MEMORY WRITE is a control strobe directing memory to accept data from the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.
24	XIOR	I/O	Active LO X BUS IO READ is a control strobe directing an IO port to place data on the data bus. It is sourced either from the 82C301 when the 80386 is the master or from the DMA.
25	XIOW	I/O	Active LO X BUS IO WRITE is a control strobe directing an IO port to accept data from the data bus. It is sourced either from the 82C305 when the 80386 is the master or from the DMA.
55	XBHE	I/O	Active LO X BUS BYTE HIGH ENABLE indicates that the high byte (bits <15 08>) on the bus has valid data. It is sourced from the 82C301 when 80386 or DMA2 (16 bit) is the master.
35-34	XD<7 6>	I/O	X DATA BUS bits <7 6>
32-27	XD<5 0>	I/O	X DATA BUS bits <5 0>
57	SDIR	O	SYSTEM BUS DIRECTION controls the direction of data transfer between the IO channel and the local bus. When LO the it enables data transfer from the IO channel to local bus.
58	ACEN	O	Active LO ACTION CODE ENABLE when active validates the action code signals AC<3 0>
59-62	AC<3 0>	O	ACTION CODE is a four-bits encoded command for bus size control and byte assembly operations performed by the 82A305s.
Memory Control			
77	AF32	I	Active LO AF32 when active indicates that a bus cycle is a local bus access without any data size conversion or AT cycle simulation treated as a 32-bit access.
76	BUSY	I	Active LO BUSY from memory controller.
83	MALE	O	Active LO Address Latch Enable for accesses to on board memory/IO. It also indicates start of a new CPU cy[illegible].
11	TMRGATE	O	Active Hi TIMER GATE signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
12	TMROUT2	I	Active HI. TIMER OUT 2 is the output from the timer 8254. It can be read from port B.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
13	SPKDATA	O	Active HI SPEAKER DATA is used to gate the 8254 tone signal to the speaker.
17	INTA	O	Active LO. Interrupt acknowledge output to the interrupt controller.
45	ATEN	O	Active LO AT ENABLE when active indicates the current CPU access is an AT bus cycle.
73	XA00	I/O	Address bit 0. It is sourced from the 82C301 when 80386 or DMA (16 bit) is a bus master.
74	XA01	I/O	Address but 1. It is sourced from the 82C301 when 80386 is a bus master.
26,36	NC		Reserved
21,42 63,84	VDD VDD		Power
1 22,33 43,64	VSS VSS VSS		Ground

82C302 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks and Control			
44	CLK2	I	Processor Clock
46	SCLK	O	Generated CLK2/2 for reference
41	RESET	I	Active HI. When active resets 82C302
49	REF	I	Active LO. DRAM refresh control signal.
47	MALE	I	Active LO. Address Latch Enable
33	W/R	I	System WRITE/READ status input
48	SMCMD	I	Active LO. System Memory Command. Indicates that the current command is for memory.
37	XIOR	I	Active LO. I/O READ command used to qualify IO2XCS
38	XIOW	I	Active LO. I/O WRITE command used to qualify IO2XCS
35	XMEMR	I	Active LO. X Bus memory READ command.
36	XMEMW	I	Active LO. X Bus memory WRITE command.
45	HLDA1	I	Active HI. HOLD ACKNOWLEDGE 1 input from 82C301.
63	LPAR	I	Active LO. Parity error indication during a DRAM read. The failing address will be latched inside the chip for diagnostic purposes.
8	HIROM	I	Active LO. High ROM address chip select asserted when the highest 16 MBytes of memory is addressed (A<31:A24>=FFH). Unlatched. This is used in conjunction with the remaining address bits to generate the ROMCS signal.
7	L64MEG	I	Active LO. Low 64M address that is asserted when A<31:26>=00H. Unlatched.
65	ROMCS	O	Active LO. Chip select for the BIOS EPROMs that is qualified with W/R and SMCMD.
6	IO2XCS	I	Active LO. IO address 22 and 23 chip selects. I/O port 22 is the index register for the configuration register set and and I/O 23 is accessed as the 8 bit configuration register selected by the index written to I/O port 22.
09-32	A<25:02>	I	Address from the CPU local bus.
64	XA00	I	Address from the X Bus.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
34	$\overline{\text{READY}}$	I/O	Active LO. System ready indicating the end of current 386 bus cycle. It goes inactive when the requested memory transfer has been completed. It becomes an input when the current bus cycle is for the AT IO expansion channel ($\overline{\text{AF32}}$ = 0).
39	$\overline{\text{BUSY}}$	O	Active LO. Indicates that the memory controller is still servicing a previous request. This should be connected to IOCHRDY through an open collector buffer. This signal should not be confused with the BUSY of 80386.
40	$\overline{\text{AF32}}$	O	Active LO, open drain. If asserted indicates that the current address is for local memory on the system board (DRAM or possibly EPROM). Otherwise the current address is assumed to be on the AT IO channel.
Memory Expansion			
61-60	BA<1 0>	O	Addresses that may be externally decoded to gate RAS to the correct block of 4 banks of DRAMs. These will always be zero.
2	$\overline{\text{DRD}}$	O	Active LO. DRAM Read controls the direction of data transfer between the DRAM and local bus. When LO it controls the transfer from the memory data bus toward CPU and from the CPU to memory otherwise.
DRAM Interface			
70-67	$\overline{\text{RAS}}$<3 0>	O	Active LO. Row Address Strobe. There is one for each bank.
71	$\overline{\text{CAS}}$	O	Active LO. Column Address Strobe. Used to latch data in the 82A305 data buffer.
56-55 53-52	$\overline{\text{CAS}}$<3 2> $\overline{\text{CAS}}$<1 0>	O	Active LO. Column Address Strobe. A strobe per bank that must be externally gated with byte enables for each byte of DRAM chips.
58	OSC/12	I	1.19MHz Clock input used for RAS pulse width time-out. Replaces CA3 on Cache controller.
66	$\overline{\text{DWE}}$	O	Active LO. DRAM Write Enable.
51	$\overline{\text{FBE}}$	O	Active LO. Force Byte Enable. Will always be inactive.
72-73	DA<9:8>	O	Remaining DRAM address bits.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
75-82	XDA<7:0>	I/O	Multiplexed bidirectional data pins for XD<7:0>. DA<7:0> are the lower address bits for the DRAM array
83	$\overline{XDEN}$	O	Active LO. XD bus buffer Enable. $\overline{XDEN}$ is asserted during IO access cycles to 022H and 023H if 022H access is for an internal register of 82C302. $\overline{XDEN}$ is used to control the chip enable for the buffer between the XD and XDA buses
3	$\overline{PCHK}$	O	Active LO. Parity Check Strobe
4	$\overline{PEN}$	O	Active LO. Overall Parity Enable
50	$\overline{MDEN}$	O	Active LO. MEMORY DATA BUFFER ENABLE. This signal is by default always LO and is connected to $\overline{MDEN}$ of 82A305
Miscellaneous			
5,57,59	NC		Reserved
42,62,84	VDD		Power
1,43 54,74	VSS VSS		Ground

82A303 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	MASTER	I	Active LO. Bus MASTER is generated by a device that is active on the expansion bus. After MASTER is force LO by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. MASTER must not be held LO for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.
15	HLDA1	I	Active HI. HOLD ACKNOWLEDGE from 82C301.
20	MALE	I	Active LO. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising edge.
21	REF	I	Active LO. REFRESH. Schmitt Trigger
16	ATEN	I	Active LO. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	LIOCS	O	Active LO. LOW IO ADDRESS CHIP SELECT is asserted when A<15:12>=0.
24	LMEGCS	O	Active LO. LOW 1 MB SELECT is active when the access address decodes to the low 1MB address space. A<31:20> = 0.
13	L64MEG	O	Active LO. LOW 64 MB SELECT is active when the access address decodes to the low 64MB address space. A<31:26> = 0.
14	HIROM	O	Active LO. HI ROM SELECT is active when A<31:26> = 3FH.
Processor/Bus Interface			
12-2	A<31:21>	I/O	Local Address Bus
68-60	A<20:12>	I/O	
58-54	XA<26:22>	I/O	X Address Bus
51-42	XA<21:12>	I/O	
22	XAHE	I	Active LO. Enable bits 26:24 from the XA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
41-36	SA<26:21>	I/O	24mA. System Address Bus
34-26	SA<20:12>	I/O	

82A303 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	$\overline{SAHE}$	I	Active LO Enable bits 26:24 from the SA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
59	MA12	O	Memory Address Bus Latched on the trailing edge of MALE
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A304 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active LO. BUS MASTER is generated by a device active on the expansion bus.
15	HLDA1	I	Active HI. HOLD ACKNOWLEDGE 1 from 82C301.
20	$\overline{\text{MALE}}$	I	Active LO. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising (trailing) edge.
21	$\overline{\text{REF}}$	I	Active LO. REFRESH Schmitt trigger.
16	$\overline{\text{ATEN}}$	I	Active LO. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	I	Active LO. LOW IO ADDRESS CHIP SELECT.
54	$\overline{\text{XIOR}}$	I	Active LO. X BUS IO Read.
55	$\overline{\text{XIOW}}$	I	Active LO. X BUS IO Write.
57	$\overline{\text{XDIR}}$	O	X BUS DIRECTION is used to control the drivers between the X bus and S bus. The drivers should be used such that S bus signals are driven toward X bus when XDIR is LO and in the other direction when HI.
26	EXDEC	I	Active HI. EXTENDED IO DECODE. A strapping option that when LO ignores A<11:10> and $\overline{\text{LIOCS}}$ (which is decoded based on A<15:12>) for decoding the system board IO ports. An internal pullup is provided.
58	$\overline{\text{IO2XCS}}$	O	Active LO. IO 2x SELECT is decode of IO address 022H or 023H.
63	$\overline{\text{8042CS}}$	O	Active LO. 8042 SELECT is decode of 8042 address at 060H or 064H.
59	$\overline{\text{PORTBCS}}$	O	Active LO. PORTB SELECT is decode of Port B address at 061H.
60	$\overline{\text{NMICS}}$	O	Active LO. NMI SELECT is decode of NMI address at 070H.
61	$\overline{\text{287CS}}$	O	Active LO. 80287 SELECT is decode of 287 address at 0E0-0FFH.
56	$\overline{\text{ACK}}$	O	Active LO. ACKNOWLEDGE indicates that AEN1 OR AEN2 has been asserted. This signal is used to generate AEN signal on the AT I/O channel.
62	AS	O	Active HI. Address Strobe for the RTC. IO address 7xH is conditioned with XIOW.

82A304 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
24	$\overline{\text{INTA}}$	I	Active LO INTERRUPT ACKNOWLEDGE bus cycle indication
Processor/Bus Interface			
14-5	A<11 02>	I/O	Local address
51-40	XA<11 00>	I/O	X bus address
39-36	SA<11 08>	I/O	24mA System address
34-27	SA<07 00>	I/O	
4-2	MA<11 09>	O	Memory address
68-64	MA<08 04>	O	
23	$\overline{\text{TEST}}$	I	Active LO TEST when active resets the refresh counter to zero A pullup is provided
22	NC		Reserved
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A305 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
15-12	AC<3:0>	I	Action Code (bus size/assembly command)
16	ACEN	I	Active LO. Action Code Enable when active validates the action codes.
17	SDIR	I	System bus DIRection. When LO enables data transfers from the System to Local busn and in the other direction otherwise.
25	$\overline{\text{ATEN}}$	I	Active LO. AT bus ENable
23	HLDA1	I	Active HI. HoLD Acknowledge.
20	$\overline{\text{MDEN}}$	I	Active LO. MEMORY DATA BUFFER ENABLE. When LO enables the memory data buffers for transfer between the processor and memory subsystem. When HI disables these bus buffers. Should be connected to $\overline{\text{MDEN}}$ on the 82C302.
19	$\overline{\text{LDEN}}$	I	Active LO. Selects LD as a source for the SD bus during MASTER or DMA reads. When HI selects MD. Asserting $\overline{\text{MRD}}$ overrides $\overline{\text{LDEN}}$ and gates MD to the SD bus. A pullup is provided.
21	$\overline{\text{MRD}}$	I	Active LO. Memory Bus DIRection. When LO enables data movement for a processor read from the memory to local bus. $\overline{\text{MRD}}$ when HI enables drivers from local to memory bus.
22	$\overline{\text{DLE}}$	I	Active LO. Data Latch Enable.
Data Paths (Bit numbers are for the upper 4 bits slice of each byte and should be 4 less for the lower nibble slice).			
11, 9	D<31:30>	I/O	
8, 6	D<29:28>	I/O	
5-2	D<23:20>	I/O	Local Data Bus
68-65	D<15:12>	I/O	
64-61	D<07:04>	I/O	
45,43	MD<31:30>	I/O	
42,40	MD<29:28>	I/O	
39-36	MD<23:20>	I/O	Memory Data Bus
34-31	MD<15:12>	I/O	
30-27	MD<07:04>	I/O	
49-46	PP<03:00>	O	Memory Partial Parity

82A305 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
59,57	SD<15:14>	I/O	IO Channel Data Bus
56,55	SD<13:12>	I/O	
54-53	SD<07:06>	I/O	
51-50	SD<05:04>	I/O	
7,24	NC		Reserved
41,58	NC		
Power Supplies			
18,52	VCC		Power
1,10	VSS		Ground
26,35	VSS		
44,60	VSS		

82A306 Pin Description

Pin No.	Symbol	Pin Type	Description
64	ATSCLK	I	AT IO channel SYSCLK input.
59	SYSCLK	O	24mA. Buffered SYSCLK to AT IO channel. Nominally one half of the bus state machine clock frequency.
Control			
54	CX1	I	14.318MHz oscillator input from crystal.
55	CX2	O	14.318MHz oscillator output to crystal.
56	OSC	O	24mA. System 14.318MHz output.
57	OSC/12	O	24mA. 14.318MHz/12 = 1.19MHz output.
17	$\overline{\text{MALE}}$	I	Active LO. Address Latch Enable for on board access.
12-15	$\overline{\text{BE}}$<3:0>	I	Active LO. BYTE ENABLE.
4-7	$\overline{\text{LBE}}$<3:0>	O	Active LO. LATCHED BYTE ENABLE on the trailing edge of $\overline{\text{MALE}}$.
24	$\overline{\text{FBE}}$	I	Active LO. FORCE BYTE ENABLE Forces all byte enables $\overline{\text{LBE}}$ active independent of $\overline{\text{MALE}}$ and the $\overline{\text{BE}}$<3:0> inputs.
67	$\overline{\text{REF}}$	I	Active LO. REFRESH.
8	A<31>	I	Local Address Bus bit 31.
10	M/$\overline{\text{IO}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
9	D/$\overline{\text{C}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
68	$\overline{\text{LMEGCS}}$	I	Active LO. LOW MEGABYTE CHIP SELECT.
11	$\overline{\text{AF32}}$	O	Active LO, Tri-state output. $\overline{\text{AF32}}$ when active indicates a local bus memory access cycle on the system board. It is generated from M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, A<31>, and HLDA1.
66	$\overline{\text{MASTER}}$	I	Active LO. Bus MASTER input from the AT IO channel.
3	RESET	I	Active HI. RESET input. Should be connected to RESET4 of 82C301.
62	RESETB	O	Active HI. Buffered RESET to X bus.
61	RDRV	O	Active HI. 24mA. RESET to AT bus.
2	ALE	I	Active HI. ALE for AT bus.
40	$\overline{\text{XBHE}}$	I/O	Active LO. X Bus BHE.
44	$\overline{\text{XMEMR}}$	I/O	Active LO. X Bus Memory Read.
43	$\overline{\text{XMEMW}}$	I/O	Active LO. X Bus Memory Write.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
42	$\overline{XIOR}$	I/O	Active LO. X Bus IO Read.
41	$\overline{XIOW}$	I/O	Active LO. X Bus IO Write.
60	BALE	O	Active HI. 24mA. Buffered ALE to AT bus.
45	$\overline{SBHE}$	I/O	Active LO. 24mA. System bus BHE.
51	$\overline{SMEMR}$	O	Active LO. 24mA. System bus MEMory Read.
50	$\overline{SMEMW}$	O	Active LO. 24mA. System bus MEMory Write.
49	$\overline{MEMR}$	I/O	Active LO. 24mA. Memory Read.
48	$\overline{MEMW}$	I/O	Active LO. 24mA. Memory Write.
47	$\overline{IOR}$	I/O	Active LO. 24mA. IO Read.
46	$\overline{IOW}$	I/O	Active LO. 24mA. IO Write.
16	HLDA1	I	Active HI. HOLD ACKNOWLEDGE from 82C301.
22	SCLK	I	CLK2/2 clock input. Should be connected to SCLK output of 82C302.
27-30	PPH<3:0>	I	PARTIAL PARITY HIGH computed by 82A305 for the high nibble data bits.
31-34	PPL<3:0>	I	PARTIAL PARITY LOW computed by 82A305 for the low nibble data bits.
36-39	MP<3:0>	I/O	Data Parity bits for the DRAMs.
21	$\overline{CAS}$	I	Active LO. Read Parity latch enable.
20	$\overline{PCHK}$	I	Active LO. PARITY CHECK STROBE for generating $\overline{LPAR}$ from the partial parity and data parity bits.
26	$\overline{PEN}$	I	Active LO. Overall PARITY CHECK ENABLE.
23	$\overline{WPE}$	I	Active LO. WRITE PARITY ENABLE. Enables the sourcing of write parity onto the MP bus. A pullup is provided.
25	$\overline{LPAR}$	O	Active LO. LATCHED PARITY ERROR signal.
65	$\overline{TEST}$	I	Active LO. Enables testing of the OSC/12 counter. A pullup is provided.
63	IN1	I	Input to an uncommitted 24mA non-inverting buffer.
58	OUT1	O	24mA. Output of the IN1 buffer.
Power Supply			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82C301 BUS CONTROLLER

- Optional Independent AT Bus Clock
- Processor Clock Selection
- AT Bus Timing Configuration
- CPU Interface and Bus Control
- Port B Register

OVERVIEW

The 82C301 provides a clock generation circuitry to solve two basic problems. One is to provide system designers the choice of a particular AT bus clock most adequate for their applications. The other is to allow the processor to run at the full speed and optionally at a speed to match timing dependent application software. Because many AT adapter boards are designed with built in timing assumptions, independent programmable controls are provided for AT bus command timing and wait state generation for IO accesses and for 8, 16, and 32 bit memory accesses.

The 82C301 interfaces directly with the 80386 and implements the state machines required for controlling all bus accesses. It also features a status register known as Port B register used in a standard IBM PC AT.

FUNCTIONAL DESCRIPTION

The 82C301 has the following function blocks as illustrated in figure 1-1:

- Clock generation and reset control
- CPU bus access state machine
- AT bus access state machine
- Port B register and NMI logics
- Bus Arbitration and refresh logic

Clock Generation and Reset Control

The 82C301 provides three major system clocks: the processor clock CLK2, the BCLK clock for AT bus state machine of 82C301, and the AT bus clock SYSCLK. The BCLK (SYSCLK * 2) is a clock internal to the 82C301 and is used in this document to describe the system operation.

The clock generation circuitry shown in figure 1-2 contains two external clocks CLK2IN and ATCLK1 used as selectable clock sources. CLK2IN is assumed to be greater than 20MHz and should come from a packaged crystal oscillator while an oscillator circuit is provided for the ATCLK1 signal so that it can be connected to either a packaged oscillator or a crystal. This ATCLK1 input is required only if BCLK need be derived from an independent clock source other than CLK2IN. When required ATCLK1 frequency should be between 10 and 20 MHz for a typical PC AT. Notice that by design SYSCLK is always the BCLK divided by two.

The clock switching logic is guaranteed to provide a "clean" transition with no phases shorter than the minimum values or longer than the maximum values. This allows the clock selections be done dynamically.

Processor clock selection

Referring to figure 1-2, the CLK2 and SCLK signal can be selected from two sources:

—the external oscillator connected to CLK2IN,
—the AT bus state machine clock BCLK.

This selection is made by programming bit 4 of the configuration register 4 which defaults to CLK2IN upon reset. By design, if SCLK is selected as the source for BCLK, CLK2 must not be sourced from BCLK. In all but some special cases, CLK2IN should match the rated processor speed, and the BCLK can be either subdivisions of CLK2IN or ATCLK1.

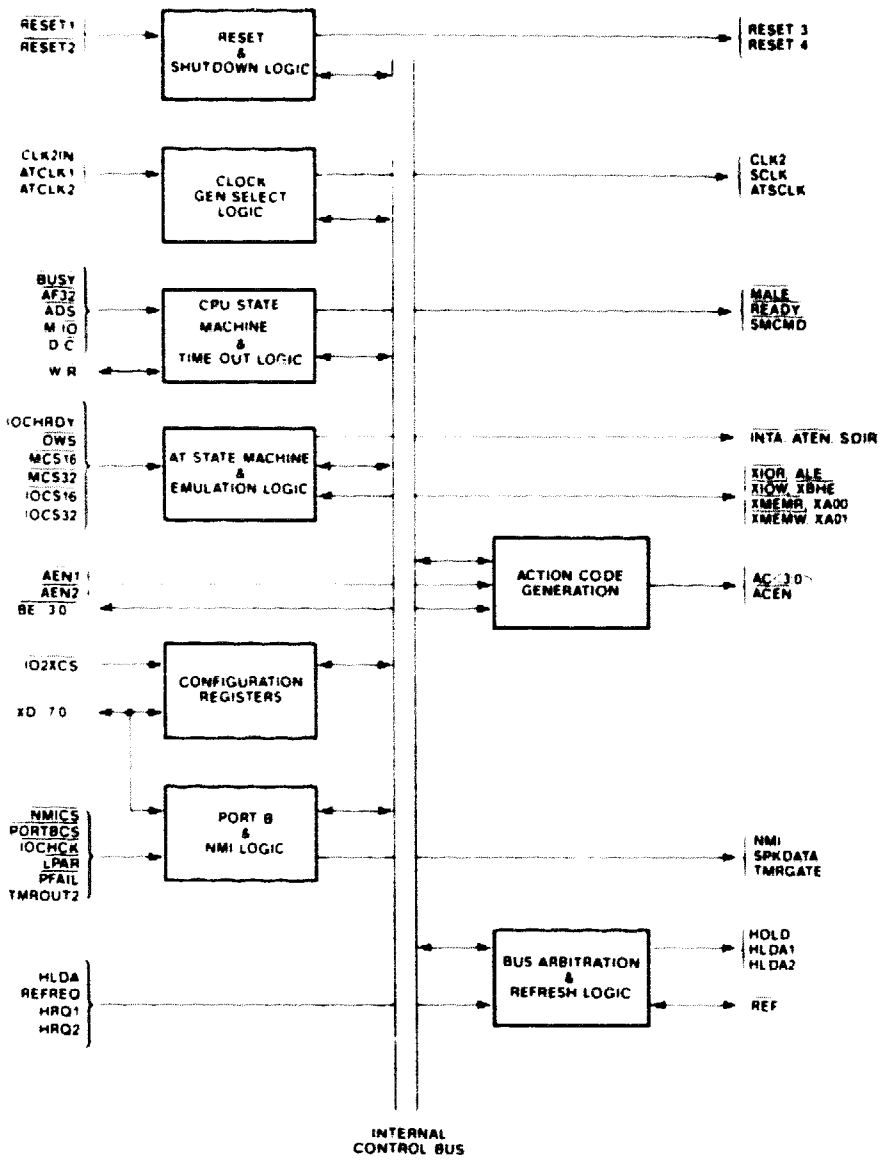


Figure 1-1. 82C301 Functional Block Diagram

AT bus clock selection

The 82C301 provides flexible software controlled selection of the clock used for the AT bus state machine. The clock can be synchronous (related but not necessarily equal) to the processor CLK2 or unrelated (requiring synchronization between the AT and processor bus state machines). While synchronization logic has been provided in all interface signals between the CPU and the AT state machines, it is highly recommended that the AT bus state machine clock (BCLK) be sourced from SCLK. An internal programmable divider has been provided allowing BCLK frequency of CLK2/2 or CLK2/3. This eliminates the need for an additional oscillator for some system designs. If the divide by 3 option is selected the resulting waveform will have an approximately 50% duty cycle.

The SYSCLK signal generated by the 82C301 is one half of the AT bus state machine clock BCLK. Since this clock is used to drive the AT bus, it is recommended that the the divide ratio be set for a SYSCLK of about 6 and 8MHz. The table 1-1 shows the combination of clock frequencies obtainable from CLK2IN with this selection scheme.

CLK2IN	SCLK	Ratio	BCLK	SYSCLK
24	12	/2	12	6
32	16	/2	16	8
32	16/3	10.7	5.4	

Table 1-1. Examples of BCLK and SYSCLK derived from CLK2

Reset control

When $\overline{\text{RESET1}}$ signal is asserted 82C301 asserts RESET3 and RESET4 for a system reset. For warm restart not requiring the extensive reset, $\overline{\text{RESET2}}$ can be asserted to generate the RESET3 for resetting only the processor and some specific devices. RESET3 is also asserted when CPU shut down condition is detected. This differentiation of reset is

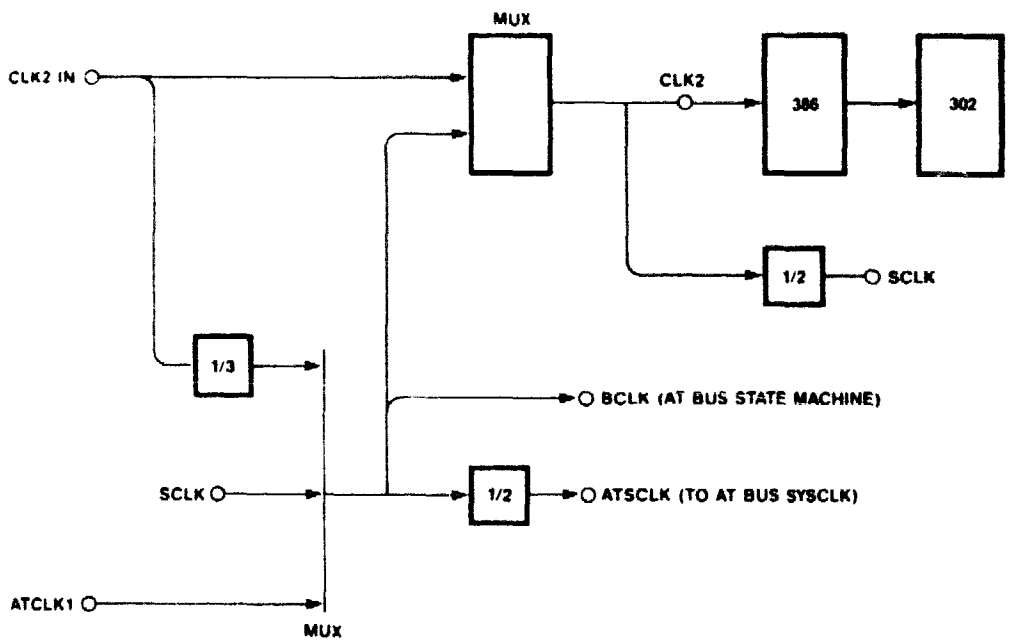


Figure 1-2. CLK2 and ATSCLK Clock Selection

provided so that some register states can be maintained through the reset if so desired.

Bus Arbitration, CPU bus and AT bus State Machines

The 82C301 performs the synchronization and control required between the local processor bus, the memory subsystem and the AT IO channel. It controls all bus activities and handles HRQ1, HRQ2, and REFREQ by generating HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner. Upon CPU asserting HLDA the arbitration logic in turn responds by asserting HLDA1 (for HRQ1) or HLDA2 (for HRQ2), and the requesting DMA or master device has the control of the bus until it de-asserts HRQ1 (or HRQ2) to terminate the HLDA cycle. During the HLDA cycle, the 82C301 generates both SMCMD and action codes AC<3:0> to control the buffer enable and directions for the address and data buffers. Bus size conversions are not supported by 82C301 for these bus cycles and if necessary should be performed by the requesting device.

The CPU state machine and AT state machine control CPU accesses to the devices on the local bus and non-local buses respectively. The CPU state machine supports only 32 bit transfers between the 80386 and system memory (or memory mapped IO) and no bus size conversions are done. Thus BS16 input on the 80386 is not used in a CS8230 system and should be connected to a HI level. The AT state machine responsible for all non-local bus CPU accesses controls the AT bus and supports bus size matching.

All CPU access cycles are started by 82C301 asserting MALE. The CPU state machine then samples AF32 one SCLK clock cycle later. If AF32 is active, it is assumed to be a local bus cycle and the CPU state machine terminates this cycle when it detects READY signal active. In response to an MALE, if the AF32 is detected inactive the control is passed to AT state machine. At the end of the bus access cycle, the AT state machine generates READY to terminates the processor access cycle as well as the CPU state machine cycle.

CPU State Machine

Interface to the 80386 requires interpretation of the status lines upon assertion of ADS and synchronization and generation of a READY response to the CPU upon completion of the requested operation. By interpreting the CPU status lines and ADS, the 82C301 generates control signals MALE and SMCMD. In response to each ADS generated by CPU, an MALE is generated by the 82C301 to indicate the start of a new CPU access cycle. In a non-pipelined CPU cycle, MALE is generated in response to ADS being asserted by the 80386. In a pipelined cycle, MALE is generated when the assertion of READY is detected for the previous CPU cycle. If AF32 is not active one cycle after MALE is asserted, control is passed to the AT bus state machine. The CPU state machine then waits for READY becoming active to terminate the access cycle. In CS 8230 CHIPset, the READY can be generated by 82C302 which controls the system memory access.

SMCMD indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles it is generated for all memory cycles by decoding M/IO, D/C and W/R signals. During non-CPU cycles it is active when XMEMR or XMEMW is active.

NA Pipeline Control

The 82C301 supports both pipelined and non-pipelined cycles of the 80386. The NA (Next Address) input on the 80386 can be always asserted in a CS8230 system for higher performance.

Bus Timeout

An optional feature allows generation of an NMI if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32 is asserted in response to MALE and READY is not returned to the 82C301 within 128 CLK2 cycles. A control bit in the 82C301 configuration registers enables this feature.

AT Bus State Machine

The AT state machine gains the control of the buses when AF32 is detected inactive by the

CPU state machine. It uses BCLK having a frequency twice that of the IO channel clock SYSCLK. When ATCLK1 is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C301 supports 8, 16 or 32 bit transfers between the processor and 8, 16 or 32 bit memory or IO devices located on the IO channel.

An AT bus cycle is initiated by asserting ALE decoded from the CPU status signals and is terminated by asserting READY. On the falling (or trailing) edge of the ALE, MCS16, IOCS16, MCS32, IOCS32 are sampled to determine the bus size conversion required. It then enters the command cycle. The AT bus state machine provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide for timing emulation of lower speed IO channels to maintain compatibility with AT or PC/XT IO adapters and memory cards. The command cycle is terminated by detecting 0WS or IOCHRDY active.

IO Channel Speed Control

The AT state machine can be programmed to insert wait states in units of ATSCLK and to delay the generation of XIOR, XIOW, XMEMR, and XMEMW commands in one half units of ATSCLK (BCLK) within the selected wait states. The command phase delay can be selectively defined for IO cycles and for 8, 16, and 32 bit wide memory cycles by setting the corresponding fields in REG05H. REG06H controls the IO Channel wait state generation for 8, 16, and 32 bit accesses.

The bus clock BCLK is selected by setting REG06H<1:0>. It should be noted that the processor clock source should be set to CLK2IN whenever the BCLK is selected to be SCLK.

Data Conversion

The AT bus access state machine performs data conversion for CPU accesses to devices not on the local bus when AF32 is not asserted. AT bus data conversions are performed for the following types of transfers:

—32 bit to 8/16 bit,
—24 bit to 8/16 bit,
—16 bit to 8/16 bit.

Larger transfers are broken into smaller AT bus reads or writes and the action code AC<3:0> to the 82A306 is generated. Byte addresses XA<01:00> are generated to drive the lower two bits of the AT address bus.

The 82C301 responds to IOCS16, MCS16, IOCS32, and MCS32 in determining what size of data the IO channel needs. If none of the above signals are asserted, 8 bit transfers are assumed and the request is converted into 2, 3 or 4 IO channel cycles based on BE<3:0>. For either MCS16 or IOCS16, the AT bus state machine converts a 32-bit access into two 16 bit AT bus accesses.

The bus state machine also supports 32-bits transfer between the processor and memory and IO devices on the IO channel. IOCS32 and MCS32 inputs allow a device to request a 32-bits transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32 and MCS32 override IOCS16 and MCS16.

In performing these data conversions, a 4-bits action code AC<3:0> is generated to control the buffers in 82A305 for the alignment of data path, and direction control between D, MD, and SD data buses. The definition for the action codes is given in the functional description of 82A305.

Port B Register

The 82C301 provides access to Port B defined for a PC AT as shown in figure 1-3. PORTBCS enables the access to Port B register and is provided as an output from 82A304. Table 1-2 gives the Port B register bit definition.

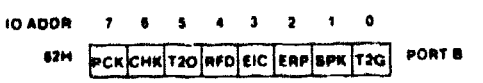


Figure 1-3. Port B register definition

Addr	Bits	Function	
62H		Port B Register	
	7	Read only	PCK - System memory parity check
	6	Read only	CHK - IO channel check
	5	Read only	T2O - Timer 2 out
	4	Read only	RFD - Refresh Detect
	3	Read/write	EIC - Enable IO channel check
	2	Read/write	ERP - Enable system memory parity check
	1	Read/write	SPK - Speaker Data
	0	Read/write	T2G - Timer 2 Gate Speaker

Table 1-2. Port B Register Definition

CS 8230 Internal Register Access Ports

The CS 8230 have internal registers used for system configurations and for diagnostics. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of IO addresses required to access all registers needed to configure and control CS 8230 chips. Each access (either read or write) to an internal register is done by first writing its index into port 22H. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data port is being accessed again.

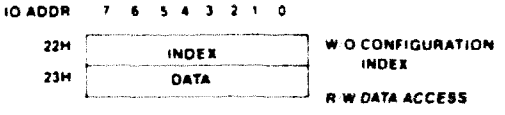


Figure 1-4. Configuration Register Access Ports

Configuration Registers

There are 3 bytes of configuration and diagnostic registers in 82C301 as shown in figure 1-5. The definitions for these registers are given in table 1-3.

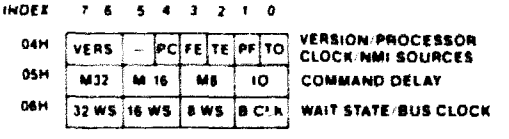


Figure 1-5. 82C301 Internal Configuration Registers

Index	Bits	Function
04H		Version/Processor clock select/NMI source
	7:6	Read only. Version 0 Initial version
	5	Reserved
	4	Processor Clock Select. If SCLK is selected as the source for BCLK, CLK2 source must not be selected as BCLK. 0 Use processor oscillator input. Default. 1 Use AT bus state machine clock (SYSCLKx2).
	3	Power Fail Warning Enable 0 Power Fail NMI not enabled. Default. 1 Power Fail NMI enabled
	2	Local Bus READY timeout NMI Enable 0 READY timeout NMI not enabled. Default. 1 READY timeout NMI enabled
	1	Read only. Power Fail warning active during last NMI arbitration. 0 Power Fail warning pin not active. Default. 1 Power Fail warning pin was active.
	0	Read only. Local bus READY timeout 0 READY timeout has not occurred. Default. 1 READY timeout has occurred
05H		Command delay The value for each one of the command delay field is defined as: 0 0 cycle delay 1 1 cycle delay 2 2 cycle delay 3 3 cycle delay
	7:6	AT Bus 32 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 32 bit memory cycle. Default is 0.
	5:4	AT Bus 16 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 16 bit memory cycle. Default is 0.

Table 1-3. 82C301 Configuration Register Definitions

Index	Bits	Function
05H	3:2	AT Bus 8 bit memory command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 8 bit memory cycle. Default is 1.
	1:0	AT Bus I/O Cycle command delay Specifies between 0 and 3 BCLK cycles for command delay during an AT bus IO cycle. Default is 1.
06H		Wait State/Bus Clock Source
	7:6	32 bit AT Bus wait state select 0-3 wait states per 32 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	5:4	16 bit AT Bus wait state select 0-3 wait states per 16 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	3:2	8 bit AT Bus wait state select 2-5 wait states per 8 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 5. 0 5 cycle delay 1 4 cycle delay 2 3 cycle delay 3 2 cycle delay
	1:0	Bus Clock Source Select 0 Use Proc Clock/3 for AT bus state machine. Default. 1 Use Proc Clock/2 for AT bus state machine. 2 Reserved. 3 Use ATCLK input pin for the AT bus state machine.

Table 1-3. 82C301 Configuration Register Definitions (Continued)

82C301 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C301 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C301 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 16 MHz Clock	I_{CC}		40	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA
CLK2 Output Low Voltage @ I_{OL} = 5 mA	V_{OLC}		0.45	V
CLK2 Output High Voltage @ I_{OH} = -1 mA	V_{OHC}	4.0		V

NOTE:
1. $\overline{REF}$ has I_{OL} = 16mA. CLK2, $\overline{MALE}$ have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C301 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t101	CLK2 period		31		ns
t102	CLK2 low time (at 32 MHz)	9			ns
t103	CLK2 high time (at 32 MHz)	9			ns
t104	CLK2 rise time			8	ns
t105	CLK2 fall time			8	ns
t106	SCLK delay from CLK2↑		4		ns
t107	RESET3, RESET4 set-up time		15		ns
t108	RESET3, RESET4 hold time		8		ns
t109	SMCMD delay from MALE active		7		ns
t110	AF32 set-up time to CLK2↑	22			ns
t111	AF32 hold time to CLK2↑	0			ns
t112	HOLD delay from CLK2↑		25		ns
t113	READY input set-up time to CLK2↑	13			ns
t114	READY input hold time from CLK2↑	5			ns
t115	ATEN active delay from CLK2↑		20		ns
t116	ATEN inactive delay from CLK2↑		20		ns
t117	MALE active delay from CLK2↑		15		ns
t118	MALE inactive delay from CLK2↓		15		ns
t119	READY output active delay from CLK2↑		20		ns
t120	READY output inactive delay from CLK2↑		20		ns
t121	ATSCLK period		125		ns
t122	ATSCLK low time		62		ns
t123	ATSCLK high time		62		ns
t124	ATSCLK rise time			8	ns
t125	ATSCLK fall time			8	ns
t126	ALE delay from ATSCLK (↑ or ↓)		5		ns
t127	XIOR, XMEMR, INTA active delay from ATSCLK (↑ or ↓)		10		ns
t128	XIOR, XMEMR, INTA inactive delay from ATSCLK↑		10		ns
t129	IOCHRDY set-up time to ATSCLK↑		17		ns

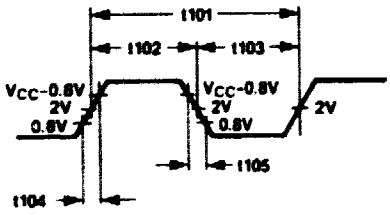
82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

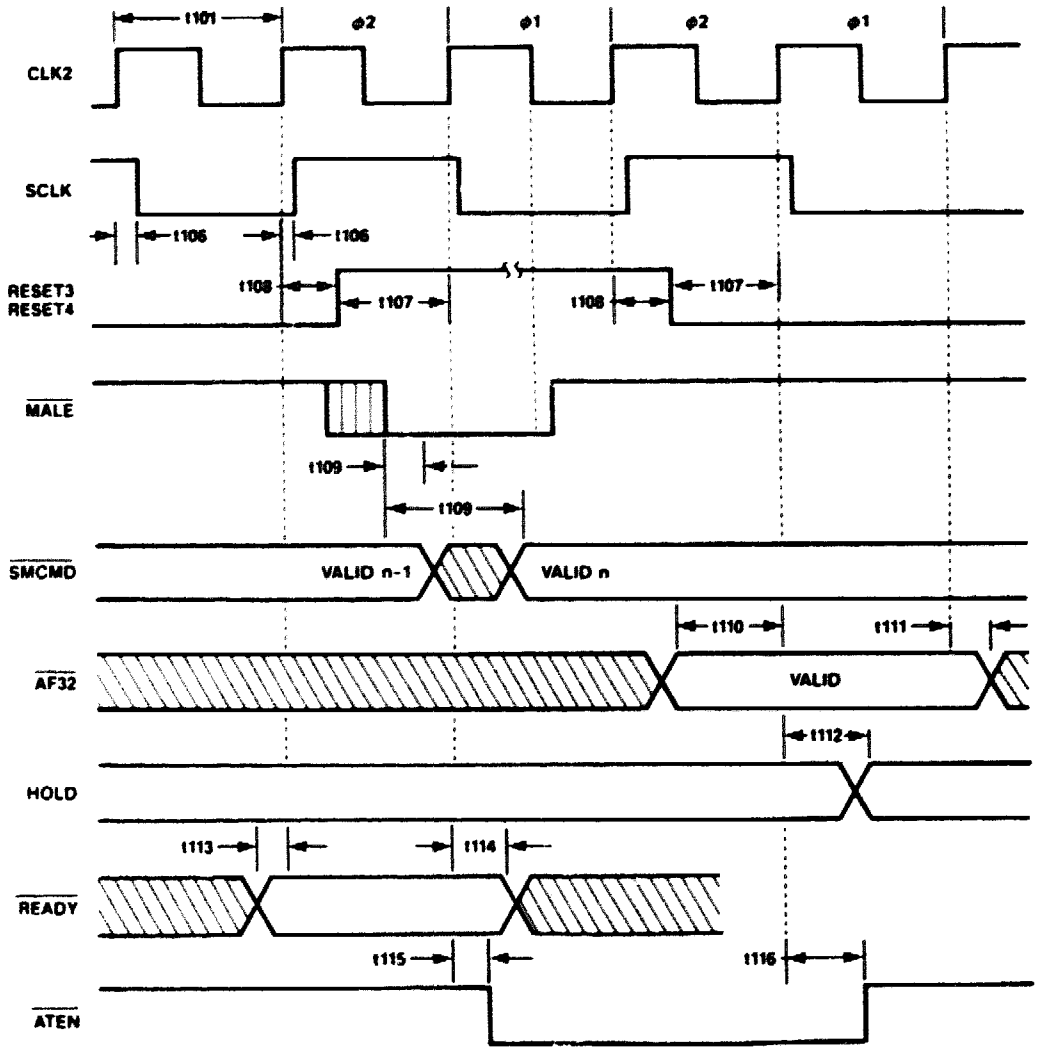
Sym	Description	Min.	Typ.	Max.	Units
t130	IOCHRDY hold time to ATSCLK↓	0			ns
t131	MCS16, IOCS16 set-up time to ATSCLK↑	35			ns
t132	MCS16, IOCS16 hold time from ATSCLK↓		25		ns
t133	MCS32, IOCS32 set-up time to ATSCLK↑	35			ns
t134	MCS32, IOCS32 hold time from ATSCLK↓		25		ns
t135	XA00, XA01, SBHE active delay from ATSCLK↓		20		ns
t136	XA00, XA01, SBHE inactive delay from ATSCLK↓		10		ns
t137	ACEN active delay (read cycle) from ATSCLK↓		20		ns
t138	ACEN inactive delay (read cycle) from ATSCLK↑		10		ns
t139	AC<3:0> active delay from ATSCLK↑		20		ns
t140	AC<3:0> inactive delay from ATSCLK↓		10		ns
t145	XMEMR, XMEMW active delay from ATSCLK↑ (with zero command delay)		15		ns
t146	ACEN active delay (write cycle) from ATSCLK↑		10		ns
t147	ACEN inactive delay (write cycle) from ATSCLK↓	0			ns
t148	0WS set-up time to ATSCLK↓		17		ns
t149	0WS hold time from ATSCLK↑	0			ns
t151	NMICS set-up time to XIOW active	20			ns
t152	NMICS hold time from XIOW inactive	20			ns
t153	Data (XD7) set-up time to XIOW inactive	30			ns
t154	Data (XD7) hold time from XIOW inactive	20			ns
t155	NMI delay from XIOW inactive		25		ns
t156	PORTBCS set-up time to XIOR, XIOW active	20			ns
t157	PORTBCS hold time from XIOR, XIOW inactive	20			ns
t158	Data (XD<7:0>) valid delay from XIOR active	15			ns
t159	Data (XD<7:0>) hold time from XIOR inactive	15			ns
t160	IO2XCS set-up time to XIOR, XIOW active		10		ns
t161	IO2XCS hold time from XIOR, XIOW inactive		15		ns
t162	LPAR, IOCHK, PFAIL pulse width		15		ns
t165	REFREQ pulse width	15			ns

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

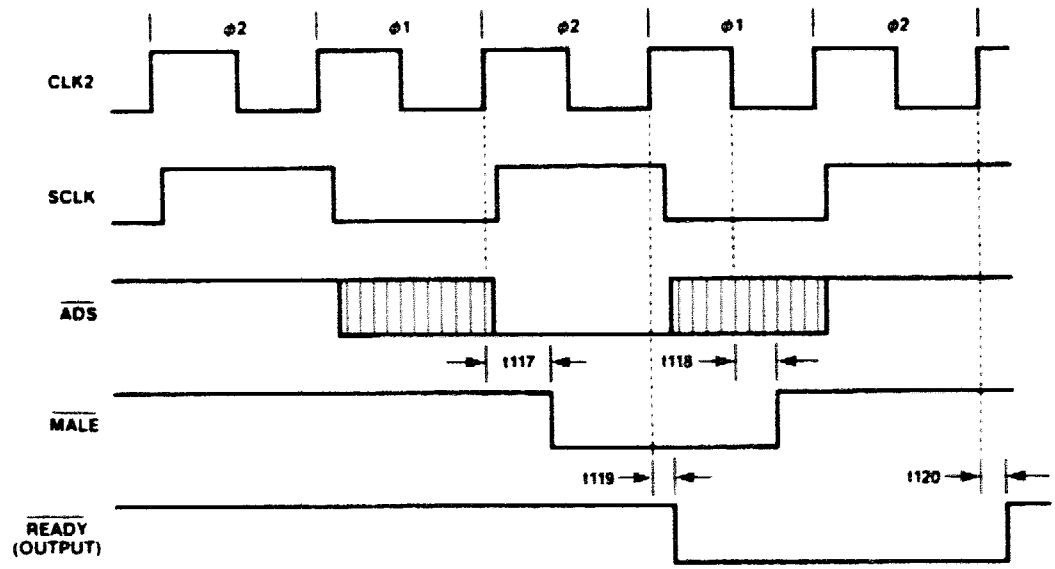
Sym	Description	Min.	Typ.	Max.	Units
t166	$\overline{REF}$ set-up time to ATSCLK↑		10		ns
t167	$\overline{XMEMR}$ active delay (refresh cycle) from ATSCLK↑		15		ns
t168	$\overline{XMEMR}$ inactive delay (refresh cycle) from ATSCLK↑		15		ns
t169	IOCHRDY set-up time (refresh cycle) to ATSCLK↑	25			ns
t170	IOCHRDY hold time (refresh cycle) from ATSCLK↑	0			ns
t171	$\overline{BE<3:0>}$ active delay from XA0, XA1, $\overline{XBHE}$ valid		15		ns
t172	$\overline{BE<3:0>}$ inactive delay		15		ns
t173	$\overline{SMCMD}$ active delay from $\overline{XMEMR}$, $\overline{XMEMW}$ active		20		ns
t174	$\overline{SMCMD}$ inactive delay from $\overline{XMEMR}$, $\overline{XMEMW}$ inactive		20		ns
t175	$\overline{ACEN}$ active delay from HLDA1 active		20		ns
t176	$\overline{ACEN}$ inactive delay from HLDA1 inactive		20		ns
t177	AC<3:0> active delay from XA0, XA1, $\overline{XBHE}$ not valid		TBD		
t178	AC<3:0> inactive delay from XA0, XA1, $\overline{XBHE}$ valid		TBD		
t179	AC<3:0> active delay from $\overline{XMEMR}$ active		TBD		
t180	AC<3:0> inactive delay from $\overline{XMEMR}$ inactive		TBD		

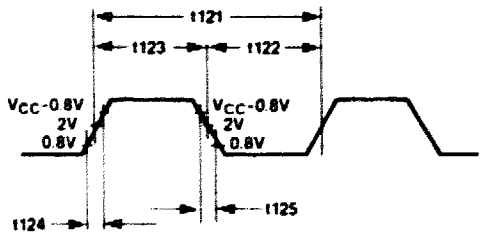
82C301 TIMING DIAGRAMS



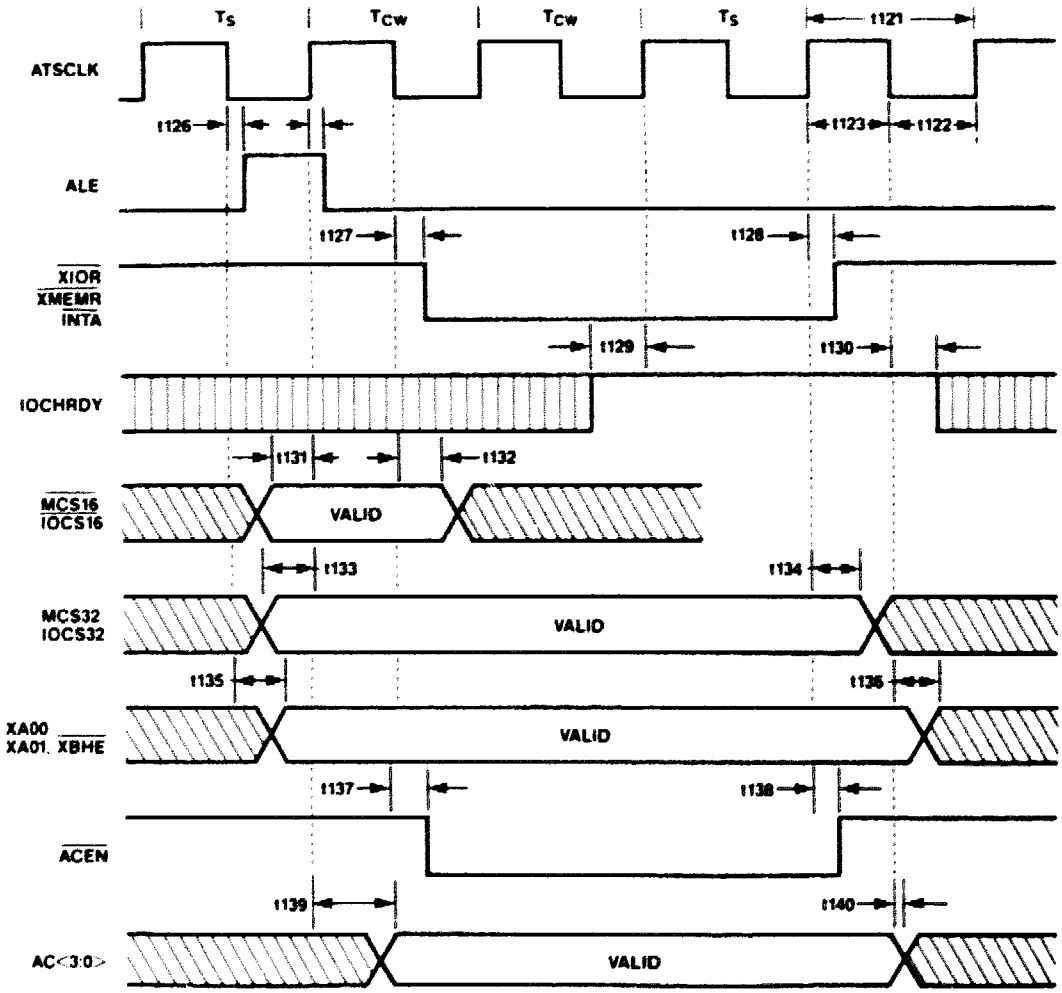


82C301 TIMING DIAGRAMS

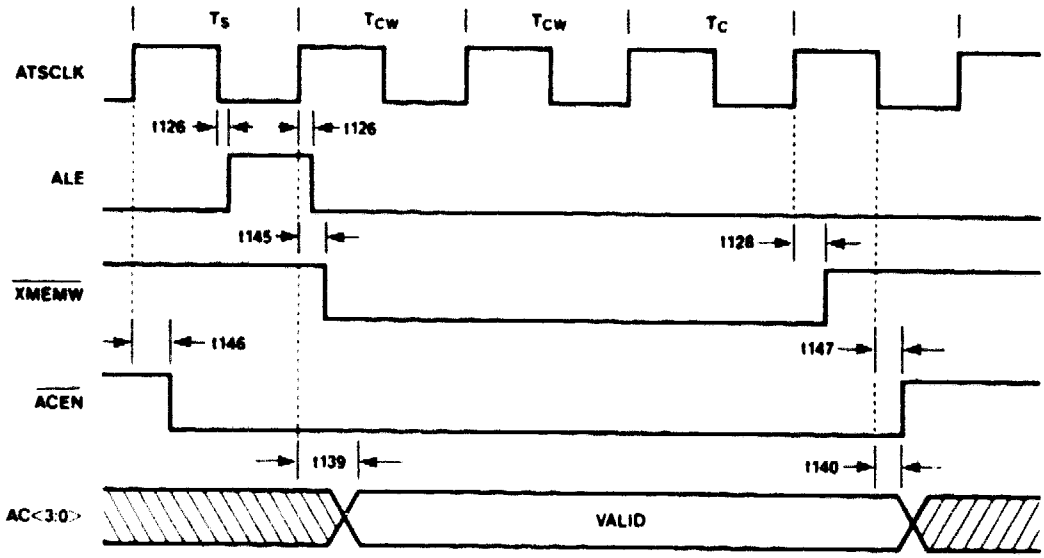


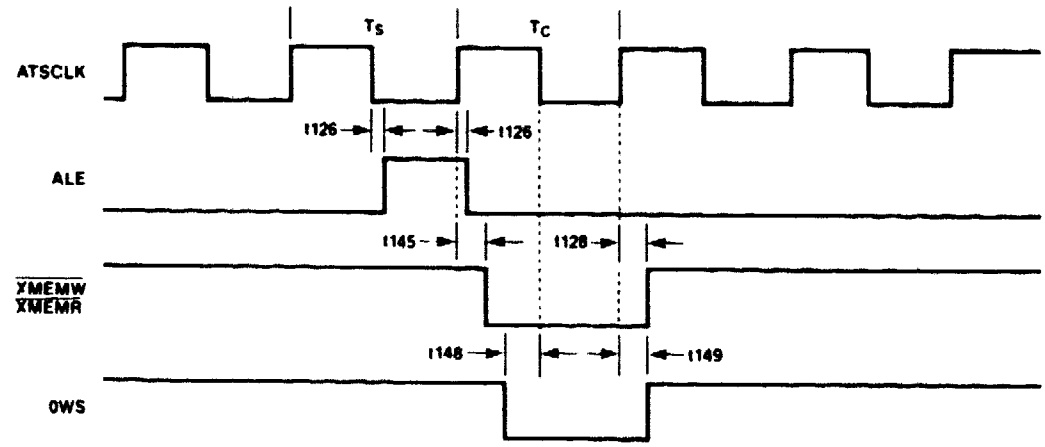


82C301 TIMING DIAGRAMS

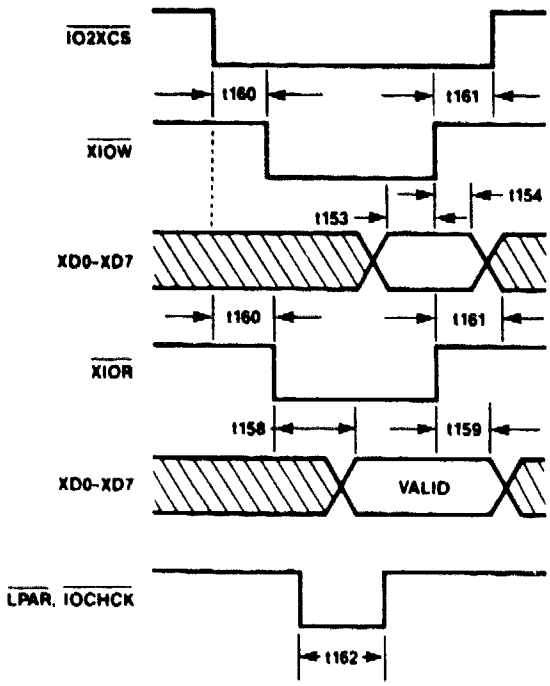


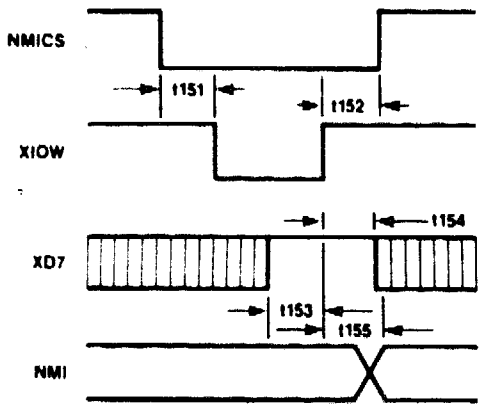
82C301 TIMING DIAGRAMS

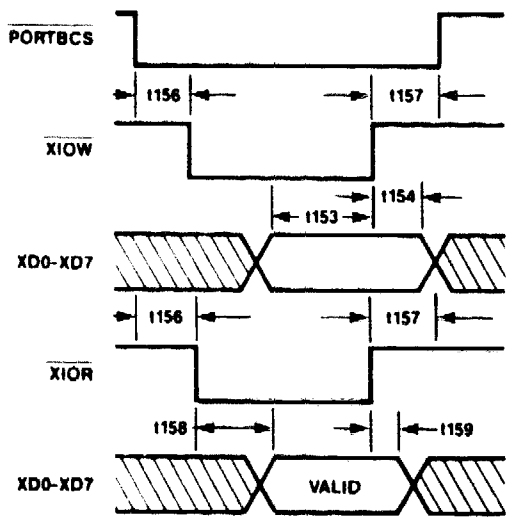




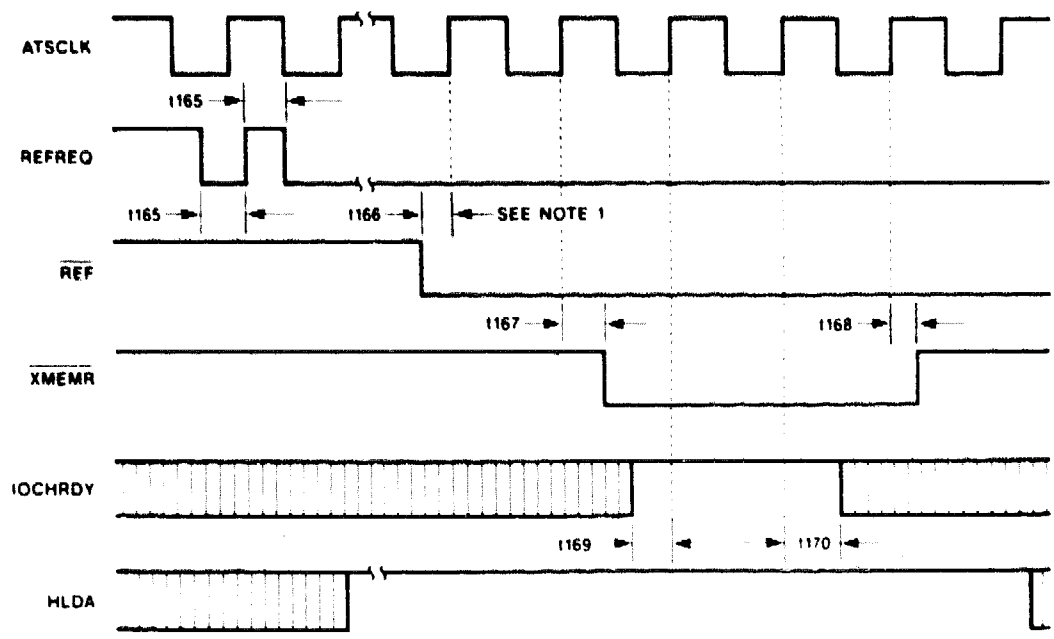
82C301 TIMING DIAGRAMS





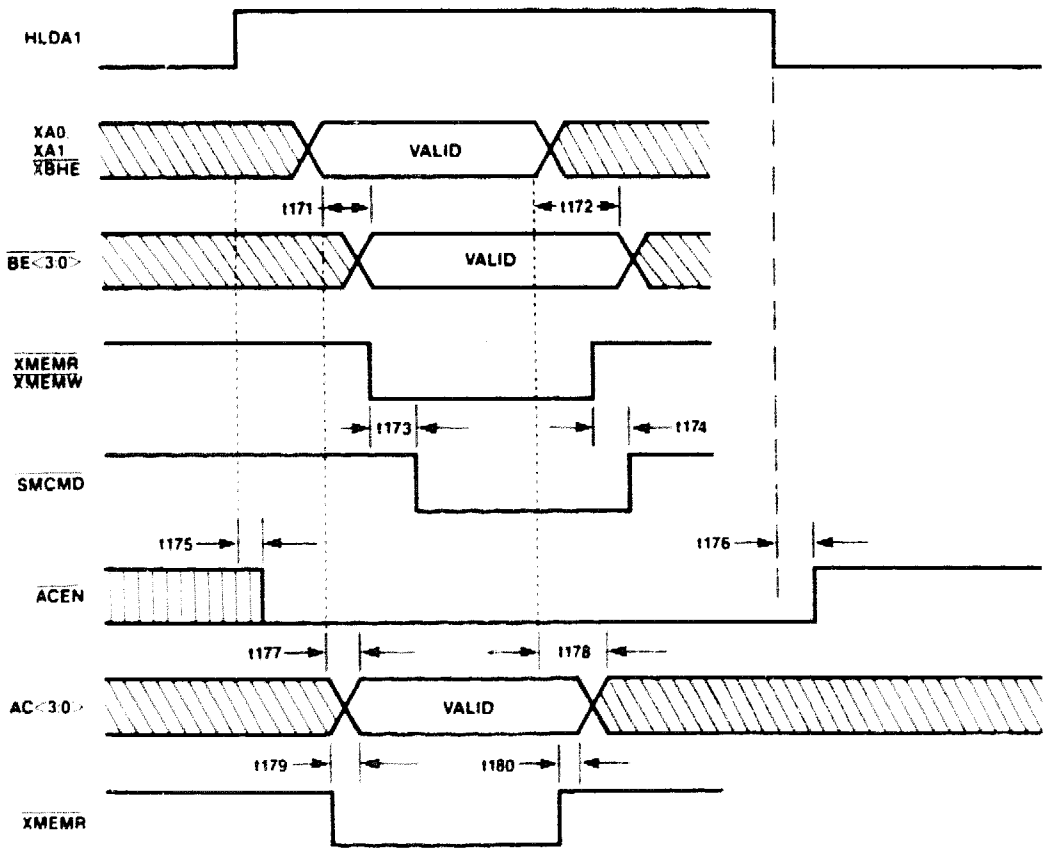


82C301 TIMING DIAGRAMS



NOTE
REF is an asynchronous signal and the setup time is specified only to guarantee starting a refresh cycle on that clock cycle instead of next one

82C301 TIMING DIAGRAMS



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82C302 PAGE/INTERLEAVE MEMORY CONTROLLER

- Page mode access with interleaved memory banks achieves higher performance than conventional DRAM arrays
- Zero wait state access at 16MHz using 100nS DRAMs
- Minimum configuration of 1 bank of 36 bits, 1MB using 256K x 1 or 4MB using 1M × 1 DRAMs
- Maximum configuration of 4 banks of 36 bits, 4MB using 256K × 1 or 16MB using 1M × 1 DRAMs
- Memory configurations of 1, 2 and 4 banks
- Staggered refresh to reduce power supply noise

OVERVIEW

The 82C302 performs the memory control functions in a 80386-based systems that utilizes page mode access DRAMs. The memory configurations can be one bank (non-interleaved) or multiple banks (2 or 4) interleaved on 2KB-page basis.

Array Configuration

The 82C302 organizes memory as banks of 36 bits consisting of 32 bits of data and 4 bits of parity. A common design may use either 36 by-1 DRAMs or 8 by-4 and 4 by-1 DRAMs. The minimum configuration can be a single bank operating in non-interleaved mode or can be one to two pairs of banks operating in two-way page interleaved mode at higher performance.

The memory controller is designed such that the memory can be up-graded from one to two banks by making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair due to the interleaved configuration. However, each pair of banks can use different DRAM types with one or two banks of smaller DRAM types and later upgraded with additional pairs of banks of larger DRAMs.

Page Interleaved Operation

The 82C302 uses a page interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses in the other. If accesses are sequential (or at least to alternating even and odd addresses) the RAS precharge time of one set can be overlapped with the access time of the second set. Typically the hit rate (fraction of times that the required bank is available) is 50%. This is especially true since operand accesses (which tend to be more random) can be interspersed with (most likely sequential) instruction fetches.

Page mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256K × 1) that are subsequently selected using the column address. Once a row access has been made higher speed random access can be made to any bit (1 of 512) within the row. The page mode access and cycle times are typically half that of the normal access and cycle times respectively. If 36 256K × 1 DRAMs are used to implement a bank, a page would have 512 × 4 bytes = 2KB. Thus memory could be interleaved on a 2KB page rather than 4B basis. Any access to the currently active RAS page would occur in the page access rather than the normal access time and any subsequent access could be to anywhere in the same 2KB without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving. There are two reasons for this:

— The page mode access is faster than the normal access time. This permits more relaxed timing in order to achieve the same 0 wait-state "hit" access.

— The frequency of the next access being fast (same or alternate page vs. alternate address in interleaved mode) is significantly higher. This is because of the principle of locality of reference, instructions and data tend to be clustered together.

However, the complexity is somewhat higher in the page mode controller, making VLSI an ideal implementation vehicle.

FUNCTIONAL DESCRIPTION

The 82C302 performs four major functions as shown in figure 2-1.

- DRAM memory access arbitration
- DRAM memory access cycle control
- DRAM refresh
- Memory mapping

Memory Access State Machines and Arbitration

The 82C302 controls the DRAM memory access from three sources: CPU, DMA, and refresh requests. These accesses are arbitrated based on the inputs HLDA1 and $\overline{REF}$ and are handled by three state machines controlling each type of accesses. The CPU cycle state machine controls the memory operation for CPU accesses, the DMA cycle state machine for DMA accesses, and the refresh cycle state machine controls the DRAM refresh operation.

The refresh state machine is in control whenever $\overline{REF}$ is active. When HLDA1 is active the DMA state machine is in control. In all other cases, the CPU state machine is in control for valid DRAM memory accesses as defined by the memory map in the configuration registers. The arbitration is not preemptive in that the current active state machine always runs to completion before relinquishing the control. Therefore, it is possible for the HLDA1 with active $\overline{XMEMW}$ or $\overline{XMEMR}$ to prevent refresh cycles to take place.

CPU Access State Machine

The CPU initiated accesses are decoded according to the memory map defined in the configuration registers. These are the only accesses that uses the page mode operation of the DRAMs. The 82C302 maintains four page registers storing the page addresses of the most recently accessed DRAM pages of the two-way page-interleaved banks. These four registers are called active page registers. Accesses to the active pages are called "hits" and are faster because the DRAM is operated in the page mode with the RAS staying asserted.

The 82C302 supports memory configurations with either one, two, or four banks. Since one active register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration only one active page register is in use. For each active page register in use, the corresponding $\overline{RAS}$ stays asserted after the previous access. If an access does not hit any active pages, a "miss" cycle, normal DRAM access cycle is entered by first de-asserting the $\overline{RAS}$ associated with the bank accessed. Refer to the timing diagram for the timing sequence for each of these cases.

RAS and CAS Generation

The 82C302 is based on 2K byte page-interleaved organization. To maintain this organization, the following table shows the address lines used for the different organizations.

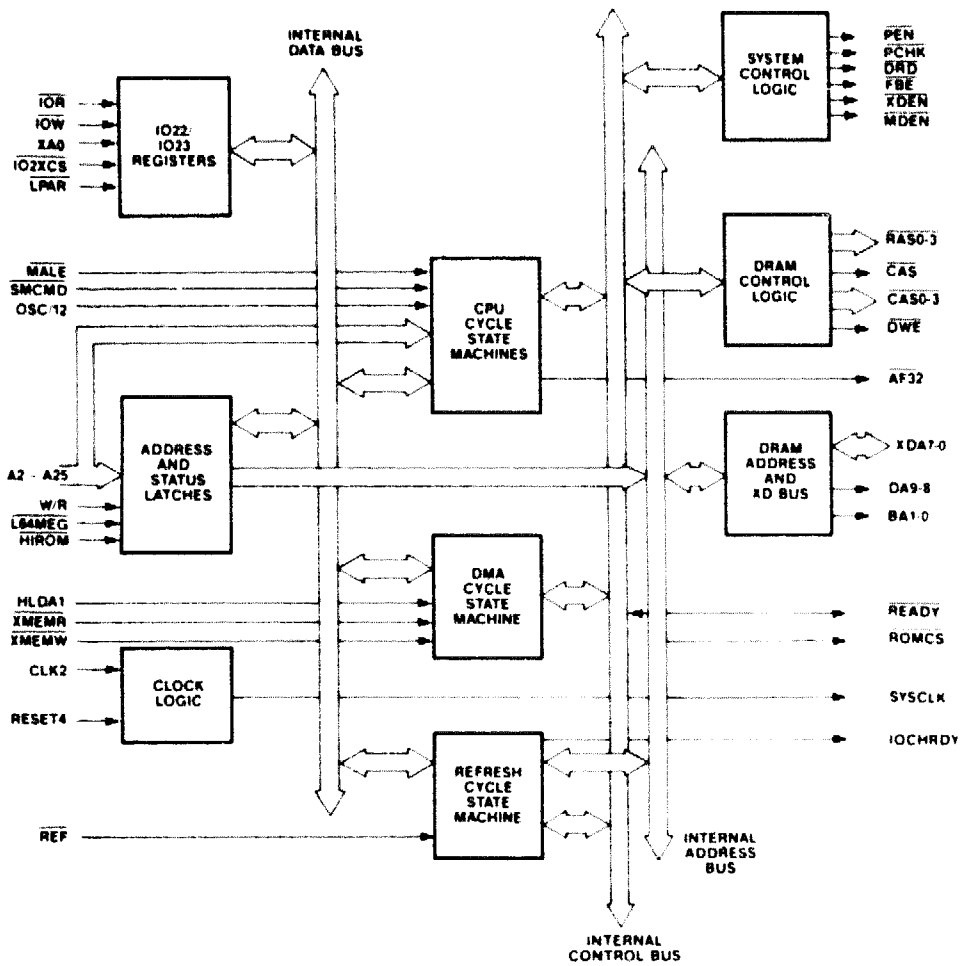


Figure 2-1. 82C302 Functional Block Diagram

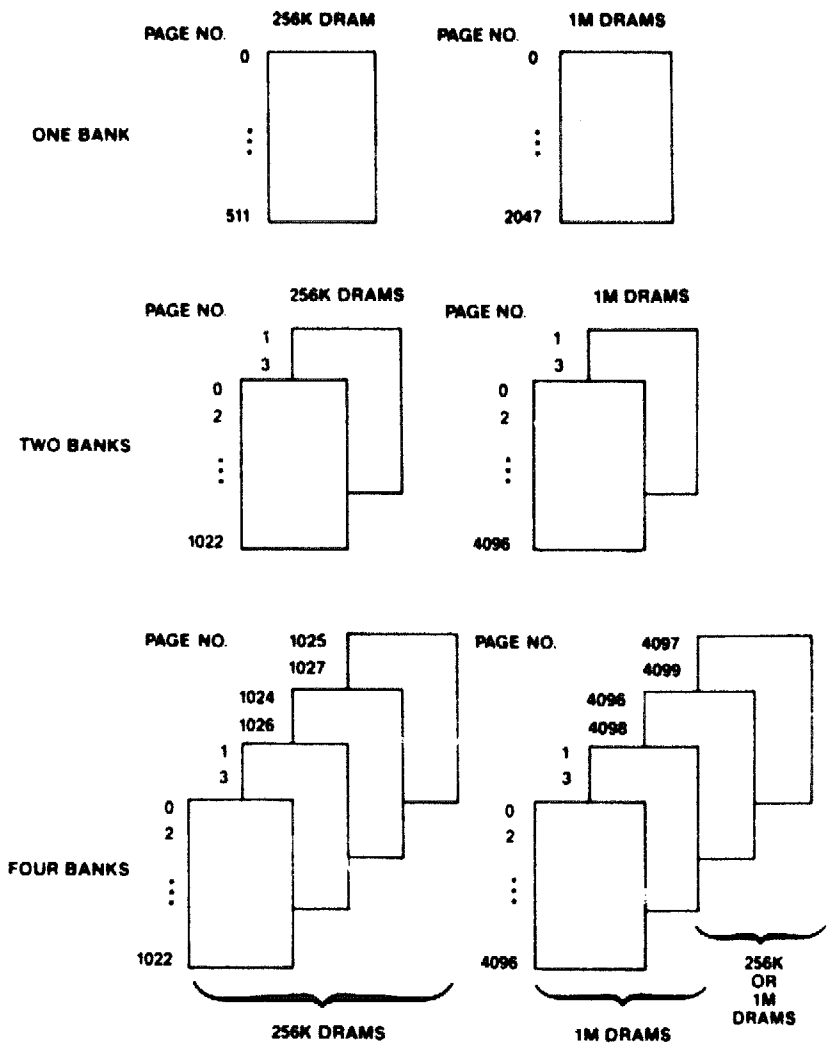


Figure 2-2. Memory Addressing

For non-interleaved operation (one bank only):

	Row	Column
256K DRAM's	A<19:11>	A<10:2>
1M DRAM's	A<21:12>	A<11:2>

For interleaved memory(two or four banks):

	Row	Column
256K DRAM's	A<20:12>	A<10:2>
1M DRAM's	A<21:12>	A<22>, A<10:2>

Table 2-1. Row and Column Address Definition

In interleaved memory cases bit A<11> determines which one of the even page banks or odd page banks is accessed in the two-way interleaved organization. For configurations using only 256K DRAM's, A<11> and A<21> are used to control RAS<3:0>, and for 1M DRAM only configurations A<11> and A<23> are used. When 256K and 1M DRAMs are used, it is required that the 1M DRAMs occupy the first two-banks and the 256K DRAMs occupy the second two-banks. This constrain is there to ensure that the there will not be a hole in the address space without actual DRAM's. Figure 2-2 shows the memory addressing scheme for the allowable memory configurations.

RAS Timeout

When using DRAM page mode, the maximum RAS pulse width must be observed. For most DRAMs this is 10 microseconds (although some have 30 or 100 microsecond limits). Timers are maintained for each bank to assure data integrity using the OSC/12 (1.19MHz = 840nS) clock available on the system board. RAS is de-asserted for each bank when its counter times out at about 10 microseconds intervals. The configuration register bit REG13H<7> can be programmed to set desired RAS time out intervals.

CPU Access Cycles Sequences

There are many basic CPU memory access patterns: memory read-hit access, memory write-hit access, memory read-miss access, and memory write-miss access, and CPU IO access to 82C301 configuration registers. These basic access sequences and timing for the critical signals are shown in the timing charts. In addition to these basic patterns, the configuration register REG13H<6> may be programmed to have one wait state inserted for supporting slow DRAM's. Note that the default setting after the system reset is for one wait state insertion.

DMA Access State Machine

DMA accesses are initiated by asserting HLDA1. The XMEMR an XMEMW determines if it is a read or a write memory access. The bytes accessed are controlled externally with the BE<3:0> signals generated by the 82C301 Bus Controller. The DMA state machine makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers. Refer to the timing charts for a DMA access cycle sequence and timing.

Dynamic RAM Access Logic

The DRAM control logic generates the necessary RAS, CAS and DWE signals for all DRAM acesses. CPU, DMA, and refresh access cycles use DA<9:8> and XDA<7:0> and bank select signals BA<1:0>. (Note that in the current version of 82C302, the signals BA<1:0> default to zero.) The system control logic provides MDEN to control the buffer chips. MDEN enables data buffers for MD bus in 82A305's for non-refresh DRAM access cycles.

Refresh Cycles

To reduce power supply noise generation due to the surges caused during RAS transitions, RAS pulses to each bank are staggered by one CLK2 cycle, as shown in Figure 2-3. Because all RAS's could be active for page mode operation, a refresh cycle requires that all RAS's be first de-asserted then asserted with the correct refresh address.

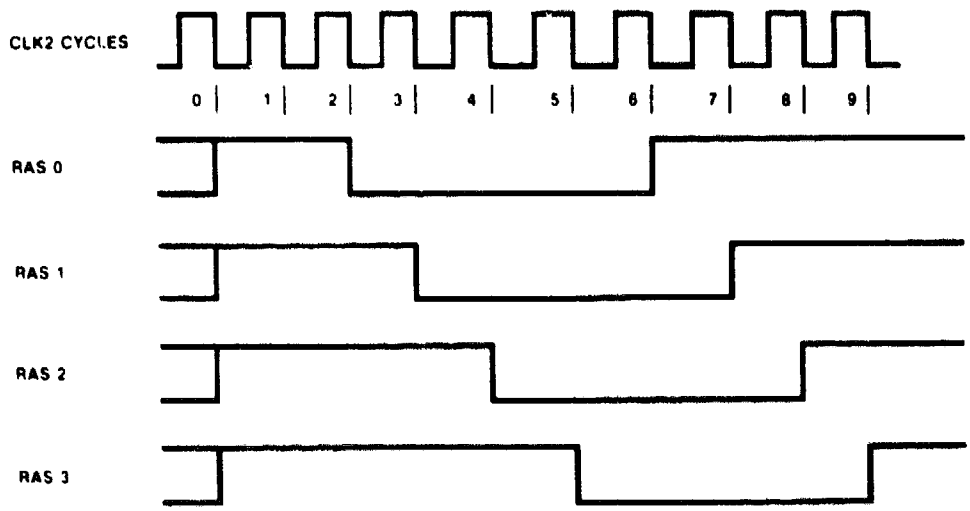


Figure 2-3. Staggered RAS pulses during refresh

Memory Mapping Logic

The configuration registers REG08H to REG13H define what is a valid local memory access, and what is a ROM memory access according to the local bus addresses. REG08H and REG09H determines how ROM areas (as defined by an IBM PC AT) between 768K to 1M address range are accessed.

For valid local memory accesses it asserts the AF32 to indicate that it has control of the local bus and also asserts the READY signal at the end of the access cycle. If an access is a ROM access, it asserts ROMCS to provide controls for the ROM's or PROM's, in this case, the READY signal must be provided to the CPU and 82C302 by another source (82C301 will provide this signal in a chip set solution).

Clock, Reset and Other Miscellaneous Logic

The RESET4 input causes all internal registers to be reset to their default values. Configuration registers not specified with a default value is not reinitialized and may not retain its old value. The system control logic generates the PCHK and PEN signals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

There are 14 bytes of configuration and diagnostic registers in the 82C302. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. Accesses to these configuration and diagnostic registers are done first by writing the index of the desired register into port 22H and then followed by an access (either read or write) to 23H for the data. XDEN is asserted for these accesses to control the buffer connecting the XD and XDA buses.

Memory Configuration Registers

The configuration registers REG08H to REG0FH are used to control how the CPU memory accesses are defined. They define all address as ROM accesses, system memory accesses (or DRAM accesses for short), other local CPU bus accesses, or as IO channel accesses. These provisions are made because the low one megabyte is both occupied by DRAM's, ROM's and also devices on the AT bus. For ROM accesses it generates the ROMCS to control the PROM access;for system memory accesses it generates the necessary DRAM controls to the system memory

under its control, it generates AF32 for all other local CPU bus accesses, and it does not control the IO channel accesses.

The 82C301 provides three 256KB areas where the ROM's can be located. The low ROM space is located just below the 1MB address, the middle ROM space is located below 16MB address, and the high ROM space is below 4GB address. The low ROM is used for 8086 compatible operation, the middle ROM is for 80286, and the high ROM is for 80386. Upon system reset, the default configuration register setting causes accesses to these three ROM areas to generate ROMCS. With the exception of the high ROM area which is always recognized as ROM accesses, the other two ROM areas can be mapped to be either ROM or RAM accesses.

After reset, REG08<4:3> may be programmed to make the entire middle ROM area mapped to DRAM and with write protection if desired. REG08H<2> determines if the 82C301 recognizes the addresses generated beyond 16 MB as local CPU bus cycles. REG08H<1> is used to enable REG0AH to REG0FH which controls the "Low Meg DRAM" (40000H to FFFFFH) address mapping for 256KB to 1MB addresses in 16 KB blocks. This bit defaults upon reset so that only the 0 to 256KB areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed. REG08H<0> defaults to single bank memory configuration upon reset and must be programmed to enable page/interleaved operation.

The REG09H control the address mapping and write protection for the low ROM area (from C0000H to FFFFFH) in 64KB blocks. REG0AH to REG0FH define for each 16 KB address range if it is a DRAM block in the system memory or on the IO channel.

INDEX	7	6	5	4	3	2	1	0	
08H	0	VER5		MW	MR	HM	SM	NI	IDENTIFICATION
09H	R3	R2	R1	R0	D3	D2	D1	D0	ROM CONFIGURATION
0AH	368K						256K		MEMORY ENABLE (16KB RESOLUTION)
0BH	496K						384K		•
0CH	624K						512K		•
0DH	752K						640K		•
0EH	880K						768K		•
0FH	1008K						896K		MEMORY ENABLE (16KB RESOLUTION)

Figure 2-5. Control and Address Space Map Register Summary

Index	Bits	Function
08H		Identification
	7	Controller Type Part type
		0 Interleaved Memory Controller (82C302)
	6 5	Version
		0 Initial
	4	MW - Middle Boot Space Write Protect. This bit is used in conjunction with bit 3 allowing the BIOS code to be copied into RAM and write protected at this location as well as below 1MB. It should only be used if there is RAM present at this address (16MB installed). Executing out of RAM will result in better performance than out of narrower (usually 8 or 16 bits) EPROMs.
		0 Read/Write of 256KB RAM at 16128K 00FC0000H. Default. 1 Read-Only of 256KB RAM at 16128K 00FC0000H
	3	MR - Middle Boot ROM disable
		0 The boot/BIOS ROM located just below 16MB is enabled. This is necessary for 286 compatibility. Default. 1 The boot/BIOS ROM located just below 16MB is disabled.
	2	HM - 16MB IO Channel Memory Limit
		0 AF32 will not be asserted for addresses ≥ 16MB. This should only be used if external logic can recognize addresses above 16MB. Default. 1 AF32 is asserted for addresses ≥ 16MB (01000000H). Since IO channel memory cannot normally be configured above 16MB, accessing above 16MB will cause a READY timeout if that feature is enabled. This is necessary during setup because memory address above 16MB that are not enabled for local memory could wrap into a valid IO channel memory location.
	1	SM - Minimum memory configuration after reset. Used during initialization.
		0 256K only enabled. Default. Ignore memory address configuration registers 0AH to 0FH. 1 Normal configuration controlled by registers 0AH to 0FH.
	0	NI - Single bank/interleave select 0 Disable interleave (single bank). Default. 1 Enable interleave

Table 2-2. Memory Configuration Register Definition

Index	Bits	Function
09H		RAM/ROM Configuration in boot area
	7	RAM at 768K C0000-CFFFFH (EGA)
	6	RAM at 832K D0000-DFFFFH
	5	RAM at 896K E0000-EFFFFH
	4	RAM at 960K F0000-FFFFFH (BIOS)
		Bits 7 4 disable writing to RAM located in the BIOS area in 64KB blocks BIOS data 0 Read/Write Default 1 Read-Only
	3	ROM at 768K C0000-CFFFFH (EGA)
	2	ROM at 832K D0000-DFFFFH
	1	ROM at 896K E0000-EFFFFH
	0	ROM at 960K F0000-FFFFFH (BIOS)
		Bits 3 0 enable substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks This should be done after the BIOS code is copied from the ROM and the RAM locations have been write protected using bits 7 4 0 Disabled 1 Enabled Default
0AH		Address Map 256K 040000-05FFFFH (16K Resolution)
0BH		Address Map 384K 060000-07FFFFH
0CH		Address Map 512K 080000-09FFFFH
0DH		Address Map 640K 0A0000-0BFFFFH
0EH		Address Map 768K 0C0000-0DFFFFH
0FH		Address Map 896K 0E0000-0FFFFFH 0 Address is on or controlled by the system board 1 Address is on the IO Channel This permits 16K blocks of memory to be disabled allowing ROMs, memory expansion mechanisms (EMS or XMA) or memory mapped IO devices to reside within the lower 1MB address space.

Table 2-2. Memory Configuration Register Definition (Continued)

DRAM Array Configuration and Timing

The configuration registers REG10H to REG13H provides the DRAM type definition and starting address for each pair of banks, banks 0 and 1, and banks 2 and 3. The REG10H<7:6> and REG12H<7:6> defines if the DRAM's are enabled, uses 256K DRAM's, or uses 1M DRAM's. These bits defaults to 256K DRAM's upon reset. The REG10H<6:0> and REG12H<6:0> defines the address bits <25:20> of the starting address of the pairs of banks. Some of these bits may not be valid because the memory banks must start at some predefined boundaries. For 256K DRAM's, all bits <25:20> are valid if only single bank is enabled-it can be on any 1MB boundary; otherwise only bits <25:21> are valid starting address bits on 2MB boundaries. For 1M DRAM's, only bits <25:23> are valid forcing it on 8 MB boundaries. The REG11H<7> and REG13H<7> define the RAS precharge time required when a page miss occurs so that DRAM's of different speeds can be supported for each pair of banks. The REG11H<6> and REG13H<6> define the wait state to be inserted to meet the DRAM speed. These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions on the DRAM speed and the memory configuration. Refer to Table 2-3 for details of the bit definitions.

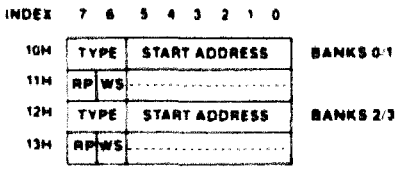


Figure 2.5. DRAM Configuration/Timing Register Summary

Index	Bits	Function
10H		bank 0/1 Type/Start Address
12H		bank 2/3 Type/Start Address
	7:6	DRAM Type
		0 none (bank disabled)
		1 256K words, default value for REG10H and REG12H
		2 1M words
		3 Reserved
	5:0	Starting Address 25:20 The DRAM type determines which address bits are valid in the address recognition process. This field of REG10H defaults to zero after reset.
		25:20 256K DRAM's. 1MB boundary 1MB per bank, single bank only. Valid for the first register only.
		25:21 256K DRAM's. 2MB boundary 1MB per bank, two banks required for interleaved operation.
		25:23 1M DRAM's. 8MB boundary 4MB per bank, two banks required for interleaved operation.

Table 2-3. DRAM Configuration and Timing Register Definition

280

Index	Bits	Function
11H		banks 0/1 Timing
13H		banks 2/3 Timing
	7	DRAM RAS precharge. Specifies the amount of time for RAS precharge when a page miss occurs. 0 3 CLK2 times (93 nS at 16MHz) 1 5 CLK2 times (155nS at 16MHz). Default
	6	Access wait states Specifies the number of wait states in SCLK units to allow the use of slower DRAMs. 0 0 wait-states 1 1 wait-states. Default
	5:0	Reserved

Table 2-3. DRAM Configuration and Timing Register Definition (Continued)

Diagnostic Access Register

REG28H<7> controls the parity check enable and defaults to "disable" after reset. This bit generates the $\overline{PEN}$ signal for enabling the parity check by 82A306. When parity errors occur REG28H<1:0> and REG29H<7:0> will latch the error address <25:16>.

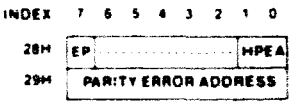


Figure 2.7. Diagnostic Access Register Summary

Index	Bits	Function
28H		Error Source/Address (MSBs)
	7	Parity check disable 0 Enabled 1 Disabled
	6:2	Not used, returns unpredictable value
	1:0	High Parity Error Address bits <25:24>
29H		Parity Error Address (LSBs)
	7:0	Error address bits <23:16>

Table 2-4. Diagnostic Access Registers Definition

82C302 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C302 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C302 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTE:
1. SYSCLK, $\overline{DWE}$, $\overline{RAS}$<3:0>, CAS, $\overline{CAS}$<3:0> have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C302 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t200	CLK2 input cycle time (t0 used as reference)	31		42	ns
t201	CLK2 fall time	2		5	ns
t202	CLK2 rise time	2		5	ns
t203	CLK2 low time	10			ns
t204	CLK2 high time	10			
t205	RESET hold time	6			ns
t206	RESET set-up time	5			ns
t207	SCLK delay t[illegible]	6	12	22	ns
DMA Sequence					
t210	$\overline{RAS}_I$ de-assertion time from HLDA1		13		ns
t211	$\overline{RAS}_I$ active delay from commands active		16		ns
t212	Address set-up time to commands active	35			ns
t213	Address hold time from commands inactive	0			ns
t214	AF32 active time from commands active		26		ns
t215	$\overline{DRD}$ active time from commands active	10			ns
t216	Row address set-up time to $\overline{RAS}$ active	10			ns
t217	Row address hold time from $\overline{RAS}$ active	0.5t0			ns
t218	$\overline{CAS}_I$ active delay from $\overline{RAS}$ active for DMA memory read cycle	1.0t0			ns
t219	$\overline{CAS}_I$ active delay from $\overline{RAS}$ active for DMA memory write cycle	1.5t0			ns
t220	$\overline{DWE}$ active delay from $\overline{RAS}$ active	0.5t0			ns
t221	$\overline{READY}$ active delay from $\overline{RAS}$ active	1.5t0			ns
t222	$\overline{RAS}_I$ de-assertion time from commands inactive		13		ns
t223	Column address hold time from commands active		29		ns
t224	$\overline{CAS}_I$ de-assertion from commands inactive		22		ns
t225	AF32 tri-state delay from commands inactive		21		ns
t226	$\overline{DWE}$ de-assertion time from commands inactive		11		ns
t227	$\overline{READY}$ de-assertion time from commands inactive		16		ns
t228	$\overline{DRD}$ de-assertion time from commands inactive		12		ns

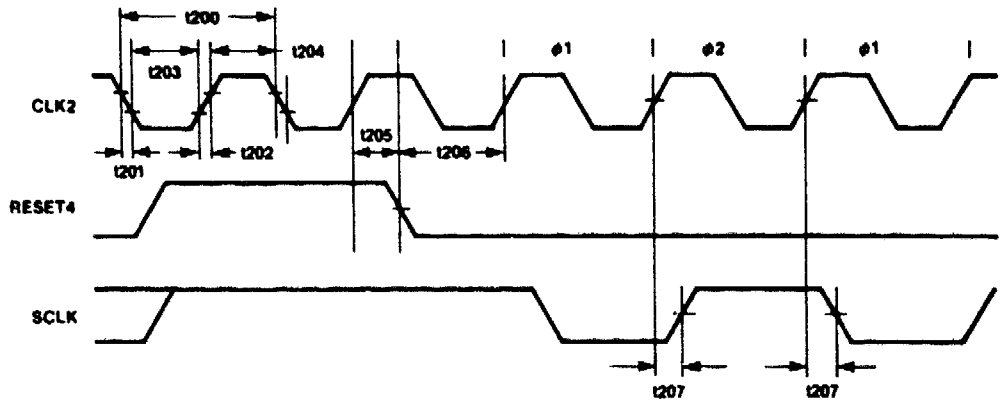
82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
ROMCS Sequence					
t235	$\overline{ROMCS}$ active delay from CLK2↑		27		ns
t236	$\overline{ROMCS}$ inactive delay from CLK2↑		22		ns
t237	$\overline{READY}$ input set-up time to CLK2↓	8			ns
t238	$\overline{READY}$ input hold time from CLK2↑	0			ns
Refresh Sequence					
t240	IOCHRDY going low from $\overline{REF}$ active		14		ns
t241	IOCHRDY floating from CLK2↑		18		ns
t242	$\overline{RAS0}$ precharge time		3t0		ns
t243	$\overline{RASi}$ (i = 0 to 3) pulse width		4t0		ns
t244	RAS(i+1) active delay from $\overline{RASi}$ active		1t0		ns
t245	Refresh address set-up time to $\overline{RASi}$		3t0		ns
t246	Refresh address hold time from $\overline{RASi}$		2t0		ns
t247	$\overline{RASi}$ inactive delay from CLK2↑		14		ns
t248	$\overline{RASi}$ active delay from CLK2↑		15		ns
IO Read/Write Sequence					
t250	IO2XCS set-up time to $\overline{XIOR}$↓ or $\overline{XIOW}$↓	10			ns
t251	XA0 set-up time to $\overline{XIOR}$↓ or $\overline{XIOW}$↓	10			ns
t252	IO2XCS hold time from $\overline{XIOR}$↑ or $\overline{XIOW}$↑	15			ns
t253	XA0 hold time from $\overline{XIOR}$↑ or $\overline{XIOW}$↑	15			ns
t254	XDEN active delay from $\overline{XIOR}$↓ or $\overline{XIOW}$↓		15		ns
t255	XDEN inactive delay from $\overline{XIOR}$↑ or $\overline{XIOW}$↑		12		ns
t256	XDA<7:0> input set-up time to $\overline{XIOW}$↑	10			ns
t257	XDA<7:0> input hold time to $\overline{XIOW}$↑	8			ns
t258	XDA<7:0> output valid delay from $\overline{XIOR}$↓		37		ns
t259	XDA<7:0> hold time from $\overline{XIOR}$↑		14		ns
CPU to Memory Sequence					
t260	$\overline{MALE}$ active set-up time to CLK2↑		TBD		
t261	$\overline{MALE}$ inactive delay from CLK2↓		TBD		
t262	Address/Status set-up time to CLK2↑		TBD		

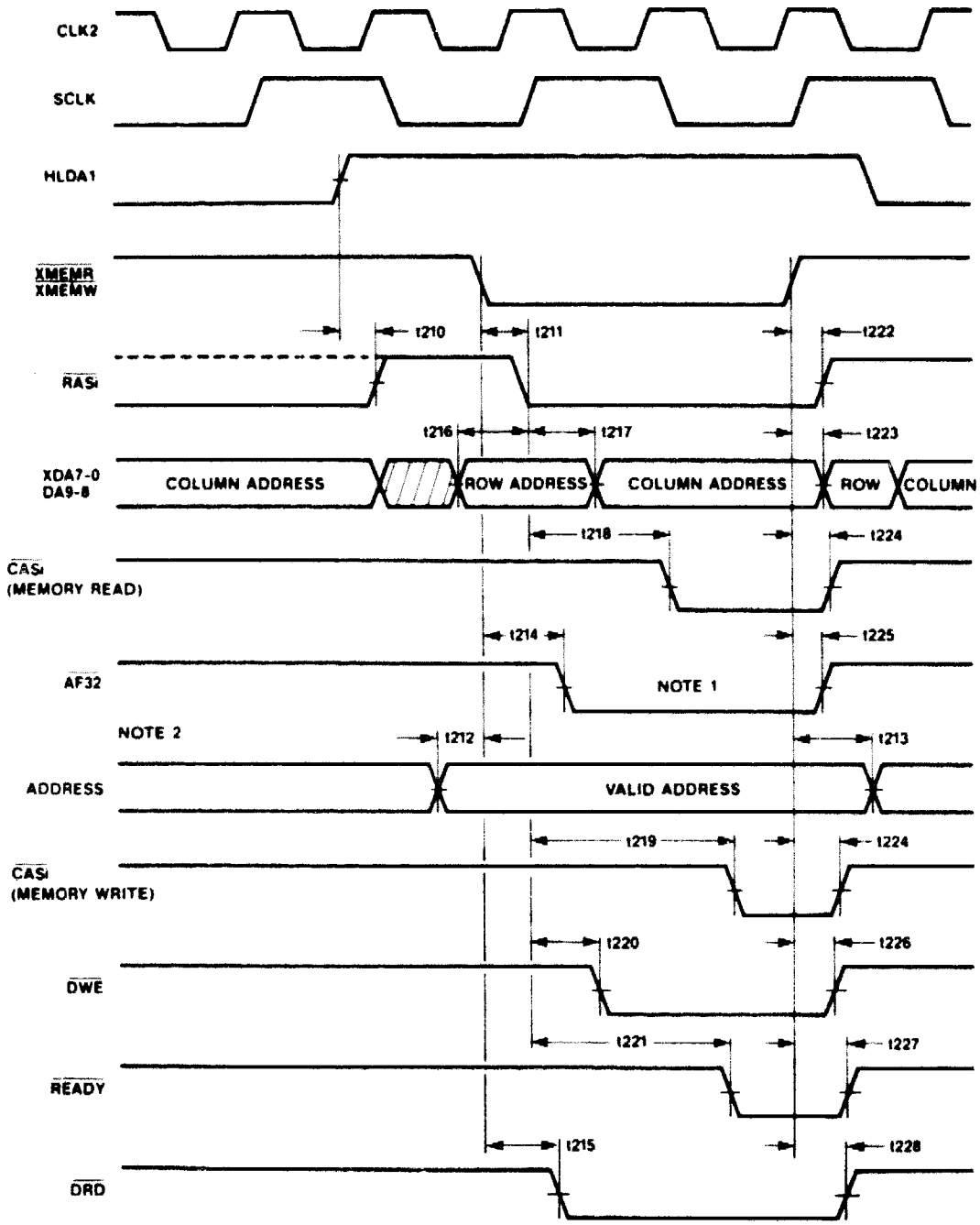
82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t263	Address/Status hold time from MALE↑		TBD		
t264	L64MEG, HIROM set-up time to CLK2↑		TBD		
t265	L64MEG, HIROM hold time to MALE↑		TBD		
t266	SMCMD active delay from MALE↓		TBD		
CPU Cycle Timing					
t270	AF32 active delay from CLK2↓		26		ns
t271	AF32 inactive delay from CLK2↓		17		ns
t272	CAS↓ active delay from MALE↑ for read-hit cycle		19		ns
t273	CAS↓ inactive delay from CLK2↑		16		ns
t274	CAS active delay from MALE↑ for read-hit cycle		20		ns
t275	CAS inactive delay from CLK2↑		18		ns
t276	Column Address stable from MALE↓		25		ns
t277	DRD active delay from CLK2↓		21		ns
t278	DRD inactive delay from CLK2↑		17		ns
t279	FBE active delay from CLK2↓		23		ns
t280	FBE inactive delay from CLK2↓		19		ns
t281	READY active delay from CLK2↑		20		ns
t282	READY inactive delay from CLK2↑		18		ns
t283	RAS↓ active delay from CLK2↑		18		ns
t284	Row address set-up time to RAS↓	10			ns
t285	Row address hold time from CLK2↑		12		ns
t286	CAS↓ active delay from CLK2↑		17		ns
t287	CAS active delay from CLK2↑		18		ns
t288	RAS↓ inactive delay from CLK2↑		17		ns
t289	RAS↓ precharge time	3t0			ns
t290	CAS↓ precharge time		1.5t0		ns
t291	DWE active delay from CLK2↑		16		ns
t292	DWE inactive delay from CLK2↑		17		ns

82C302 TIMING DIAGRAM (RESET SEQUENCE)



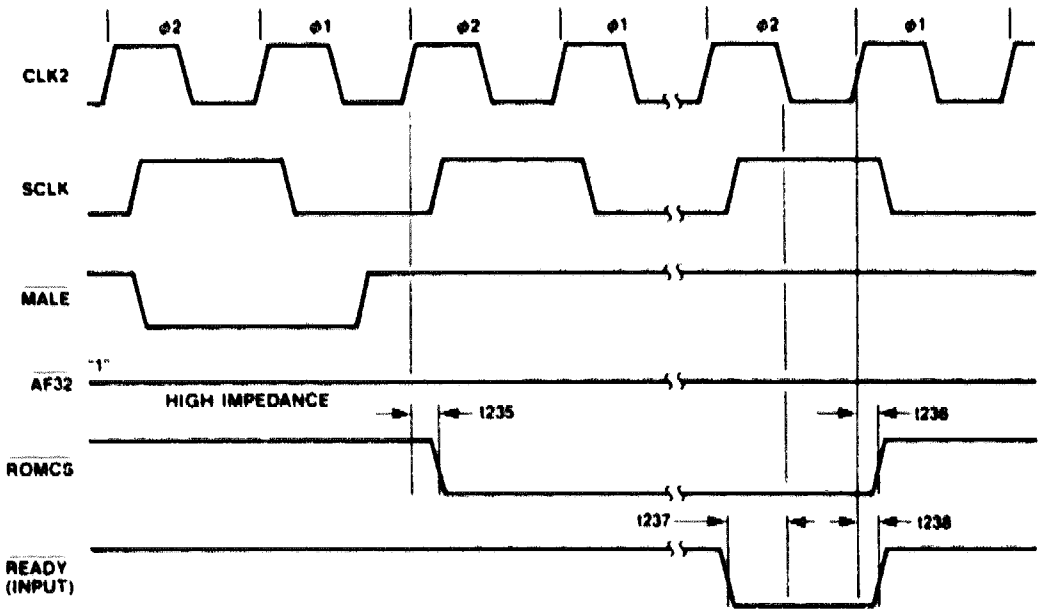
82C302 TIMING DIAGRAM (DMA CYCLES)



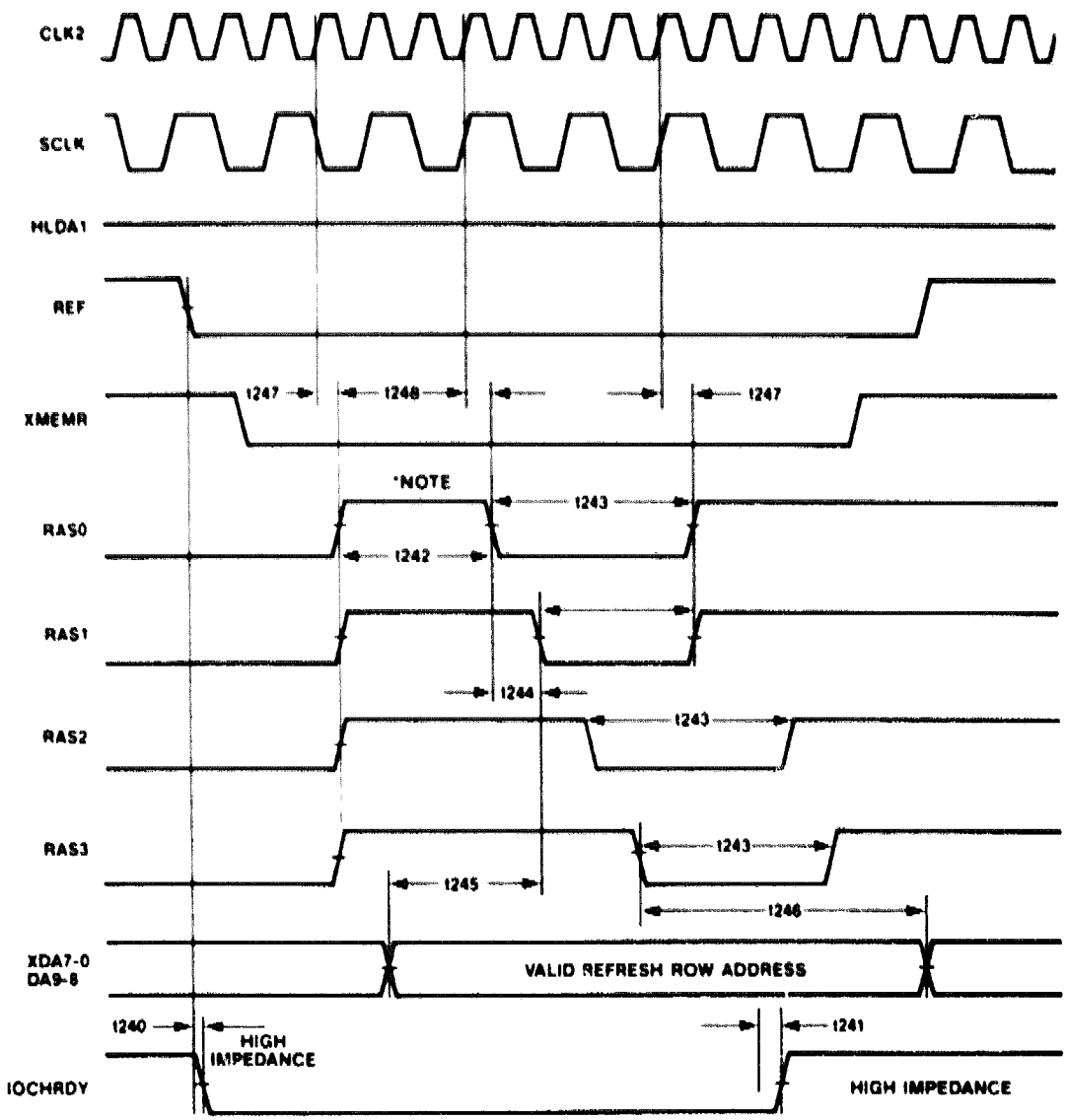
NOTE

1. During DMA cycles, only $\overline{RASi}$ will become active if $\overline{AF32}$ = 1 (not local memory)
2. The address includes L64MEG and HIROM input signals.

82C302 TIMING DIAGRAM (ROM READ CYCLE)

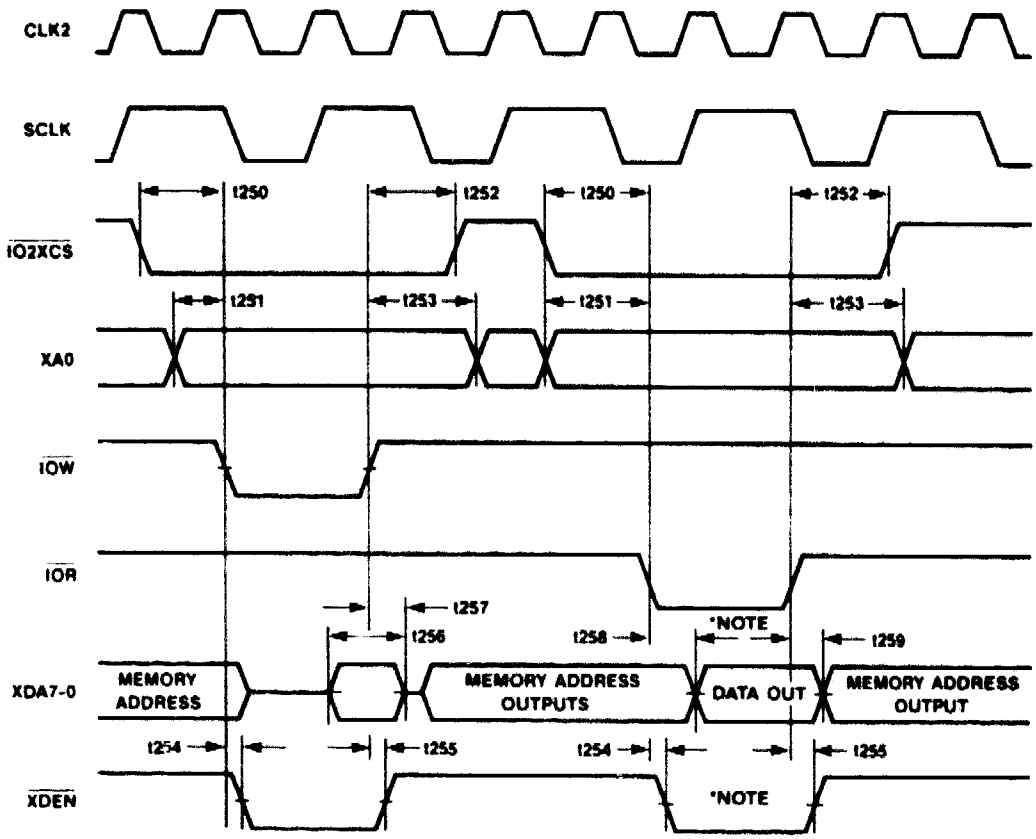


82C302 REFRESH CYCLE WAVEFORM



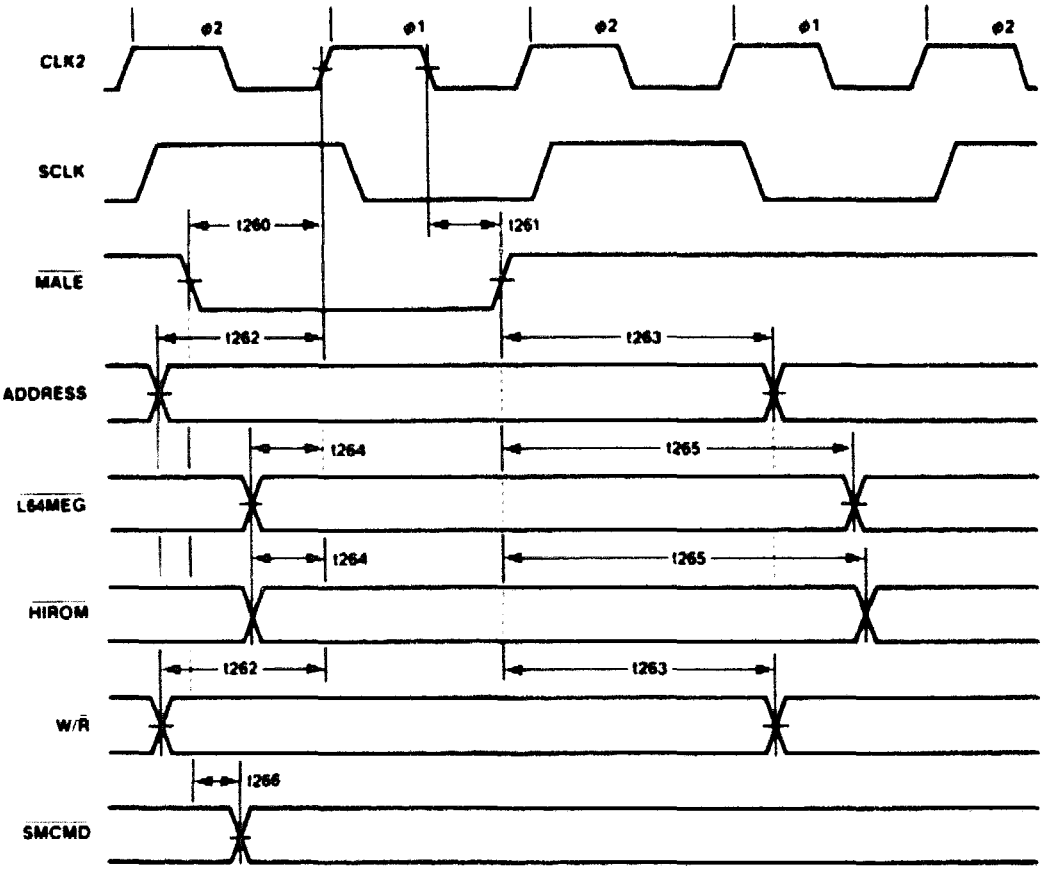
* **NOTE**: Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1

82C302 TIMING DIAGRAM (IO READ/WRITE)

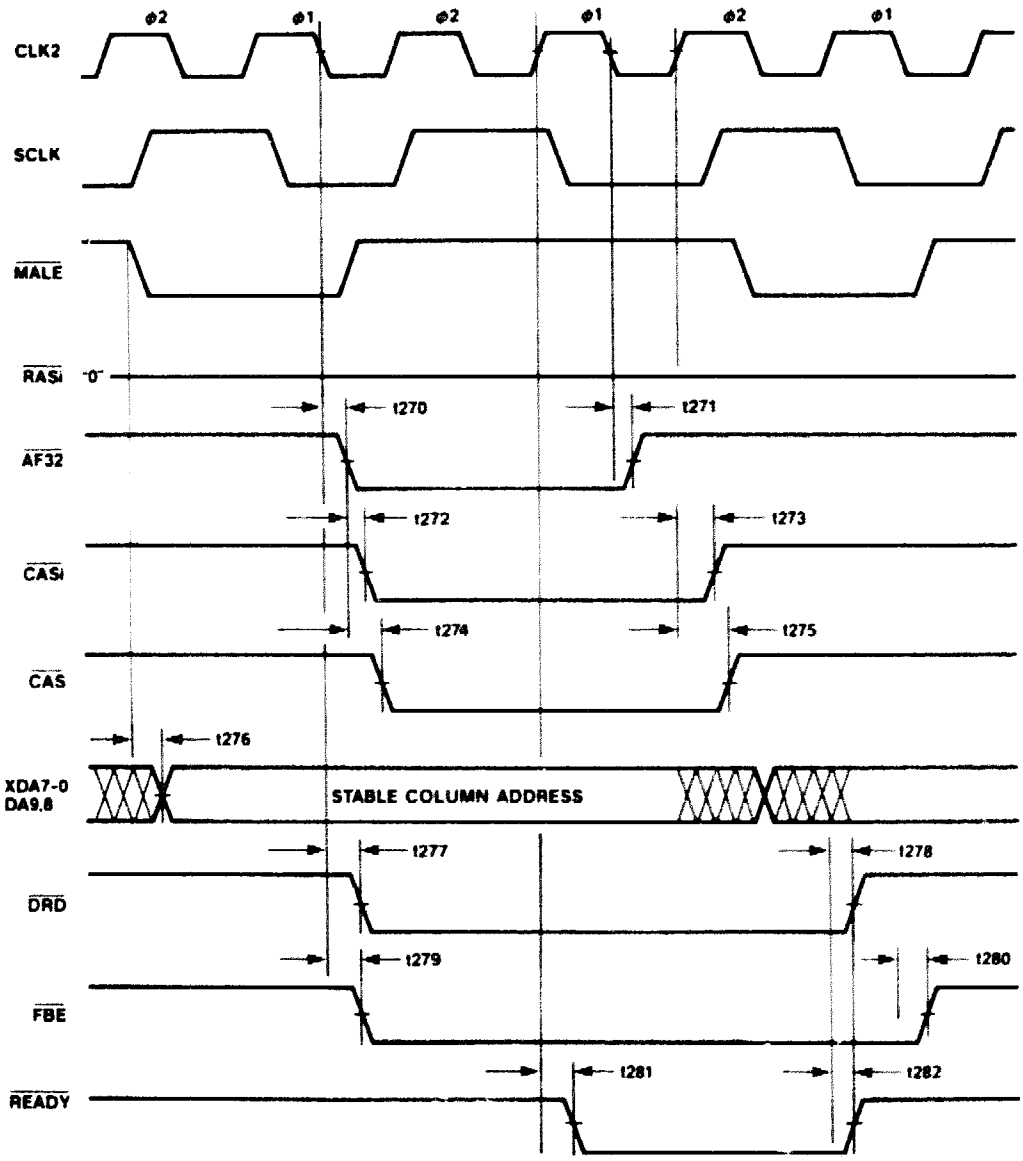


***NOTE:** No data output and XDEN is inactive if the index set up by the previous IO22 Write doesn't point to a valid IO23 register of 82C302.
Valid registers of IO23: 08H-0FH, 10H-13H, 28H-29H.

82C302 TIMING DIAGRAM (INPUT SETUP/HOLD TIME FOR CPU CYCLES)



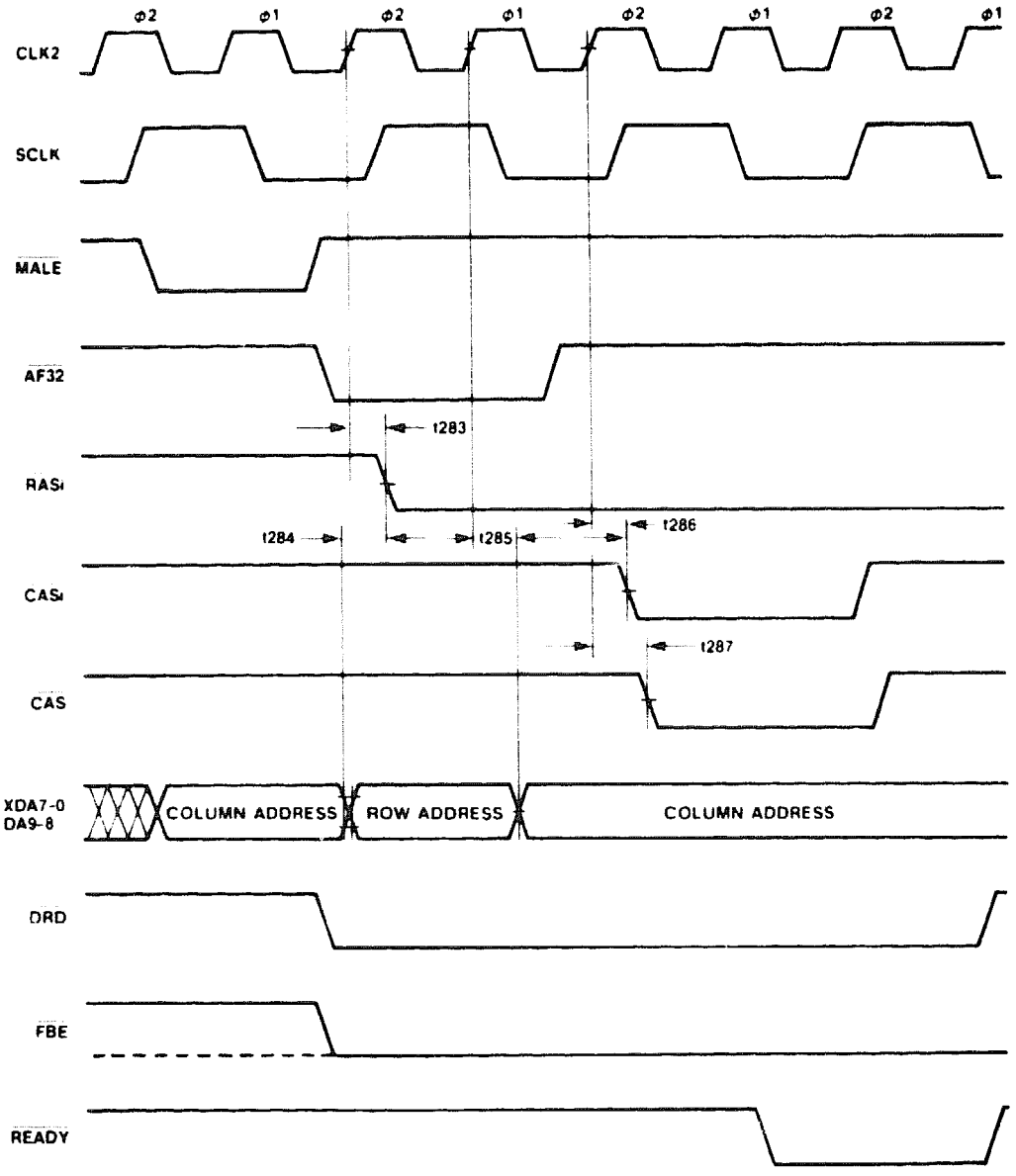
82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY CYCLE) READ HIT, ϕ WAIT STATE



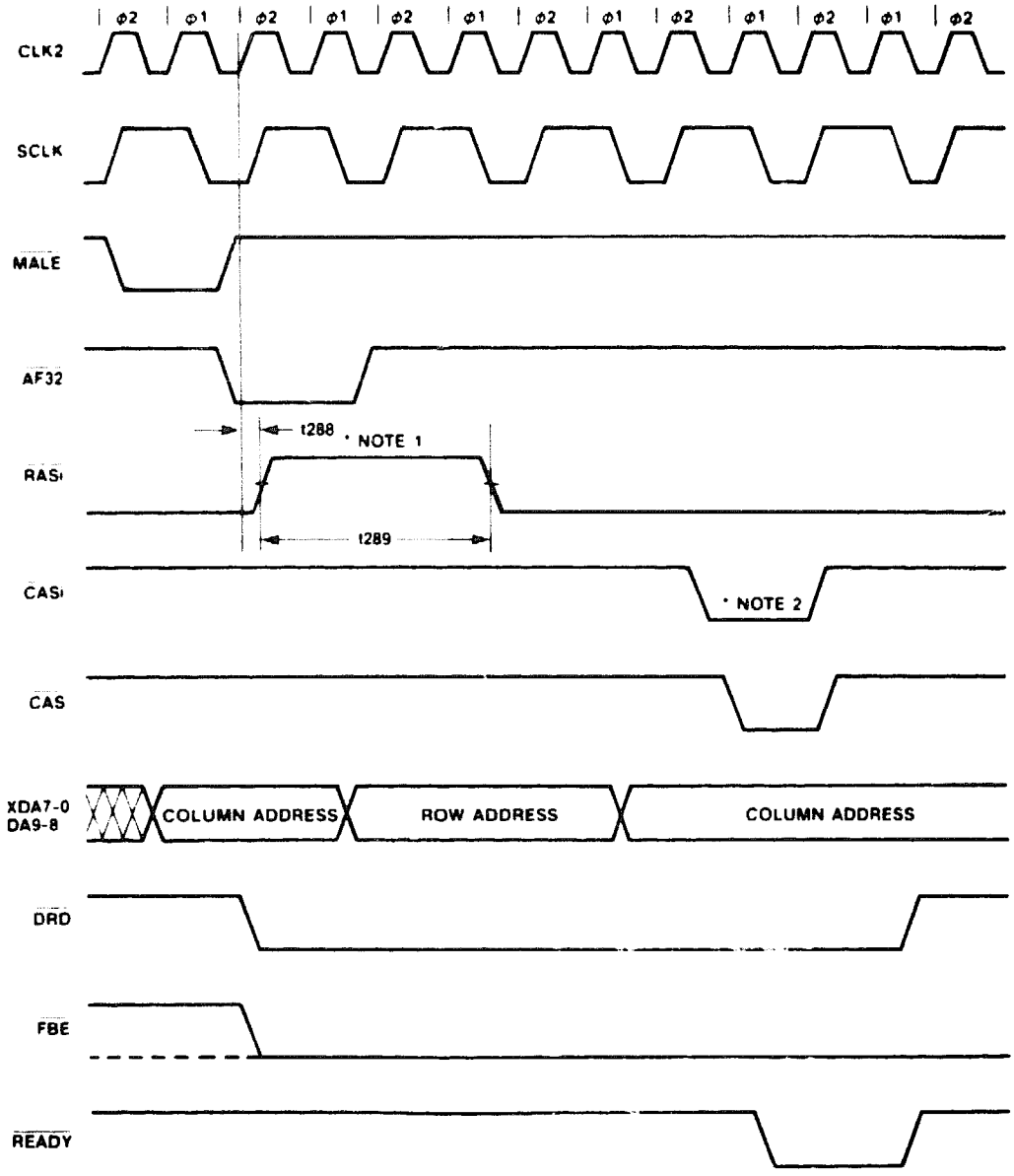
NOTE: Assume bit 6 of Register 11 (or 13) is programmed to "0".

DEVICES (CONT'D)

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ CYCLE WITH RAS BEING INACTIVE



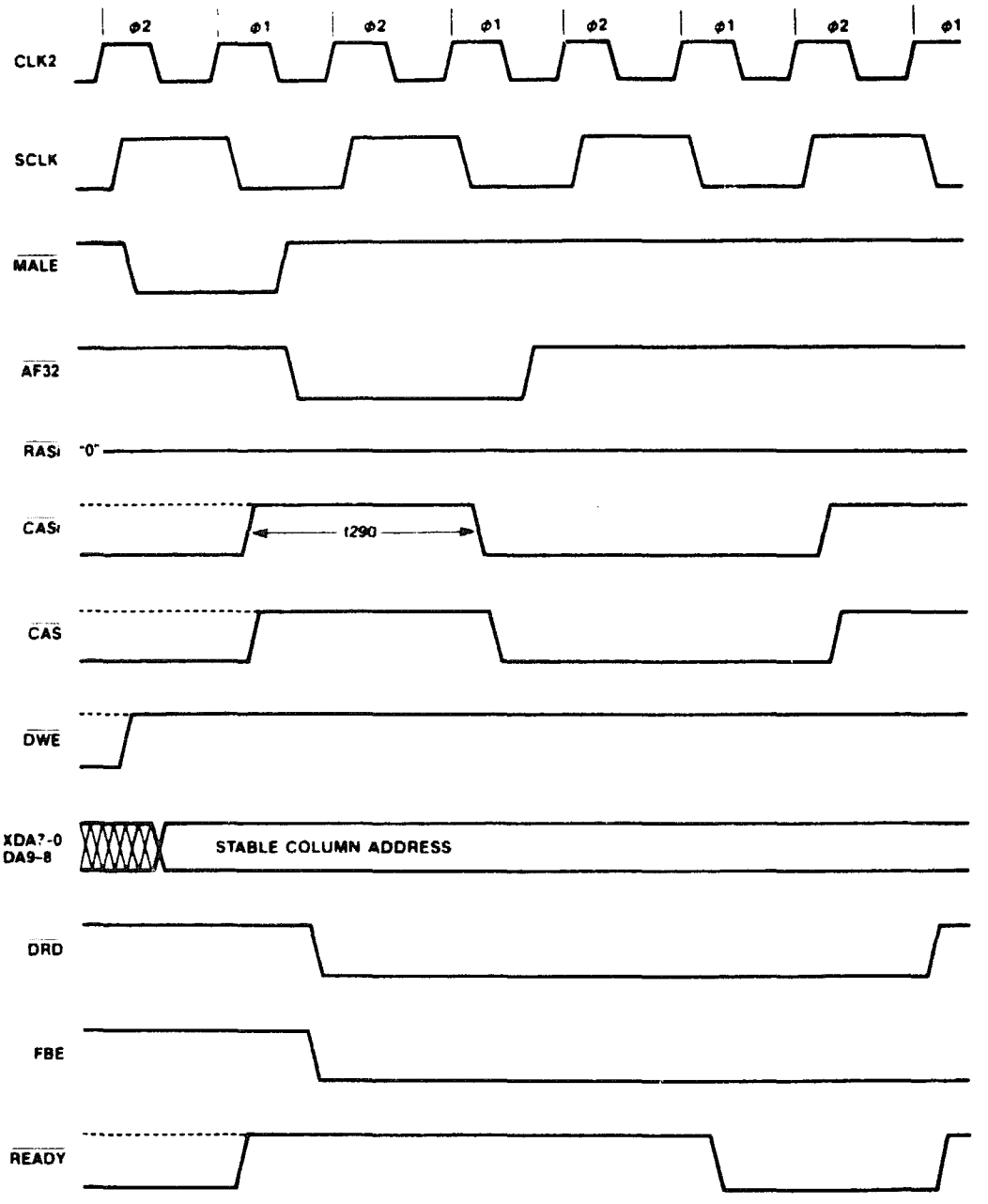
82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ MISS CYCLE



NOTES

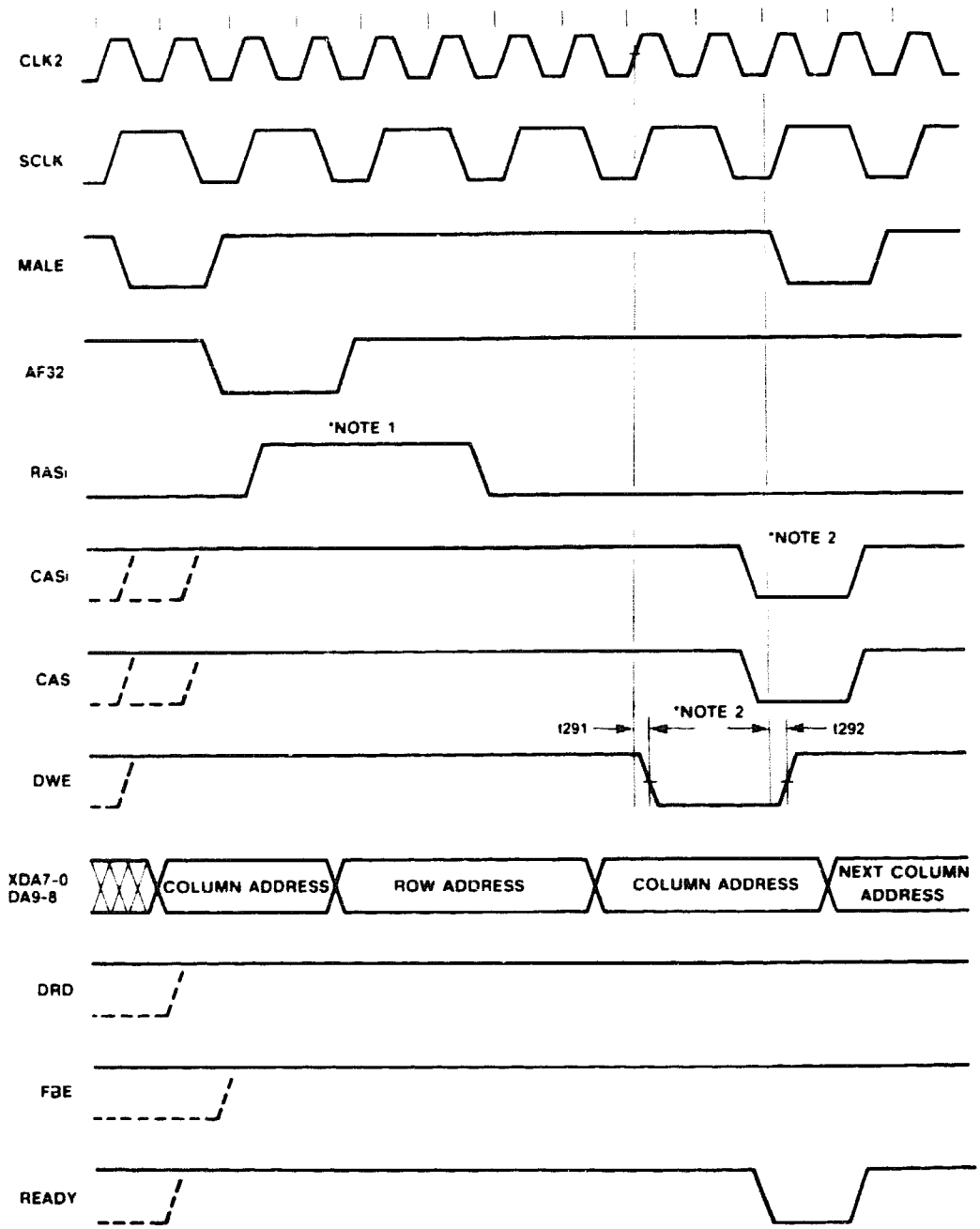
1. RASi precharge time will be increased by 2 CLK2 cycles if bit 7 of Register 11 (or 13) is programmed to "1".
2. CASi (and CAS) pulse width will be increased by 2 CLK2 cycles if bit 6 of registers 11, (or 13) is programmed to "1".

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY CYCLE) READ HIT FOLLOWING A WRITE OR 1 WAIT STATE READ-HIT CYCLE



NOTE: The read cycle will be identical to this waveform (regardless whether the previous cycle is a Write or not) if bit 6 of Register 11 (or 13) is programmed to "1"

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY) WRITE MISS CYCLE



NOTES

1. $\overline{\text{RASi}}$ precharge time will be increased by 2 CLKZ cycles if bit 7 of Register 11 (or 13) is programmed to "1".
2. $\overline{\text{CASi}}$ (and $\overline{\text{CAS}}$) pulse widths will be increased by 2 CLK2 cycles if bit 6 of register 11, (or 13) is programmed to "1".

82A303 HIGH ADDRESS BUFFERS

- Buffer for bits 31 12 of the Local, X and System address buses
- X and S address bus can be extended to 27 bits (128MB)
- Direct interface to AT Bus
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTIONS

The 82A303 as shown in figure 3-1 provides two functions.

- Generation of address decoding signals required by other chips
- Interface between the local X and System address bus

Address Decode

The address decoding circuit provides as outputs LIOCS, LMEGCS, L64MEG and HIROM. These signals are active if the address accesses satisfy the conditions defined in table 3-1. The signal decodes for LIOCS and LMEGCS are controlled by HLDA1 and latched on the trailing edge of MALE. The L64MEG and HIROM are simply decoded from the address signals.

Signal	Decode Condition
LIOCS	A<15 12> = 00H
LMEGCS	A<31 20> = 00H
L64MEG	A<31 26> = 00H
HIROM	A<31 26> = 3FH

Table 3-1. High Address Decodes Definition

Address Bus Interfaces

The 82A303 interconnects the local, X and system address buses with bidirectional drivers connecting each bus and the internal buses. Theses drivers have 24mA current drives for direct connection to the system address bus. The table 3-2 shows how the drivers are configured between the buses for each type of active bus requests. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

For all CPU sourced accesses, the addresses are latched on the trailing edge of MALE.

Active	Source	Target
HLDA1	XA	SA, A, MA
MASTER	SA	XA, A, MA
REF	-	SA driven LO
ATEN	A	XA, SA, MA
default	A	MA

Table 3-2. High Address Bus Control

27 bit Address Extensions

The standard AT implementation supports only 24-bit addresses. The CS 8230 allows for address extension on the SA and XA buses to 27 bits (128MB). This is done by grounding the enable pin XBHE for XA bus and SBHE for SA bus. Internal pullups are provided so that if the enable pins are left unconnected bits 24 to 27 of the respective bus are forced LO.

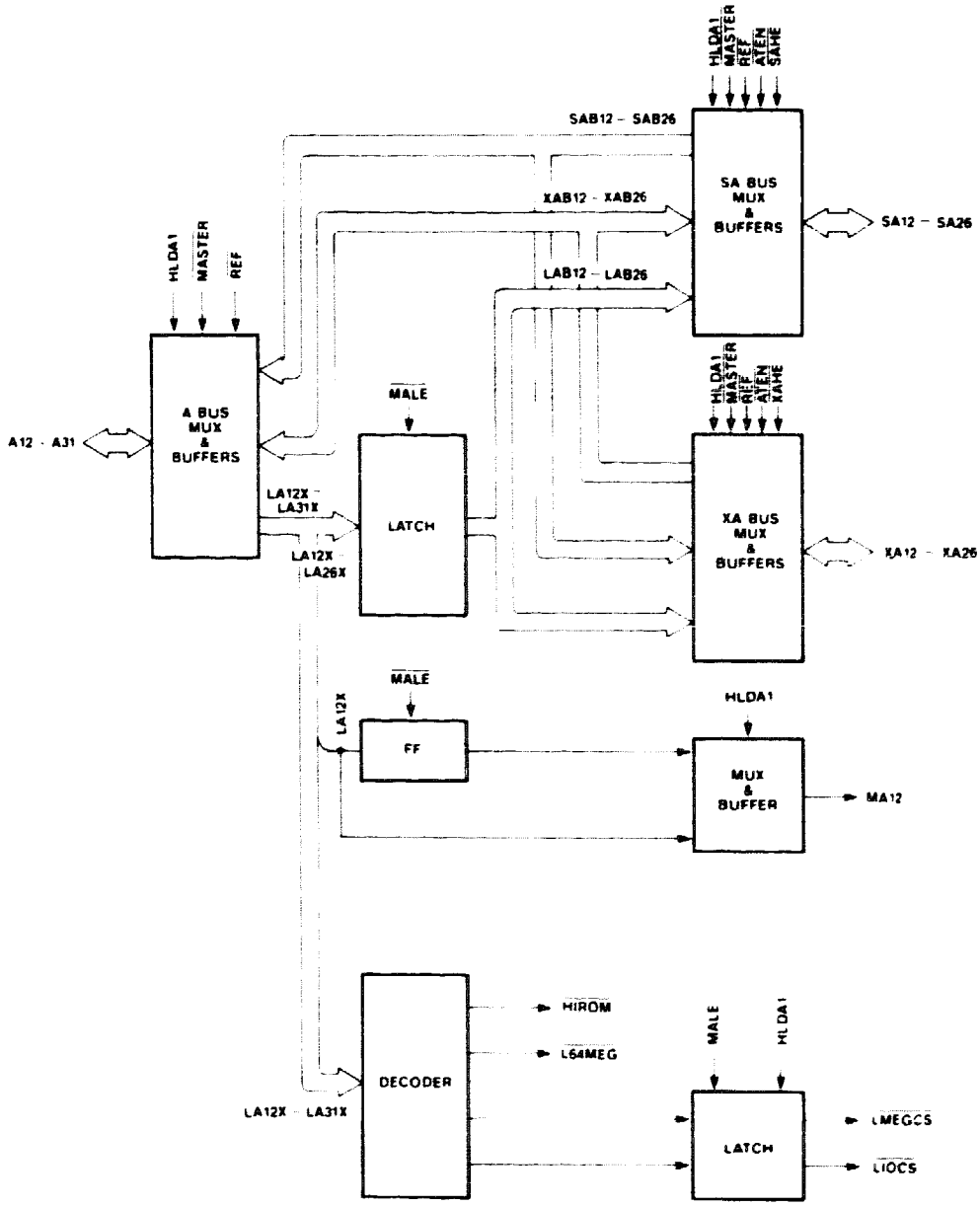


Figure 3-1. 82A303 Functional Block Diagram

82A303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A303 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}=-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA₀-20, 12> and XA₀-26, 21>
2. All SA₀-20, 12> and XA₀-26, 21> have I_{OL} = 24mA
3. All outputs and bidirectional pins

82A303 AC Characteristics

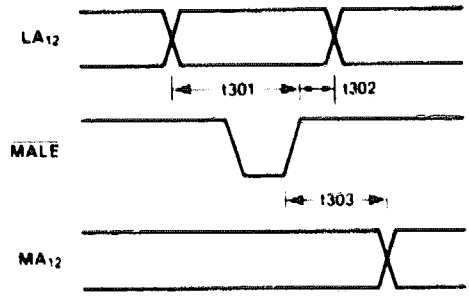
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

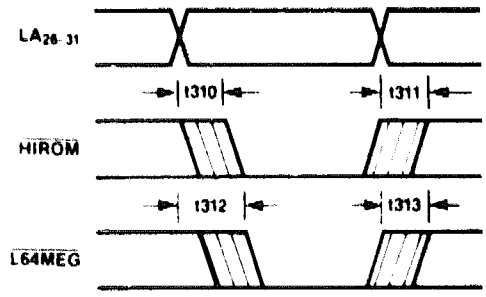
Sym	Description	Min.	Typ.	Max.	Units
t301	A to MA input set-up time to $\overline{MALE}$↑		TBD		
t302	A to MA input hold time from $\overline{MALE}$↑		TBD		
t303	MA output valid delay from $\overline{MALE}$↑	5		33	ns
t304	A to SA,XA input set-up time to $\overline{MALE}$↑		TBD		
t305	A to SA,XA input hold time from $\overline{MALE}$↑		TBD		
t306	SA output valid delay from $\overline{ATEN}$ active	8		33	ns
t307	SA tri-state delay from $\overline{ATEN}$ inactive	6		28	ns
t308	XA output valid delay from $\overline{ATEN}$ active	11		42	ns
t309	XA tri-state delay from $\overline{ATEN}$ inactive	9		38	ns
t310	$\overline{HIROM}$ decode active from A<32:26> valid	4		19	ns
t311	$\overline{HIROM}$ decode inactive from A<32:26> invalid	2		16	ns
t312	$\overline{L64MEG}$ decode active from A<32:26> valid	4		19	ns
t313	$\overline{L64MEG}$ decode inactive from A<32:26> invalid	2		17	ns
t314	$\overline{LIOCS}$ decode active from $\overline{MALE}$ active	6		26	ns
t315	$\overline{LIOCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns
t316	$\overline{LMEGCS}$ decode active from $\overline{MALE}$ active	6		26	ns
t317	$\overline{LMEGCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns
t318	A data valid delay from SA data valid	4		27	ns
t319	XA data valid delay from SA data valid	7		35	ns
t320	MA data valid delay from SA data valid	9		49	ns
t321	$\overline{LIOCS}$ decode active from SA data valid	13		50	ns
t322	$\overline{LIOCS}$ decode inactive from SA data invalid	10		39	ns
t323	$\overline{L64MEG}$ decode active from SA data valid	12		47	ns
t324	$\overline{L64MEG}$ decode inactive from SA data invalid	9		35	ns
t325	$\overline{LMEGCS}$ decode active from SA data valid	14		53	ns
t326	$\overline{LMEGCS}$ decode inactive from SA data invalid	10		40	ns
t327	A data valid delay from XA data valid	4		27	ns
t328	SA data valid delay from XA data valid	6		34	ns
t329	MA data valid delay from XA data valid	9		49	ns
t330	$\overline{LIOCS}$ decode active from XA data valid	13		50	ns

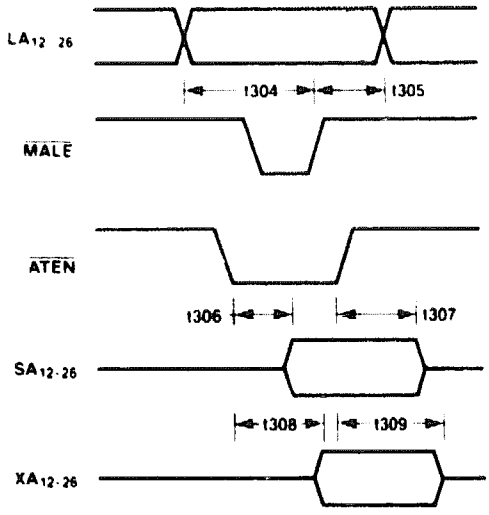
82A303 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

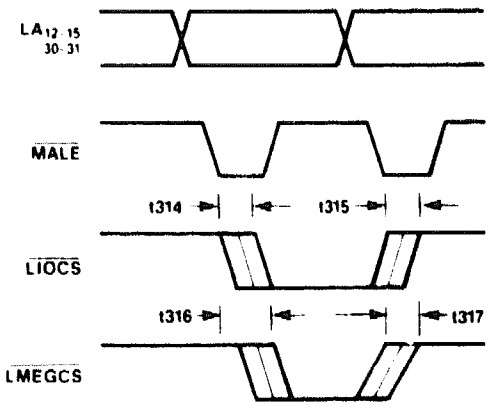
Sym	Description	Min.	Typ.	Max.	Units
t331	LIOCS decode inactive from XA data invalid	9		38	ns
t332	L64MEG decode active from XA data valid	12		47	ns
t333	L64MEG decode inactive from XA data invalid	9		35	ns
t334	LMEGCS decode active from XA data valid	14		53	ns
t335	LMEGCS decode inactive from XA data invalid	10		40	ns
t336	SA valid delay from REF active	18		64	ns
t337	SA tri-state delay from REF inactive	8		33	ns

82A303 TIMING DIAGRAMS

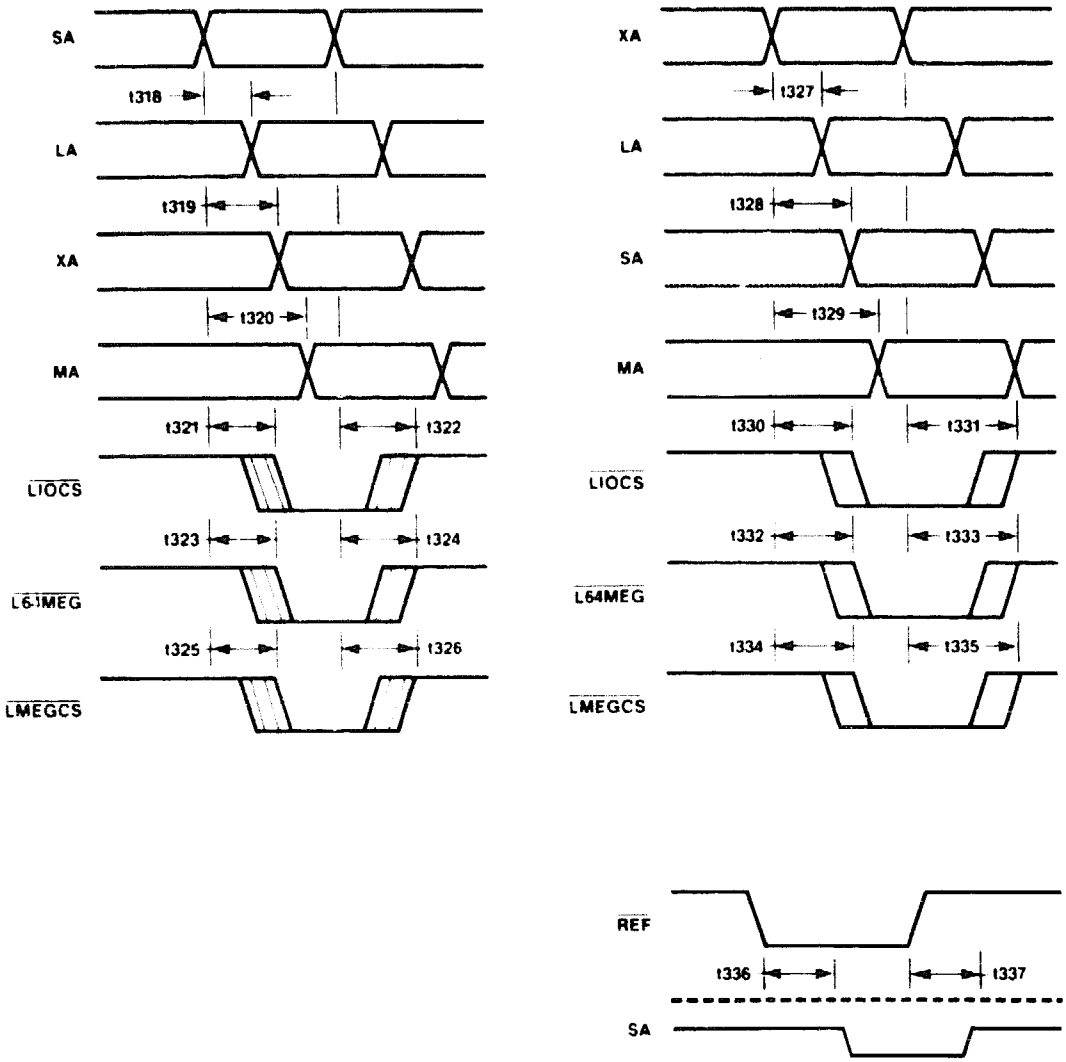








82A304 TIMING DIAGRAMS



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82A304 LOW ADDRESS BUFFERS

- Buffer for bits 11:00 of the Local, X and System address buses.
- Peripheral device decode
- Direct interface to AT Bus
- Refresh Address Generation
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTIONS

Address Decode

The signals IO2XCS, 8042CS, PORTBCS, NMICS, 287CS, and AS provide the lower address decodes for the corresponding devices after being qualified by the LIOCS generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT IO addresses and is as shown in table 4-1. For applications where these devices are required to be relocated, the EXDEC can be tied LOW to ignore the LIOCS qualification and the MA<11:10> address bits.

Signal	Addresses Decoded
IO2XCS	022H, 023H
8042CS	060H, 064H
PORTBCS	061H
NMICS	070H
287CS	0E0H to 0FFH

Table 4-1. Low Address Decode Definition

Address Bus Interfaces

The 82A304 interfaces between the bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER, REF, and ATEN to drive the signals from the source to the target buses as defined by table 4-2 for each signal when active. When REF is asserted, the refresh counter is gated to the SA bus as refresh row address and is incremented. When none of the listed signals are active, the default buffers configuration is that the A bus drives the MA bus for memory accesses by CPU.

The SA<11:00> are 24mA address buffers for direct interface to the AT bus.

Active	Source	Target
HLDA1	XA	SA, MA, A
MASTER	SA	XA, MA, A
REF	Counter	SA
ATEN	A<11:2>	SA<11:2>, XA<11:2>, MA<11:4>
	XA<1:0>	SA<1:0>
default	A	MA

Table 4-2. Bus Control Definition

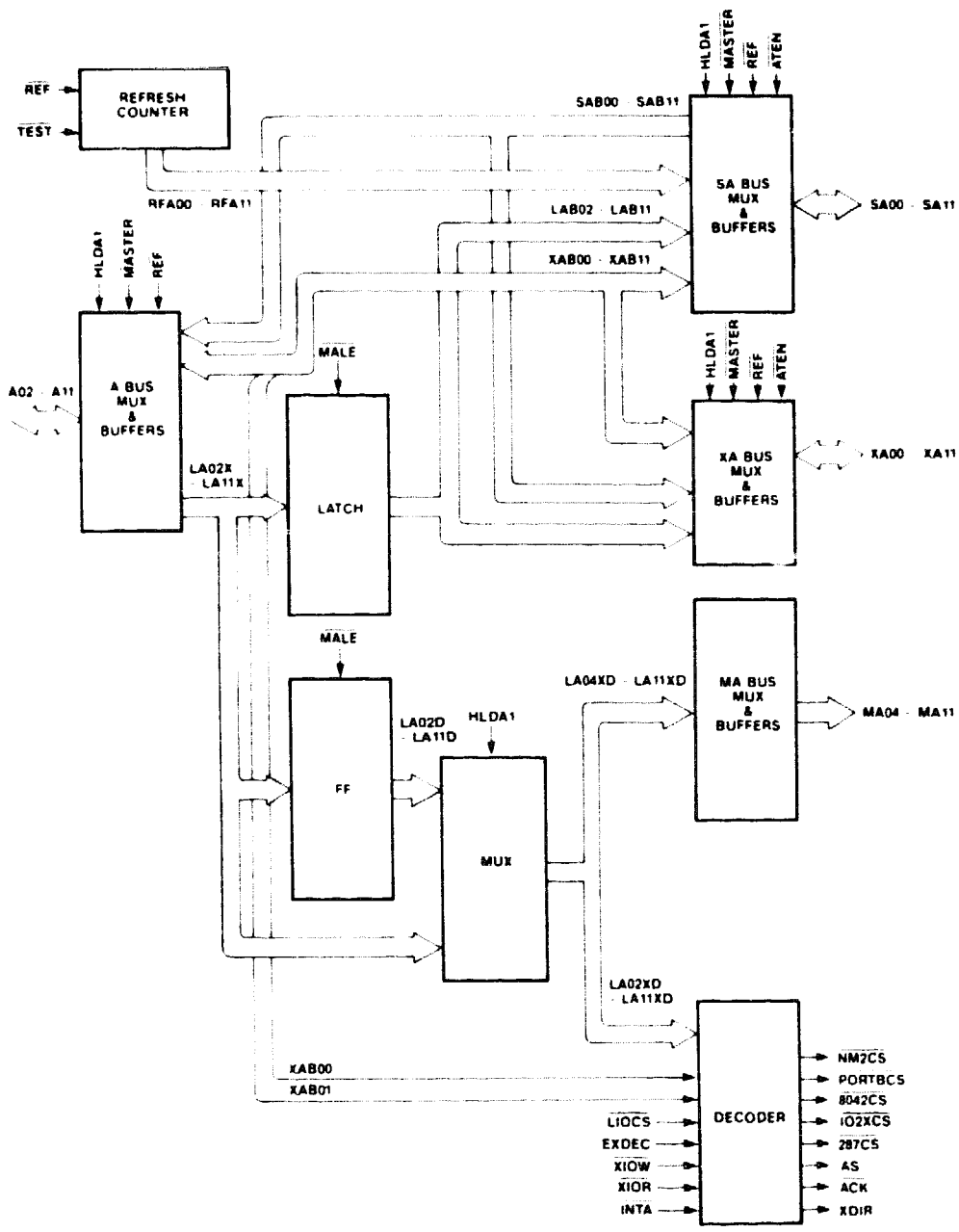


Figure 4-1. 82A304 Functional Block Diagram

82A304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL} 10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL} 24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH} -3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<11:00>
2. All SA<11:00> have I_{OL} = 24mA
3. All outputs and bidirectional pins

82A304 AC Characteristics

(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t401	A to MA input set-up time to MALE*		TBD		
t402	A to MA input hold time from MALE*		TBD		
t403	MA output valid delay from MALE*	5		34	ns
t404	A to SA, XA input set-up time to MALE*		TBD		
t405	A to SA, XA input hold time from MALE*		TBD		
t406	SA output valid delay from ATEN active	8		33	ns
t407	SA tri-state delay from ATEN inactive	6		28	ns
t408	XA output valid delay from ATEN active	10		41	ns
t409	XA tri-state delay from ATEN inactive	9		37	ns
t410	NMICS decode active from MALE*	11		44	ns
t411	NMICS decode inactive from MALE*	10		40	ns
t412	PORTBCS decode active from MALE*	11		44	ns
t413	PORTBCS decode inactive from MALE*	10		40	ns
t414	8042CS decode active from MALE*	11		44	ns
t415	8042CS decode inactive from MALE*	10		40	ns
t416	IO2XCS decode active from MALE*	11		44	ns
t417	IO2XCS decode inactive from MALE*	10		40	ns
t418	287CS decode active from MALE*	11		44	ns
t419	287CS decode inactive from MALE*	10		40	ns
t420	A data valid delay from SA data valid	4		26	ns
t421	XA data valid delay from SA data valid	3		35	ns
t422	MA data valid delay from SA data valid	9		49	ns
t423	NMICS decode active from SA data valid	14		58	ns
t424	NMICS decode inactive from SA data invalid	11		46	ns
t425	PORTBCS decode active from SA data valid	15		59	ns
t426	PORTBCS decode inactive from SA data invalid	11		46	ns
t427	8042CS decode active from SA data valid	15		59	ns
t428	8042CS decode inactive from SA data invalid	11		46	ns
t429	IO2XCS decode active from SA data valid	12		59	ns
t430	IO2XCS decode inactive from SA data invalid	12		46	ns

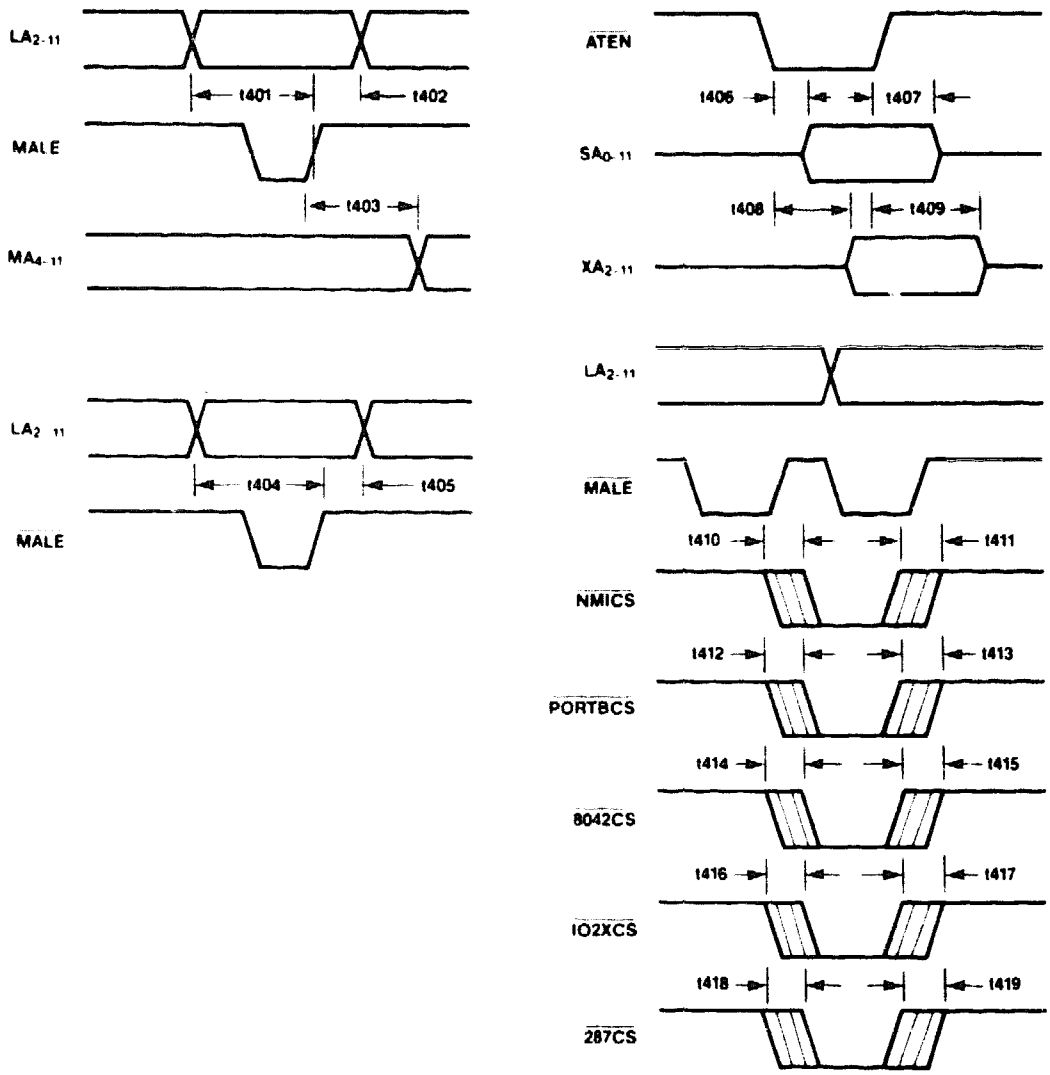
82A304 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t431	$\overline{287CS}$ decode active from SA data valid	16		59	ns
t432	$\overline{287CS}$ decode inactive from SA data invalid	13		46	ns
t433	$\overline{XDIR}$ decode active from SA data valid	15		59	ns
t434	$\overline{XDIR}$ decode inactive from SA data invalid	15		60	ns
t435	A data valid delay from XA data valid	4		26	ns
t436	SA data valid delay from XA data valid	7		34	ns
t437	MA data valid delay from XA data valid	9		49	ns
t438	$\overline{NMICS}$ decode active from XA data valid	14		58	ns
t439	$\overline{NMICS}$ decode inactive from XA data invalid	11		46	ns
t440	$\overline{PORTBCS}$ decode active from XA data valid	15		59	ns
t441	$\overline{PORTBCS}$ decode inactive from XA data invalid	11		46	ns
t442	$\overline{8042CS}$ decode active from XA data valid	15		59	ns
t443	$\overline{8042CS}$ decode inactive from XA data invalid	11		46	ns
t444	$\overline{IO2XCS}$ decode active from XA data valid	12		59	ns
t445	$\overline{IO2XCS}$ decode inactive from XA data invalid	12		46	ns
t446	$\overline{287CS}$ decode active from XA data valid	16		59	ns
t447	$\overline{287CS}$ decode inactive from XA data invalid	13		46	ns
t448	$\overline{XDIR}$ decode active from XA data valid	15		55	ns
t449	$\overline{XDIR}$ decode inactive from XA data invalid	15		55	ns
t450	$\overline{NMICS}$ decode active from $\overline{LIOCS}$ active	7		31	ns
t451	$\overline{NMICS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t452	$\overline{PORTBCS}$ decode active from $\overline{LIOCS}$ active	7		31	ns
t453	$\overline{PORTBCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t454	$\overline{8042CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t455	$\overline{8042CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t456	$\overline{IO2XCS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t457	$\overline{IO2XCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t458	$\overline{287CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns
t459	$\overline{287CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns
t460	$\overline{XDIR}$ decode active from $\overline{LIOCS}$ active	8		32	ns

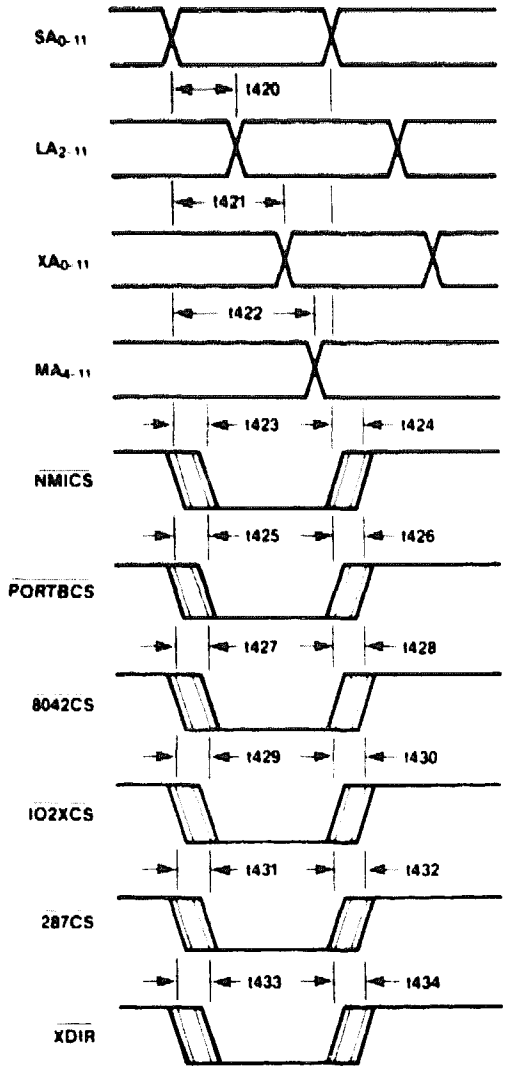
82A304 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

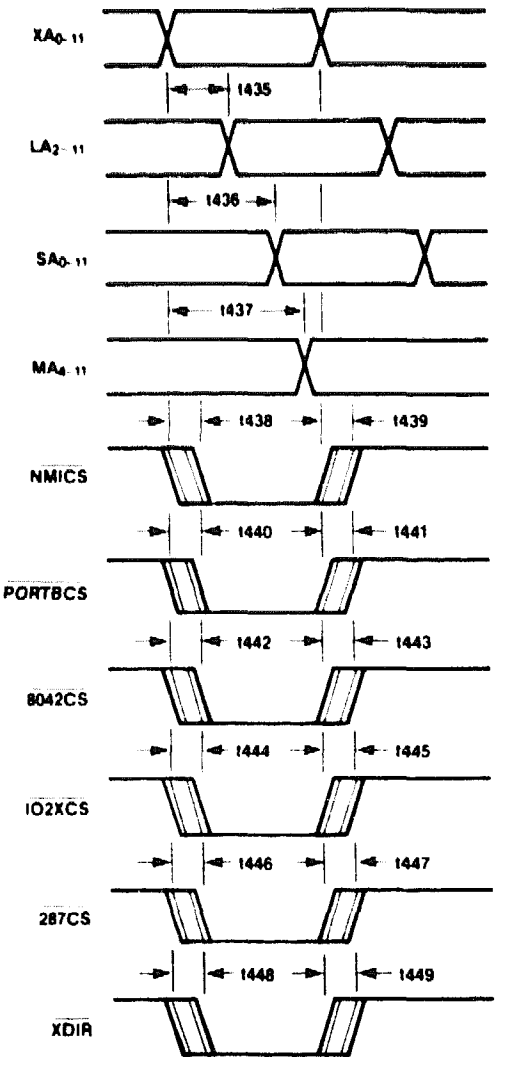
Sym	Description	Min.	Typ.	Max.	Units
t461	$\overline{XDIR}$ decode inactive from $\overline{LIOCS}$ inactive	5		26	ns
t462	$\overline{XDIR}$ decode active from $\overline{INTA}$ active	4		23	ns
t463	$\overline{XDIR}$ decode inactive from $\overline{INTA}$ inactive	2		17	ns
t464	$\overline{XDIR}$ decode active from $\overline{XIOR}$ active	6		27	ns
t465	$\overline{XDIR}$ decode inactive from $\overline{XIOR}$ inactive	4		20	ns
t466	$\overline{ACK}$ decode active from HLDA1 active	9		37	ns
t467	$\overline{ACK}$ decode inactive from HLDA1 inactive	7		32	ns
t468	$\overline{ACK}$ decode active from MASTER active	8		33	ns
t469	$\overline{ACK}$ decode inactive from MASTER inactive	6		26	ns
t470	SA data valid delay from $\overline{REF}$ active	18		64	ns
t471	SA tri-state delay from $\overline{REF}$ inactive	8		33	ns

82A304 TIMING DIAGRAMS

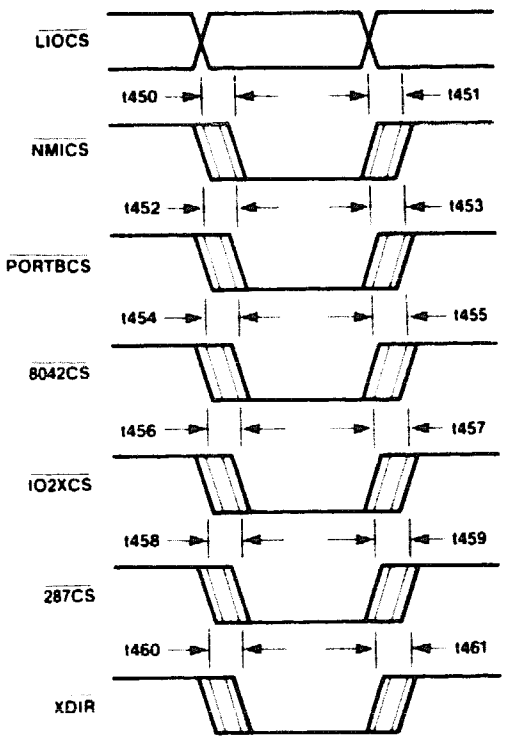


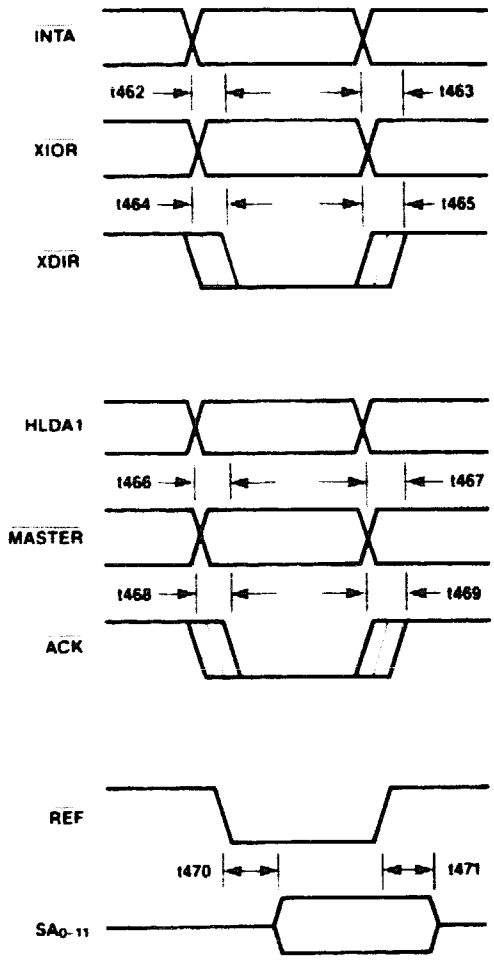
82A304 TIMING DIAGRAMS





82A304 TIMING DIAGRAMS





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82A305 DATA BUFFER

- Nibble Slice of Memory and AT Data Bus Interface
- Data Size Conversion
- Advanced Schottky technology

FUNCTIONAL DESCRIPTION

The 82A305 interfaces between the Local Memory and System (AT IO channel) data busses and provides data alignment and size conversion for AT IO channel operations. It is designed as a nibble slice to reduce pin count and simplify system design and two parts are used to interface all data buses.

Bus Controls

The 82A305 controls the bus buffers according to the signals HLDA1, ATEN, MDEN, LDEN, SDIR, MRD, and AC<3:0>. The first group of signals HLDA1, ATEN, MDEN, and LDEN determines which buses are connected, and the second group of signals SDIR, MRD, and AC<3:0> determines the direction of the buffers drivers. Table 5-1 shows the bus connections for different bus cycles.

All drivers are active for the active buses, and external bus controls are required if selective data bits need be controlled. For the DRAM interface, the LBE<3:0> must be used to ensure that only the valid data bytes are written into the DRAM's during a write cycle.

Bus Cycles	From Bus	To Bus	Direction Control
HLDA1=0, ATEN=1	D	MD	MRD=1
	MD	D	MRD=0
HLDA1=0, ATEN=0	D	SD	SDIR=1
	SD	D	SDIR=0
HLDA1=1	SD	MD,D	SDIR=0, MRD=1
	MD	SD	SDIR=1, MRD=0
	D	SD	SDIR=1, MRD=1, LDEN=0

Table 5-1. Bus Control Definitions

Data Conversion

The 82A305 provides the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action codes AC<3:0> are used to control how bus bits are connected between the IO channel SD bus and the CPU local bus D or the system memory MD bus. The action codes are provided by the 82C301 bus controller for CPU to AT bus access cycles and is qualified by the ACEN. The meaning of the action codes are

AC<3:0>	FROM	TO
0	MD,D<15:0>	SD<15:0>
1	MD,D<15:8>	SD<15:8>, SD<7:0>
2	MD,D<31:16>	SD<15:0>
3	MD,D<31:24>	SD<15:8>, SD<7:0>
4	MD,D<31:0>	SD<31:0>
5	SD<7:0>	MD,D<7:0>
6	SD<7:0>	MD,D<15:8>
7	SD<7:0>	MD,D<23:16>
8	SD<7:0>	MD,D<31:24>
9	SD<15:0>	MD,D<15:0>
A	SD<15:0>	MD,D<31:16>
B	reserved	
C	SD<31:0>	MD,D<31:0>
D	reserved	
E	reserved	
F	reserved	

Table 5-2. Action Code Definition

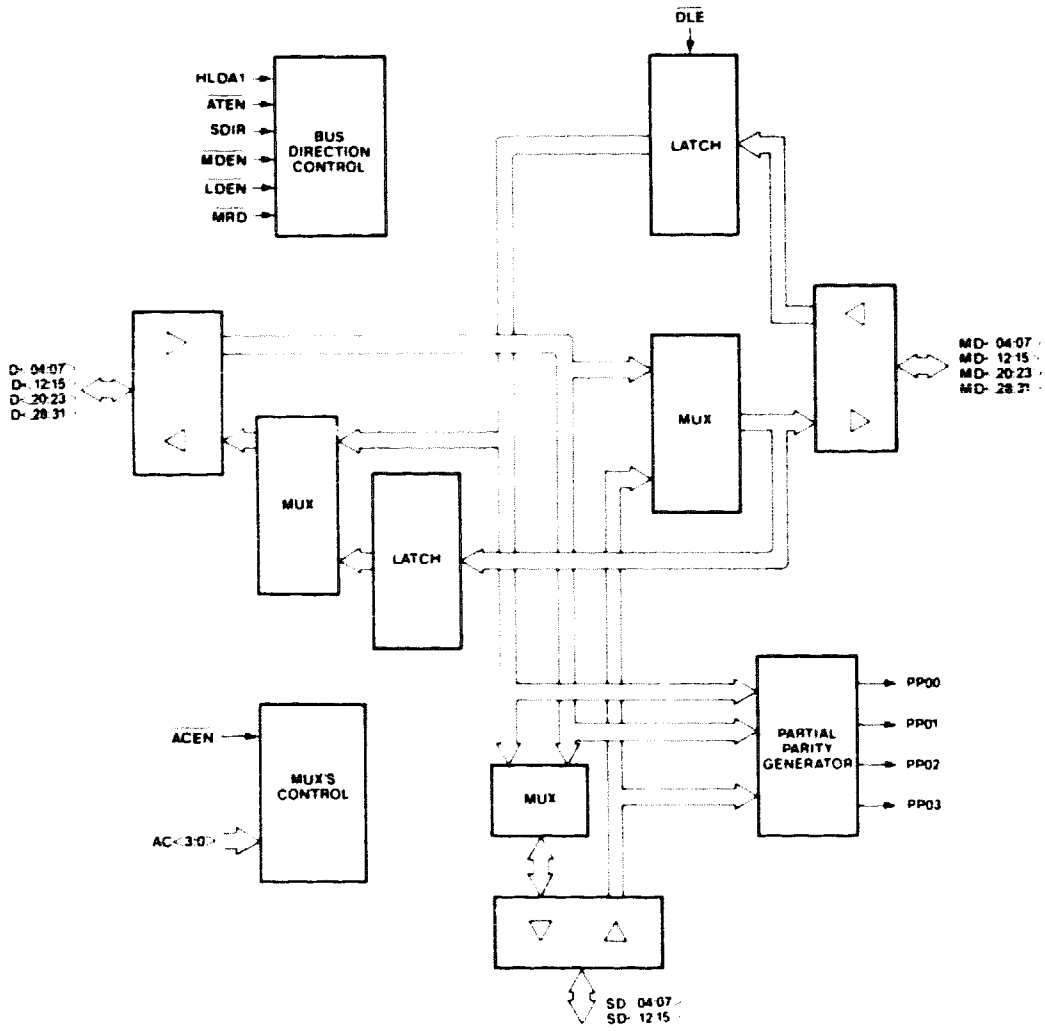


Figure 5-1. 82A305 Functional Block Diagram

82A305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL} 10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL} 24mA	V_{OL2}		0.5	V
Output High Voltage I_{OH} -3.3mA (Note 2)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

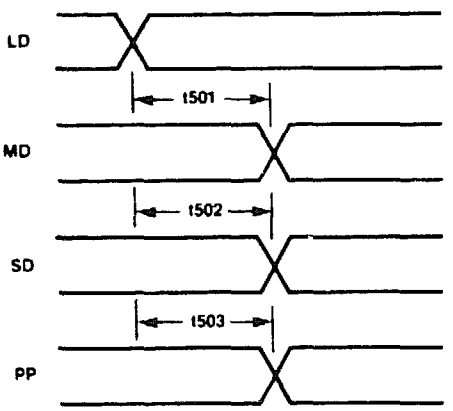
NOTES
1. All bus outputs and PP<3.0> have I_{OL} = 10mA
2. All outputs and bidirectional pins

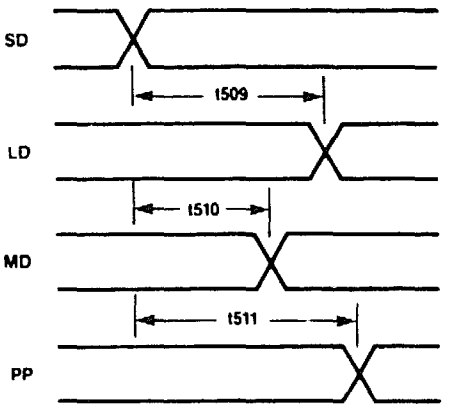
82A305 AC Characteristics

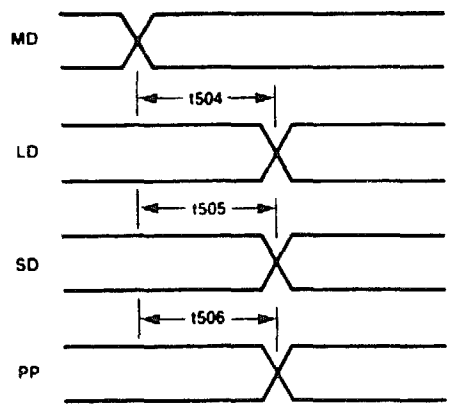
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

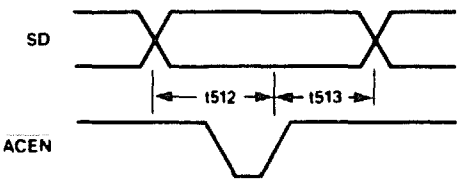
Sym	Description	Min.	Typ.	Max.	Units
t501	MD data valid delay from LD data valid	4		27	ns
t502	SD data valid delay from LD data valid	4		27	ns
t503	PP data valid delay from LD data valid	5		29	ns
t504	LD data valid delay from MD data valid	4		28	ns
t505	SD data valid delay from MD data valid	4		28	ns
t506	PP data valid delay from MD data valid	5		30	ns
t507	MD data set-up time to $\overline{DLE}$↑		TBD		
t508	MD data hold time from $\overline{DLE}$↑		TBD		
t509	LD data valid delay from SD data valid	8		38	ns
t510	MD data valid delay from SD data valid	4		27	ns
t511	PP data valid delay from SD data valid	5		33	ns
t512	SD data set-up time to $\overline{ACEN}$↑		TBD		
t513	SD data hold time from $\overline{ACEN}$↑		TBD		
t514	MD data valid delay from $\overline{MDEN}$↓	7		29	ns
t515	MD tri-state delay from $\overline{MDEN}$↑	5		23	ns
t516	LD data valid delay from $\overline{MDEN}$↓	7		30	ns
t517	LD tri-state delay from $\overline{MDEN}$↑	5		23	ns

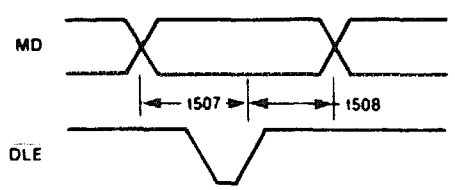
82A305 TIMING DIAGRAMS

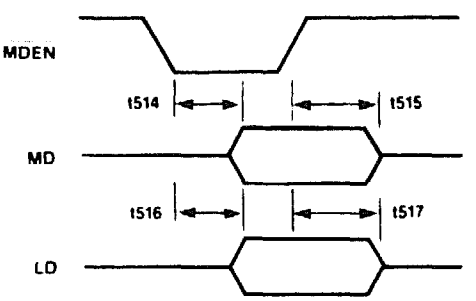












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82A306 CONTROL BUFFER

- 14.318MHz oscillator and divide by 12 counter
- Byte enable latch
- Parity Checking
- Direct interface to AT Bus
- Advanced Schottky TTL technology

FUNCTIONAL DESCRIPTION

14MHz Oscillator and Divider

The color reference oscillator is provided eliminating the 8224 normally used in AT compatible systems. A divide by 12 counter is also included to generate the OSC/12 (1.19MHz) signal used on the system board.

AF32 Generation

The AF32 is used in the CS 8230 system to indicate that the current bus cycle is a CPU local bus cycle.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located on the 82A306. An additional input FBE is provided to force all byte enables active during certain memory operations. A pullup resistor is provided on the FBE input for implementations not requiring this feature.

Parity Checking and Generation

The 82A306 provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH<3:0> and PPL<3:0> generated on the two (nibble wide) data buffers 82A305.

For a memory read access, read parity PPH<3:0> and PPL<3:0> are checked against the parity bits MP<3:0> read from memory. These parity bits are latched by $\overline{CAS}$ and $\overline{PCHK}$ so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes which are not valid. The OR'ed byte-wise parity error is then latched as the output LPAR if PEN input is asserted.

During a memory write access, write parity for each byte is generated from PPH<3:0> and PPL<3:0> and can be gated onto the memory parity bus MP<3:0> if enabled by $\overline{WPE}$ controlling the tri-state drivers. If an external parity generation circuit is used, an internal pullup resistor is provided for $\overline{WPE}$ to disable the write parity output buffers if left unconnected.

Bus Drivers

24mA drivers are provided for some of the control signals on the IO channel. These include SYSCLK, OSC, OSC/12, RDRV, $\overline{SBHE}$, BALE, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{SMEMR}$, $\overline{SMEMW}$ and OUT1.

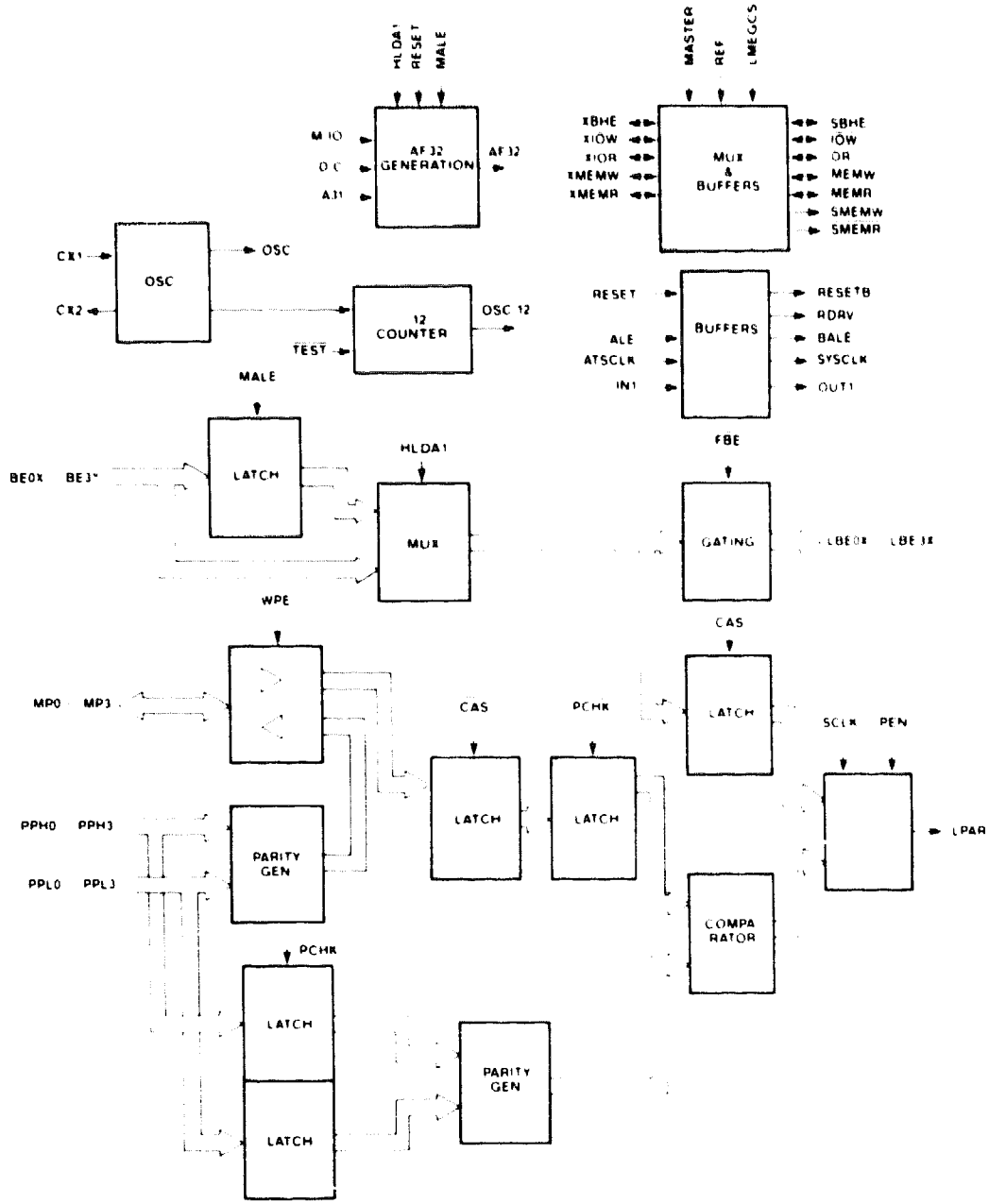


Figure 6-1. 82A306 Functional Block Diagram

82A306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{STG}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL} = 10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL} = 24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH} = -3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	µA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	µA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	µA
Output Short Circuit Current V_O = 0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	µA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	µA

NOTES
1. MP<3:0>, XIOW, XIOR, XBHE, XMEMW, XMEMR, RESTEB, LBE<3:0> all have I_{OL} = 10mA
2. SBHE, IOW, IOR, MEMW, MEMR, SMEMW, SMEMR, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA
3. All outputs and bidirectional pins

82A306 AC Characteristics

(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Typ.	Max.	Units
t601	OSC- delay from CX1'	4		22	ns
t602	OSC' delay from CX1-	5		26	ns
t603	OSC 12' delay from CX1'	9		35	ns
t604	OSC 12- delay from CX1-	9		37	ns
t605	BE<3:0> set-up time to MALE'		TBD		
t606	BE<3:0> hold time to MALE'		TBD		
t607	LBE<3:0> valid delay from MALE'	7		35	ns
t608	LBE<3:0> valid delay from BE<3:0> valid	3		25	ns
t609	LBE<3:0> LO delay from FBE-	5		25	ns
t610	LBE<3:0> de-asserted from FBE'	3		19	ns
t611	PPH<3:0> PPL<3:0> set-up time to PCHK'		TBD		
t612	PPH<3:0> PPL<3:0> hold time to PCHK'		TBD		
t613	MP<3:0> valid delay from corresponding PPH<3:0> and PPL<3:0>	2		21	ns
t614	MP<3:0> set-up time from CAS'		TBD		
t615	MP<3:0> hold time from CAS'		TBD		
t616	LPAR' delay from SCLK'	4		23	ns
t617	LPAE- delay from SCLK'	6		24	ns
t618	LPAR' delay from PEN'	1		13	ns
t619	LPAR- delay from PEN-	3		19	ns
t620	MEMW- (or MEMR-) delay from XMEMW- (or XMEMR-)	3		19	ns
t621	MEMW' (or MEMR') delay from XMEMW' (or XMEMR')	1		14	ns
t622	XMEMW- (or XMEMR-) delay from MEMW- (or MEMR-)	4		21	ns
t623	XMEMW' (or XMEMR') delay from MEMW' (or MEMR')	1		14	ns
t624	SMEMW- (or SMEMR-) delay from XMEMW- (or XMEMR-)	5		23	ns
t625	SMEMW (or SMEMR) LO to HI-Z transition delay from LMEGCS-	4		23	ns

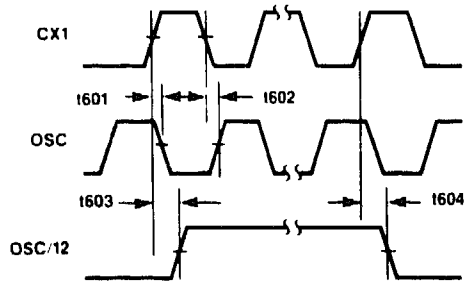
82A306 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

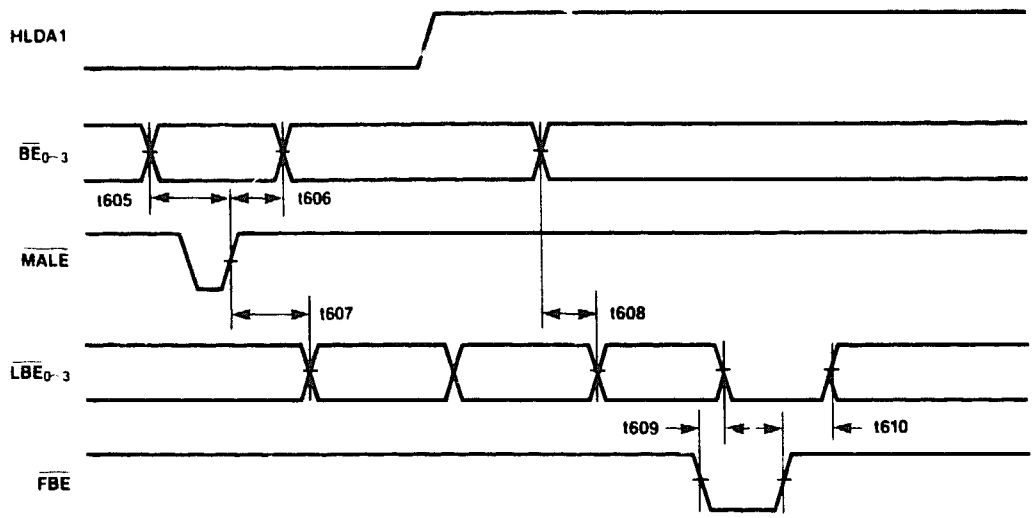
Sym	Description	Min.	Typ.	Max.	Units
t626	SMEMW (or SMEMR) HI-Z to LO transition delay from LMEGCS↑	6		28	ns
t627	SMEMW (or SMEMR) LO to HI-Z transition delay from REF↓	6		28	ns
t628	SMEMW (or SMEMR) HI-Z to LO transition delay from REF↑	8		32	ns
t629	SMEMW↑ (or SMEMR↑) delay from XMEMW↑ (or XMEMR↑)	3		19	ns
t630	SMEMW (or SMEMR) HI to HI-Z transition delay from LMEGCS↓	4		23	ns
t631	SMEMW (or SMEMR) HI-Z to HI transition delay from LMEGCS↑	6		28	ns
t632	SMEMW (or SMEMR) HI to HI-Z transition delay from REF↓	6		28	ns
t633	SMEMW (or SMEMR) HI-Z to HI transition delay from REF↑	8		32	ns
t634	SMEMW↓ (or SMEMR↓) delay from MEMW↓ (or MEMR↓)	5		23	ns
t635	SMEMW↑ (or SMEMR↑) delay from MEMW↑ (or MEMR↑)	3		19	ns
t636	IOW↓ (or IOR↓) delay from XIOW↓ (or XIOR↓)	3		18	ns
t637	IOW↑ (or IOR↑) delay from XIOW↑ (or XIOR↑)	1		14	ns
t638	XIOW↓ (or XIOR↓) delay from IOW↓ (or IOR↓)	4		21	ns
t639	XIOW↑ (or XIOR↑) delay from IOW↑ (or IOR↑)	1		14	ns
t640	SBHE↓ delay from XBHE↓	3		18	ns
t641	SBHE↑ delay from XBHE↑	1		14	ns
t642	XBHE↓ delay from SBHE↓	4		21	ns
t643	XBHE↑ delay from SBHE↑	1		14	ns
t644	RESETB↓ delay from RESET↓	3		20	ns
t645	RESETB↑ delay from RESET↑	1		14	ns
t646	RDRV↓ delay from RESET↓	3		18	ns

82A306 AC Characteristics (Continued)
(T_A = 0°C to 60°C, V_{CC} = 5V ± 5%)

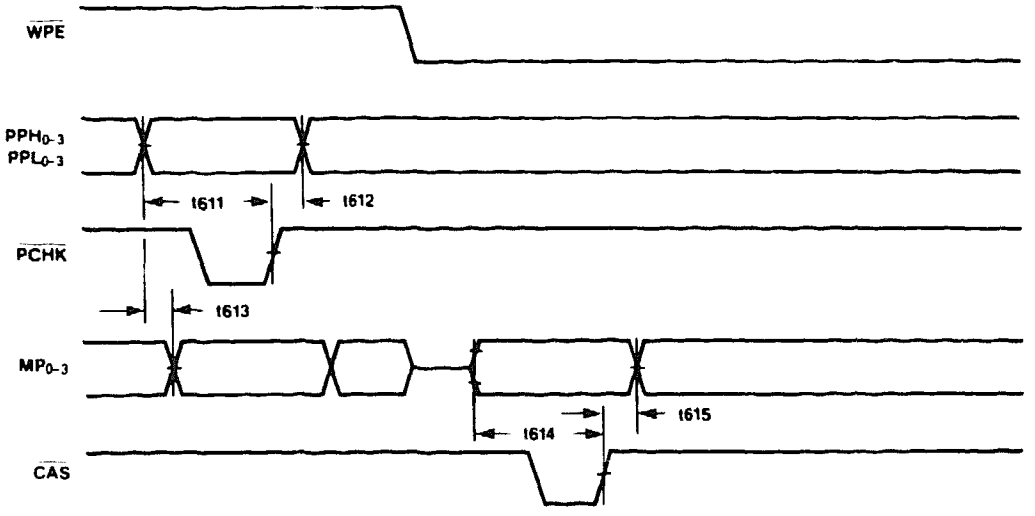
Sym	Description	Min.	Typ.	Max.	Units
t647	RDRV↑ delay from RESET↑	1		14	ns
t648	BALE↓ delay from ALT↓ SYSCLK↓ delay from ATSCLK↓ OUT1↓ delay from IN1↓	2		17	ns
t649	BALE↑ delay from ALT↑ SYSCLK↑ delay from ATSCLK↑ OUT1↑ delay from IN1↑	1		13	ns
t650	M/$\overline{IO}$, D/$\overline{C}$, A31 set-up time to MALE↑		TBD		
t651	M/$\overline{IO}$, D/$\overline{C}$, A31 hold time to MALE↑		TBD		
t652	$\overline{AF32}$ HI-Z to LO transition delay from MALE↑	7		32	ns
t653	$\overline{AF32}$ LO to HI-Z transition delay from MALE↑	6		29	ns
t654	$\overline{AF32}$ LO to HI-Z transition delay from RESET↑	6		28	ns
t655	$\overline{AF32}$ LO to HI-Z transition delay from HLDA1↑	6		29	ns

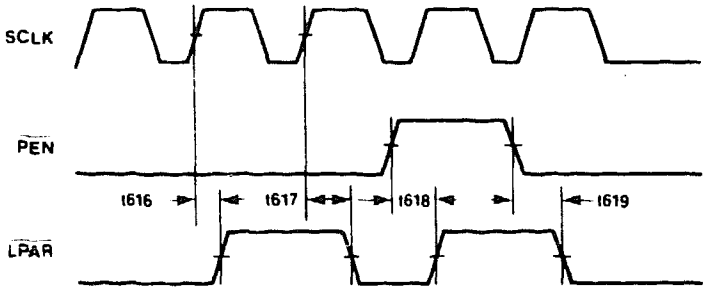
82A306 TIMING DIAGRAMS



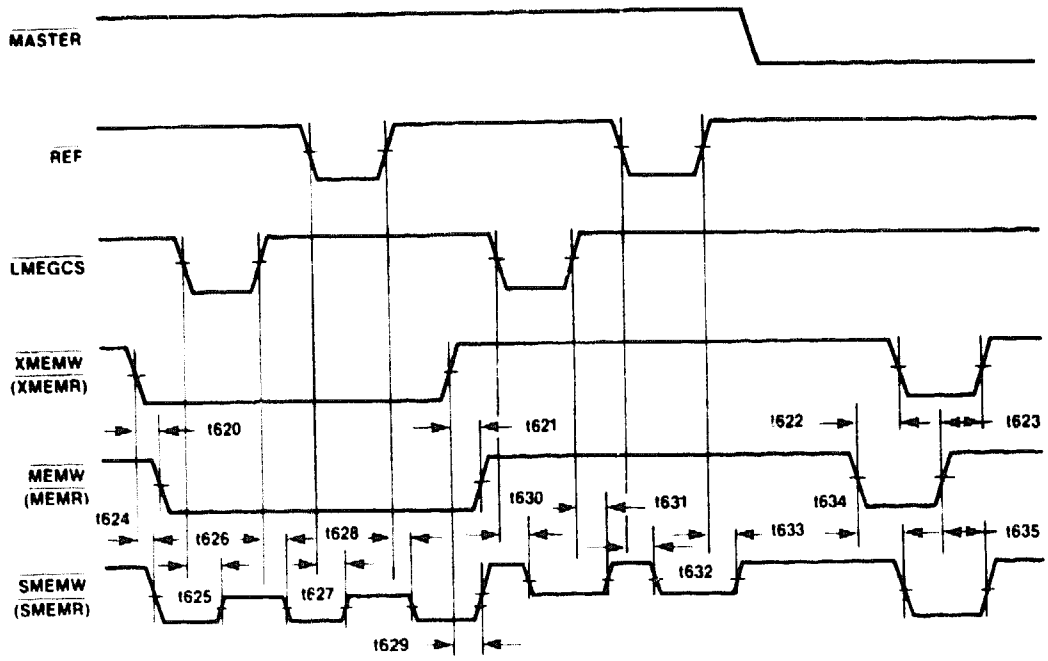


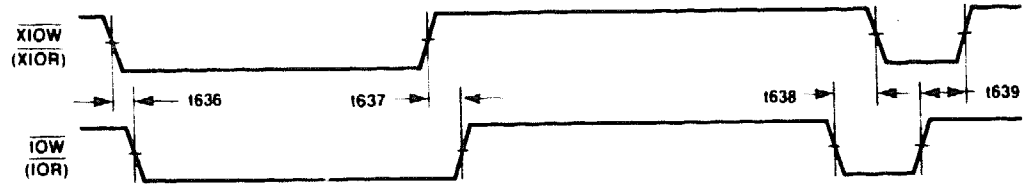
82A306 TIMING DIAGRAMS

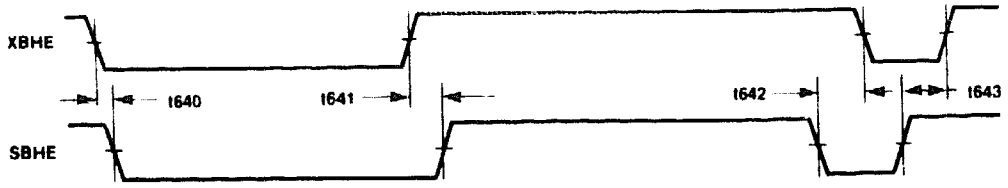




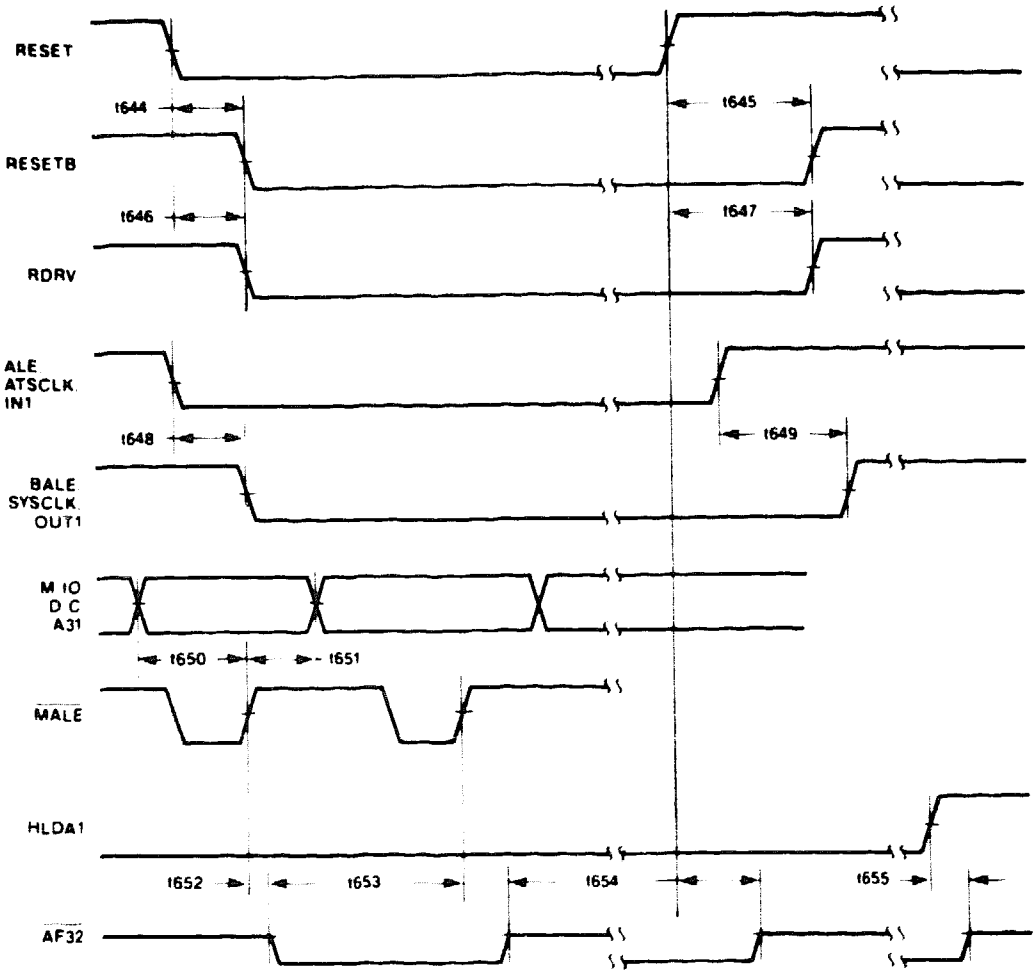
82A306 TIMING DIAGRAMS







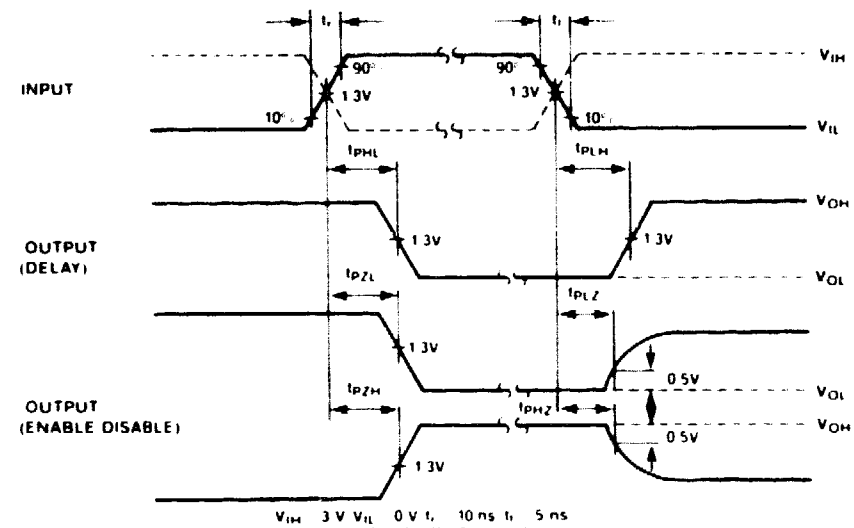
82A306 TIMING DIAGRAMS

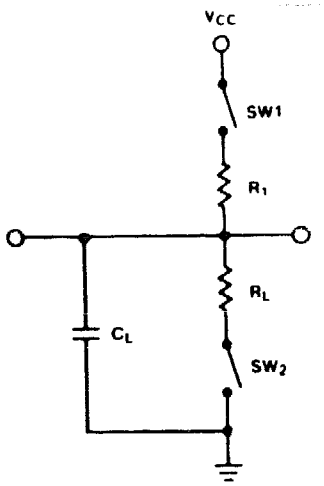


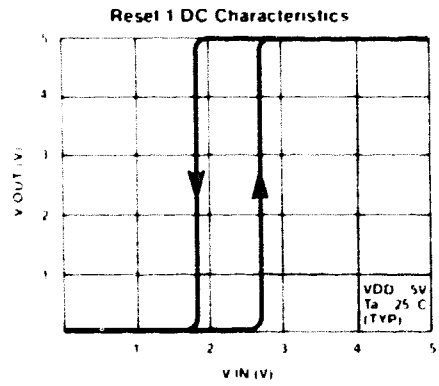
330

Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	–	1 0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0 5K	–	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0 5K	1 0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0 5K	1 0K	ON OFF	ON ON

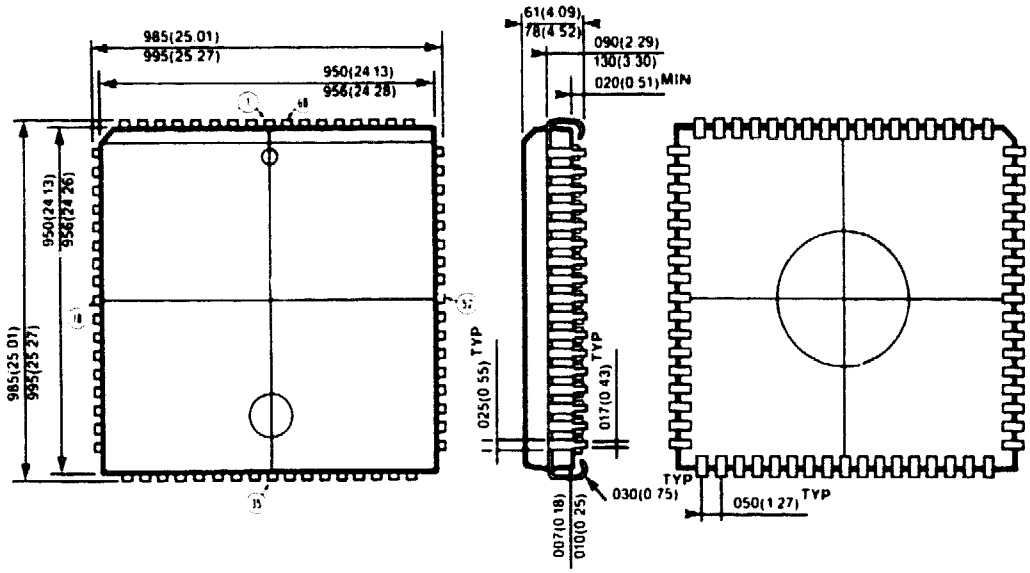






Load Circuit and AC Characteristics Measurement Waveform

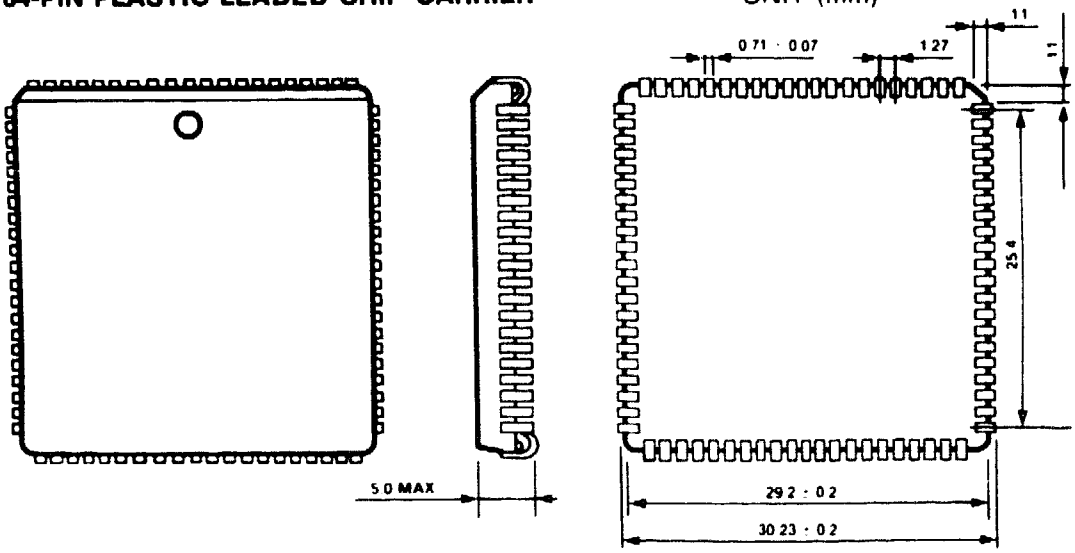
68-LEAD PLASTIC CHIP CARRIER



DIMENSIONS IN INCHES (MILLIMETERS) S = 3.6/1

84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)



82A303 Absolute Maximum Ratings

Order Number	Package Type Note 1	Remarks
P82C301	PLCC-84	C (Note 2)
P82C302	PLCC-84	C
P82A303	PLCC-68	C
P82A304	PLCC-68	C
P82A305	PLCC-68	C
P82A306	PLCC-68	C
CS8230	—	Standard CHIPSet (Note 3)

NOTES

1. PLCC = Plastic Leaded Chip Carrier 84 Pins
2. C = Commercial Range, 0° to 70° C, V_{DD} = 4 75 to 5 25 V
3. CS8230 consists of P82C301, P82C302, P82A303, P82A304, 2 of P82A305, P82A306

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8042/8742
UNIVERSAL PERIPHERAL INTERFACE
8-BIT MICROCOMPUTER

- **8042/8742: 12 MHz**
- **Pin, Software and Architecturally Compatible with 8041A/8741A**
- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **2048 x 8 ROM/EPROM, 128 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Interchangeable ROM and EPROM Versions**
- **Expandable I/O**
- **RAM Power-Down Capability**
- **Over 90 Instructions: 70% Single Byte**
- **Available in EXPRESS —Standard Temperature Range**

The Intel 8042/8742 is a general-purpose Universal Peripheral Interface that allows the designer to grow his own customized solution for peripheral device control. It contains a low-cost microcomputer with 2K of program memory, 128 bytes of data memory, 8-bit CPU, I/O ports, 8-bit timer/counter, and clock generator in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in the MCS-48™ MCS-51™, MCS-80™, MCS-85™, iAPX-88, iAPX-86 and other 8-, 16-bit systems.

The 8042/8742 is software, pin, and architecturally compatible with the 8041A, 8741A. The 8042/8742 doubles the on-chip memory space to allow for additional features and performance to be incorporated in upgraded 8041A/8741A designs. For new designs, the additional memory and performance of the 8042/8742 extends the UPI concept to more complex motor control tasks, 80-column printers and process control applications as examples.

To allow full user flexibility, the program memory is available as ROM in the 8042 version or as UV-erasable EPROM in the 8742 version. The 8742 and the 8042 are fully pin compatible for easy transition from prototype to production level designs.

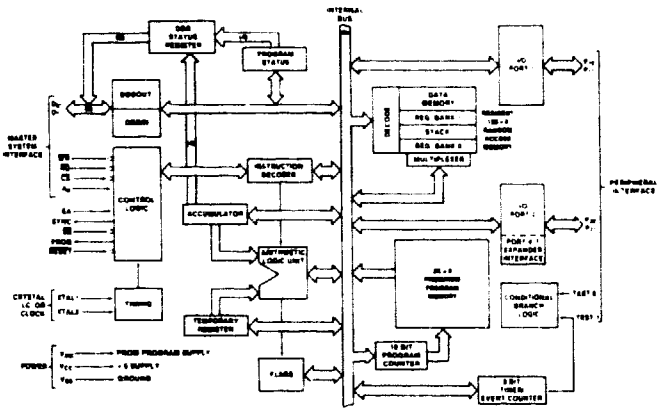


Figure 1. Block Diagram

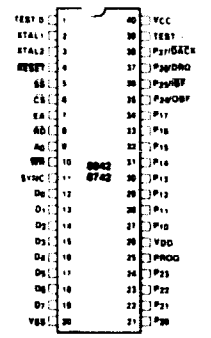


Figure 2. Pin Configuration

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FEBRUARY 1983
ORDER NUMBER: 210383-001

Table 1. Pin Description

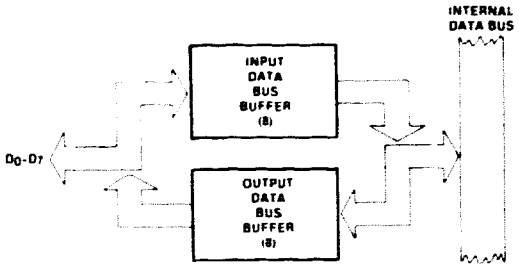
Symbol	Pin No.	Type	Name and Function
TEST 0, TEST 1	1 39	I	**Test Inputs:** Input pins which can be directly tested using conditional branch instructions. **Frequency Reference:** TEST 1 (T_1) also functions as the event timer input (under software control). TEST 0 (T_0) is used during PROM programming and verification in the 8742.
XTAL 1, XTAL 2	2 3	I	**Inputs:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
$\overline{RESET}$	4	I	**Reset:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification.
$\overline{SS}$	5	I	**Single Step:** Single step input used in conjunction with the SYNC output to step the program through each instruction. (8742 only)
$\overline{CS}$	6	I	**Chip Select:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	7	I	**External Access:** External access input which allows emulation, testing and PROM/ROM verification. This pin should be tied low if unused.
$\overline{RD}$	8	I	**Read:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A_0	9	I	**Command/Data Select:** Address input used by the master processor to indicate whether byte transfer is data ($A_0 = 0$, F1 is reset) or command ($A_0 = 1$, F1 is set).
$\overline{WR}$	10	I	**Write:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.

Symbol	Pin No.	Type	Name and Function
SYNC	11	O	**Output Clock:** Output signal which occurs once per UPI-42 instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D_0-D_7 (BUS)	12-19	I/O	**Data Bus:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-42 microcomputer to an 8-bit master system data bus.
P_{10}-P_{17}	27-34	I/O	**Port 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}-P_{27}	21-24 35-38	I/O	**Port 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}-P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P_{24}-P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full (OBF) interrupt, P_{25} as Input Buffer Full ($\overline{IBF}$) interrupt, P_{26} as DMA Request (DRQ), and P_{27} as DMA ACKnowledge ($\overline{DACK}$).
PROG	25	I/O	**Program:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
V_{CC}	40		**Power:** +5V main power supply pin.
V_{DD}	26		**Power:** +5V during normal operation. +21V during programming operation. Low power standby pin in ROM version.
V_{SS}	20		**Ground:** Circuit ground potential.

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UPI-42 FEATURES

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status



ST_4-ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4-7 of the accumulator are moved to bits 4-7 of the status register. Bits 0-3 of the status register are not affected.



3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

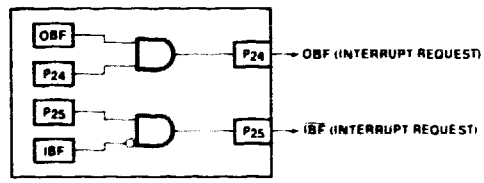


During the time that the host CPU is reading the status register, the 8042/8742 is prevented from updating this register or is 'locked out.'

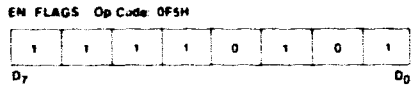
4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

   If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI-41A (in Output Data Bus Buffer).

   If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit). A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI-42 is ready for data.



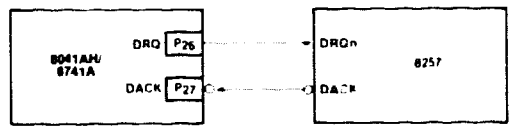
DATA BUS BUFFER INTERRUPT CAPABILITY



5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA ReQuest) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK, RD, DACK, WR, or execution of the "EN DMA" instruction.

   If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA HANDSHAKE CAPABILITY



6. The RESET input on the 8042/8742 includes a 2-stage synchronizer to support reliable reset operation for 12 MHz operation.

7. When EA is enabled on the 8042/8742, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB = P_{22}, LSB = P_{10}). On the 8042/8742 this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).

APPLICATIONS

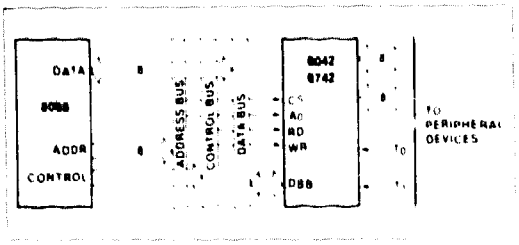


Figure 3. 8088-8042/8742 Interface

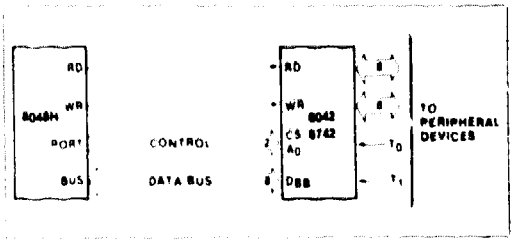


Figure 4. 8048H-8042/8742 Interface

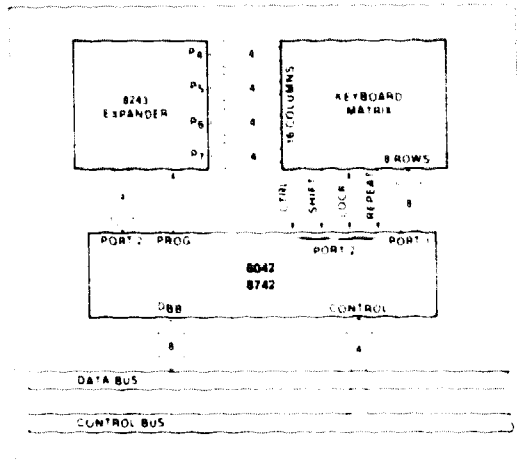


Figure 5. 8042/8742-8243 Keyboard Scanner

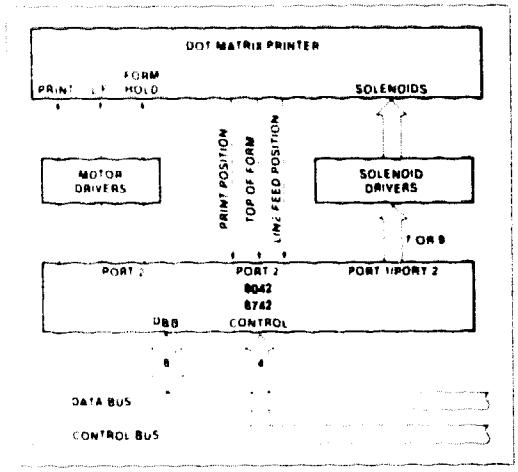


Figure 6. 8042/8742 80-Column Matrix Printer Interface

PROGRAMMING, VERIFYING, AND ERASING THE 8742 EPROM

Programming Verification

In brief, the programming process consists of activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions.

Pin	Function
XTAL 1	Clock Input
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-12	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING

An attempt to program a missocketed 8742 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. A_0 = 0V, $\overline{CS}$ = 5V, EA = 5V, $\overline{RESET}$ = 0V, TEST0 = 5V, V_{DD} = 5V, clock applied or internal oscillator operating, BUS floating, $\overline{PROG}$ = 5V
2. Insert 8742 in programming socket
3. TEST 0 = 0v (select program mode)
4. EA = 18V (active program mode)*
5. Address applied to BUS and P_{20-22}
6. $\overline{RESET}$ = 5v (latch address)
7. Data applied to BUS**
8. V_{DD} = 21V (programming power)**
9. $\overline{PROG}$ = V_{CC} followed by one 50 ms pulse to 18V**
10. V_{DD} = 5v
11. TEST 0 = 5v (verify mode)

12. Read and verify data on BUS
13. TEST 0 = 0v
14. $\overline{RESET}$ = 0v and repeat from step 5
15. Programmer should be at conditions of step 1 when 8742 is removed from socket

*When verifying ROM, EA = 12V
**Not used in verifying ROM procedure

8742 Erasure Characteristics

The erasure characteristics of the 8742 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8742 in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8742 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8742 window to prevent unintentional erasure.

The recommended erasure procedure for the 8742 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 w-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 µW/cm^2 power rating. The 8742 should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0° to +70°C, V_{CC} = V_{DD} = +5V ± 10%)

Symbol	Parameter	8042/8742 Min.	8042/8742 Max.	Units	Notes
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, RESET)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, RESET)	−0.5	0.6	V	
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, RESET)	2.0	V_{CC}	V	
V_{IH1}	Input High Voltage (XTAL1, RESET)	3.5	V_{CC}	V	
V_{IH2}	Input High Voltage (XTAL2)	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage (D_0–D_7)		0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage (P_{10}–P_{17}, P_{20}–P_{27}, Sync)		0.45	V	I_{OL} = 1.6 mA
V_{OL2}	Output Low Voltage (PROG)		0.45	V	I_{OL} = 1.0 mA
V_{OH}	Output High Voltage (D_0–D_7)	2.4		V	I_{OH} = −400 µA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			I_{OH} = −50 µA
I_{IL}	Input Leakage Current (T_0, T_1, RD, WR, CS, A_0, EA)		±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OFL}	Output Leakage Current (D_0–D_7, High Z State)		±10	µA	V_{SS} − 0.45 $\le V_{OUT} \le V_{CC}$
I_{LI}	Low Input Load Current (P_{10}–P_{17}, P_{20}–P_{27})		0.3	mA	V_{IL} = 0.8V
I_{LI1}	Low Input Load Current (RESET, SS)		0.2	mA	V_{IL} = 0.8V
I_{DD}	V_{DD} Supply Current		20	mA	Typical = 5 mA
I_{CC} + I_{DD}	Total Supply Current		135	mA	Typical = 60 mA
I_{IH}	Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27})		100	µA	$V_{IN} = V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

D.C. CHARACTERISTICS—PROGRAMMING (T_A = 25°C ± 5°C, V_{CC} = 5V ± 5%, V_{DD} = 21V ± 0.5V

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{DDH}	V_{DD} Program Voltage High Level	20.5	21.5	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	17.5	18.5	V	
V_{PL}	PROG Voltage Low Level	V_{CC}−0.5	V_{CC}	V	
V_{EAH}	EA Program or Verify Voltage High Level	17.5	18.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		1.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

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A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{SS} = 0V, V_{CC} = V_{DD} = +5V ± 10%)

DBB READ

Symbol	Parameter	8042		8742		Units
		Min.	Max.	Min.	Max.	
t_{AR}	CS, A_0 Setup to RD↓	0		0		ns
t_{RA}	CS, A_0 Hold After RD↑	0		0		ns
t_{RR}	RD Pulse Width	160		160		ns
t_{AD}	CS, A_0 to Data Out Delay		130		130	ns
t_{RD}	RD↓ to Data Out Delay		130		130	ns
t_{DF}	RD↑ to Data Float Delay		85		85	ns

DBB WRITE

Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{AW}	CS, A_0 Setup to WR↓	0		0		ns
t_{WA}	CS, A_0 Hold After WR↑	0		0		ns
t_{WW}	WR Pulse Width	160		160		ns
t_{DW}	Data Setup to WR↑	130		130		ns
t_{WD}	Data Hold After WR↑	0		0		ns

CLOCK

Symbol	Parameter	8042		8742		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	1.25	9.20	1.25	9.20	μs[1]
t_{CYC}	Clock Period	83.3	613	83.3	613	ns
t_{PWH}	Clock High Time	33		38		ns
t_{PWL}	Clock Low Time	33		38		ns
t_R	Clock Rise Time		10		10	ns
t_F	Clock Fall Time		10		10	ns

NOTE:
1. t_{CY} = 15/f(XTAL)

A.C. CHARACTERISTICS ($T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 21V \pm 0.5V$)

PROGRAMMING

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to RESET↑	$4t_{CY}$			
t_{WA}	Address Hold Time After RESET↑	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG↑	$4t_{CY}$			
t_{WD}	Data in Hold Time After PROG↓	$4t_{CY}$			
t_{PH}	RESET Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Setup Time to PROG↑	0	1.0	mS	
t_{VDDH}	V_{DD} Hold Time After PROG↑	0	1.0	mS	
t_{PW}	Program Pulse Width	50	60	mS	
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	Test 0 Hold Time After Program Mode	$4t_{CY}$			
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$		
t_{WW}	RESET Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	100	μs	
t_{CY}	CPU Operation Cycle Time	4.0		μs	
t_{RE}	RESET Setup Time Before EA↑	$4t_{CY}$			

NOTE:
If TEST 0 is high, t_{DO} can be triggered by RESET↑

A.C. CHARACTERISTICS DMA

Symbol	Parameter	8042		8742		Units
		Min.	Max.	Min.	Max.	
t_{ACC}	DACK to WR or RD	0		0		ns
t_{CAC}	RD or WR to DACK	0		0		ns
t_{ACD}	DACK to Data Valid		130		130	ns
t_{CRQ}	RD or WR to DRQ Cleared		110		130	ns[1]

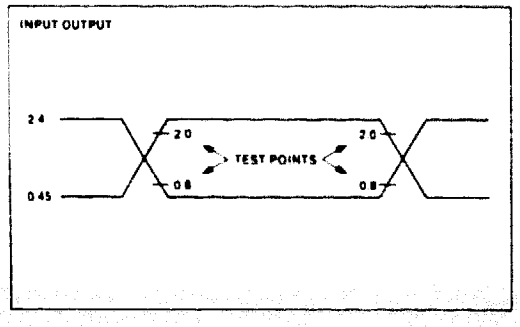
NOTE:
1. $C_L = 150$ pF

A.C. CHARACTERISTICS PORT 2 ($T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$)

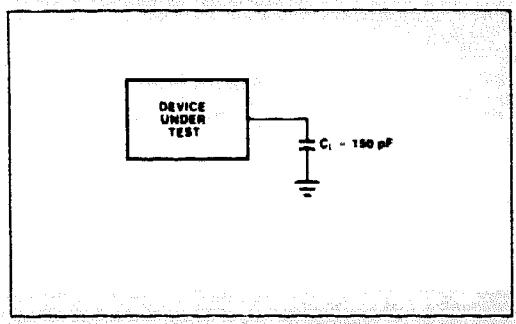
Symbol	Parameter	f(t_{CY})	8042/8742 [3]		Units
			Min.	Max.	
t_{CP}	Port Control Setup Before Falling Edge of PROG	$1/15\ t_{CY} - 28$	55		ns[1]
t_{PC}	Port Control Hold After Falling Edge of PROG	$1/10\ t_{CY}$	125		ns[2]
t_{PR}	PROG to Time P2 Input Must Be Valid	$(8/15\ t_{CY} - 16)$		650	ns[1]
t_{PF}	Input Data Hold Time		0	150	ns[2]
t_{DP}	Output Data Setup Time	$2/10\ T_{CY}$	250		ns[1]
t_{PD}	Output Data Hold Time	$1/10\ t_{CY} - 80$	45		ns[2]
t_{PP}	PROG Pulse Width	$6/10\ t_{CY}$	750		ns

NOTES:
1. $C_L = 80$ pF
2. $C_L = 20$ pF
3. $t_{CY} = 1.25\ \mu s$

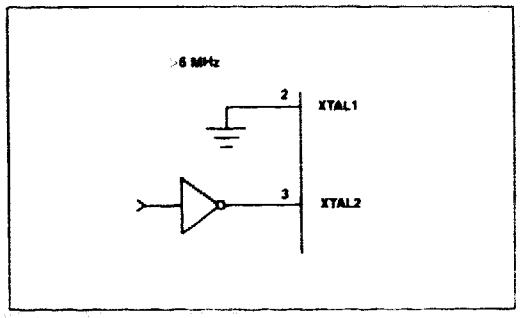
A.C. TESTING INPUT, OUTPUT WAVEFORM

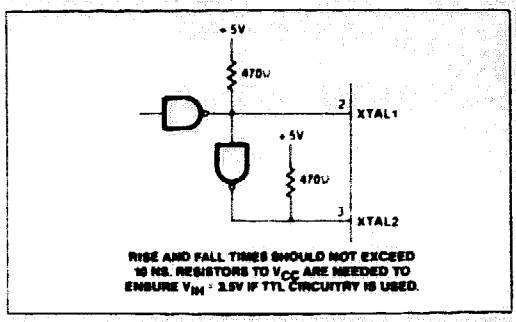


A.C. TESTING LOAD CIRCUIT



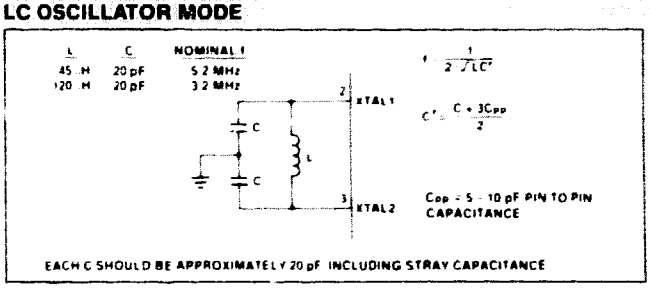
DRIVING FROM EXTERNAL SOURCE-TWO OPTIONS





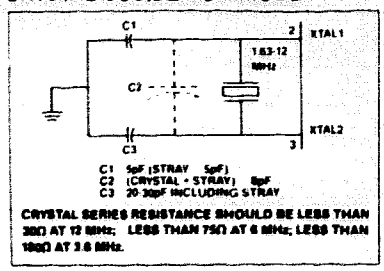
RISE AND FALL TIMES SHOULD NOT EXCEED 10 NS. RESISTORS TO V_{CC} ARE NEEDED TO ENSURE V_{IH} = 3.5V IF TTL CIRCUITRY IS USED.

LC OSCILLATOR MODE



EACH C SHOULD BE APPROXIMATELY 20 pF INCLUDING STRAY CAPACITANCE

CRYSTAL OSCILLATOR MODE

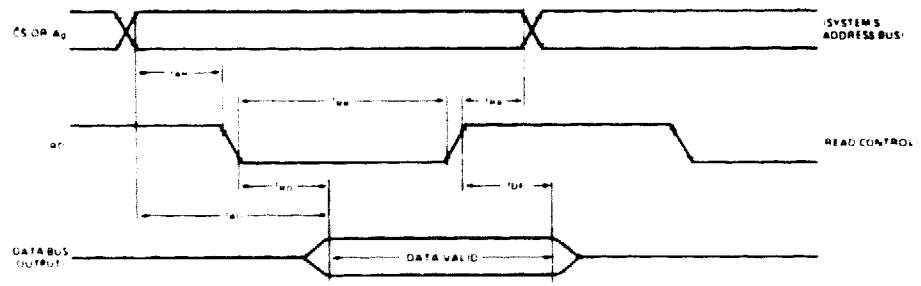


C1 5pF (STRAY 5pF)
C2 (CRYSTAL + STRAY) 8pF
C3 20-30pF INCLUDING STRAY

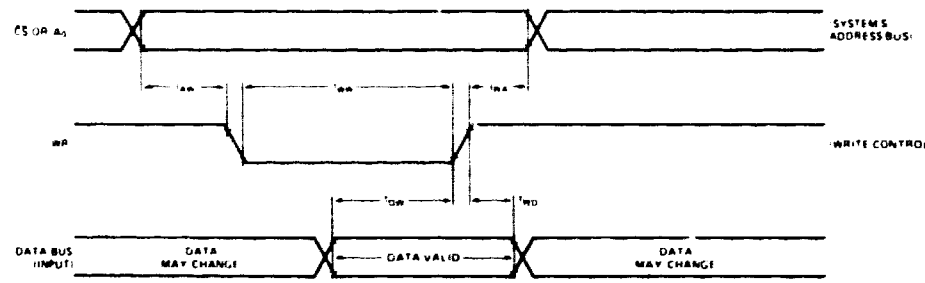
CRYSTAL SERIES RESISTANCE SHOULD BE LESS THAN 30Ω AT 12 MHz; LESS THAN 75Ω AT 6 MHz; LESS THAN 180Ω AT 3.6 MHz.

WAVEFORMS

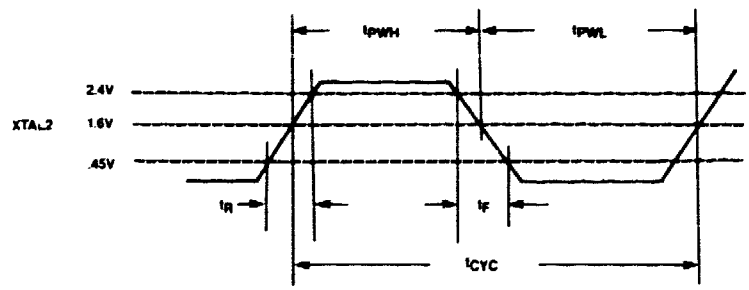
READ OPERATION—DATA BUS BUFFER REGISTER



WRITE OPERATION—DATA BUS BUFFER REGISTER



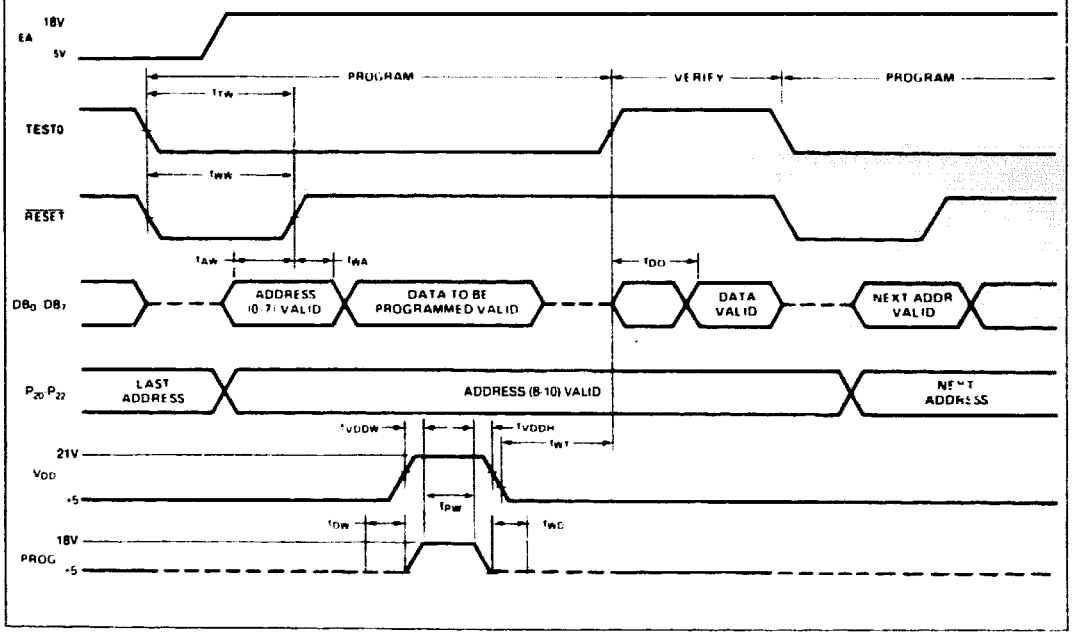
CLOCK TIMING



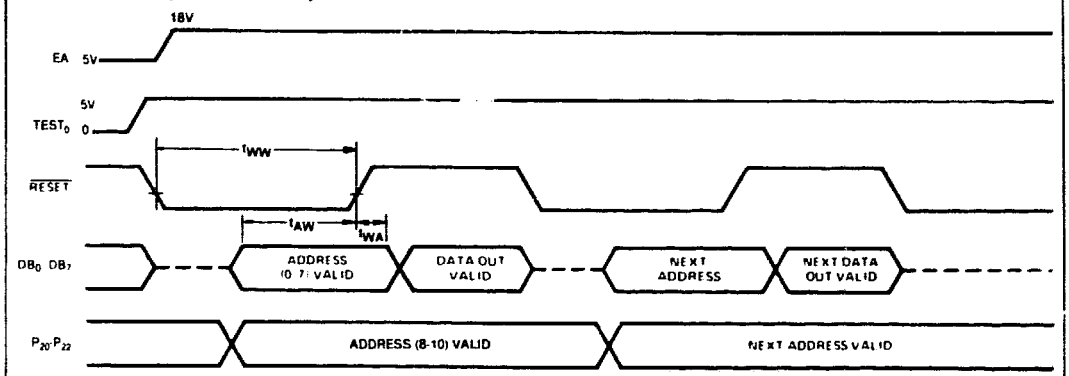
AFN-01832A

WAVEFORMS (Continued)

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



VERIFY MODE (ROM/EPROM)



NOTES:
1. PROG MUST FLOAT IF EA IS LOW OR IF $TEST_0$ = 5V FOR THE 8742. FOR THE 8042 PROG MUST ALWAYS FLOAT.
2. A_0 MUST BE HELD LOW (i.e., = 0V) DURING PROGRAM/VERIFY MODES.
3. TEST 0 MUST BE HELD HIGH.

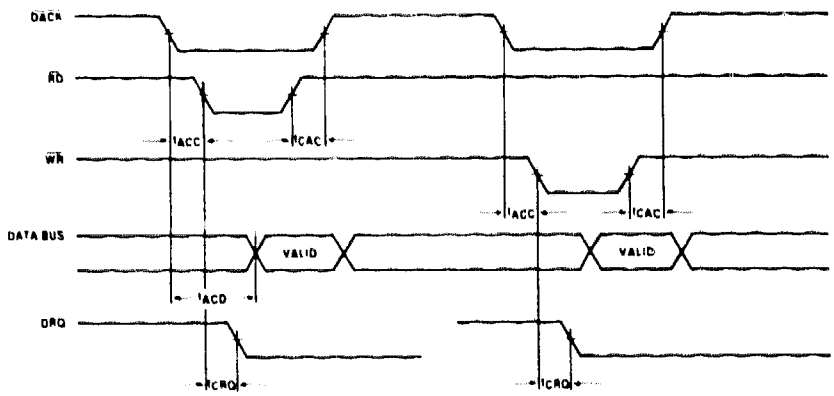
The 8742 EPROM can be programmed by the following Intel products:

1. Universal PROM Programmer (UPP 103) peripheral of the Intellec® Development System with a UPP-549 Personality Card.
2. iUP-200/iUP-201 PROM Programmer with the iUP-F87/44 Personality Module.

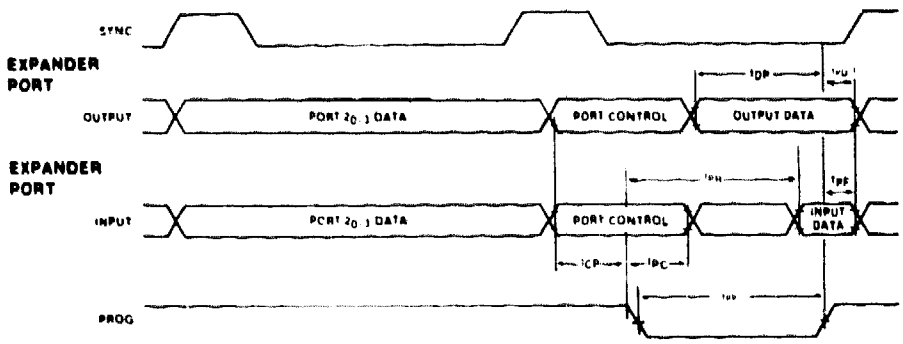
AFN-01852A

WAVEFORMS (Continued)

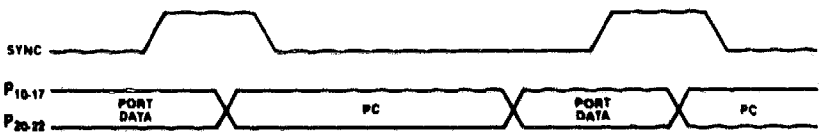
DMA



PORT 2



PORT TIMING DURING EA



ON THE RISING EDGE OF SYNC AND EA IS ENABLED. PORT DATA IS VALID AND CAN BE STROBED. ON THE TRAILING EDGE OF SYNC THE PROGRAM COUNTER CONTENTS ARE AVAILABLE

Table 2. UPI™ Instruction Set

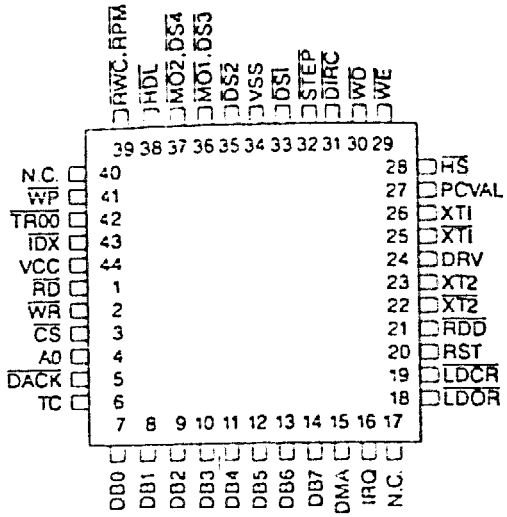
Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A, Rr	Add register to A	1	1
ADD A, @Rr	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rr	Add register to A with carry	1	1
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
ANL A, Rr	AND register to A	1	1
ANL A, @Rr	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	2
ORL A, Rr	OR register to A	1	1
ORL A, @Rr	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	2
XRL A, Rr	Exclusive OR register to A	1	1
XRL A, @Rr	Exclusive OR data memory to A	1	1
XRL A, #data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A, Pp	Input port toA	1	2
OUTL Pp, A	Output A to port	1	2
ANL Pp, #data	AND immediate to port	2	2
ORL Pp, #data	OR immediate to port	2	2
IN A, DBB	Input DBB to A, clear IBF	1	1
OUT DBB, A	Output A to DBB, set OBF	1	1
MOV STS, A	A_4-A_7 to Bits 4-7 of Status	1	1
MOVD A, Pp	Input Expander port to A	1	2
MOVD Pp, A	Output A to Expander port	1	2
ANLD Pp, A	AND A to Expander port	1	2
ORLD Pp, A	OR A to Expander port	1	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES			
MOV A, Rr	Move register to A	1	1
MOV A, @Rr	Move data memory to A	1	1
MOV A, #data	Move immediate TO A	2	2
MOV Rr, A	Move A to register	1	1
MOV @Rr, A	Move A to data memory	1	1
MOV Rr, #data	Move immediate to register	2	2
MOV @Rr, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, Rr	Exchange A and register	1	1
XCH A, @Rr	Exchange A and data memory	1	1
XCHD A, @Rr	Exchange digit of A and register	1	1
MOVP A, @A	Move to A from current page	1	2
MOVP3, A, @A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A, T	Read Timer/Counter	1	1
MOV T, A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/ Counter Interrupt	1	1
DIS TCNTI	Disable Timer/ Counter Interrupt	1	1
CONTROL			
EN DMA	Enable DMA Handshake Lines	1	1
EN I	Enable IBF Interrupt	1	1
DIS I	Disable IBF Interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

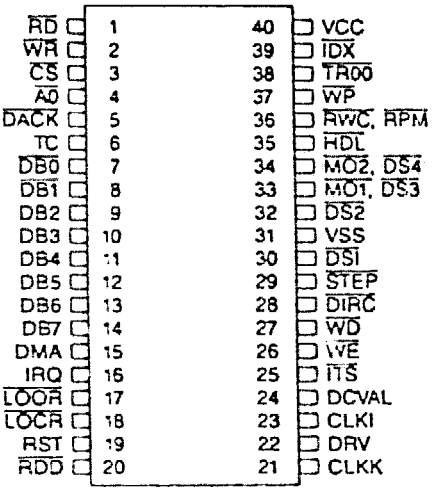
Table 2. UPI™ Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ Rr, addr	Decrement register and jump	2	2
JC addr	Jump on Carry=1	2	2
JNC addr	Jump on Carry=0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0=1	2	2
JNT0 addr	Jump on T0=0	2	2
JT1 addr	Jump on T1=1	2	2
JNT1 addr	Jump on T1=0	2	2
JF0 addr	Jump on F0 Flag=1	2	2
JF1 addr	Jump on F1 Flag=1	2	2
JTF addr	Jump on Timer Flag =1. Clear Flag	2	2
JNIBF addr	Jump on IBF Flag =0	2	2
JOBF addr	Jump on OBF Flag =1	2	2
JBb addr	Jump on Accumulator Bit	2	2

WD37C65 FLOPPY DISK SUBSYSTEM CONTROLLER



44 PIN PLCC



40 PIN DIP

FEATURES

- IBM PC/AT COMPATIBLE FORMAT (SINGLE AND DOUBLE DENSITY)
  - FLOPPY CONTROL AND OPERATIONS ON CHIP
  - IN PC/AT MODE, PROVIDES REQUIRED SIGNAL QUALIFICATION TO DMA CHANNEL
  - BIOS COMPATIBLE
  - DUAL SPEED SPINDLE DRIVE SUPPORT
- ADDRESS MARK DETECTION CIRCUITRY INTERNAL TO FLOPPY DISK CONTROLLER
- MULTISECTOR AND MULTITRACK TRANSFER CAPABILITY
- DIRECT FLOPPY DISK DRIVE INTERFACE WITH NO BUFFERS NEEDED
  - 48mA SINK OUTPUT DRIVERS
  - SCHMITT TRIGGER LINE RECEIVERS
- COMPATIBLE WITH PD8080/85, PD8086, AND PD780 (Z80 (TM)) MICROPROCESSORS
- ON CHIP CLOCK GENERATION
- TWO TTL CLOCK INPUTS FOR 40 PIN DIP
- TWO XTAL OSCILLATOR CIRCUITS FOR 44 PIN PLCC
- AUTOMATIC WRITE PRECOMPENSATION
- INNER TRACK VALUE OF 125 OR 187NS PIN SELECTABLE
- ENHANCED HOST INTERFACE
  - READ/WRITE ACCESSES COMPATIBLE REGISTERS WITH 8 OR 12 MHz 286 MICROPROCESSOR WITH 0 WAIT STATES
  - 20 LSTTL OUTPUT DRIVE CAPABILITY
  - INPUTS ARE TTL LEVEL SCHMITT TRIGGER (EXCEPT DATA BUS)
  - DMA TIMING CORRECTED
- USER PROGRAMMABLE TRACK STEPPING RATE AND HEAD LOAD/UNLOAD TIME
- DRIVES UP TO FOUR FLOPPY OR MICRO FLOPPYDISK (TM) DRIVES
- DATA TRANSFER IN DMA OR NON-DMA MODE
- PARALLEL SEEK OPERATIONS
  - ON UP TO FOUR DRIVES
- HIGH PERFORMANCE, CLASSICAL 2ND ORDER, TYPE 2, PHASE LOCKED LOOP DIGITAL DATA SEPARATOR
- 125, 250, 300, 500 KBITS/SEC DATA RATES
- CMOS LOW POWER 125mW
- +5VDC POWER SUPPLY

November, 1986

DESCRIPTION

The WD37C65 *Floppy* Disk Subsystem Controller is an LSI device that provides all the needed functionality between the Host processor peripheral bus and the cable connector to the floppy disk drive. This 'superchip' intergrates: Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive Interface Drivers and Receivers.

On the disk drive interface, the WD37C65 includes Data Separation that has been designed to address high performance error rates on floppy disk drives, and contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write Precompensation is included, in addition to the usual Formatting, Encoding/Decoding, Stepper Motor Control, and Status Sensing Functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with the drivers meeting the 48 mA ANSI Specification.

The Host interface has been improved for speed operation supporting 8 or 12 MHz, 286 microprocessor bus without the use of wait states, the inputs are Schmitt Triggers (except the data bus). Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC/AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, Data Rate Selection, Drive Selection, and Stepper Motor Control have been output ports of the Host processor architecture. In the PC/AT these functions are latched into registers addressed within the I/O mapping of the system. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65.

All Clock Generation: SCLK – Sampling Clock, WCLK – Write Clock, and MCLK – Master Clock, are included in the WD37C65. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillators in the WD37C65; one at 16 MHz that handles all standard data rates (500, 250, and 125 Kb/Sec). The other oscillator is at 9.6 MHz to support the 300 Kb/Sec data rate used in PC/AT designs. Some AT compatibles use two-speed disk drives. If two-speed disk drives are used, the drive type input pin is grounded and only the 16 MHz clock is required. A $\overline{RPM}$ output signal will become active when a spindle speed rate of 300 RPM is desired.

PIN DESCRIPTIONS

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1/1	$\overline{RD}$	$\overline{READ}$	I	Control signal for transfer of data or status onto the data bus by the WD37C65.
2/2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data from the bus into the WD37C65 Buffer Register.
3/3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the Host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (=1) or status (=0) information. (A0 – logic 0 during $\overline{WR}$ is illegal).
5/5	$\overline{DACK}$	$\overline{DMA\ ACKNOWLEDGE}$	I	Used by the DMA controller to transfer data from the WD37C65 onto the bus. Logical equivalent to $\overline{CS}$ and A0-1. In Special or PC/AT Mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL COUNT	I	This signal indicates to WD37C65 that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In PC/AT or Special Mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in PC/AT Mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA Host operation. Programmed I/O in PC/AT Mode will cause an abnormal termination error at the completion of a command.
7-14 7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).

PIN DESCRIPTIONS (cont.)

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or PC/AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base Mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or PC/AT Mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.
17				Not connected in the 44 pin PLCC.
17/18	$\overline{LDOR}$	$\overline{LOAD\ OPERATIONS\ REGISTER}$	I	Address decode which enables the loading of the Operations Register. Internally gated with $\overline{WR}$ creates the strobe which latches the data bus into the Operations Register.
18/19	$\overline{LDCR}$	$\overline{LOAD\ CONTROL\ REGISTER}$	I	Address decode which enables loading of the Control Register. Internally gated with $\overline{WR}$ creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base Mode, not PC/AT or Special Mode.
20/21	$\overline{RDD}$	$\overline{READ\ DISK\ DATA}$	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6MHz for 300 Kb/s, and can only be selected from the Control Register.
/22	$\overline{XT2}$	$\overline{XTAL2}$	O	XTAL oscillator drive output.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a two-speed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	$\overline{XT1}$	$\overline{XTAL1}$	O	XTAL oscillator drive output.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.
24/27	PCVAL	PRECOMPEN-SATION VALUE	I	PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 – 125ns, Logic 0 – 187ns.
25/28	$\overline{HS}$	$\overline{HEAD\ SELECT}$	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 – side 0. Logic 0 – side 1.
26/29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.

PIN DESCRIPTIONS (cont.)

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
27/30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O	This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
28/31	$\overline{DIRC}$	$\overline{DIRECTION}$	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion. Logic 0 = inward motion.
29/32	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	This HCD output, when active low is $\overline{DRIVE\ SELECT\ 1}$, in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. In Base, or Special Mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND		Ground.
32/35	$\overline{DS2}$	$\overline{DRIVE\ SELECT\ 2}$	O	This HCD output when active low is $\overline{DRIVE\ SELECT\ 2}$, in PC/AT Mode, enabling the interface in this disk drive. This signal comes from the Operations Register. In Base or the Special Mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$	O	This HCD output when active low is MOTOR ON enable for disk drive #1, in PC/AT Mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	O	This HCD output when active low is MOTOR ON enable for disk drive #2, in PC/AT mode. This signal comes from the Operations Register. In the Base or Special Mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HCD output when active low causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output when active low causes a $\overline{REDUCED\ WRITE\ CURRENT}$ when bit density is increased toward the inner tracks, becoming active when tracks > 28 are accessed. This condition is valid for Base or Special Mode, and is indicative of when write precompensation is necessary. In the PC/AT mode, this signal can be used on two-speed disk drives to select 300 RPM spindle rate, active low, when 250 MFM or 125 FM KB/s is selected.
40				Not connected in the 44 pin PLCC.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low, when a diskette is $\overline{WRITE\ PROTECTED}$.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$		This ST input senses status from disk drive indicating active low, when the head is positioned over the outermost track, $\overline{TRACK\ 00}$.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive indicating active low, when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC		Input power supply.

ARCHITECTURE

The WD37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the Host processor peripheral bus and the cable connector to the floppy disk drive. This "superchip" integrates: Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive Interface Drivers and Receivers.

Figure 1 illustrates a block diagram of the WD37C65 Floppy Disk Subsystem Controller.

Figure 2 illustrates a typical WD37C65 system.

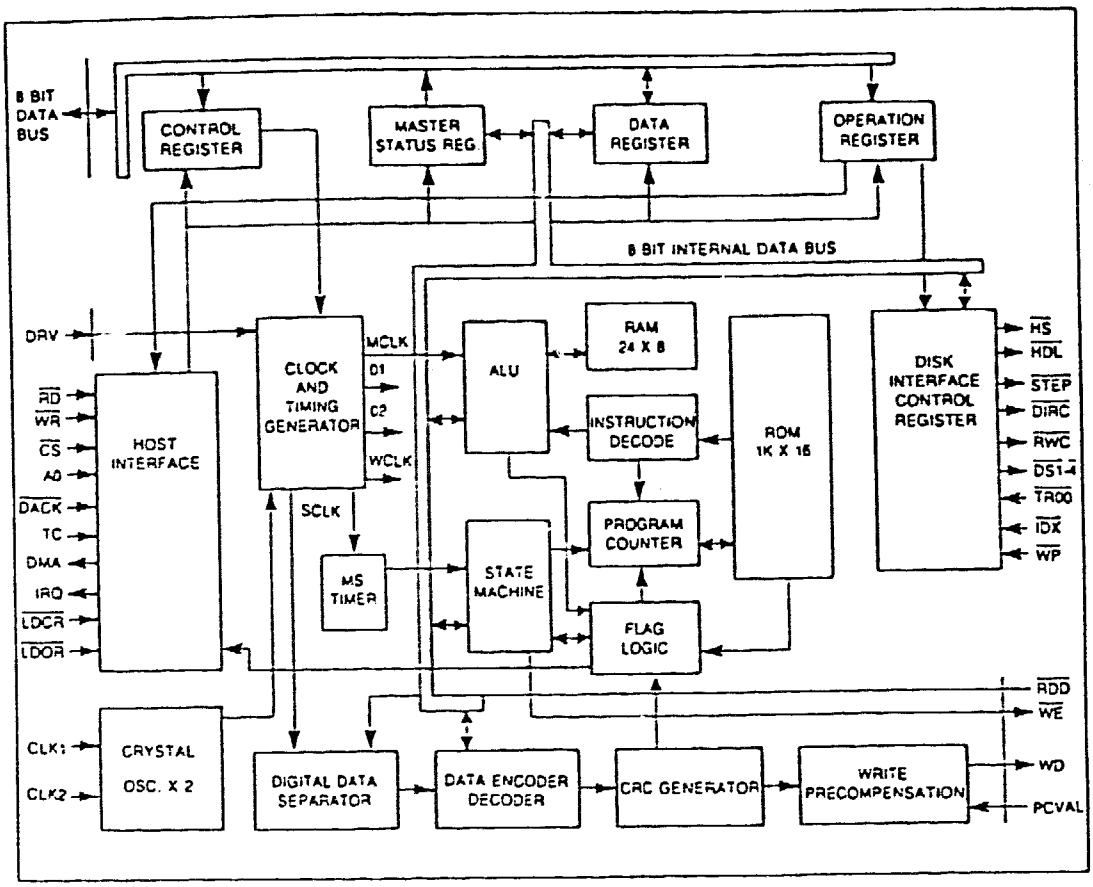


FIGURE 1. WD37C65 BLOCK DIAGRAM

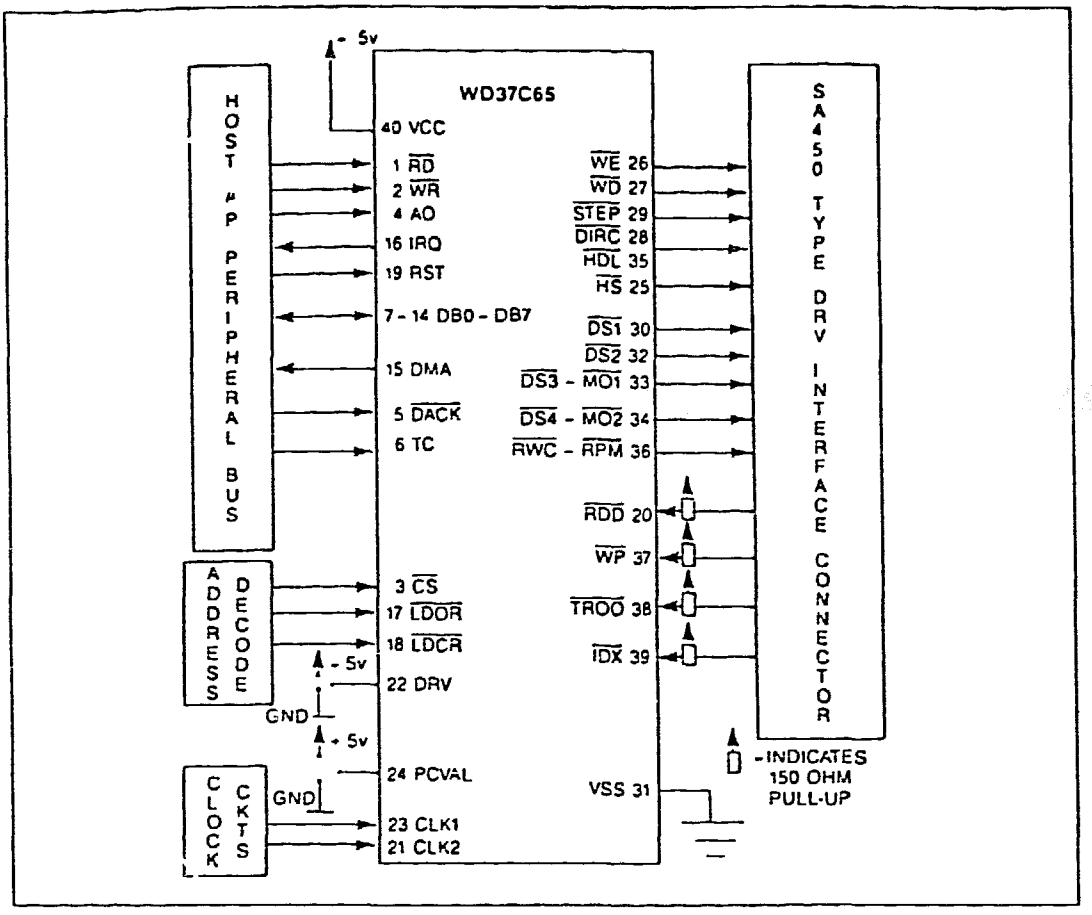


FIGURE 2. TYPICAL WD37C65 SYSTEM

HOST INTERFACE

The Host Interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or PC/AT Modes, IRQ and DMA request are tri-stated and qualified by DMA enable, internally provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs, except the data bus, are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU should wait for 12μs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65. Many of the commands require multiple bytes, as result the Main Status Register must be read prior to each byte transfer to the WD37C65. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65 is required only in the Command and Result phases, and not during the Execution phase.

During the Execution phase, the Main Status Register need not be read. If the WD37C65 is in the non-DMA Mode, then the receipt of each data byte (WD37C65 is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal ($\overline{RD}$=0) or Write signal ($\overline{WR}$=0) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM Mode and 27μs for the FM Mode), then it may poll the Main Status Register and bit D7 (ROM) functions as the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA Mode it is necessary to examine the Main Status Register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65 is in the DMA Mode, no interrupt signals are generated during the Execution phase. The WD37C65 generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both $\overline{DACK}$ - 0 (DMA Acknowledge) and an $\overline{RD}$ - 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ - 0), then the DMA Request is cleared (DMA - 0). If a Write Command has been issued then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ - 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is automatically cleared (IRQ - 0).

It should be noted that in PC/AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65 will successfully complete commands, but will always give abnormal termination error status since $\overline{TC}$ is qualified by an inactive $\overline{DACK}$.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed $\overline{I/O}$ operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA Mode is chosen, the $\overline{DACK}$ signal should be pulled up to Vcc. It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data Command. The WD37C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65 contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65 to form the Command phase, and are read out of the WD37C65 in the Result phase, must occur in the order shown in the Command Table. The Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65 is ready for a new command.

CONTROL REGISTER

The Control Register provides support logic that latches the two LSBs of the data bus upon receiving $\overline{LDCR}$ and $\overline{WR}$. These bits are used to select the desired data rate which in turn controls the internal clock generation. Clock switchover is internally "deglitched", allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64X the desired MFM data rate, up to a maximum frequency of 16 MHz. This implies a maximum data rate of 250 Kb/s unless the Control Register is used. Switching this clock must be "glitchless" or the device will need to be reset. Table 1 presents the Control Register.

TABLE 1. CONTROL REGISTER

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (IN PC/AT MODE)
0	0	X	500 K	MFM	1
0	0	X	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM	0
1	0	X	250 K	MFM, RST Default	1
1	0	X	125 K	FM, RST Default	1
1	1	X	125 K	FM	0

MASTER STATUS REGISTER

The Master Status Register is an 8-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65. The DIO and ROM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and ROM getting set is 12μs if 500 Kb/s MFM data rate is selected. (If 250 Kb/s MFM is selected, the delay is 24μs.) For this reason everytime the Master Status Register is read the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB4 (FDC busy) goes low is 12μs.

The bits in the Master Status Register are listed in Table 2.

TABLE 2. MASTER STATUS REGISTER BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE Commands.
DB4	FDC BUSY	CB	A READ or WRITE Command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution Phase in non-DMA Mode. When DB5 goes low Execution Phase has ended and Results Phase has started. It operates only during non-DMA Mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The bits in Status Register 0 are listed in Table 3.

TABLE 3. STATUS REGISTER 0 BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
			D7=0 and D6=0. Normal Termination of command was completed and properly executed. D7=0 and D6=1. Abnormal Termination of command, (AT).
D7	INTERRUPT CODE	IC	Execution of command was started but was not successfully completed.
D6			D7=1 and D6=0. Invalid Command issue, (IC). Command which was issued was never started. D7=1 and D6=1. Abnormal Termination because during command execution the ready signal from FDD changed state.
D5	SEEK END	SE	When the FDC completes the SEEK Command this flag is set to 1 (high).
D4	EQUIPMENT CHECK	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 255 step pulses (Recalibrate Command) then this flag is set.
D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

The bits in Status Register 1 are listed in Table 4.

TABLE 4. STATUS REGISTER 1 BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6			Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the Host system during data transfers within a certain time interval, this flag is set.
D3			Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN Command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID Command if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK Command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK Command, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

The bits in Status Register 2 are listed in Table 5.

TABLE 5. STATUS REGISTER 2 BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7			Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and the contents of ***C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN Command if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN Command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

The bits in Status Register 3 are listed in Table 6.

TABLE 6. STATUS REGISTER 3 BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
D7		-	Not used. Will always be logic 0.
D6	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D3	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

* CRC - Cyclic Redundancy Check
** IDR - Internal Data Register
*** C - Cylinder

DATA REGISTER

The 8-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals $\overline{RD}$, $\overline{WR}$, and A0 are shown in Table 7.

TABLE 7. MASTER STATUS AND DATA REGISTERS RELATIONSHIP

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving $\overline{LDOR}$ and $\overline{WR}$. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8 represents the Operations Register.

TABLE 8. OPERATIONS REGISTER

ORO	DSEL	; Drive Select, if low and MOEN1 = 1, then $\overline{DS1}$ is active. If high and MOEN2 = 1, then $\overline{DS2}$ is active, but only in the PC/AT Mode.
OR1	(X)	; Has no defined function. A spare.
OR2	$\overline{SRST}$	; Soft reset, active low.
OR3	DMAEN	; DMA enable, active in Special and PC/AT Mode. Qualifies DMA and IRQ outputs and $\overline{DACK}$ input.
OR4	MOEN1	; Motor On enable, inverted output $\overline{MO1}$ is active only in PC/AT Mode.
OR5	MOEN2	; Motor On enable, inverted output $\overline{MO2}$ is active only in PC/AT Mode.
OR6	(X)	; Has no defined function. A spare.
OR7	(X)	; Mode Select. During a soft reset condition, may be used to select between Special Mode and PC/AT Mode.

BASE, SPECIAL, AND PC/AT MODES

Base, Special, and PC/AT Modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

Base Mode

After a hardware reset, RST active, the WD37C65 will be held in soft reset, $\overline{SRST}$ active, with the normally driven signals, DMA request and IRQ request outputs tri-stated. Base Mode may be initiated at this time by a chip access by the Host. Although this may be any read or write, it is strongly recommended that the Base Mode user's first chip access be a read of the Master Status Register. Once Base Mode is entered the soft reset is released, and IRQ and DMA are driven. Base Mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, $\overline{DS1}$ to $\overline{DS4}$, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin $\overline{RWC}$ represents Reduce Write Current and is indicative of when write precompensation is necessary.

Special Mode

Special Mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset $\overline{SRST}$. To enter Special Mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting Mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing $\overline{SRST}$ to be active. Then a read of the Control Register address, $\overline{LDCR}$ and $\overline{RD}$, will set the device into Special Mode. The $\overline{DS1}$ through $\overline{DS4}$ is again offered in this mode, as is $\overline{RWC}$.

PC/AT Mode

For PC/AT compatibility, users will write to the Operations Register, $\overline{LDOR}$ and $\overline{WR}$, this action performed after a hardware reset, or in the Base Mode, initiates PC/AT Mode. PC/AT Mode can also be entered from Special Mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing $\overline{SRST}$ to be active. Then a read of the Control Register address sets the device into PC/AT Mode. The $\overline{DS}$ outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and $\overline{SRST}$ are supported and compatible with the current BIOS. $\overline{RWC}$ pin function is now $\overline{RPM}$ so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute, to 300 revolutions per minute when active low, or used to reduce write current when a slower data rate is selected for a given drive.

POLLING ROUTINE

After any reset the WD37C65, a hard RST or soft $\overline{SRST}$, US0 and US1, will automatically go into a Polling Routine. In between commands (and between step pulses in the SEEK Command) the WD37C65 polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special or PC/AT Modes, if DMAEN is not valid prior to 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65 occurs continuously between commands. Each drive is polled every 1.024ms except during the READ/WRITE Commands. For mini-floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3.

Figure 2 illustrates the Drive Select Polling Timing.

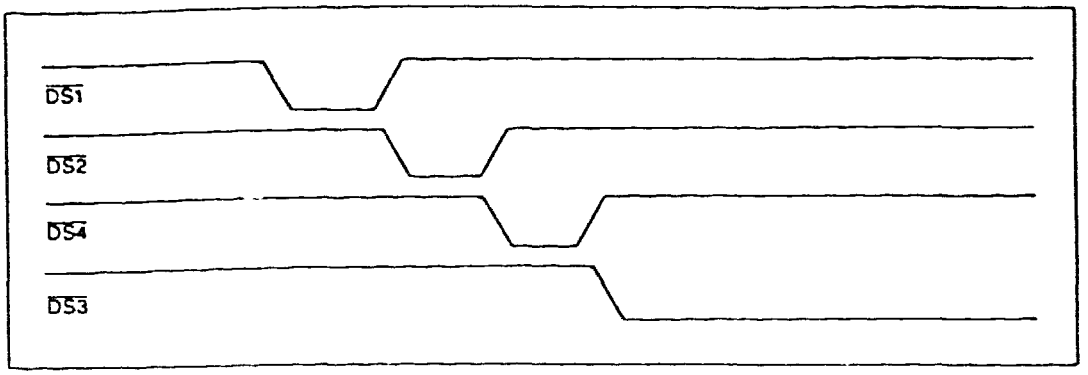


FIGURE 2. DRIVE SELECT POLLING TIMING

DEVICE RESETS

The WD37C65 supports both hardware reset (RST) pin (19), and a software reset ($\overline{SRST}$), through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base Mode, and default selects 250K MFM (or 125K FM, code dependent) as the data rate (16 MHz input clock). $\overline{SRST}$ will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. Both RST and $\overline{SRST}$, when active, will disable the high current driver outputs to the disk drive.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide a superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the WD37C65 system. Figure 3 illustrates the WD92C32 simplified block diagram.

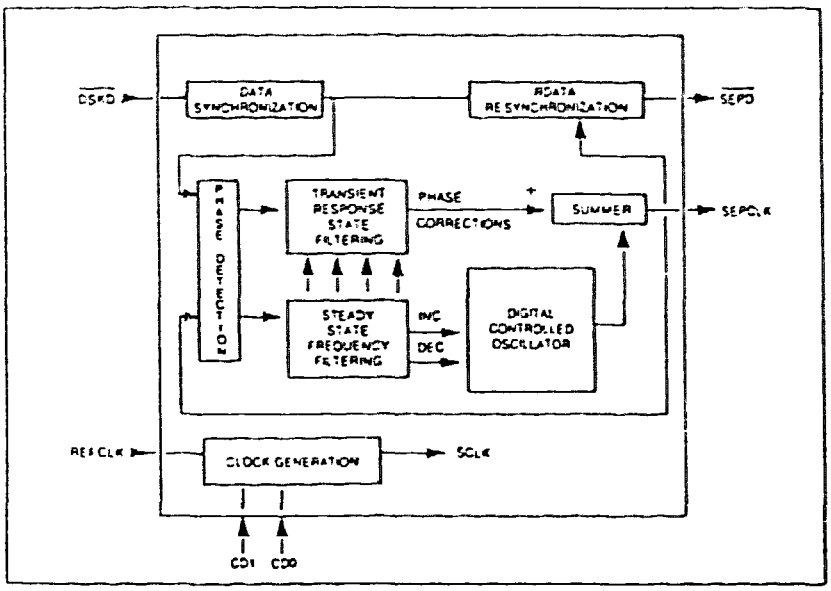


FIGURE 3. WD92C32 SIMPLIFIED BLOCK DIAGRAM

WRITE PRECOMPENSATION

The WD37C65 maintains the standard first level algorithm to determine when Write Precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz clock, if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., ¼ of the bit cell period, and equal to ½ the WCLK period.

When PCVAL pin (24) = 1 all data will be precompensated by ± 125ns regardless of track number and data rate, however, this is only for MFM encoding. There is no Write Precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187ns precompensation will be generated. For frequencies other then 16 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard data rate using CLK2 is chosen, the MFM precompensation will always be 2 clock cycles. For 9.6 MHz this is ± 208ns. In this case, the PCVAL function is disabled.

CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32X the selected data rate.

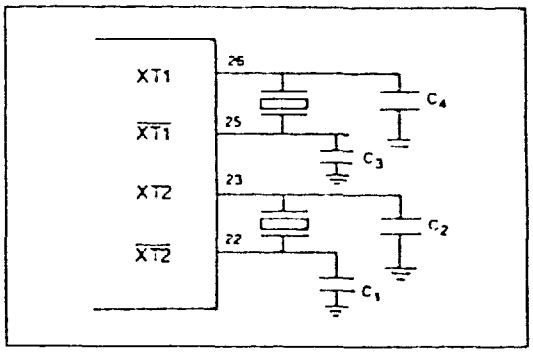
WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency 2X the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{\text{MCLK}}$ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to 8X the selected MFM data rate or 16X the FM data rate. Table 9 presents the Clock Data Rate.

TABLE 9. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
500 Kb/S	MFM	16.0 MHz	4.0 MHz	1.0 MHz
250 Kb/S	FM	8.0 MHz	4.0 MHz	500 KHz
250 Kb/S	MFM	8.0 MHz	2.0 MHz	500 KHz
125 Kb/S	FM	4.0 MHz	2.0 MHz	250 KHz
300 Kb/S	MFM	9.6 MHz	2.4 MHz	600 KHz

Figure 4 illustrates the XTAL oscillator circuits for the 44 pin PLCC configuration.



SERIES RESONANT XT 2		SERIES RESONANT XT 1	
9.6 MHz	± 100 ppm	16.0 MHz	± 100 ppm
R series	= 30 ohm max	R series	= 30 ohm max
C shunt	= 10 pf max	C shunt	= 10 pf max
C1	= 68 pf 5% mica	C3	= 47 pf 5% mica
C2	= 56 pf 5% mica	C4	= 15 pf 5% mica

FIGURE 4. XTAL OSCILLATOR CIRCUITS FOR THE 44 PIN PLCC

COMMANDS

The WD37C65 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command Phase, Execution Phase, and the Result Phase.

Command Phase – The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

Execution Phase – The FDC performs the operation it was instructed to do.

Result Phase – After completion of the operation, status and other housekeeping information are made available to the processor.

Table 10 lists the 15 WD37C65 commands.

TABLE 10. WD37C65 COMMANDS

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK

Tables 11 through 25 are presented to show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

TABLE 11. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	*Command Codes*
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 12. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 13. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 14. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	.	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 15. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 16. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information read during Execution Phase from floppy disk.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 17. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			N				→	Bytes/Sector
	W	←			SC				→	Sectors/Track
	W	←			GPL				→	Gap 3
	W	←			D				→	Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	In this case, the ID information has no meaning.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 18. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 19. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← STP →								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 20. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← STP →								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 21. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 22. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	←			ST0				→	Status information about the FDC at the
	R	←			PCN				→	end of seek operation.

TABLE 23. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	←	SRT	→		←		HUT	→	
	W	←		HLT					ND	

TABLE 24. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R	←			ST3				→	Status information about the FDC.

TABLE 25. SEEK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			NCN				→	
EXECUTION										Head is positioned over proper cylinder on the diskette.

Table 26 defines, in alphabetical order, the symbols used in Command Tables 11 through 25.

TABLE 26. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.

TABLE 26. COMMAND SYMBOL DESCRIPTIONS (cont.)

SYMBOL	NAME	DESCRIPTION
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1, as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of Sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0 - 3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0 - 3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C (32°F) to 70°C (158°F)
Storage Temperature ..... -55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground ..... -0.3V to VCC +0.3V
Supply Voltage with respect to ground 7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	+5VDC Power Supply	4.5	5.5	V
VIL	Input Low Voltage - Data Bus & XTOSC		0.8	V
VIH	Input High Volt - Data Bus & XTOSC	2.0		V
VILT	Input Low Threshold - Schmitt Trigger	0.9	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	1.9	V
VOL	Output Low - DBx,IRQ,DMA.; Io = 12.0mA		0.4	V
VOH	Output High - DBx,IRQ,DMA.; Io = -5.0mA	2.8		V
VOLHC	Output Low - High Current; Io = 48.0mA		0.4	V
ILUL	Latch Up Current Low	40.0		mA
ILUH	Latch Up Current High	-40.0		mA
ILL	Leakage Current Low		10.0	uA
ILH	Leakage Current High		-10.0	uA
ICC	Supply Current - 100uA Source Loads		35.0	mA
ICCHL	Supply Current - 5.0mA Source Loads		85.0	mA
PD	Power Dissipation - ICC Max *		375.0	mW
PDHL	Power Dissipation - ICCHL Max *		525.0	mW

* Includes open drain high current drivers at Vol = 0.4V.

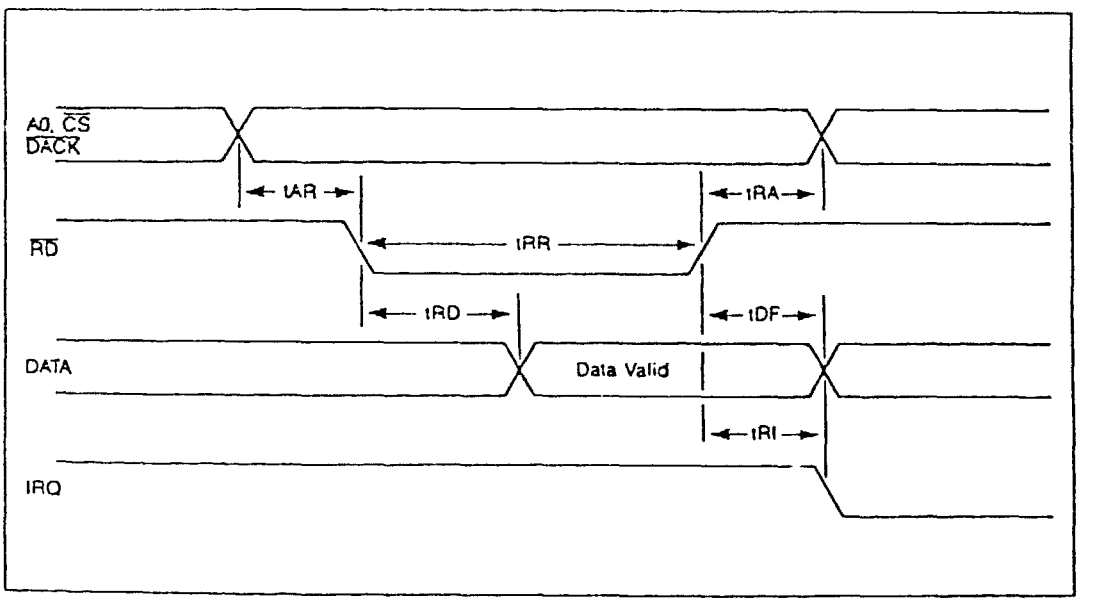


FIGURE 5. READ TIMING

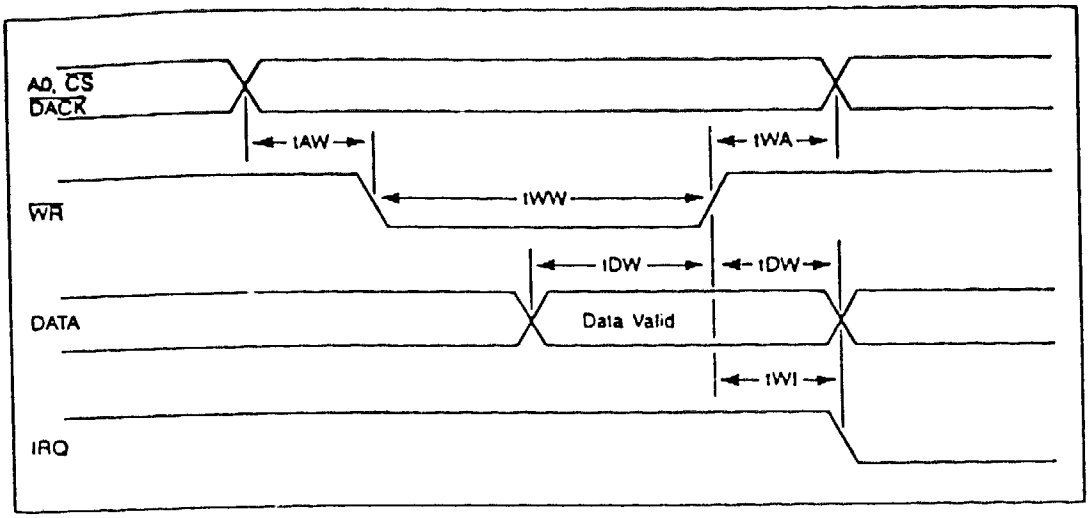


FIGURE 6. WRITE TIMING

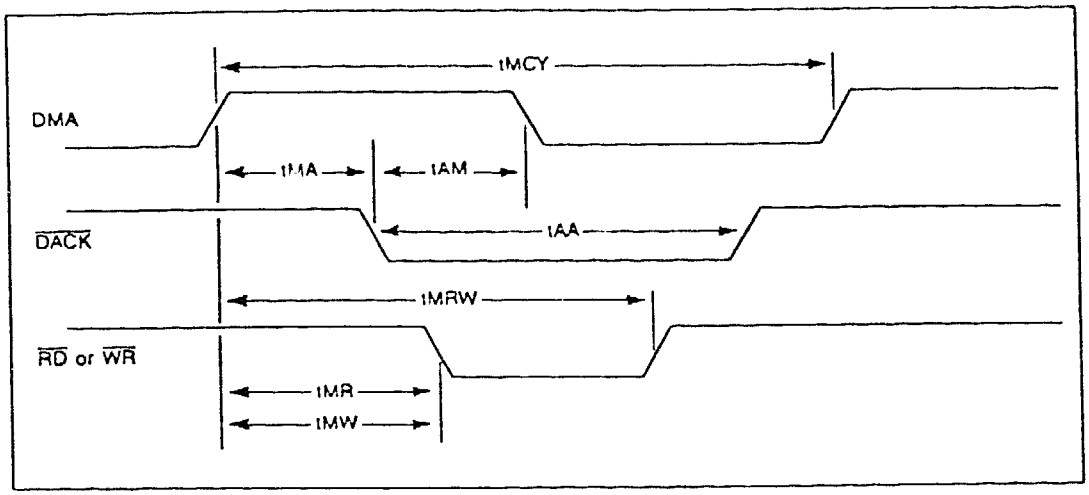


FIGURE 7. DMA TIMING

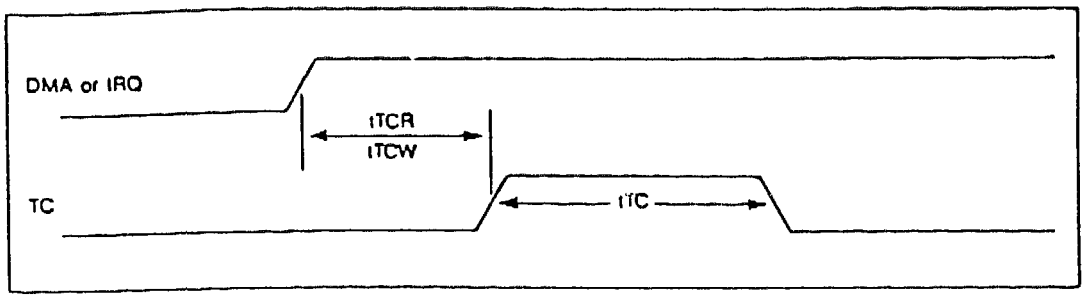


FIGURE 8. TERMINAL COUNT TIMING

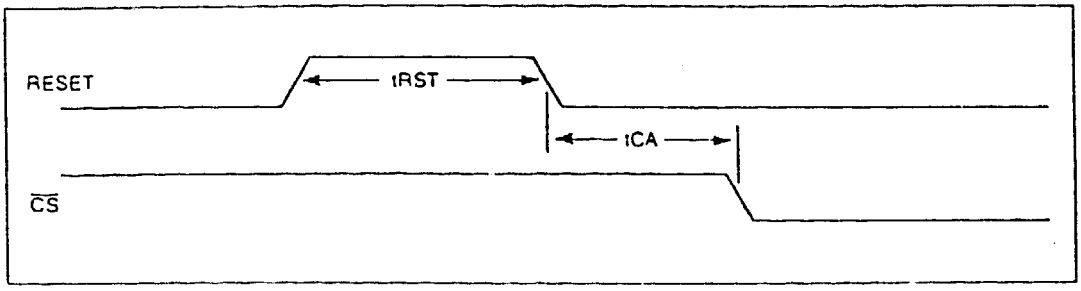


FIGURE 9. RESET TIMING

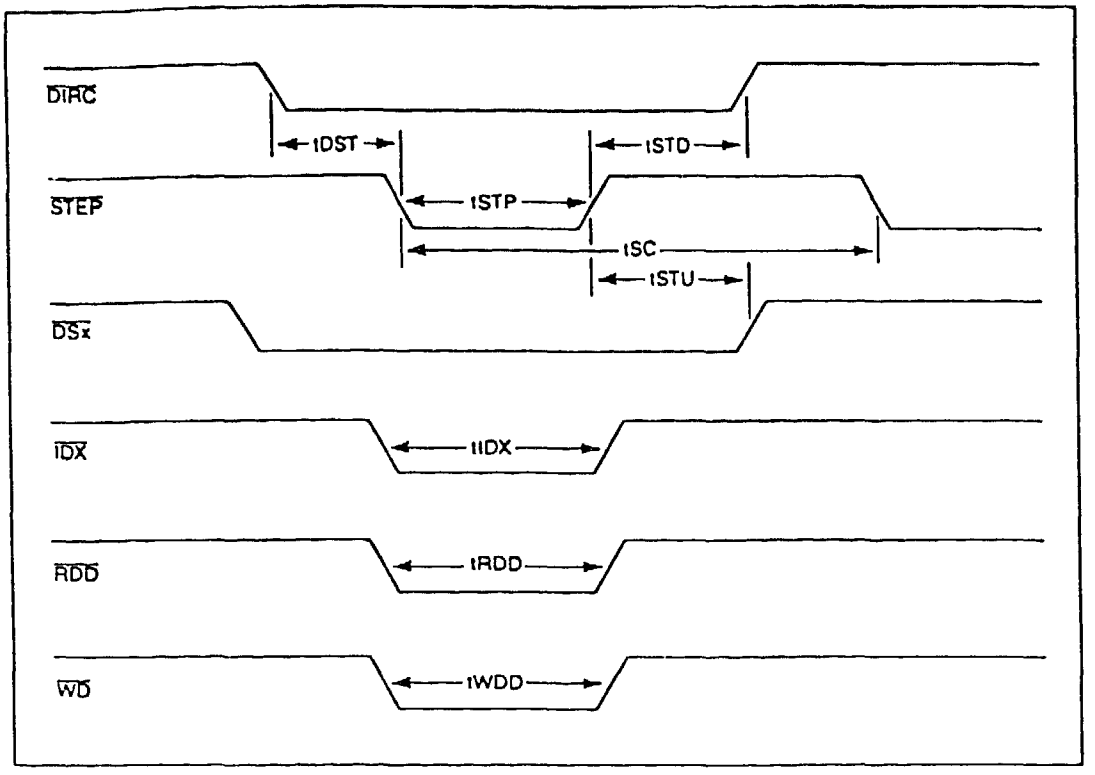


FIGURE 10. DISK DRIVE TIMING

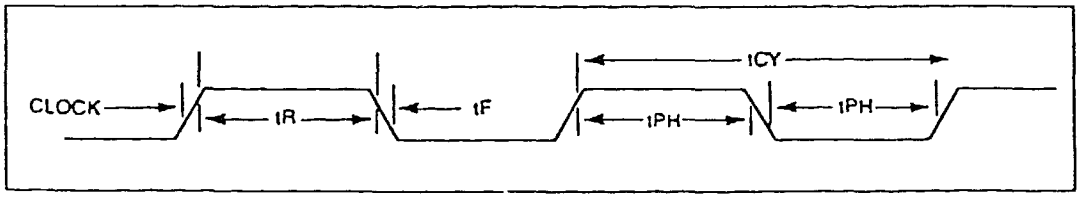
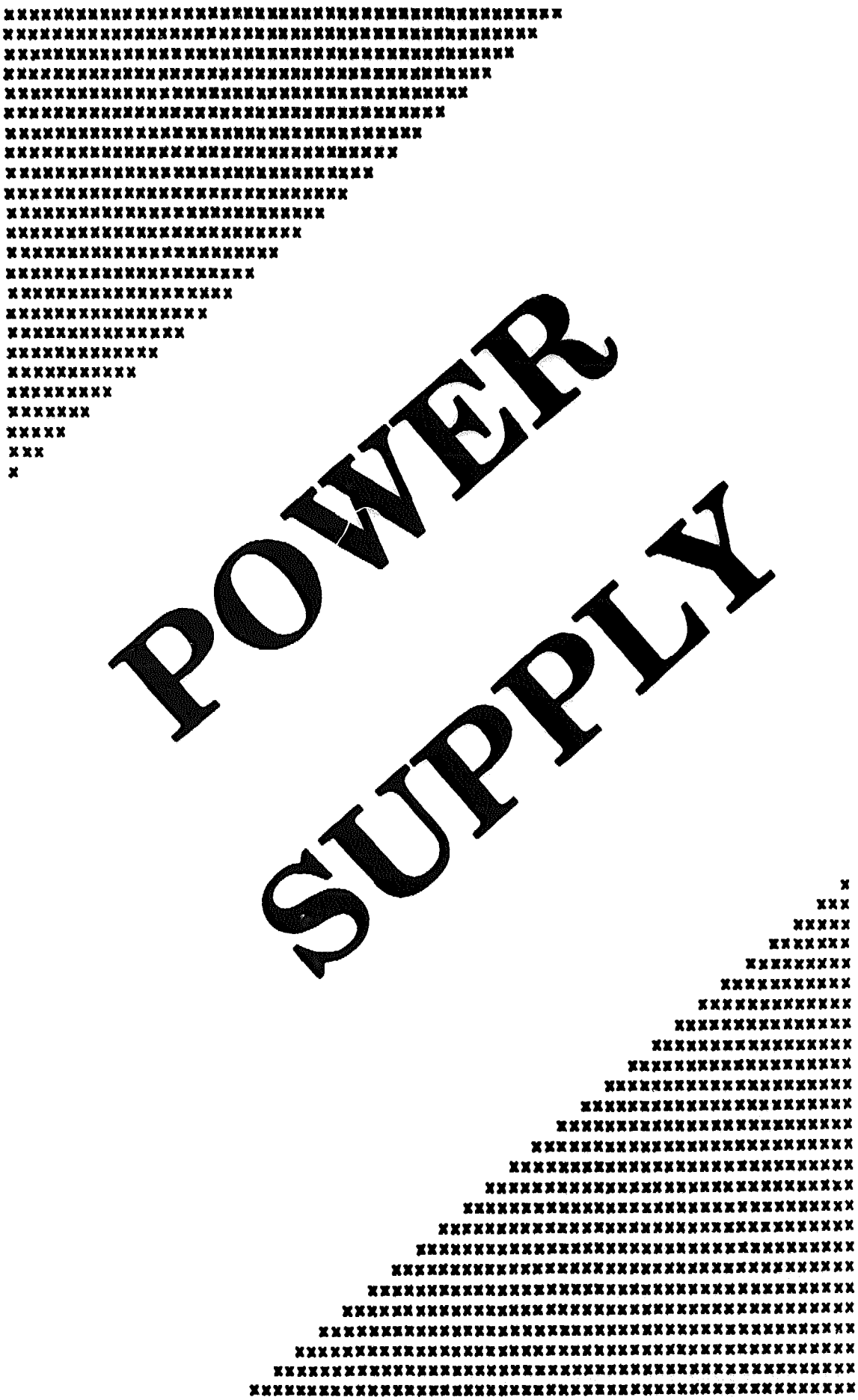


FIGURE 11. CLOCK TIMING

AC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%
CL = 100pf

SYMBOL	PARAMETER	MIN	MAX	UNITS
tCY	Clock Period	60		nS
tPH	Clock Active (High or Low)	25		nS
tR	Clock Rise Time (Vin 0.8 to 2.0)		5	nS
tF	Clock Fall Time (Vin 2.0 to 0.8)		5	nS
tAR	AO,$\overline{CS}$,$\overline{DACK}$ Set Up Time to $\overline{RD}$ Low	0		nS
tRA	AO,$\overline{CS}$,$\overline{DACK}$ Hold Time to RD High	0		nS
tRR	$\overline{RD}$ Width	90		nS
tRD	Data Access Time From $\overline{RD}$ Low		90	nS
tDF	DB To Float Delay From $\overline{RD}$ High	10	65	nS
tAW	AO,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Set Up Time To $\overline{WR}$ Low	0		nS
tWA	AO,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Hold Time From $\overline{WR}$ High	0		nS
tWW	$\overline{WR}$ Width	60		nS
tDW	Data Set Up Time To $\overline{WR}$ High	80		nS
tWD	Data Hold Time From $\overline{WR}$ High	0		nS
tRI	IRQ Reset Delay Time From $\overline{RD}$ High		1MCY	+150nS
tWI	IRQ Reset Delay Time From $\overline{WR}$ High		1MCY	+150nS
tMCY	DMA Cycle Time	52		MCY
tAM	DMA Reset Delay Time From $\overline{DACK}$ Low		140	nS
tMA	$\overline{DACK}$ Delay Time From DMA High	0		nS
tAA	$\overline{DACK}$ Width	2		MCY
tTC	TC Width	60		nS
tRST	Reset Width - TTL Driven CLK1	224		CY
tSRST	Reset Width - Software Reset	5		MCY
tRDD	$\overline{RDD}$ Active Time Low	40		nS
tWDD	$\overline{WD}$ Write Data Width Low	1/2 (TYP)		WCY
tDST	$\overline{DIRC}$ Hold & Set Up To $\overline{STEP}$ Low	4		MCY
tSTU	$\overline{DSX}$ Hold Time From $\overline{STEP}$ Low	20		MCY
tSTP	$\overline{STEP}$ Active Time Low	24		MCY
tSC	$\overline{STEP}$ Cycle Time	132		MCY
tSTD	$\overline{DIRC}$ Hold Time After $\overline{STEP}$	96		MCY
tIDX	$\overline{IDX}$ Index Pulse Width	2		MCY
tMR	$\overline{RD}$ Delay From DMA	0		nS
tMW	$\overline{WR}$ Delay From DMA	0		nS
tMRW	$\overline{RD}$ Or $\overline{WR}$ Response From DMA High		48	MCY
tCA	Chip Access Delay From RST Low - TTL	32		MCY
tCAS	Chip Access Delay From tSRST Low	40		MCY
tXCA	Chip Access Delay from RST - OSC XT1 At 16 MHz	500		uS
tXTS	XT2 Access Delay After RST 9.6 MHz	1000		uS
tTCR	TC Delay From Last DMA Or IRQ, $\overline{RD}$	0	192	MCY
tTCW	TC Delay From Last DMA Or IRQ, $\overline{WR}$	0	384	MCY

CY Specifies CLK1 or XT1 period
MCY Specifies MCLK period, dependent on selected data rate
WCY Specifies WCLK period, dependent on selected data rate


POWER
SUPPLY

Astec Power Supply

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AA13265 Theory of Operation

Introduction

The Astec P/N AA13265 is a feed forward mode off-line switching power supply accepting either 115 VAC or 230 VAC nominal input and delivering four regulated DC outputs at a total of 192 watts.

General Theory

The AC voltage from the power is routed through the EMI filter, rectified, and develops approximately 300 VDC across the capacitive input filters. By turning on the switching transistor this 300 VDC is applied across the primary winding of the power transformer. Due to the phasing of the power transformer windings, the output rectifiers are forward biased during the primary conduction time. Energy is transferred to the output filters and then to the load.

The control circuit senses the +5 VDC and the +12 VDC outputs. It determines the point at which the turn-off circuitry disables the switching transistor.

The protection circuitry senses over and under voltage conditions on all four outputs, over current on the +/−12 VDC rails, and also generates a power good signal. Should the protection circuitry sense a fault, it shuts down the power converter until the power is recycled.

EMI Filter

The EMI filter consists of a common mode choke (T201), differential mode chokes (L201, L202), line to line caps (C201, C202), and line and neutral to ground caps (C203, C204). The purpose of this circuit is to suppress conducted Electro Magnetic Interference which is being fed back into the AC mains by the power supply and the logic systems connected to the power supply.

Surge Protection

Because the AA13265 has a capacitive input filter, input surges can be very high due to the fact that the input capacitors act like a short circuit when power is first applied. Thermistors are designed into the input circuit to limit the turn-on surge. As current passes thru the thermistors (R203, R204, R205) they heat up and consequently their resistance drops to near zero.

Capacitive Input Filter and Voltage Select

C205 and C206 make up the energy storage from which the power stage draws to deliver energy to the loads. These two capacitors are wired in series which allows us to tap off from the center point. When the voltage select is in the 230 VAC position this center cap is left unconnected. In this situation, the diode bridge is connected as a full wave bridge rectifier and produces a DC voltage equivalent to 1.414 times the input voltage (approximately 300 VDC). When the voltage select is in the 115 VAC position the center tap is connected to the neutral line. This converts the input capacitor array into a capacitive doubler, charging C206 down approximately 150 VDC during the negative half-cycle of the AC waveform and charging C205 up 150 VDC during the positive half-cycle of the AC waveform. This results in B+ voltage across the full capacitor array of approximately 300 VDC. Consequently, the primary winding and switching transistor see the same B+ operating voltage at both voltage select positions.

Power Conversion

As explained in General Theory, the power transistor (Q11) turns on, drawing current through the primary winding to return, developing a magnetic field with a linear current ramp. Please notice the dot location on this winding. When Q11 is on, the polarity is such that the dot end of the winding is positive. The secondary windings have the polarity. With dots marking the positive end of the windings at this instant of the cycle, the output rectifiers (D12, D13) are forward biased and conduct. Thus the energy being stored in the input caps is transferred to the output filters and the load.

A common core output choke (L2) is placed between the output rectifiers (D12, D13) and the output filters. This choke serves two purposes. One, it stores energy delivered from T1 in order to help compensate for load surges on the +12V and +5V outputs. Two, it acts as a transformer sourcing energy for the -12 and -5V outputs. The -12V and -5V outputs are derived from separate windings on L2.

The output filters are of Pi filter configuration with inductors preceded and followed by capacitors. For example, on the +5V output the filter consists of C19 followed by L4 followed by C26. The +12V and -12V outputs have similar filters. The -5 output is via a 3T regulator (IC3).

Control Circuit

The control circuit consists of an Astec developed chip (IC2), a pulse transformer (T2), and associated timing and reference generating components. IC2 compares the output with a generated reference voltage. When the output starts to rise beyond a preset limit, IC2 feeds a pulse thru the primary of T2. This pulse is transferred to the turn-off circuitry in the base control of switch transistor (Q11). Consequently, Q11 is quickly turned off preventing further energy transfer to the secondary of T1 on that cycle.

Turn-on/Turn-off Circuits

This section of the circuit consists of seven different parts:

- The clock consists of Q6 and Q7 along with associated components. The clock timing is established by R12 and C4.
- The clock is inhibited during Q11 on time by Q5. It is inhibited during Q11 recovery time by Q4.
- When Q11 is turned on, positive feedback for base drive is supplied thru T3.
- The normal method of turn-off for Q11 is via a pulsed signal fed back from the output thru T2 to the base of Q9. Q9 turns on and quickly robs Q11 of base drive, thereby turning Q11 off.
- Q11 can also be turned off via the primary volt/second limiter. (R17, C6, Q8) or primary current limiter. When Q11 is conducting, a voltage is developed across R35. The voltage is directly proportional to the collector current of Q11. Should the current become too great, due to an overload on the secondary side of T1, the voltage across R35 will turn on Q8. This transistor then turns on Q10 and Q9, which turns off Q11.
- If for some reason control of Q11 can not be maintained, R23 which is a fusible resistor will open the collector current path preventing further damage to the power supply.
- The shut down latch can also control Q11 turn-off by inhibiting the clock pulse. The latch is initially triggered from the secondary protection circuitry thru opto coupler (IC1). Q3 provides a regenerative latch in conjunction with the transistor side of IC1. R1, R2 and Z1 provide a regulated voltage source to keep the latch on until prime power is recycled. In addition, Q2 inhibits false triggering of the latch upon power supply startup.

Protection Circuit

As stated in the General Theory section, the protection circuit fulfills numerous functions.

1. +/-12V over current protection - +12V output current is drawn via transformer (T4). The secondary of T4 provides a voltage proportional to the output current that is rectified and then fed to the base of transistor (Q104). When Q104 turns on, it turns off Q105 which turns Q12 and the LED portion of IC1 on. The -12V current is sensed as a voltage potential across resistor (R48). This voltage is then applied to the base of Q104 in the same manner as the +12V sense voltage. Capacitor (C103) is used to provide surge ride thru capability on the two outputs.
2. Overvoltage protection (OVP) and undervoltage protection (UVP) are provided via Q101, Q102, Q103, Q104, Q105 and associated components. The precision reference for this circuit is generated by programmable zener IC101. Should any of the outputs be overvoltage (or be +5V undervoltage) this circuit will activate, Q12 and the LED portion of IC1 are turned on.
3. Power good is indicated by IC101 and its associated components. The power good signal is tied to the +5V output thru R141. This Circuit supervises the AC input voltage and the four DC output voltages. When transistor (Q106) is turned on, the power good signal is low and vice versa. The power good is low when AC input voltage or any one of the four output voltages are lower than predetermined value.

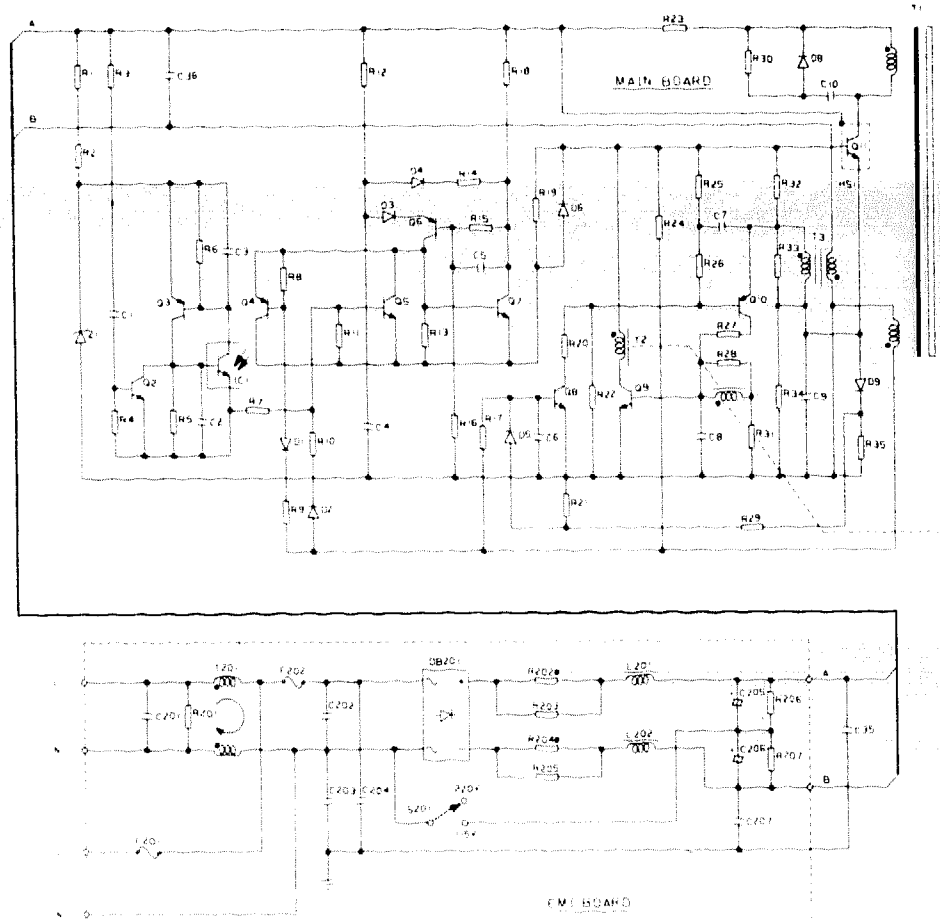
Fan Control

A 12 VDC fan is operated from the -12 VDC output. This circuit contains a fan speed control consisting of a normally open thermal switch in parallel with a ten ohm resistor. Under normal operation, the switch is open and the fan operates at a low speed. Should the power supply become too warm, the switch closes, shorting out the resistor, and the fan operates at full speed. When the power supply cools down, the switch opens again, slowing down the fan. In this manner a nearly constant temperature is maintained within the power supply.

Astec Power Supply Switch Setting

Check to be sure that switch, S201, (on the power supply's EMI/FILTER board) is set to the proper voltage for the location in which the system is to be installed.

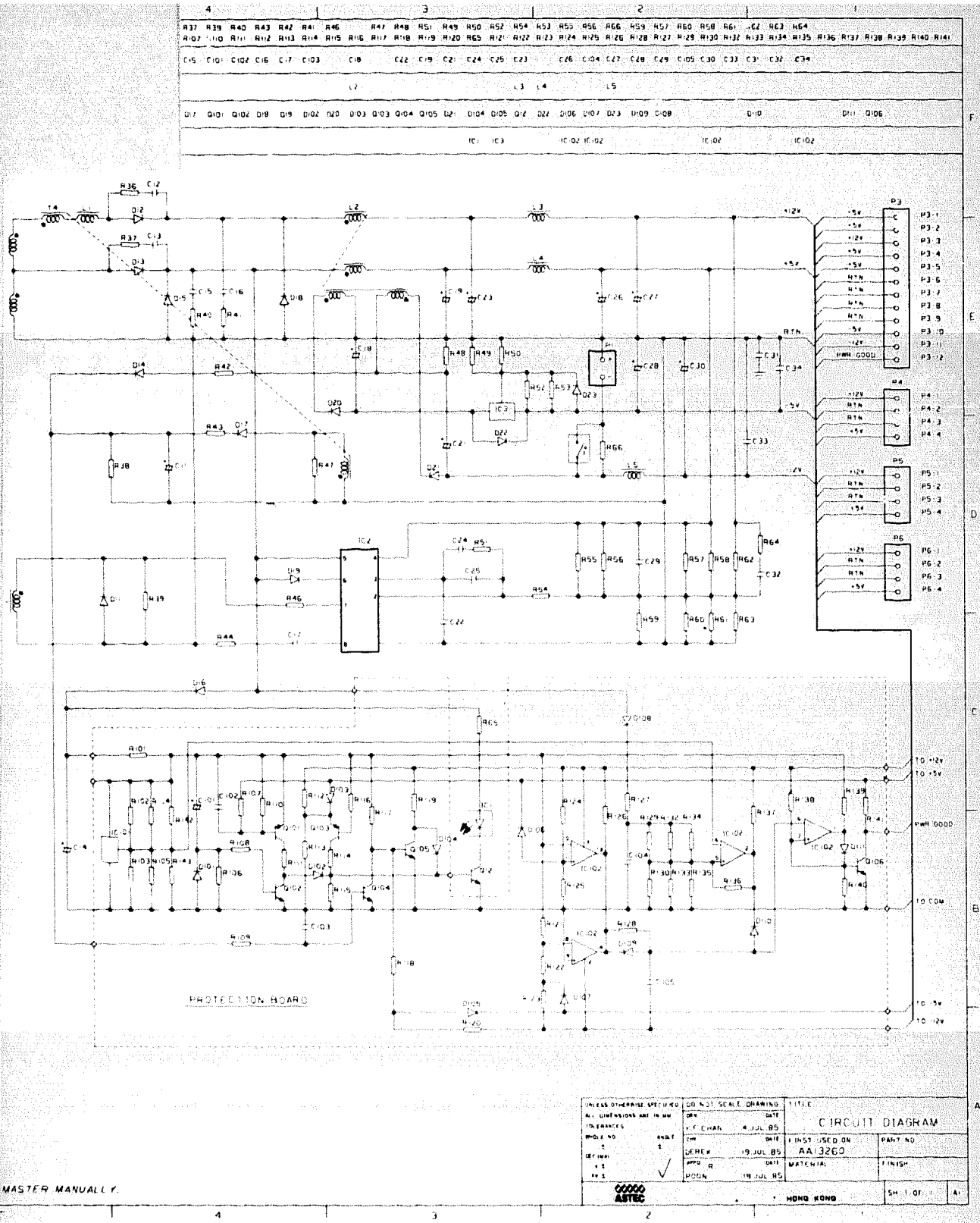
	8	7	6	5
R	R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R145 R146 R147 R148 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174 R175 R176 R177 R178 R179 R180 R181 R182 R183 R184 R185 R186 R187 R188 R189 R190 R191 R192 R193 R194 R195 R196 R197 R198 R199 R200 R201 R202 R203 R204 R205 R206 R207
C	C1 C201 C36 C2 C3 C202 C203 C204 C4 C5 C6 C8 C7 C205 C206 C9 C10 C207 C35 C14 C12 C13 C11
T/L	T201 T2 L201 L202 T3 T1 T4 L1
D/Q	Q2 Q3 Q4 D1 D2 D3 D5 D4 D6 D7 D5 D8 D6 Q9 Q10 D8 Q11 D9 D11 D12 D13 D14 D15 D16 D101
MISC	Z1 F201 IC1 F202 DB201 HS1 IC101



ISSUE	REVISIONS	APPD	CHK	DATE	ECN
4	CHANGE C14 AND C41	GORDAN	DEREK	22 DEC 88	E14189
3	ADD H66	POON	DEREK	20 AUG 88	E13093
2	DELETE H66	POON	DEREK	10 JUN 88	E16769
1	REL DRAWING	POON	DEREK	19 JAN 88	

NOTE: THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER. DO NOT UPDATE

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UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN MM TOLERANCES WHOLE NO ANGLE ± ± DECIMAL ± 0.1 ± 0.05	DO NOT SCALE DRAWING	TITLE	
	DRN DATE	CIRCUIT DIAGRAM	
	Y.F.CHAN 4 JUL 85		
	CHK DATE	FIRST USED ON	PART NO
	DEREK 19 JUL 85	AA13260	
	APPD DATE	MATERIAL	FINISH
	PDGN 19 JUL 85		
ASTEC	HONG KONG	SH 1 OF 1	A1

MASTER MANUALLY.

DELTA POWER SUPPLY MODEL DPS-200EP REV.C4

THEORY OF OPERATION

This theory of operation aims to provide detailed technical information about the switching power supply DPS-200EP REV.C produced by Delta Electronic Ind. Co., Ltd.

1. The DPS-200EP model is composed of half-bridge power supplies.

2. Raw B+ rectified from the AC input circuit consists of CR101, C101 and C102.

3A. The auxiliary power supply consists of local transformer T101, rectifiers D110, D103, D104 and C105.

3B. +12VDC output provides power for IC1, T102, Q101 and Q102.

4. Thermistors NTC101 and NTC102 are in series with the rectifier CR101 output and used to limit AC inrush current.

5A. IC1 TL494 is a PWM whose functions are as follows:

a) Low duty cycle when output is lower load.
b) High duty cycle when output is higher load.
c) Low duty cycle when AC input voltage is higher.
d) High duty cycle when AC input voltage is lower.

5B. The duty cycle IC1 output is subject to the comparison of voltages between Pin 2 and Pin 1, which sense the +5.0V and +12.0V outputs.

Output switching transistors Q103 and Q104 are driven by driver stage Q101 and Q102 which are controlled by IC1 Pin 10 and Pin 9 outputs, respectively.

5C. The snubber circuit is composed of R107 and C103. It is used to protect Q103 and Q104 and reduce the noise of their outputs.

5D. The major function of D101 and D102 is to protect Q103 and Q104 from overstress when Q103 and Q104 turn off alternacively.

5E. To prevent T103 from saturation due to DC current, a capacitor C104 is used.

5F. The second snubber circuit is composed of R111-R116, C106-C110 and C111 and is used to protect CR102-CR104, D106, D107.

6. The overpower protection circuit composed of CT101, D1, R14-R16, C7, D3, VR2, D2, Q1, and Q2 senses the current of T101 and T102. When the output is shorted, the sampling voltage from current transformer CT101 and Pin 14 of IC1 can trigger the shut down circuit, composed of Q1, Q2 and also make the Pin 4 voltage of IC1 over 3V, which will cause no output signal at Pin 9 and Pin 10 of IC1, causing the power supply to shut down.

7. The +5V AND +12V overvoltage protection circuit is composed of ZD1, ZD2 and other relevant components. It is triggered when the +5V and/or +12V fluctuate over a range of 5.7V-6.7V and 13V-13.9V due to the abnormal operation of the control circuit.

8. +5V output is rectified from the components composed of L101, L104, C113, C115, CR103, CR104

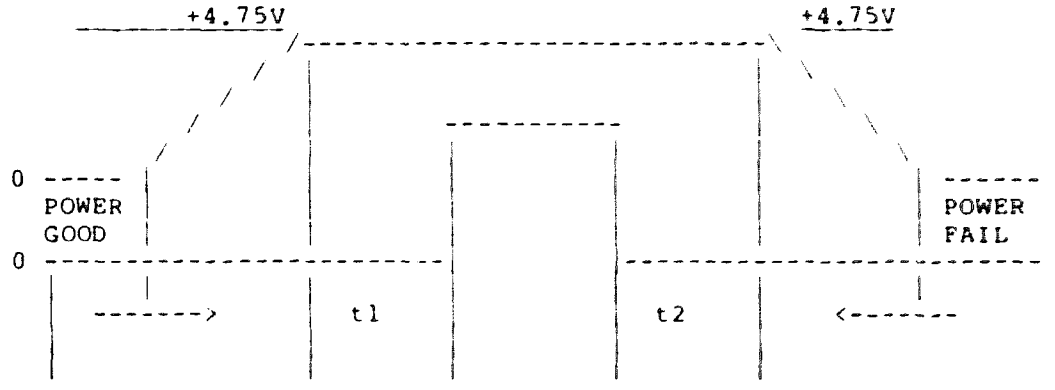
The other supply voltages are rectified by:
+12V : L101, L103, C114, C116, CR102
-12V : L101, L102, C112, D106, D107
- 5V : L101, L105, C117, C118, D109

9. The DC OK signal consists of IC101, D110, C121, VR101 R126-R140.

The function of the DC OK signal is described as follows:

During power up, an active high signal (DC OK signal) will be provided to indicate the 5V output to be in regulation. The delay time of this DC OK signal after 5V output in regulation shall be within 100 - 500ms. During power-off, the signal should go to a low level by 1msec before the +5V is out of regulation. The low level is 0V to 0.8V and the high level is 4.75V to 5.25V.

*TIMING DIAGRAM



*t1 : Delay Turn-On (100 < t3 < 500 msec.)
*t2 : Delay Turn-Off (1msec. min.)

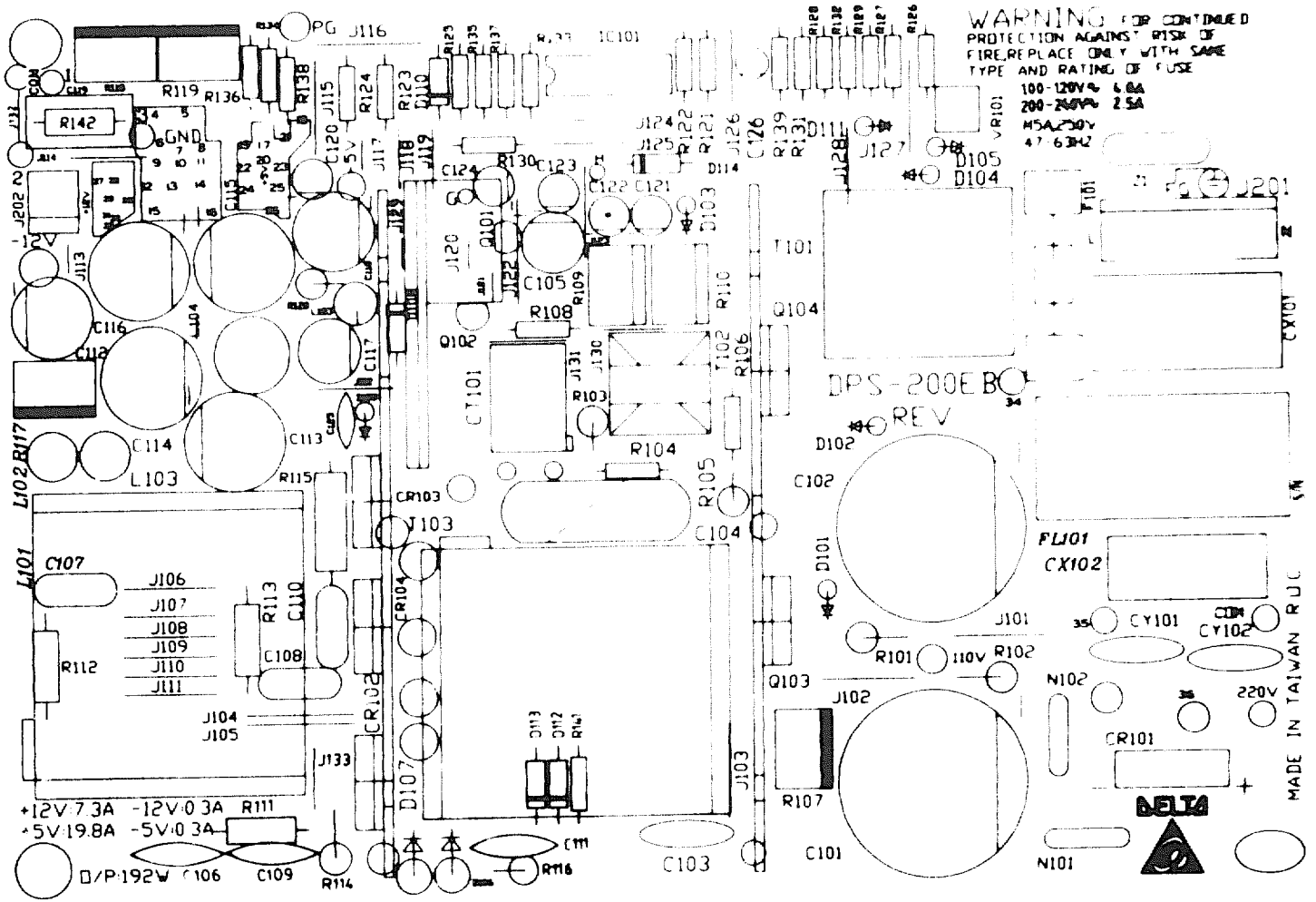
DELTA POWER SUPPLY PARTS LIST MODEL NO. :DPS-200EP REVC
P/N :B/M-200EP REVC

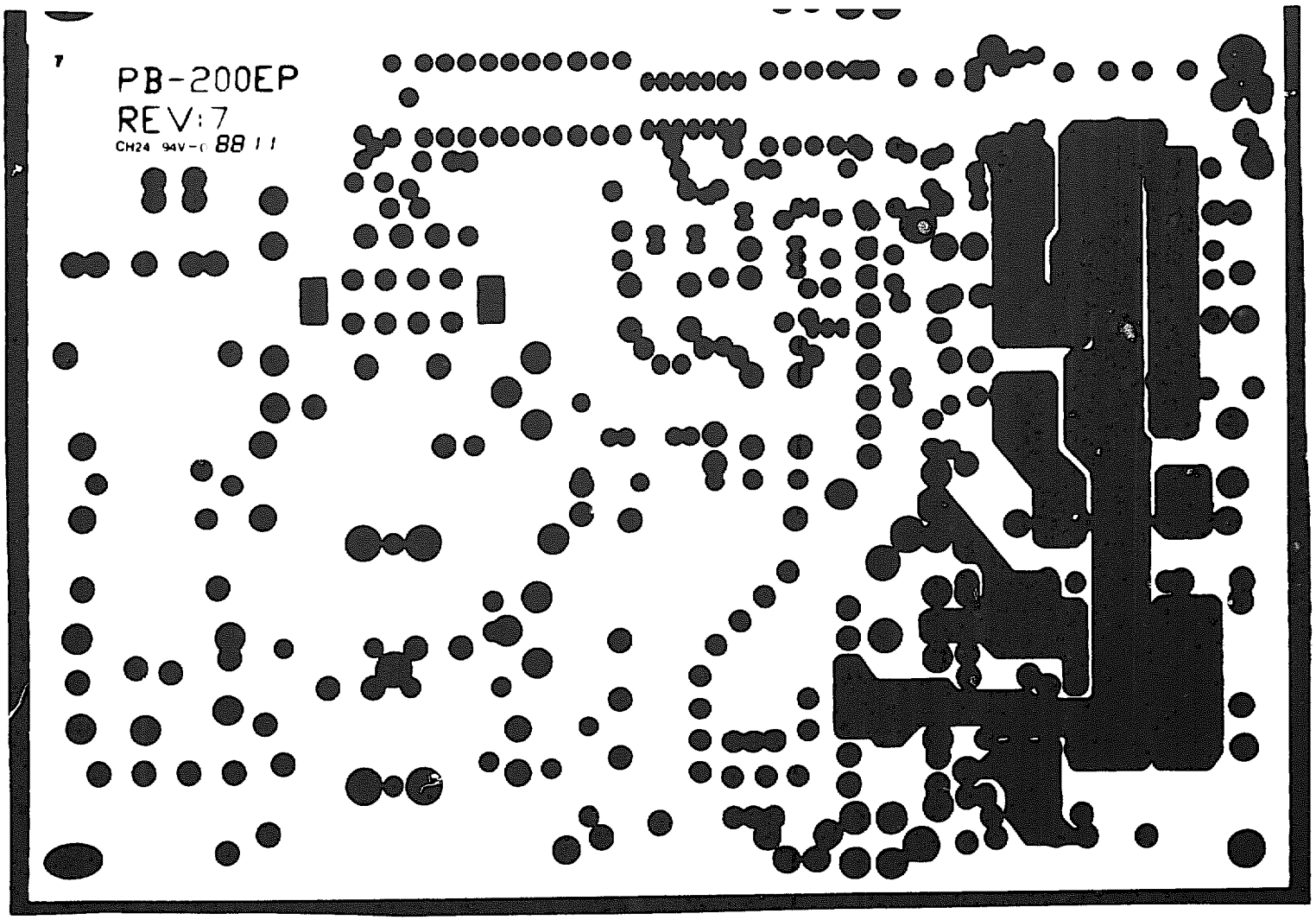
PART NO.	DESCRIPTION	REFERENCE NO.
SMKBU8K	BRIDGE DIODE KBU8K 8A 800V	'CR101
SMS12KC20	S12KC20 12A 200V	'CR102
SMS30SC4M	Io=30A Vrm=40V S30SC4M	'CR103 CR104
SMRGP10J	FAST RECOVERY DIODE 1A 600V	'D101 D102
SMRGP10B	FAST RECOVERY DIODE 1A 100V	'D103 D104 D108 D109
SMRGP20B	FAST RECOVERY DIODE 2A 100V	'D106 D107
SM1N4148	DIODE 1N4148 150mA 75V	'D110 D112 D113 D114
SM339	VOLTAGE COMPARATOR 600mW 36V	'IC101
SM2SD468	TRANSISTOR 1A 20V	'Q101 Q102
SM2SC3164	TRANSISTOR 10A 400V	'Q103 Q104
06SEEG3H	EMI FILTER	*
ST-U12-01	TRANSFORMER	*CT101
LF-R31-03-A	LINE FILTER	*FL101
CE-42H-08	CHOKE	*L101
CB-6.2-06	CHOKE	*L102
CB-6.5-07	CHOKE	*L103
CB-6.5-04	CHOKE	*L104
CD-6.0-04	CHOKE	*L105
PT-3576-1	TRANSFORMER	*T101
DT-E16-16A	TRANSFORMER	*T102
SMT-42H-93A	TRANSFORMER	*T103
10000-0086-51	PACKAGE	.
CUS-03-3	CTRL BOARD ASS'Y REV:4	.
LB-19	LABEL (UL,CSA,TUV)	.
PB-200EP	PCB REV:7 (CEM-1) CODE NO.7	.
G100	PIN	.FOR 115V-230V SELECT
JPC1522-02	HOUSING LINE INPUT L=75mm	.FOR 115V/230V SELECT
G891S	RIVET ID=1.8mm	.FOR C101 C102
T34*.0025MFR	MYLAR TAPE	.FOR C101 L=60mm
T12*0.25HFR	HEAT SHRINKABLE TUBING	.FOR C111 L=25mm
T1.0*0.4PVCFR	PVC TUBING BLACK	.FOR C126 L=12mm
D-012	INSULATOR	.FOR C102 CR103 CR104
F3*0.5*12D	SCREW L=12mm	.FOR CR102 CR103 CR104
F3*0.5*3.ON	NUT	.FOR CR102 CR103 CR104 TM85
T27*.0025MFR	MYLAR TAPE	.FOR CX101(100)
T17*.0025MFR	MYLAR TAPE	.FOR CX102 L=75mm
FC-01	FUSE CLIP	.FOR F101

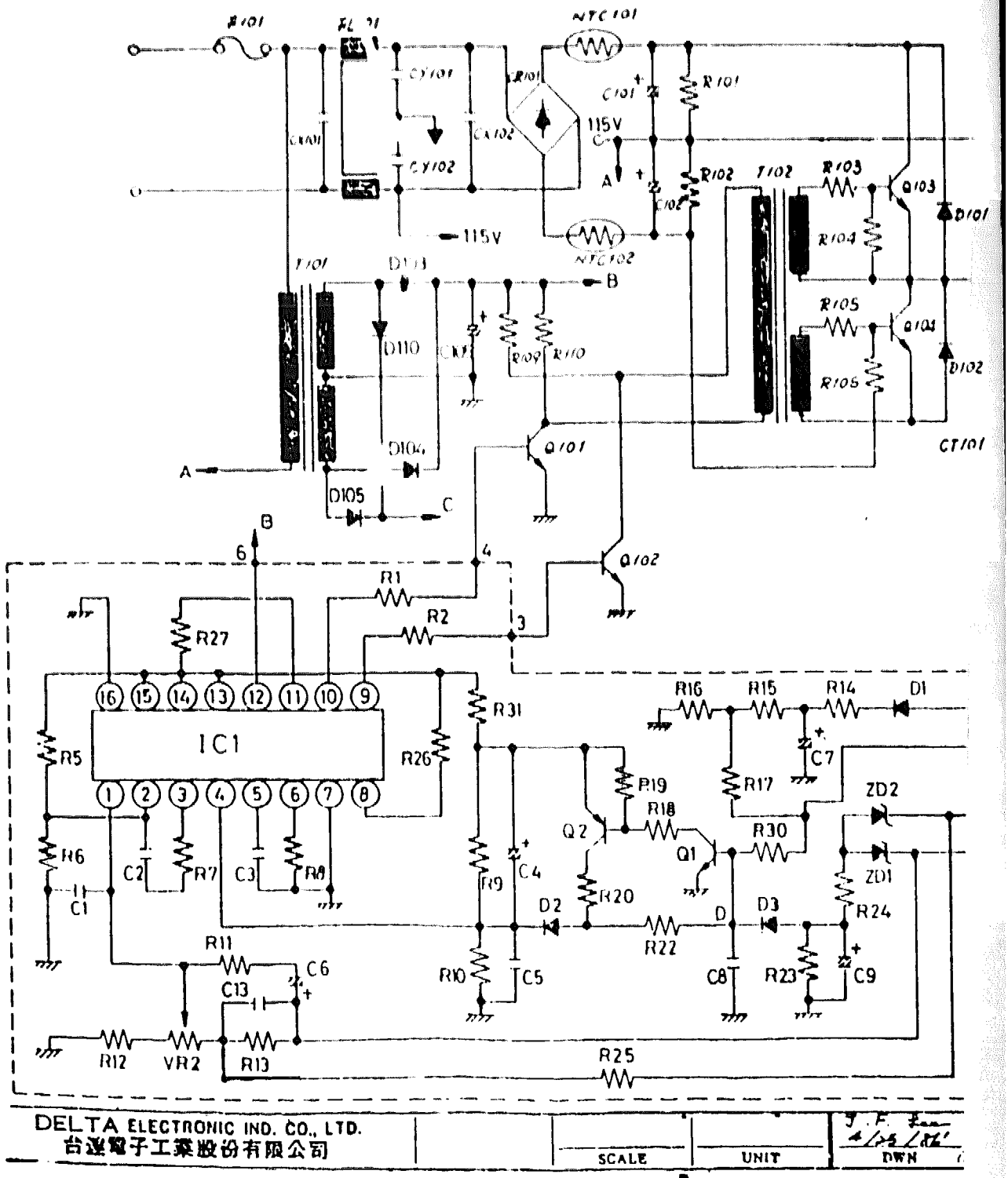
FU-5L	FUSE 5A 250V (LONG)	.FOR F101
F-15	PLASTIC STAND OFF H=10mm	.FOR HS-071-3
F-17	PLASTIC STAND OFF H=6.35mm	.FOR HS-071-3
TM45	45 OHM	.FOR J113
LB-3	LABEL (115V)	.FOR JPC1522-02
CONO718*12-3	CONNECTOR	.FOR OUTPUT
CONO718*4-35	OUTPUT CABLE	.FOR OUTPUT
F-10A	CABLE TIE L=140mm	.FOR OUTPUT
F-10C	CABLE TIE L=80mm	.FOR OUTPUT
D-025	INSULATOR	.FOR Q103 Q104
F-37A	SPRING CLIP	.FOR Q103 Q104
HS-071-3	HEAT SINK REV:2	.FOR Q103 Q104 CR102 103 104
F3*0.5*8D	SCREW L=8mm	.FOR TM45
JTS06-15	JUMPER WIRE 0.6D L=15mm	.J101 J102 J103 J115 J123 J127
JTS06-17.5	JUMPER WIRE -.6D L=17.5mm	.J104 J105
JTS06-15	JUMPER WIRE 0.6D L=15mm	.J106 J107 J108 J109 J110 J111
JTS06-12.5	JUMPER WIRE 0.6D L=12.5mm	.J112 J114 J125 J126 J128
JTS06-17.5	JUMPER WIRE 0.6D L=17.5mm	.J116 J122
JTS06-5	JUMPER WIRE 0.6D L=5mm	.J117 J120 J121 J129
JTS06-10	JUMPER WIRE 0.6D L=10mm	.J118 J119 J124 J133
JTS08-10	JUMPER WIRE 0.8D L=10mm	.J130
JTS08-12.5	JUMPER WIRE 0.8D L=12.5mm	.J131
JTS06-7.5	JUMPER WIRE 0.67D L=7.5mm	.J132
CONY5273-05B	CONNECTOR 3 circuits	.J201
CONY5273-02A	CONNECTOR 2 circuits	.J202
G891V	RIVET ID=1.5mm	.L101 T103 C112 C113 C115 C116
CEA681MC2D	680uF 200V +-20% 30*40(mm)85 C	C101 C102
CD332MY5U2GAC	3300PF 400VAC +-20%	C103
CMP225M2E-S	2.2UF 250V +-20%	C104
CEA471MX1C	470UF 16V +-20% 5	C105 C112 C117 C118
CD103MZ5U3A4	0.01UF 1KV +-20% 10	C106 C109 C110 C111
CD102MZ5P3A4	1000PF 1KV +-20% Tc=+-10% 10	C107 C108
CEA472MX1A	4700UF 10V +-20% 7.5	C113
CEA222MX1E	2200UF 25V +-20% 7.5	C114 C115 C116
CMM104M2EAC	0.1UF 250VAC +-20% MEF	C119
CEA4R7MB1V	4.7UF 35V +-20% +105 DEGREE C	C121 C126
CEA220MB1C	22UF 16V +-20%	C122
CEA470MB1E	47UF 25V +-20% +105 DEGREE C	C123
CEA1ROMB1H	1UF 50V +-20% +105 DEGREE C	C124
CMM105M2EAC	1UF 250VAC +-20% MEF	CX101
CMM334M2EAC	0.33UF 250VAC +-20% MEF	CX102
CD222MY5U2GAC	2200PF 400VAC +-20%	CY101 CY102
TM003	15SP003	NTC101 NTC102
RM473J21-L	47K OHM 2W +-5% LEAD=38mm	R101 R102
RC1R0J12	1 OHM 1/2W +-5%	R103 R105

RC102J14	1K OHM 1/4W +-5%	R104 R106
		R128 R138
RQ270J51-1	27 OHM 5W +-5%	R107
RC121J14	120 OHM 1/4W +-5%	R108
RQ400J51-1	40 OHM 5W +-5%	R109 R110
RC100J12	10 OHM 1/2W +-5%	R111 R114
RC3R9J12	3.9 OHM 1/2W +-5%	R112 R113
RM101J21	100 OHM 2W +-5%	R115
RM220J21-L	22 OHM 2W +-5% LEAD=38mm	R116
RQ470J51-1	47 OHM 5W +-5%	R117 R118 R119
RM390J21-L	39 OHM 2W +-5% LEAD =38mm	R120
RC103J14	10K OHM 1/4W +-5%	R122
RC512J14	5.1K OHM 1/4W +-5%	R123 R124
RC103J14	10K OHM 1/4W +-5%	R125
RC821J14	820 OHM 1/4W +-5%	R126
RC153J14	15K OHM 1/4W +-5%	R127
RC393J14	39K OHM 1/4W +-5%	R129
RC472J14	4.7K OHM 1/4W +-5%	R130
RC104J14	100K OHM 1/4W +-5%	R131 R133
RC122J14	1.2K OHM 1/4W +-5%	R132 R134
RC682J14	6.8K OHM 1/4W +-5%	R135 R136 R137
		R139
RC100J14	10 OHM 1/4W +-5%	R141
JTS06-4	JUMPER WIRE 0.6D L=4mm	VR101

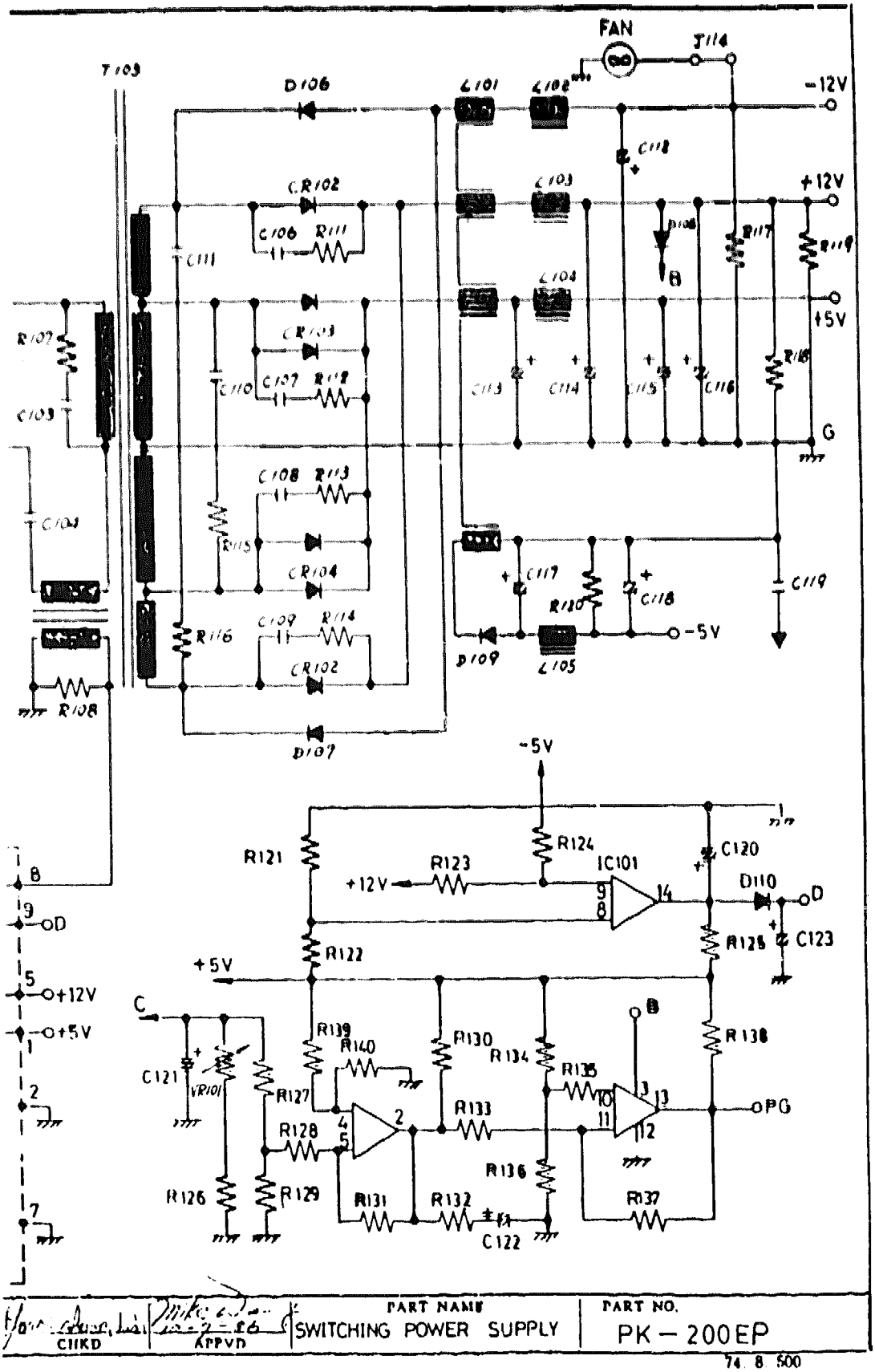
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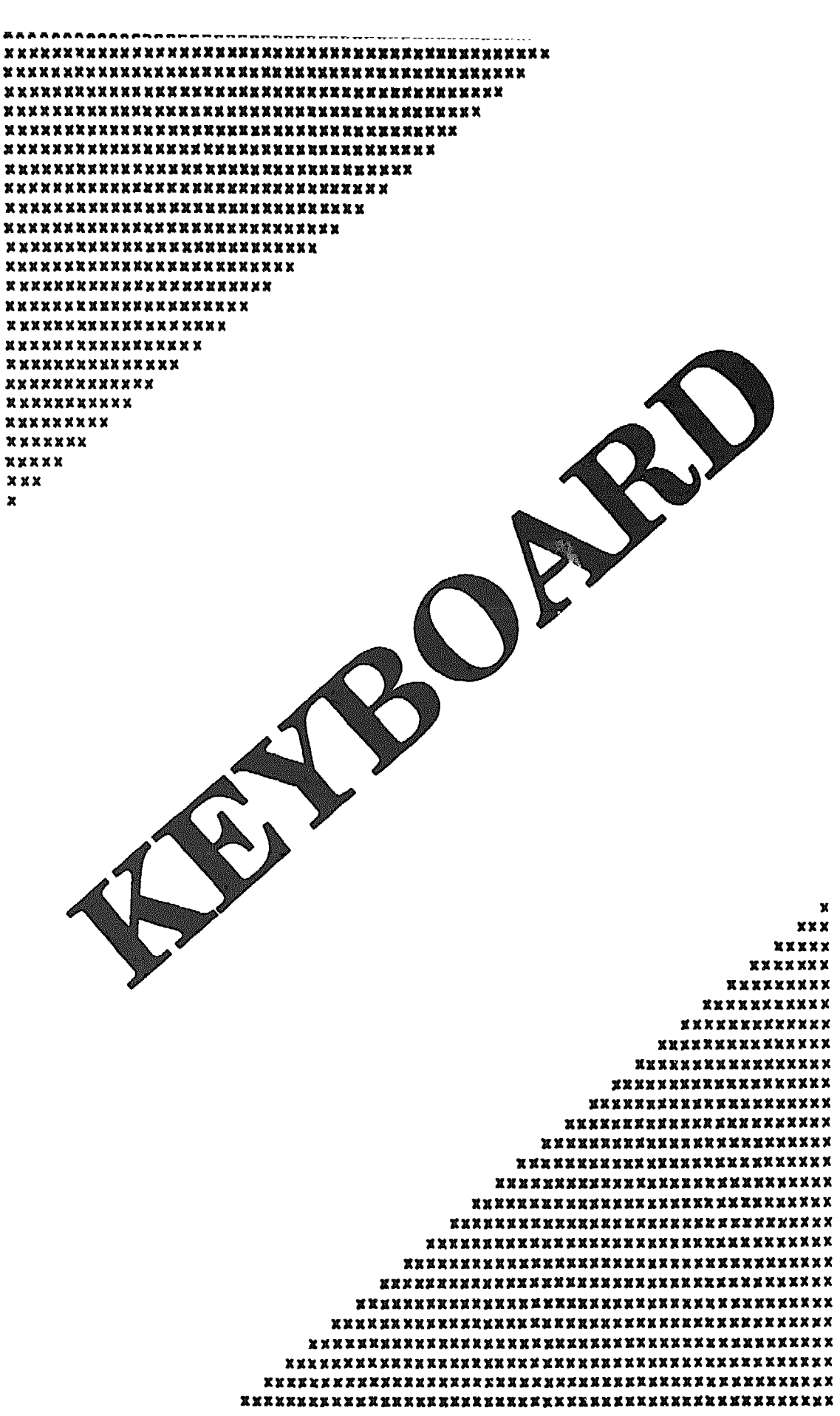

WARNING
PROTECTION AGAINST RISK OF
FIRE, REPLACE ONLY WITH SAME
TYPE AND RATING OF FUSE
DPS-200EB
REV
MADE IN TAIWAN R.O.C
DELTA
+12V 7.3A -12V 0.3A R111
+5V 19.8A -5V 0.3A
O/P 192W
110V
220V


PB-200EP
REV:7
CH24 94V-0 88 11



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FAN
T114
T103
D106
L101
L102
-12V
C118
C.R102
L103
+12V
C106
R111
C111
D108
R117
R119
B
L104
+5V
R107
C103
CR103
C110
C107
R112
C113
C114
C115
C116
R118
G
C108
R113
C101
R115
CR104
C117
R120
C118
C119
R116
C109
R114
CR102
D109
L105
-5V
R108
D107
-5V
R121
R124
C120
R123
+12V
IC101
D110
D
B
R122
R125
C123
+5V
C
R139
R140
R130
R134
R135
R138
C121
VR101
R127
R133
PG
R128
R136
R126
R129
R131
R132
R137
C122
PART NAME
SWITCHING POWER SUPPLY
PART NO.
PK-200EP
74. 8. 500


KEYBOARD

Fujitsu Keyboard Assembly
N860-4703-T

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Fujitsu Keyboard Assembly
N860-4703-T

1.0 General

The keyboard is a direct, plug-compatible replacement for the Enhanced Keyboard for the IBM PC, XT, and AT personal computer. No software modification or special interface is needed by the user.

2.0 Scope

This specification describes the functional, mechanical, electrical, environmental, and reliability characteristics of the FUJITSU N860-4703-T Keyboard assembly.

The keyboard is encoded in such a way as to produce a unique output code for each key that is pressed and/or released. The communication with the host computer is a synchronous serial link. The Key Layout, Switch Encoding and Serial Communication are all compatible with the IBM PC, XT and AT.

3.0 Mechanical Specification

3.1 Key Layout, Legends, and Colors

Figure 1 shows keytop layout, appropriate legends and keytop colors. The keys are numbered from left to right starting with the spacebar row (Row A) and ending with the function key row (Row F).

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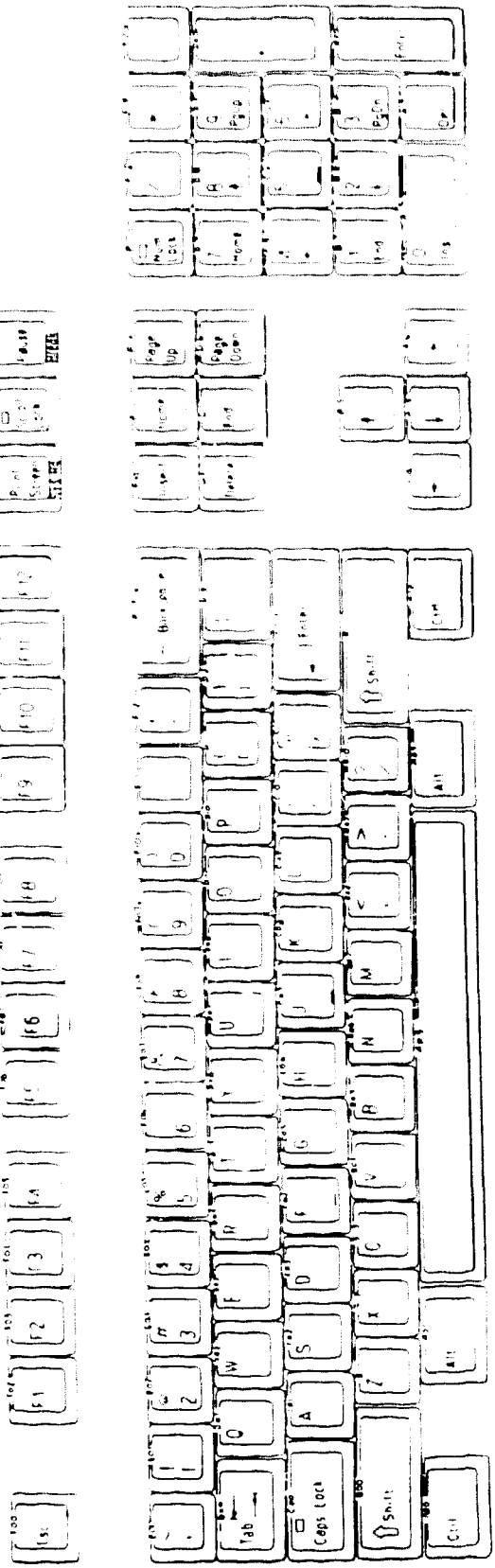


FIGURE 1

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3.2 Keyswitch

3.2.1 Total Travel: 0.150", +/- 0.020" (3.8, +/-0.5mm)

3.2.2 Force: All keyswitches shall utilize a 2.0 ounce (+/- 0.9 oz) operating force. This is accomplished using both a rubber keyswitch membrane and springs.

3.2.3 Breakover Feedback: The keyswitches utilize a tactile feedback to assure the operator that the key has been fully pressed.

4.0 Functional Requirements

4.1 Scan Codes

The keyboard generates a unique Hex scan code for each keyswitch that is pressed (make code) and released (break code). For the AT Mode, the break code is the same as the make code preceded by "F0" Hex. Example: The make code for the "ESC" key is 76 Hex and the break code is two bytes, F0 76 Hex. For the XT Mode, the break code is 80 Hex, plus the make code. Example: The make code for the "ESC" key is 01 Hex and the break code is 81 Hex. The keyswitch-to-scan-code (make and break codes) assignments, Standard ASCII Codes, and Extended ASCII Codes are listed on the following pages.

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
1	Esc	76	F076	01	81	011B	011B	011B	-----	011B	011B	011B	0100
2	F1	05	F005	3B	BB	3B00	5400	5E00	6800	3B00	5400	5E00	6800
3	F2	06	F006	3C	BC	3C00	5500	5F00	6900	3C00	5500	5F00	6900
4	F3	04	F004	3D	BD	3D00	5600	6000	6A00	3D00	5600	6000	6A00
5	F4	0C	F00C	3E	BE	3E00	5700	6100	6B00	3E00	5700	6100	6B00
6	F5	03	F003	3F	BF	3F00	5800	6200	6C00	3F00	5800	6200	6C00
7	F6	0B	F00B	40	C0	4000	5900	6300	6D00	4000	5900	6300	6D00
8	F7	83	F083	41	C1	4100	5A00	6400	6E00	4100	5A00	6400	6E00
9	F8	0A	F00A	42	C2	4200	5B00	6500	6F00	4200	5B00	6500	6F00
10	F9	01	F001	43	C3	4300	5C00	6600	7000	4300	5C00	6600	7000
11	F10	09	F009	44	C4	4400	5D00	6700	7100	4400	5D00	6700	7100
12	F11	78	F078	57	D7	-----	-----	-----	-----	8500	8700	8900	8B00
13	F12	07	F007	58	D8	-----	-----	-----	-----	8600	8800	8A00	8C00
14	Print Scrn	E07C	E0F07C	F02AE037	E0B7E0AA	Note[1]	Note[1]	7200	-----	Note[1]	Note[1]	7200	-----
15	Scroll Lock	7E	F07E	46	C6	Note[2]	Note[2]	------	Note[2]	Note[2]	Note[2]	-----	Note[2]
16	Pause Break	E11477	E1F014F077	E11D45	E19DC5	Note[3]	Note[3]	Note[4]	Note[3]	Note[3]	Note[3]	Note[4]	Note[3]
17	~ or \	0E	F00E	2B	AB	2960	297E	-----	-----	6000	7E00	-----	2900
18	! or 1	16	F016	02	82	0231	0221	-----	7800	0231	0221	-----	7800

Table 1

KEYBOARD SCAN CODES

Key #	Key Descript	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
19	@ or 2	1E	F01E	03	83	0332	0340	0300	7900	0332	0340	0300	7900
20	# or 3	26	F026	04	84	0433	0423	-----	7A00	0433	0423	-----	7A00
21	$ or 4	25	F025	05	85	0534	0524	-----	7B00	0534	0524	-----	7B00
22	% or 5	2E	F02E	06	86	0635	0625	-----	7C00	0635	0625	-----	7C00
23	^ or 6	36	F036	07	87	0736	075E	071E	7D00	0736	075E	071E	7D00
24	& or 7	3D	F03D	08	88	0837	0826	-----	7E00	0837	0826	-----	7E00
25	* or 8	3E	F03E	09	89	0938	092A	-----	7F00	0938	092A	-----	7F00
26	(or 9	46	F046	0A	8A	0A39	0A28	-----	8000	0A39	0A28	-----	8000
27	) or 0	45	F045	0B	8B	0B34	0B29	-----	8100	0B34	0B29	-----	8100
28	_ or -	4E	F04E	0C	8C	0C2D	0C5F	0C1F	8200	0C2D	0C5F	0C1F	8200
29	+ or =	55	F055	0D	8D	0D3D	0D2B	-----	8300	0D3D	0D2B	-----	8300
30	Backspace	66	F066	0E	8E	0E08	0E08	0E7F	-----	0E08	0E08	0E7F	0E00
31	Insert	E070	E0F070	E02AE052	E0D2E0AA	5200	5200	-----	-----	52E0	52E0	92E0	A200
32	Home	E06C	E0F06C	E02AE047	E0C7E0AA	4700	4700	7700	-----	47E0	47E0	77E0	9700
33	Pg Up	E07D	E0F07D	E02AE049	E0C9E0AA	4900[S]	4900[S]	8400	----- [S]	49E0[S]	49E0[S]	84E0	9900[S]
34	Num Lock	77	F077	45	C5	Note[S]	Note[S]	-----	Note[S]	Note[S]	Note[S]	----	Note[S]
35	/	E04A	E0F04A	E035	E0B5	352F	352F	-----	-----	E02F	E02F	9500	A400
36	*	7C	F07C	37	B7	372A	372A	-----	-----	372A	372A	9600	3700
37	-	7B	F07B	4A	CA	4A2D	4A2D	-----	-----	4A2D	4A2D	8E00	4A00

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
38	Tab	0D	F00D	0F	8F	0F90	0F00	.....	.....	0F09	0F00	9400	A500
39	Q or q	15	F015	10	90	1071	1051	1011	1000	1071	1051	1011	1000
40	W or w	1D	F01D	11	91	1177	1157	1117	1100	1177	1157	1117	1100
41	E or e	24	F024	12	92	1265	1245	1205	1200	1265	1245	1205	1200
42	R or r	2D	F02D	13	93	1372	1352	1312	1300	1372	1352	1312	1300
43	T or t	2C	F02C	14	94	1474	1454	1414	1400	1474	1454	1414	1400
44	Y or y	35	F035	15	95	1579	1559	1519	1500	1579	1559	1519	1500
45	U or u	3C	F03C	16	96	1675	1655	1615	1600	1675	1655	1615	1600
46	I or i	43	F043	17	97	1769	1749	1709	1700	1769	1749	1709	1700
47	O or o	44	F044	18	98	186F	184F	180F	1800	186F	184F	180F	1800
48	P or p	4D	F04D	19	99	1970	1950	1910	1900	1970	1950	1910	1900
49	{ or [	54	D054	1A	9A	1A5B	1A7B	1A1B	.....	1A5B	1A7B	1A1B	1A00
50	} or]	5B	F05B	1B	9B	1B5D	1B7D	1B1D	.....	1B5D	1B7D	1B1D	1B00
51	| or \	5D	F05D	2B	AB	2B5C	2B7C	2B1C	.....	2B5C	2B7C	2B1C	2B00
52	Delete	E071	E0F071	E02AE053	E0D3E0AA	5300	5300	.....	.....	53E0	53E0	93E0	A300
53	End	E069	E0F069	E02AE04F	E0CFE0AA	4F00	4F00	7500	.....	4FE0	4FE0	75E0	9F00
54	Page Down	E07A	E0F07A	E02AE051	E0D1E0AA	5100	5100	7600	.....	51E0	51E0	76E0	A100
55	7 or Home	6C	F06C	47	C7	4700	4737	7700	Note[6]	4700	4737	7700	Note[6]
56	8	75	F075	48	C8	4800	4838	....	Note[6]	4800	4838	8D00	Note[6]
57	9 or Page Up	7D	F07D	49	C9	4900	4939	8400	Note[6]	4900	4939	8400	Note[6]

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
58	+	79	F079	4E	CE	4E2B[7]	4E2B[7]	----	----	4E2B[7]	4E2B[7]	9000	4E00[7]
59	Caps Lock	58	F058	3A	BA	Note[7]	Note[7]	----	Note[7]	Note[7]	Note[7]	----	Note[7]
60	A or a	1C	F01C	1E	9E	1E61	1E41	1E01	1E00	1E61	1E41	1E01	1E00
61	S or s	1B	F01B	1F	9F	1F73	1F53	1F13	1F00	1F73	1F53	1F13	1F00
62	D or d	23	F023	20	A0	2064	2044	2004	2000	2064	2044	2004	2000
63	F or f	2B	F02B	21	A1	2166	2146	2106	2100	2166	2146	2106	2100
64	G or g	34	F034	22	A2	2267	2247	2207	2200	2267	2247	2207	2200
65	H or h	33	F033	23	A3	2368	2348	2308	2300	2368	2348	2308	2300
66	J or j	3B	F03B	24	A4	246A	244A	240A	2400	246A	244A	240A	2400
67	K or k	42	F042	25	A5	256B	254B	250B	2500	256B	254B	250B	2500
68	L or l	4B	F04B	26	A6	266C	264C	260C	2600	266C	264C	260C	2600
69	: or ;	4C	F04C	27	A7	273B	273A	----	----	273B	273A	----	2700
70	" or '	52	F052	28	A8	2827	2822	----	----	2827	2822	----	2800
71	Enter	5A	F05A	1C	9C	1C0D	1C0D	1C0A	----	1C0D	1C0D	1C0A	1C00
72	4	6B	F06B	4B	CB	4B00	4B34	7300	Note[6]	4B00	4B34	7300	Note[6]
73	5	73	F073	4C	CC	-----	4C35	---	Note[6]	4C00	4C35	8F00	Note[6]
74	6	74	F074	4D	CD	4D00	4D36	7400	Note[6]	4D00	4D36	7400	Note[6]

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
76	Left Shift	12	F012	2A	AA	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
77	Z or z	1A	F01A	2C	AC	2C7A	2C5A	2C1A	2C00	2C7A	2C5A	2C1A	2C00
78	X or x	22	F022	2D	AD	2D78	2D58	2D18	2000	2D78	2D58	2D18	2000
79	C or c	21	F021	2E	AE	2E63	2E43	2E03	2E00	2E63	2E43	2E03	2E00
80	V or v	2A	F02A	2F	AF	2F76	2F56	2F16	2F00	2F76	2F56	2F16	2F00
81	B or b	32	F032	30	B0	3062	3042	3002	3000	3062	3042	3002	3000
82	N or n	31	F031	31	B1	316E	314E	310E	3100	316E	314E	310E	3100
83	M or m	3A	F03A	32	B2	326D	324D	320D	3200	326D	324D	320D	3200
84	< or ,	41	F041	33	B3	332C	333C	-----	-----	332C	333C	-----	3300
85	> or .	49	F049	34	B4	342E	343E	-----	-----	342E	343E	-----	3400
86	? or /	4A	F04A	35	B5	352F	353F	-----	-----	352F	353F	-----	3500
87	Right Shift	59	F059	36	B6	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
88	Up Arrow	E075	E0F075	E02AE048	E0C8E0AA	4800	4800	-----	----	48E0	48E0	8DE0	9800
89	1 or End	69	F069	4F	CF	4F00	4F31	7500	Note[6]	4F00	4F31	7500	Note[6]
90	2	72	F072	50	D0	5000	5032	----	Note[6]	5000	5032	9100	Note[6]
91	3 or Pg Dn	7A	F07A	51	D1	5100[9]	5133[9]	7600[9]	Note[6][9]	5100[9]	5133[9]	7600[9]	Note[6][9]
92	Left Ctrl	14	F014	1D	9D	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]
93	Left Alt	11	F011	38	B8	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]
94	Space	29	F029	39	B9	3920	3920	3920	3920	3920	3920	3920	3920

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
95	Right Alt	E011	F0F011	E038	F0B8	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]	Note$_9$[10]
96	Right Ctrl	E014	F0F014	E01D	F09D	Note	Note	Note	Note	Note	Note	Note	Note
97	Left Arrow	E06B	F0F06B	E02AE04B	E0CBE0AA	4B00	4B90	7300	.....	4BE0	4BE0	73E0	9B00
98	Down Arrow	E072	F0F072	E02AE050	E0D0E0AA	5000	5000	.....	.....	50E0	50E0	91E0	A000
99	Right Arrow	E074	F0F074	E024E04D	E0CDE0AA	4D00	4000	7400	....	4DE0	4DE0	74E0	9D00
100	0 or Ins	70	F070	52	D2	5200	5230	....	Note[6]	5200	523H	9200	Note[6]
101	. or Del	71	F071	53	D3	5300	532E	....	....	5300	532E	9300	.....
102	Enter	E05A	F0F05A	E01C	E09C	1C0D	1C0D	1C0A	....	E00D	E00D	E00A	A600

NOTES

Note1 —INT 05H is invoked and a screen dump is performed
Note2 —the scroll lock active bit is toggled
Note3 —the pause state is initiated
Note4 —INT 1BH is invoked
Note5 —the numlock active bit is toggled
Note6 —ALT num pad generates raw ascii code of typed number
Note7 —the caps lock active bit is toggled
Note8 —hold shift lock active until key is released
Note9 —hold control shift active until key is released
Note10—hold alternate shift active until key is released

5.0 Protocol

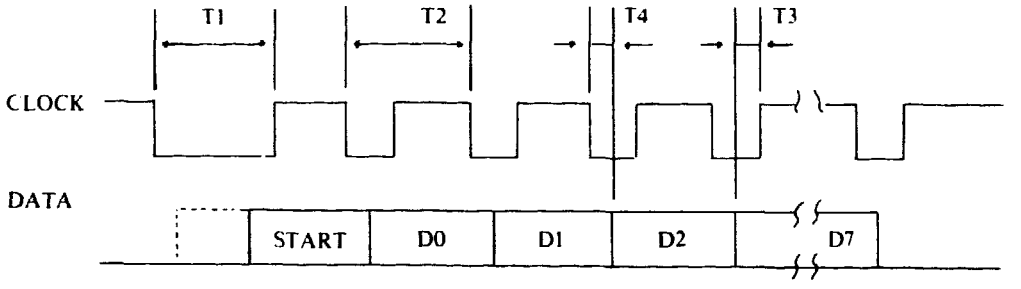
5.0.1 Communication Mode 1 (PC/XT Mode)

The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, no stop bit, and no parity are used to make up the nine bit data word. When no communications are in progress, the keyboard holds the data line low and the clock line high.

Before starting a transmission, the keyboard lowers the clock line as a Request To Send (RTS). The state of the data line is then checked. If the host system is holding the data line low, transmissions are disabled. The keyboard will retain the keycode for the pressed key in its buffer until the clock and data lines return to the idle state. The keyboard then resumes scanning the keyboard matrix until transmissions are enabled.

When transmissions are enabled, 100 to 250 microseconds after the keyboard drives the clock line low, the keyboard transmits its data in the previously described format. Data is valid during the time the clock line is high and for a minimum of 10 microseconds after the falling edge of the clock line. See Figure 2 for a timing diagram.

< KEYBOARD DATA OUTPUT-XT MODE >



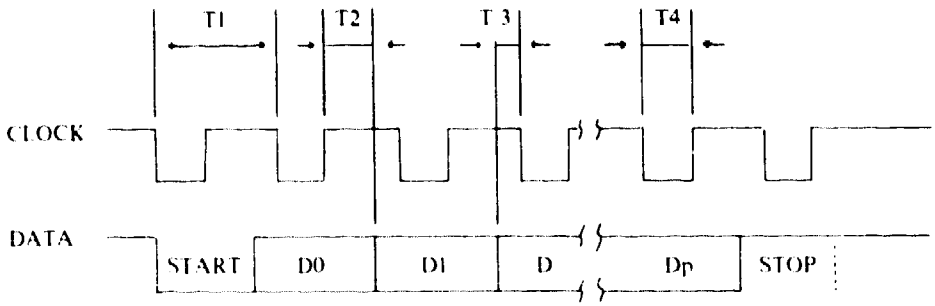
T1 ; 100~ 250μs (CHECKING TIME OF DATA OUTPUT READY OR PROHIBITION)
T2 ; 104μs ± 20%
T3 ; 10μs MIN.
T4 ; 10μs MIN.

FIGURE 2

5.0.2 Communication Mode 2 (AT Mode)

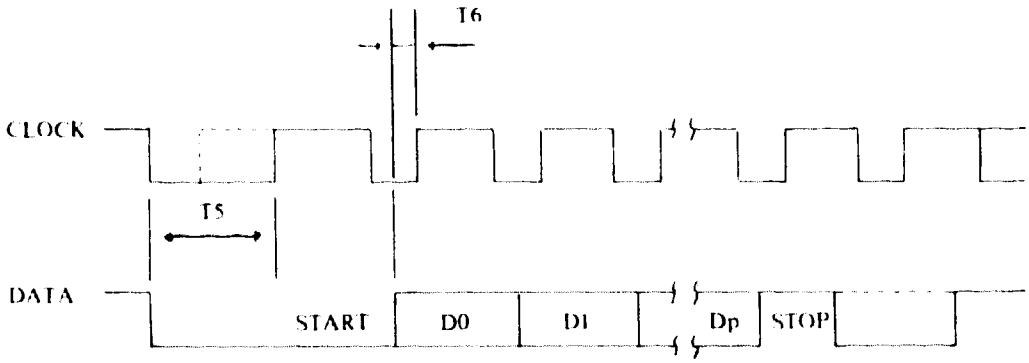
The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, odd parity, and one stop bit form the eleven bit data word. This communication is bi-directional, with the keyboard clocking all data transfers. When no communications are in progress, the data and clock lines are high, indicating an idle state.

< KEYBOARD DATA OUTPUT-AT MODE > Figure 3A



T1 ; 104μs ± 20%
T2 ; 20μs MIN.
T3 ; 20μs MIN.
T4 ; 35μs ± 20%

<KEYBOARD DATA INPUT-AT MODE > Figure 3B



T5 ; 60μs MIN. (WAITING TIME FOR HOST DATA OUTPUT)
T6 ; 5μs MIN.

FIGURE 3

Before starting a transmission, the keyboard checks the status of the clock and data lines. Transmissions are disabled if the clock line is low and the code for the pressed key is held in the keyboard buffer until transmissions are enabled. If the clock line is high and the data line is low, the host system is sending a Request To Send (RTS), and the code for the pressed key is stored in the buffer.

When transmissions are enabled and no RTS is detected from the host system, both clock and data line will be high. The keyboard starts a transmission by sending a low start bit, followed by the rest of the data word. Data is valid 20 microseconds minimum prior to the falling edge of the clock. See Figure 3 for timing diagram.

During the transmission of a data word, the keyboard periodically checks the state of the clock line. If the clock line is low during these checks prior to the rising edge of the parity bit, a data collision occurs. When a data collision occurs, the keyboard stops transmitting, returns the code for the pressed key to the keyboard buffer, and prepares to respond to actions requested by the host system.

5.1 Commands from the Keyboard to the Host System

Keyboard Buffer Overrun — AT and XT Modes

This buffer can store up to sixteen codes for pressed keys. When this buffer is full and the seventeenth code is received, this code is replaced by an Overrun Code. The following chart shows the Overrun Codes for each mode.

XT Mode FF Hex
AT Mode 00 Hex

Codes received after this code are lost until the keyboard clears additional space in the keyboard buffer.

Self Test Passed — AA Hex AT and XT Modes

The keyboard issues this command upon successful completion of the keyboard self test. The self test consists of the following:

XT Mode

1. Memory is cleared.

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2. Keyboard buffer is cleared.

3. ROM checksum is read and compared.

4. RAM is tested.

5. Self test completion code is output.

6. AA Hex is output to indicate successful self test.

7. FC Hex is output to indicate a defect in the self test.

AT Mode

1. ROM checksum is read and compared.

2. RAM is tested.

3. AA Hex is output to indicate successful self test.

4. FC Hex is output to indicate a defect in the self test.

This self test is initiated by the host system reset (Ctrl, Alt, Delete) or by Power-on Reset. Upon successful completion of the Self Test during Power-on Reset, the keyboard is set to XT mode if the keyboard detects a low level on the data line for more than 10 microseconds after 5 microseconds from the falling edge of the clock line. If this condition is not met, the keyboard is placed in the AT Mode, and Typematic Rate and Delay are set to the following defaults:

Typematic Rate 10.9 cps
Delay 500 milliseconds

Echo — EE Hex AT and XT Modes

The Echo Command (EE Hex) is sent in response to an Echo Command from the host system instead of the normal Acknowledge (ACK) for diagnostic purposes.

Acknowledge — FA Hex AT Mode

The keyboard sends an Acknowledge (FA Hex) in response to a valid command from the host system, with the exceptions of the Resend and Echo commands.

Resend — FE Hex AT and XT Modes

The keyboard issues a Resend (FE Hex) in response to inputs which have parity errors, framing errors, or invalid data received from the host system.

Keyboard Buffer Overrun — AT and XT Modes

When the 16-character keyboard buffer receives the 17th character, an overflow condition occurs. This condition is communicated to the host system by transmitting the Keyboard buffer Overrun (FF Hex for XT Mode, 00 Hex for AT Mode) to the host system.

5.2 Commands from the Host System to the Keyboard

Prior to sending commands to the keyboard, the host system must first check to see if the keyboard is sending data. If the keyboard is transmitting, and the data is past the parity bit, the host system must accept the data prior to initiating its own transmission.

If the keyboard's data has not yet reached the tenth clock pulse (Parity Bit), or is not transmitting data, the host system assumes control by lowering the clock line for a minimum of 60 microseconds, then releasing the clock line after clamping the data line low to indicate a start bit. The keyboard will respond with an RTS within 5 microseconds by clocking the start bit into the keyboard. The keyboard continues to clock data as shown in the timing diagram (Figure 3B). The host system must ensure that the data is valid prior to the rising edge and after the falling edge of the keyboard clock pulse.

After the parity bit, the host system should raise the data line to indicate a stop bit. The keyboard checks for a logical high stop bit, then clamps the data line low prior to clock in the stop bit. This signals the host system that the keyboard received the data correctly (Acknowledge). If the host system has not raised the data line to indicate a stop bit, a framing error results and the keyboard continues to clock data until the data line is raised by the host system. Upon receiving either a framing or parity error, the keyboard issues a RESEND to the host system.

All commands from the host system require a response from the keyboard. The keyboard will respond to these commands within 20 microseconds.

The following commands may be sent to the keyboard at any time, following the protocol described for the AT Mode. These commands are valid only in the AT Mode. During the reset command, the keyboard will not respond within 20 microseconds as described above.

Reset — FF Hex

Upon receiving this command, the keyboard transmits an Acknowledge to the host system. The keyboard then waits for the host system to accept the Acknowledge response. The host system will accept the Acknowledge by raising the clock and data lines for a minimum of 500 microseconds.

The keyboard then executes the self test routine similar to the Power-On Reset, and is placed in its default state.

Resend — FE Hex

Upon receiving this command, the keyboard will transmit the last byte of data sent to the host system.

Set Default — F6 Hex

This command resets the keyboard to the Power-Up default state. The keyboard responds with an Acknowledge, clears the output buffer, sets the scanset to AT Mode, sets the default typematic rate and delay, and continues to scan the matrix.

Default Disable — F5 Hex

This command is similar to the Set Default command, except the keyboard stops scanning the matrix and waits for further instructions to be sent by the host system.

Enable — F4 Hex

Upon receipt of this command the keyboard responds with an Acknowledge, clears the output buffer, and starts scanning the matrix.

Set Typematic Rate/Delay — F3 Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter

byte, the keyboard sends an Acknowledge, sets the typematic rate and delay as indicated in Table 2, and continues scanning the matrix.

If another command is received instead of the parameter byte, the set typematic rate/delay function ends with no change to the existing rate or delay parameters. The new command is processed and the keyboard continues scanning the matrix.

The parameter byte consists of an eight-bit word with Bit 7 (most significant bit) always being set. Bits 0-4 set the typematic rate and Bits 5-6 set the delay.

Example

```
1 0 1 0 1 0 1 1 Parameter Byte
7 6 5 4 3 2 1 0 Bit Number
```

The above example shows the default 10.9 cps typematic rate and 500 microsecond delay. Bits 0-4 (010111) correspond to the rate of 10.9 cps shown on Table 2 ii and Bits 5-6 (01) correspond to the 500 microsecond delay shown in Table 2 i.

See Table 2 for Typematic Rate/Delay values other than the default settings.

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i) Delay

Bit 6 5	Delay ms
0 0	250
0 1	500
1 0	750
1 0	1000

ii) Rate

Bit 4	3	2	1	0	Rate (CPS)
0	0	0	0	0	30.0
0	0	0	0	1	26.7
0	0	0	1	0	24.0
0	0	0	1	1	21.8
0	0	1	0	0	20.0
0	0	1	0	1	18.5
0	0	1	1	0	17.1
0	0	1	1	1	16.0
0	1	0	0	0	15.0
0	1	0	0	1	13.3
0	1	0	1	0	12.0
0	1	0	1	1	10.9
0	1	1	0	0	10.0
0	1	1	0	1	9.2
0	1	1	1	0	8.6
0	1	1	1	1	8.0

Bit 4	3	2	1	0	Rate (CPS)
1	0	0	0	0	7.5
1	0	0	0	1	6.7
1	0	0	1	0	6.0
1	0	0	1	1	5.5
1	0	1	0	0	5.0
1	0	1	0	1	4.6
1	0	1	1	0	4.3
1	0	1	1	1	4.0
1	1	0	0	0	3.7
1	1	0	0	1	3.3
1	1	0	1	0	3.0
1	1	0	1	1	2.7
1	1	1	0	0	2.5
1	1	1	0	1	2.3
1	1	1	1	0	2.1
1	1	1	1	1	2.0

TABLE 2

Echo — FE Hex

This command is provided for diagnostic purposes. The keyboard shall respond with EE Hex, instead of Acknowledge, and continue scanning the matrix.

Set/Reset Status Indicators — ED Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter byte, the keyboard sends an Acknowledge, sets the status indicators, and starts scanning the matrix.

If another command is received instead of the parameter byte, the keyboard disregards the Set/Reset Status Indicators command without changing the present status of the indicators, processes the new command, and starts scanning the matrix.

The parameter byte is an eight-bit word with Bits 3-7 always set to low. Bit 0 is the Scroll Lock Indicator, Bit 1 is the Num Lock Indicator, and Bit 2 is the Caps Lock Indicator. A high in each individual bit indicates that Indicator is active and the indicator lamp should be on.

Example

```
0 0 0 0 0 0 1 0 Parameter Byte
7 6 5 4 3 2 1 0 Bit Number
```

The above example shows the power-on default of the parameter byte. Bit 1 is high indicating Num Lock is active and the Num Lock indicator lamp is on.

Read Keyboard ID — F2 Hex

This command causes the keyboard to return two identification bytes AB83 Hex. The keyboard responds with an Acknowledge to the command and stops scanning the matrix. The keyboard then transmits the keyboard ID AB83 Hex and resumes scanning the matrix.

Set/Read Scan Set — F0 Hex

This command is used to select one of three Scan Sets or to tell the host system which Scan Set is currently being used. This command consists

of a command byte and a parameter byte. Upon receiving this command, the keyboard sends an Acknowledge to the host system and waits for the parameter byte. When the keyboard receives the parameter byte, it responds with an Acknowledge.

A parameter byte of 00 Hex will cause the keyboard to transmit the Hex value for the Scan Set currently in use. A parameter byte of 01 Hex selects the Scan Set 1 (XT Scan Codes), 02 Hex selects Scan Set 2 (Default AT Scan Codes), and 03 Hex selects Scan Set 3 (Special AT Scan Codes — See Table 3 for Scan Codes and Default Key State Information). The keyboard resumes scanning the matrix.

Table 3

Key Description	Make Code	Break Code	Default Key State
Esc	08	F0 08	Make Only
F1	07	F0 07	Make Only
F2	0F	F0 0F	Make Only
F3	17	F0 17	Make Only
F4	1F	F0 1F	Make Only
F5	27	F0 27	Make Only
F6	2F	F0 2F	Make Only
F7	37	F0 37	Make Only
F8	3F	F0 3F	Make Only
F9	47	F0 47	Make Only
F10	4F	F0 4F	Make Only
F11	56	F0 56	Make Only
F12	5E	F0 5E	Make Only
Print Scrn	57	F0 57	Make Only
Scroll Lock	5F	F0 5F	Make Only
Pause or Break	62	F0 62	Make Only
`	0E	F0 0E	Typematic
1	16	F0 16	Typematic
2	1E	F0 1E	Typematic
3	26	F0 26	Typematic
4	25	F0 25	Typematic
5	2E	F0 2E	Typematic
6	36	F0 36	Typematic
7	3D	F0 3D	Typematic
8	3E	F0 3E	Typematic
9	46	F0 46	Typematic
0	45	F0 45	Typematic
-	4E	F0 4E	Typematic

Key Description	Make Code	Break Code	Default Key State
=	55	F0 55	Typematic
Backspace	66	F0 66	Make Only
Insert cursor pad	67	F0 67	Make Only
Home cursor pad	6E	F0 6E	Make Only
Page Up cursor pad	6F	F0 6F	Make Only
Num Lock	76	F0 76	Make Only
/ number pad	77	F0 77	Make Only
* number pad	7E	F0 7E	Make Only
- number pad	84	F0 84	Make Only
Tab	0D	F0 0D	Typematic
q	15	F0 15	Typematic
w	1D	F0 1D	Typematic
e	24	F0 24	Typematic
r	2D	F0 2D	Typematic
t	2C	F0 2C	Typematic
y	35	F0 35	Typematic
u	3C	F0 3C	Typematic
i	43	F0 43	Typematic
o	44	F0 44	Typematic
p	4D	F0 4D	Typematic
[	54	F0 54	Typematic
]	5B	F0 5B	Typematic
\	5C	F0 5C	Typematic
Delete cursor pad	64	F0 64	Typematic
Home cursor pad	65	F0 65	Make Only
Page Up cursor pad	6D	F0 6D	Make Only
7 number pad	6C	F0 6C	Make Only
8 number pad	75	F0 75	Make Only
9 number pad	7D	F0 7D	Make Only
+ number pad	7C	F0 7C	Make Only
Caps Lock	14	F0 14	Make/Break
a	1C	F0 1C	Typematic
s	1B	F0 1B	Typematic
d	23	F0 23	Typematic
f	2B	F0 2B	Typematic
g	34	F0 34	Typematic
h	33	F0 33	Typematic
j	3B	F0 3B	Typematic
k	42	F0 42	Typematic
l	4B	F0 4B	Typematic
;	4C	F0 4C	Typematic
'	52	F0 52	Typematic

Key Description	Make Code	Break Code	Default Key State
Enter	5A	F0 5A	Typematic
4 number pad	6B	F0 6B	Make Only
5 number pad	73	F0 73	Make Only
6 number pad	74	F0 74	Make Only
Left Shift	12	F0 12	Make/Break
z	1A	F0 1A	Typematic
x	22	F0 22	Typematic
c	21	F0 21	Typematic
v	2A	F0 2A	Typematic
b	32	F0 32	Typematic
n	31	F0 31	Typematic
m	3A	F0 3A	Typematic
,	41	F0 41	Typematic
.	49	F0 49	Typematic
Right Shift	59	F0 59	Make/Break
Up Arrow cursor pad	63	F0 63	Typematic
1 number pad	69	F0 69	Make Only
2 number pad	72	F0 72	Make Only
3 number pad	7A	F0 7A	Make Only
Enter number pad	79	F0 79	Make Only
Left Ctrl	11	F0 11	Make/Break
Left Alt	19	F0 19	Make/Break
Spacebar	29	F0 29	Typematic
Right Alt	39	F0 39	Make Only
Right Ctrl	58	F0 58	Make Only
Left Arrow cursor	61	F0 61	Typematic
Down Arrow	60	F0 60	Typematic
Right Arrow	6A	F0 6A	Typematic
Ins number pad	70	F0 70	Make Only
Del number pad	71	F0 71	Make Only

Set All Keys — Typematic — F7 Hex

Set All Keys — Make/Break — F8 Hex

Set All Keys — Make Only — F9 Hex

Set All Keys — Typematic/Make/Break — FA Hex

These commands affect Scan Set 3 only, but may be sent using any Scan Set. The keyboard responds with an Acknowledge, clears the output buffer, sets all keys to the function requested by the command, and continues scanning the matrix if it was previously enabled.

Set Single Key — Typematic — FB Hex

Set Single Key — Make/Break — FC Hex

Set Single Key — Make Only — FD Hex

These commands consist of a command byte and a parameter byte. The keyboard responds to the command byte with an Acknowledge and waits for the parameter byte. The parameter byte is the scan code from Scan Set 3 for the key to be changed. Upon receiving the parameter byte, the keyboard sets the selected key to the function selected by the command byte, and continues to scan the matrix if it was previously enabled. These commands affect only Scan Set 3 operation, but may be sent using any Scan Set.

5.3 Key Rollover

The keyboard incorporates N-Key Rollover in software to avoid loss of keystroke data during high speed entry. N-Key Rollover is defined as all keys pressed and released will be output in the proper sequence. However, when the keyboard detects more than four keys pressed during a scan of the matrix, the keyboard does not output the keycodes until one or more of the keys are released. If the released key was not properly detected as a pressed key, an error condition occurs and the keyboard issues an buffer overrun code to the host system.

5.4 Autorepeat

The power-on default condition will cause the last key pressed to repeat at 10.9 characters-per-second after a 500 millisecond delay. This may

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be changed by the system when the keyboard is using the AT Communications Mode.

5.5 Buffering

The keyboard is capable of storing 16 scan codes in a first in/ first out (FIFO) circular buffer. When the buffer overflows, the last code is replaced by a Hex 00, in AT Mode and a Hex FF, in XT Mode.

5.6 Status Indicators

Three LED Status Indicators are provided: Num Lock, Caps Lock, and Scroll Lock.

These indicators are located in the keytop of each respective key. The keyboard will power up with all indicators OFF, except when the host system sets them to ON.

5.7 Internal Clock

A 6 MHz oscillator is provided for timing needed by the keyboards internal circuitry. This oscillator feeds an internal on chip oscillator embedded within the keyboard's 8051 processor. This in turn provides the keyboard clock needed for communication with the system.

6.0 Electrical Requirements

The interface consists of two bi-directional lines, clock and data, which are controlled by 74LS125 equivalent buffers. The keyboard side is terminated by 2200 Ohm resistors. All voltage levels are TTL compatible and the keyboard drivers are capable of sinking 20 mA minimum including the current sourced by the pullup resistors on the keyboard.

6.1 Connector

The connector is a 5-pin DIN connector. Connections are shown in the following table.

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Table 4

Pin #	Signal
1	Clock
2	Data
3	No Connection
4	Logic Ground
5	+5 Volts DC

6.2 Chassis Ground

Chassis ground is isolated from logic ground.

6.3 Power Requirements

The keyboard requires 5 Volts DC, +/-5%, at 500 milliamps (max).

7.0 Environmental Requirements

7.1 Temperature

Operating	0 to 50 degrees C
Non-Operating	–20 to 60 degrees C

7.2 Relative Humidity

20% to 90% non-condensing

7.3 Shock

Operating and non-operating	10G	11 mS duration

7.4 Vibration

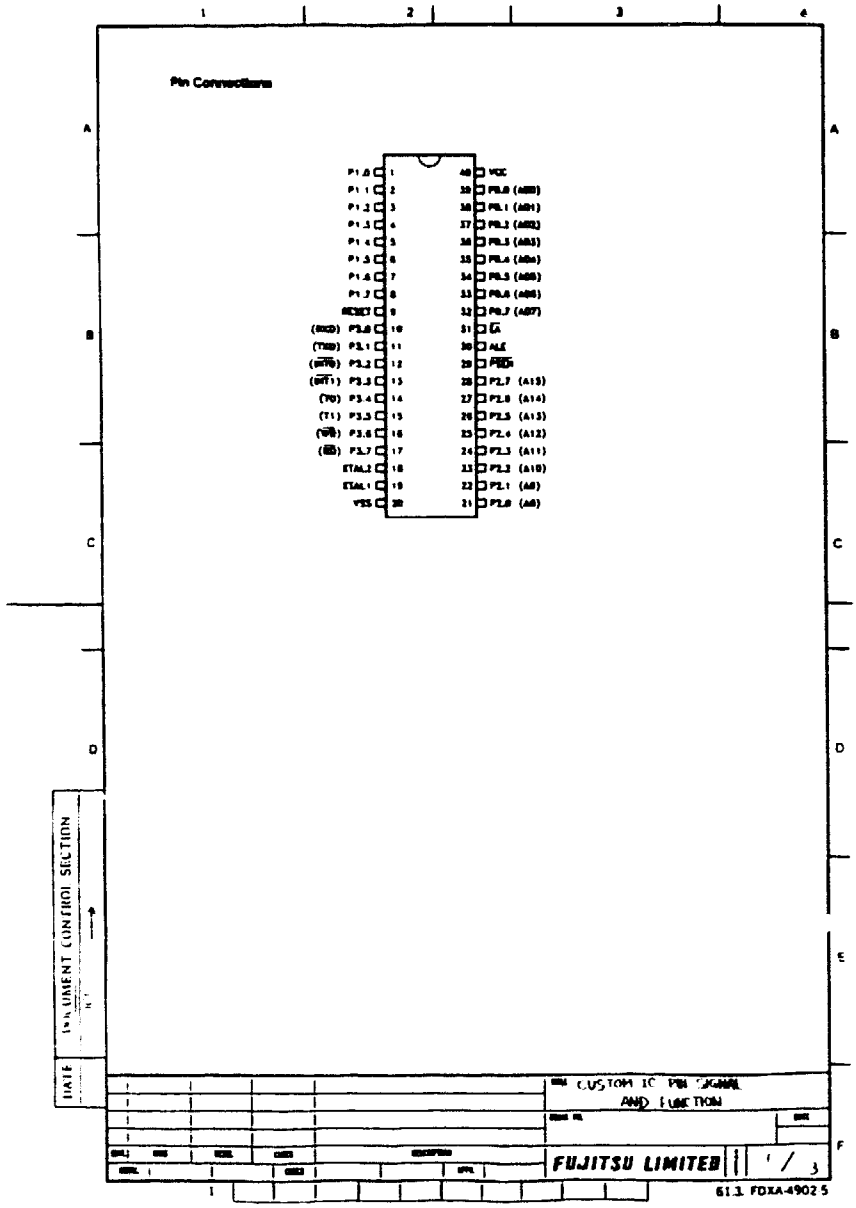
Operating and non-operating	0.3 mm amplitude 10 to 55 Hz

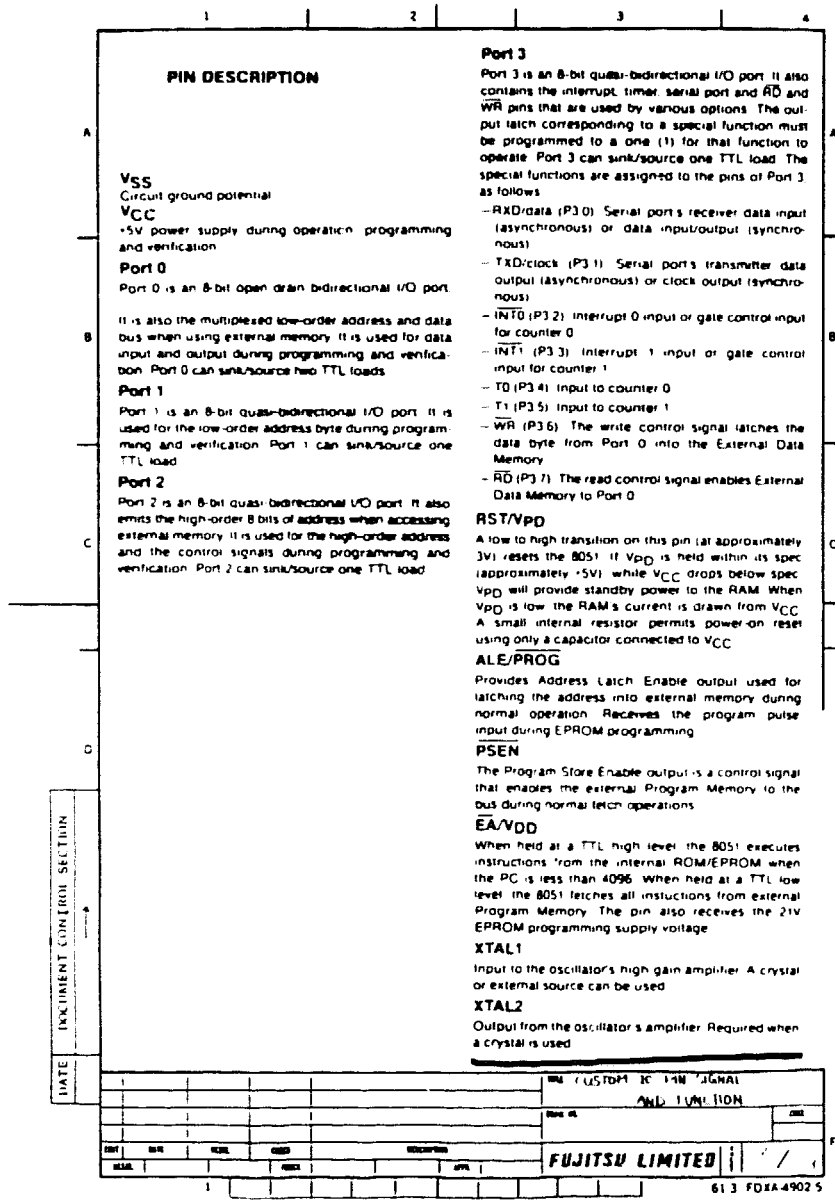
8.0 Reliability

8.1 Switch life

Switch life of the keyboard is a minimum of 20 million cycles.

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Pin Connections
FUJITSU LIMITED
61.3 FDXA-4902 5



PIN DESCRIPTION

V_{SS}
Circuit ground potential

V_{CC}
+5V power supply during operation programming and verification

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port

It is also the multiplexed low-order address and data bus when using external memory It is used for data input and output during programming and verification Port 0 can sink/source two TTL loads

Port 1

Port 1 is an 8-bit quasi-bidirectional I/O port It is used for the low-order address byte during programming and verification Port 1 can sink/source one TTL load

Port 2

Port 2 is an 8-bit quasi-bidirectional I/O port It also emits the high-order 8 bits of address when accessing external memory It is used for the high-order address and the control signals during programming and verification Port 2 can sink/source one TTL load

Port 3

Port 3 is an 8-bit quasi-bidirectional I/O port It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options The output latch corresponding to a special function must be programmed to a one (1) for that function to operate Port 3 can sink/source one TTL load The special functions are assigned to the pins of Port 3 as follows

- RXD/data (P3.0) Serial port's receiver data input (asynchronous) or data input/output (synchronous)
- TXD/clock (P3.1) Serial port's transmitter data output (asynchronous) or clock output (synchronous)
- $\overline{INT0}$ (P3.2) Interrupt 0 input or gate control input for counter 0
- $\overline{INT1}$ (P3.3) Interrupt 1 input or gate control input for counter 1
- T0 (P3.4) Input to counter 0
- T1 (P3.5) Input to counter 1
- $\overline{WR}$ (P3.6) The write control signal latches the data byte from Port 0 into the External Data Memory
- $\overline{RD}$ (P3.7) The read control signal enables External Data Memory to Port 0

RST/V_{PD}

A low to high transition on this pin (at approximately 3V) resets the 8051 If V_{PD} is held within its spec (approximately +5V) while V_{CC} drops below spec V_{PD} will provide standby power to the RAM When V_{PD} is low the RAM's current is drawn from V_{CC} A small internal resistor permits power-on reset using only a capacitor connected to V_{CC}

ALE/$\overline{PROG}$

Provides Address Latch Enable output used for latching the address into external memory during normal operation Receives the program pulse input during EPROM programming

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during normal fetch operations

$\overline{EA}$/V_{DD}

When held at a TTL high level the 8051 executes instructions from the internal ROM/EPROM when the PC is less than 4096 When held at a TTL low level the 8051 fetches all instructions from external Program Memory The pin also receives the 21V EPROM programming supply voltage

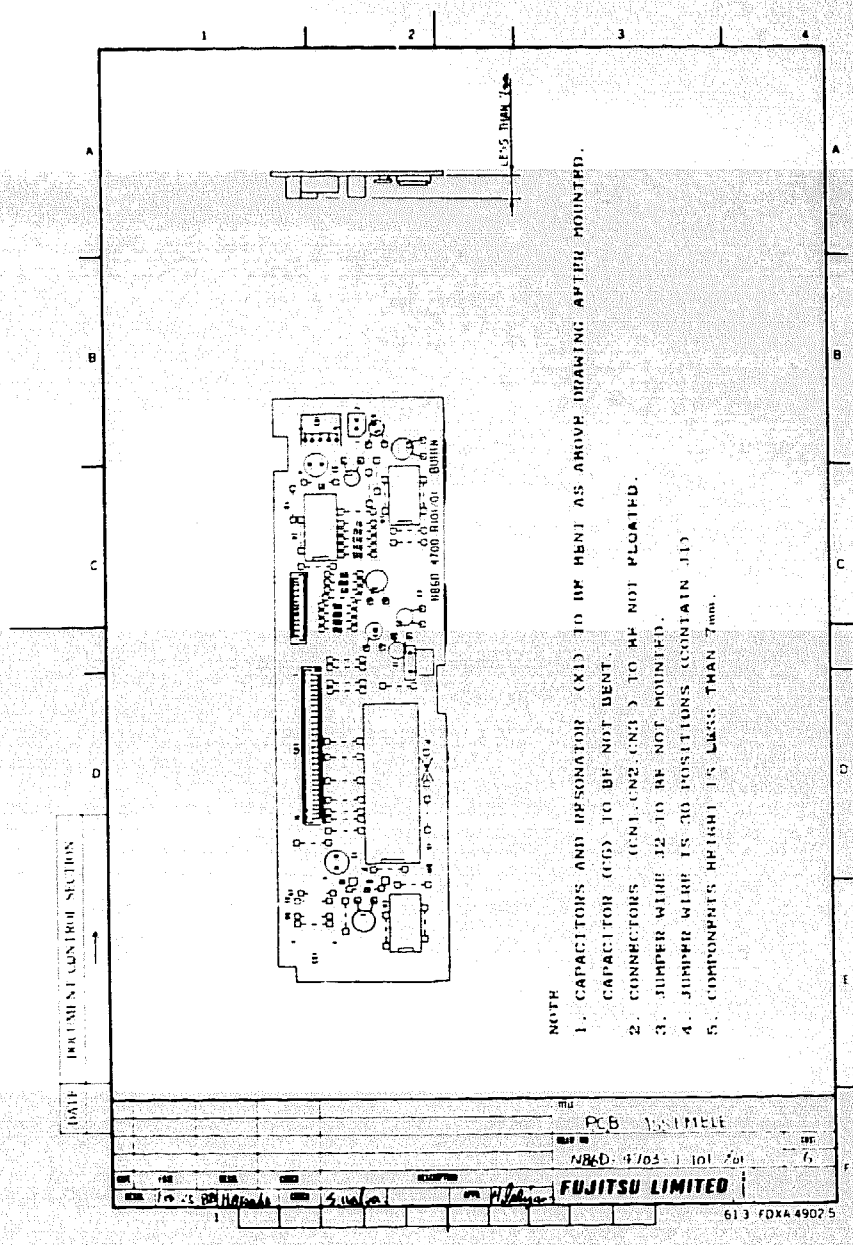
XTAL1

Input to the oscillator's high gain amplifier A crystal or external source can be used

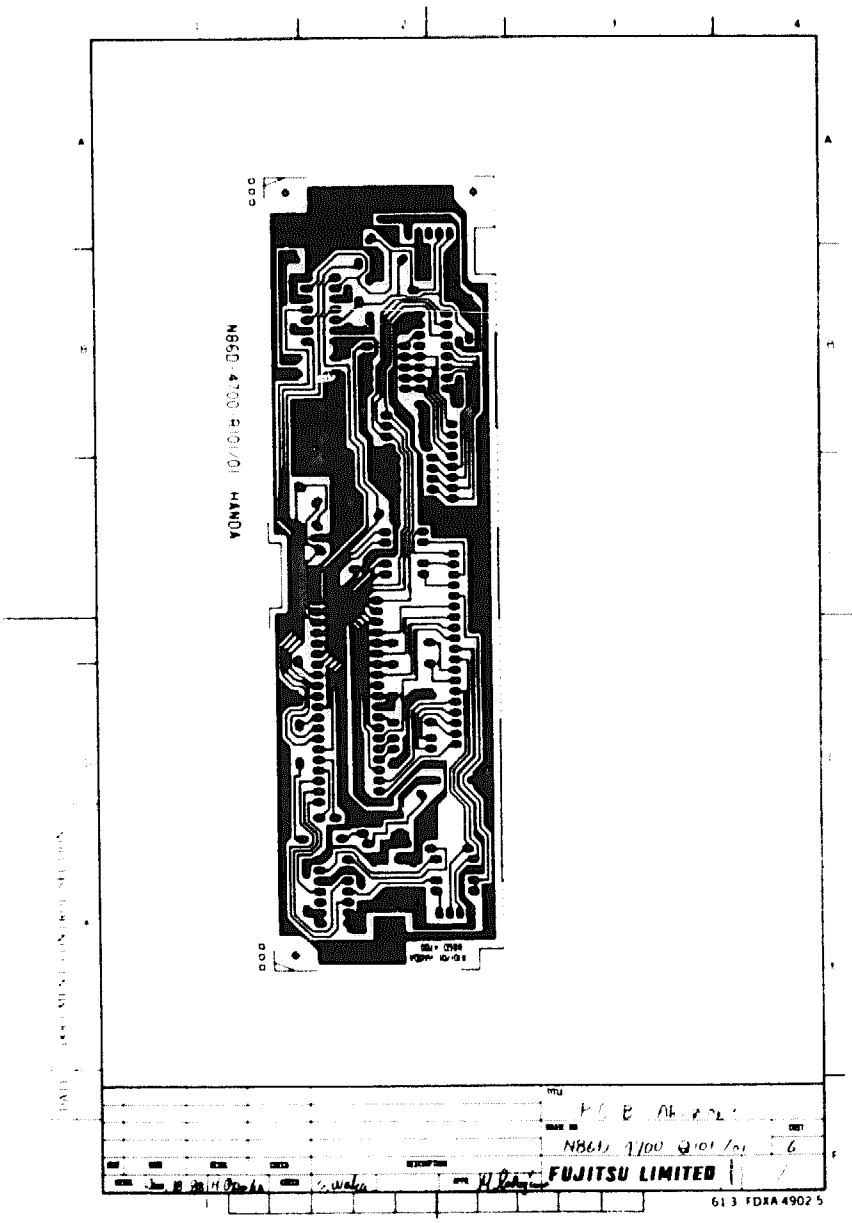
XTAL2

Output from the oscillator's amplifier Required when a crystal is used

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NOTE
1. CAPACITORS AND RESONATOR (X1) TO BE HAND AS ABOVE DRAWING AFTER MOUNTED.
CAPACITOR (C6) TO BE NOT BENT
2. CONNECTORS (CN1,CN2,CN3) TO BE NOT MOUNTED.
3. JUMPER WIRE J2 TO BE NOT MOUNTED.
4. JUMPER WIRE IS 30 POSITIONS (CONTAIN J1)
5. COMPONENTS HEIGHT IS LESS THAN 7mm.
LESS THAN 7mm
INSTRUMENT CONTROL SECTION
PCB ASSEMBLE
FUJITSU LIMITED
613 FDXA 4902 5

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FUJITSU LIMITED


DISK DRIVE

Specifications

of

MP-F73W-70D

Double Sided 80 Tracks
Recording Capacity 2MBytes
Transfer Rate 500 Kbits/sec at 2MB mode
250 Kbits/sec at 1MB mode

VALID for MP-F73W-70D,
with the following serial numbers :

30,000,001			

SONY CORPORATION

MFD TECHNICAL INFORMATION 00-0060 REV. 11-87 July 28, '87

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1. Introduction

This document describes the specifications of the MP-F73W-70D which has the capability to read and write up to 2MB data (unformatted) on a HD disk as well as read and write up to 1MB (unformatted) data on a 1MB disk. The main features of the MP-F73W-70D are: low power consumption, low height, and high reliability with a simple mechanism and electric circuit.

This drive maintains the 300rpm of the disk motor rotational speed constantly, therefore,

a. When a 2MB disk is inserted into the MP-F73W-70D, both read and write operations can be carried out and the data transfer rate is 500 kbits/sec.
b. When a 1MB disk (proposed ANSI standard) is inserted into the MP-F73W-70D, the data transfer rate becomes 250 kbits/second.

2. Specifications

2.1 Configuration

The drive consists of Read/Write heads, head positioning mechanism, disk motor, interface logic circuit and Read/Write circuit.

2.2 Physical Dimensions

The detailed physical dimensions are shown in Figure 2.1.
The main dimensions are:

1) Height : 30 mm (1.18 in.)
2) Width : 101.6 mm (4.00 in.)
3) Depth : 150 mm (5.91 in.)
4) Weight : 480g (1.06 pounds) max.

2.3 Performance

2.3.1 Recording Capacity (unformatted, MFM)

2MB mode	1MB mode
2.0 Mbytes/disk	1.0 Mbytes / disk
1.0 Mbytes/surface	0.5 Mbytes / surface
12.5 Kbytes/track	6.25 Kbytes / track

2.3.2 Transfer Rate

Burst transfer rate : 500 Kbits/sec for MFM in a 2MB mode
250 Kbits/sec for MFM in a 1MB mode

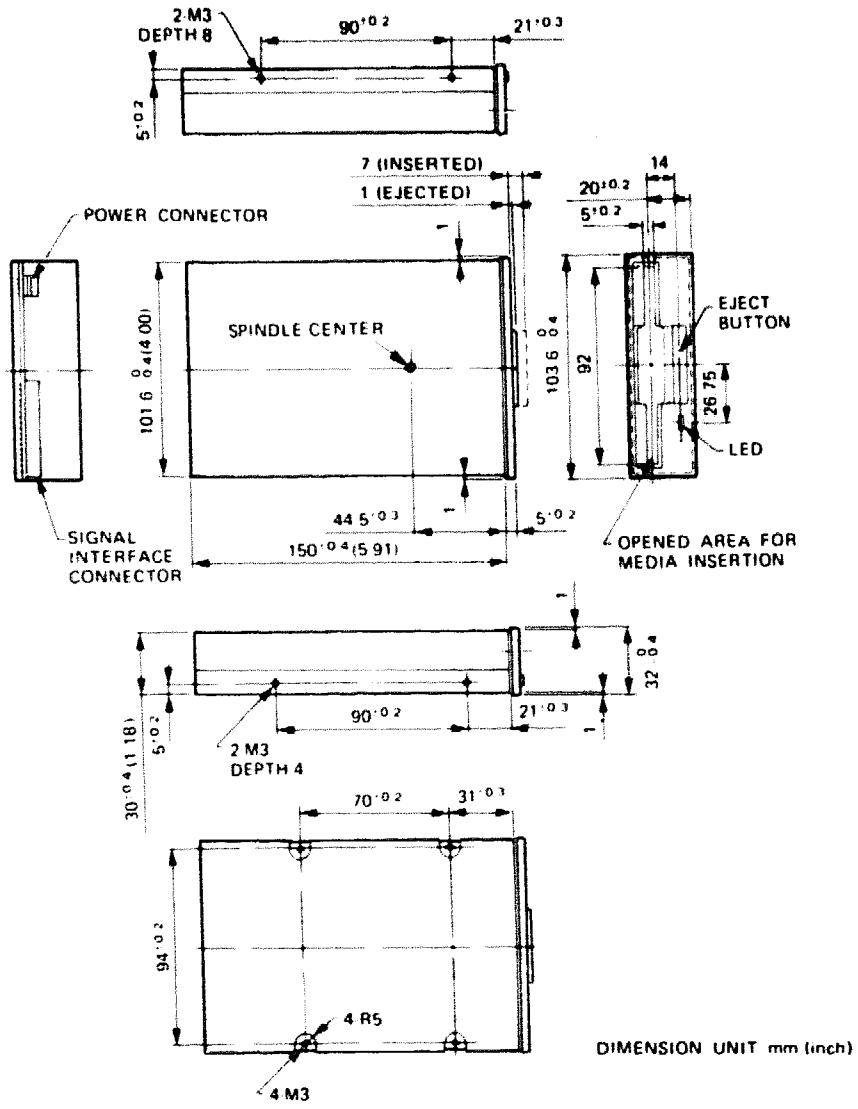


Fig. 2.1 Physical Dimensions

2.3.3 Access Time

a. Track to Track Slew Rate : 3 msec max.

b. Head Settling Time : 15 msec max.

The value of 15msec is the time necessary to stabilize the head within 0.035mm of its absolute position.

c. Motor Start Time : 500 msec max.
(700 msec max.*)

Motor start time is defined as the time period necessary to stabilise the Motor Rotational Speed variance to less than +/-1.5% after turning the MOTOR ON signal on.

NB. When a disk is inserted in the drive, the Motor Start Time will be 700 msec at maximum, but, after that it will be 500 msec max. as long as the disk is kept inserted.

2.3.4 Functional

a. Rotation Speed : 300 rpm
The continuous speed variation is within +/-1.5%.
The instantanuous speed variation is within +/-1.5%.

b. Recording Density : 17434 BPI (Side 1, Track 79) in a 2MB mode.
8717 BPI (Side 1, Track 79) in a 1MB mode.

c. Track Density : 135 TPI

d. Cylinders : 80

e. Tracks : 160

f. R/W Heads : 2

2.3.5 Reliability

a. Mean Time Between Failures (MTBF) : 10,000 POH

b. Mean Time to Repair (MTTR) : 30 minutes

c. Preventive Maintenance (PM) : Not Required

d. Components life : 5 years or 15000 POH

e. Error Rate :

1. Soft Read Error : Less than 1 per 10^9 bits read

2. Hard Read Error : Less than 1 per 10^{12} bits read

3. Seek Error : Less than 1 per 10^6 seeks

2.4 Input Power Requirements

2.4.1 Power Consumption

	TTL Interface
Standby	255 mW
Operation (read/write mode)	2.8 W

2.4.2 Supply Voltages

Voltage	Max. Ripple	Current
+12.0V +/-5%	0.1Vpp	Standby 0.3 mA Average 130 mA (Read) Peak 500 mA (Motor Start) Peak 450 mA (stepping during Motor On)
+5.0V +/-5%	0.1Vpp	Standby 50 mA Operating 240 mA

2.5 Environmental Limits

2.5.1 Temperature Range

Operating : 5°C to 50°C ambient (40°F to 122°F)

Transportation : -40°C to 60°C (-40°F to 140°F)

Storage : -20°C to 60°C (-20°F to 140°F)

2.5.2 Humidity Range

Operating : 8% to 80% relative humidity with a wet bulb temperature of 29°C (85F) and no condensation.

Transportation and Storage : 5% to 95% relative humidity and no condensation

2.5.3 Vibration

Operating : The unit can perform Read/Write operations without an error rate beyond that specified while withstanding continuous vibrations at a frequency of 10 to 500 Hz with an acceleration of no more than 0.5G along each of the three mutually perpendicular axes.

Transportation and Storage : The unit can withstand continuous vibrations from 10 to 300 Hz with a maximum acceleration of 2.0G along each of the three mutually perpendicular axes without any degradation of any characteristics below the performance specifications.

2.5.4 Shock

Operating : The unit can withstand a 5.0G shock for 11 msec with a 1/2 sine wave shape in each of the three mutually perpendicular axes while performing normal Read/Write functions without damage or any loss of data.

Transportation and Storage : The unit when unpacked can withstand an 11 msec with a 1/2 sine wave shock of 60G on any of the three mutually perpendicular axes.

2.5.5 Orientation

The drive does not necessarily need to be horizontally positioned. In fact, as seen in figure 2-3, there are many other possible orientations.

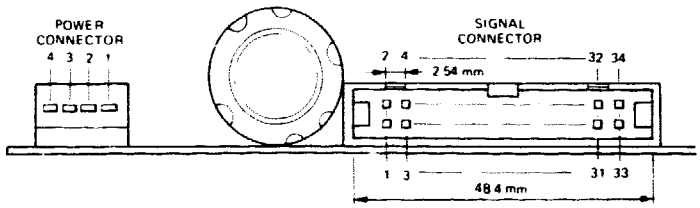
3. Signal Interface

3.1 Connector and Pin Assignments

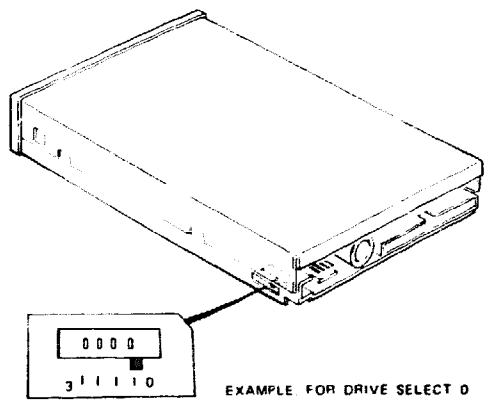
3.1.1 Signal connector

Receptacle : 3M 3414-6500xx or Equivalent

Cable : 3M 3365/34 or Equivalent



PIN ASSIGNMENT (REAR VIEW OF DRIVE)



EXAMPLE FOR DRIVE SELECT 0

DRIVE SELECT SWITCH

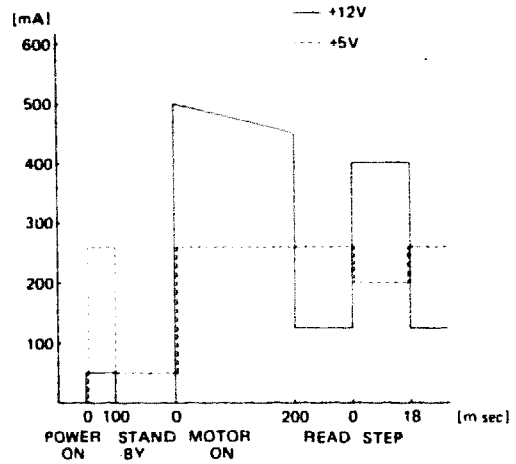


Fig. 2.2 DC Current Profile(typical)

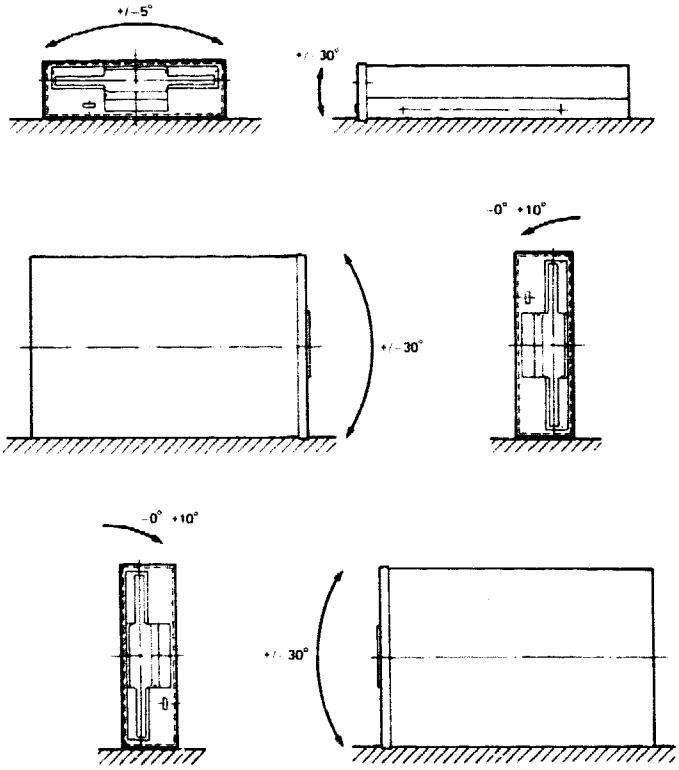


Fig. 2.3 Orientations

3.1.2 Signal Connector Pin Assignment

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	N.C.	2	N.C.
3	+5V	4	N.C.
5	+5V	6	DRIVE SELECT 3
7	+5V	8	INDEX
9	+5V	10	DRIVE SELECT 0
11	+5V	12	DRIVE SELECT 1
13	RETURN	14	DRIVE SELECT 2
15	RETURN	16	MOTOR ON
17	RETURN	18	DIRECTION
19	RETURN	20	STEP
21	RETURN	22	WRITE DATA
23	RETURN	24	WRITE GATE
25	RETURN	26	TRACK 00
27	RETURN	28	WRITE PROTECT
29	+12V	30	READ DATA
31	+12V	32	HEAD SELECT
33	+12V	34	DISK CHANGE

3.1.3 Power Supply Connector

Receptacle : AMP 171822-4 or Equivalent

Contact : AMP 170262-1 or Equivalent

Wire : AWG 20

3.1.4 Power Supply Connector Pin Assignment

PIN	SIGNAL DESCRIPTION
1	+5V
2	GND (+5V Return)
3	GND (+12V Return)
4	+12V

3.2 DC Characteristics of Interface Signals

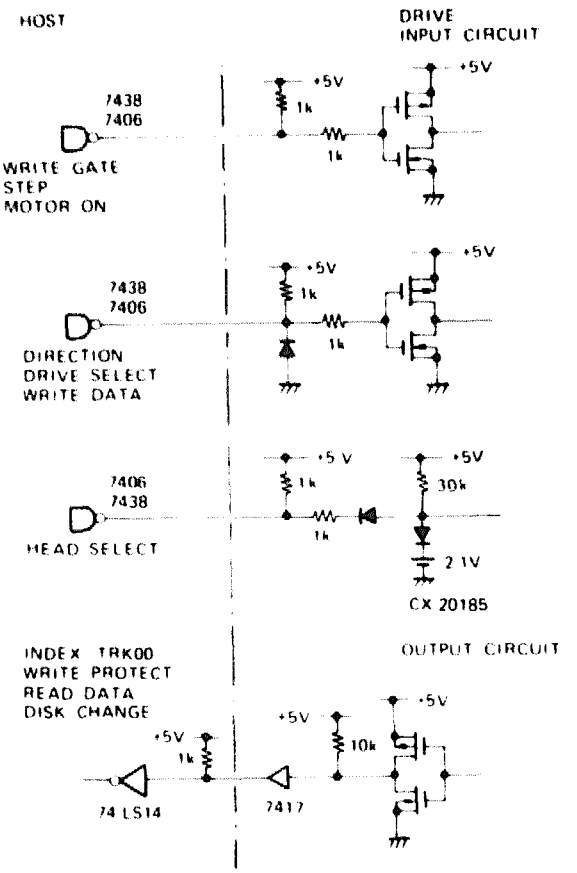
3.2.1 Output Signal from Drive

Name	Output Current IOH(mA)	IOL(mA)	Output Voltage VOH(V)	VOL(V)
TTL interface All outputs	0.25	40		0.7

3.2.2 Input Signal to Drive

Name	Input Current VIN=0.4V IIL(mA)	Input Voltage Threshold VIH(V)	VIL(V)
TTL interface All inputs	-5.0	2.2	0.8

3.2.3 Recommended Circuit for Signal Interface



1 K ohm pull-up resister is recommended to be implemented on the output line from the drive.

The cable length must be less than 1.5m.

Recommended driver IC : 7406, 7438

3.3 Signal Definitions

3.3.1 DRIVE SELECT 0,1,2,3

The SELECT lines are used to enable or disable all other interface lines except a MOTOR ON line. When the SELECT line is true (low), the drive is enabled and considered active. When the SELECT line is false (high), all controller inputs except the MOTOR ON line are ignored and all output lines are disabled.

NB. IN USE (LED) LAMP:
When a drive is selected, the IN USE lamp on the selected drive is turned on, and when a drive is not selected, it is turned off.

3.3.2 MOTOR ON

When this input is true (low) and a disk is inserted, the spindle motor starts to run. When this line is made false (high) or a disk is ejected, the spindle motor decelerates and stop.

However, if the MOTOR ON signal becomes false(high) during either a write or erase operation, the disk motor does not stop rotating until both the ERASE GATE signal and the WRITE GATE signal become high (false).

3.3.3 STEP

When a drive is selected, a true (low) pulse on this line causes the Read/Write head to move to the adjacent track. The direction of the head movement is determined by the status of the DIRECTION input at the trailing edge of the pulse.
The step operation can be performed even if there is no disk inserted in the drive.

3.3.4 DIRECTION

When a drive is selected, a false (high) level on this input causes a STEP input to move the Read/Write head away from the disk spindle. A true (low) level causes a STEP pulse input to move the Read/Write head toward the drive spindle.

3.3.5 HEAD SELECT

When a drive is selected, a true (low) level on this input causes Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected.

If the HEAD SELECT signal changes during either write or erase operation, the head will not be changed until both ERASE GATE and WRITE GATE signal becomes high (false).

3.3.6 WRITE GATE

When this line is made true (low) while a drive is selected, the write current circuits are enabled and information may be written under control of the WRITE DATA input.

3.3.7 WRITE DATA

If the WRITE GATE is true (low), a true pulse (low) on the WRITE DATA line signal causes a bit to be written on the disk. Pulses on this line is neglected when WRITE GATE signal is false (high). No pre-compensation is required.

3.3.8 INDEX

When the drive is selected, a true (low) pulse is generated on this line by each revolution of the spindle.

3.3.9 TRACK 00

This line is true (low) when the drive is selected and the Read/Write head is positioned on track 00.

3.3.10 WRITE PROTECT

If a write-protect disk is inserted while a drive is selected, this line becomes true (low) and the drive is not able to write data. At all other times, except when a disk is ejected while the drive is selected, this line becomes false (high).

3.3.11 READ DATA

When the drive is selected, a true (low) pulse is generated on this line every time a bit is detected.

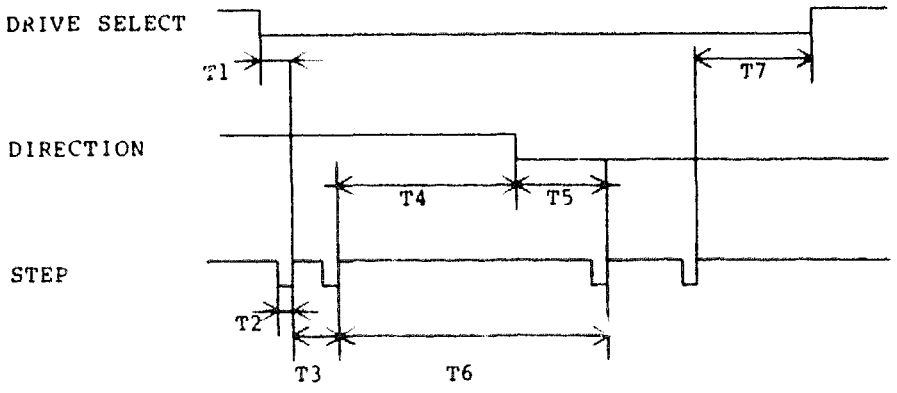
3.3.12 DISK CHANGE

This line is true (low) whenever a disk is removed from the drive. The line will remain true (low) until both the following conditions have been met:

1. A disk is inserted,
and
2. A STEP pulse has been received when the drive is selected.

3.4 Timing Requirements

3.4.1 Head Access



T1 : 0.5 us min.

T2 : 1.3 us min.

T3 : 3.0 ms min.

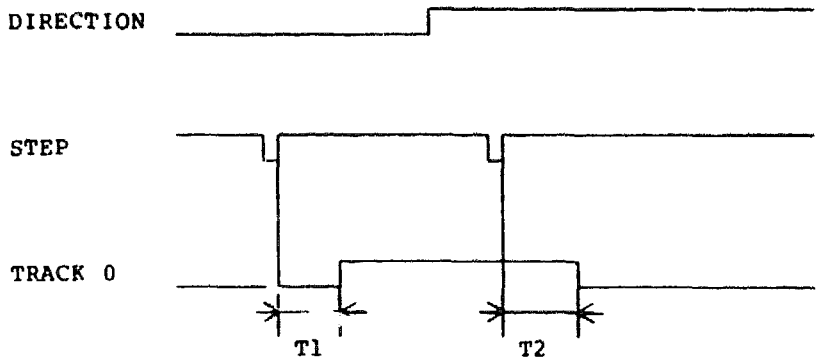
T4 : 2.4 us min.

T5 : 0.5 us min.

T6 : 18 ms min.

T7 : 2.5 us min.

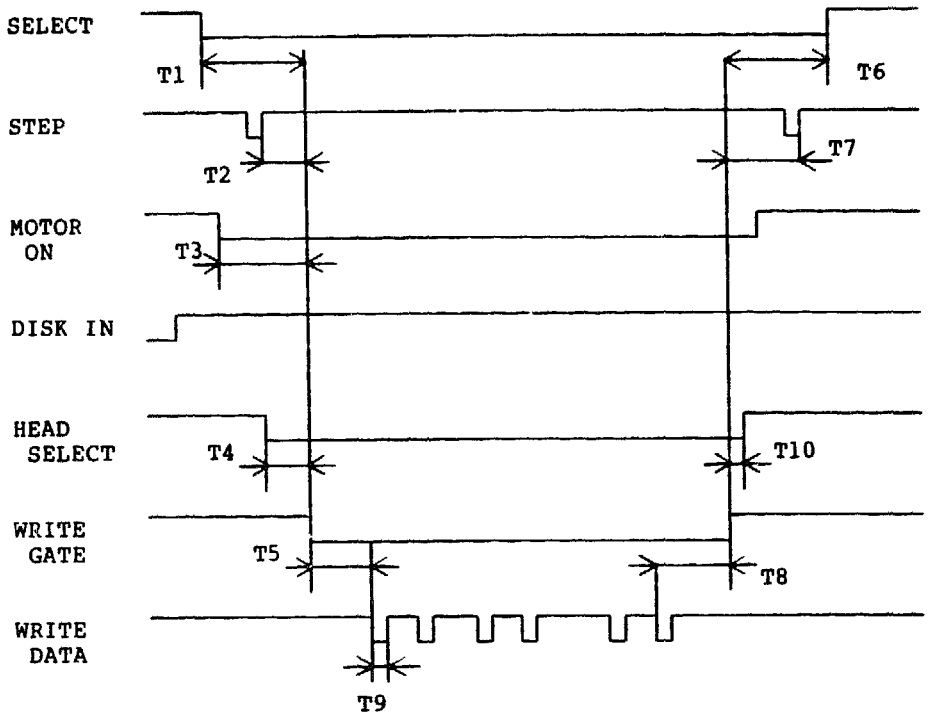
3.4.2 TRACK 00 Signal



T1 : 2.9 msec max.

T2 : 2.9 msec max.

3.4.3 Write Data Timing

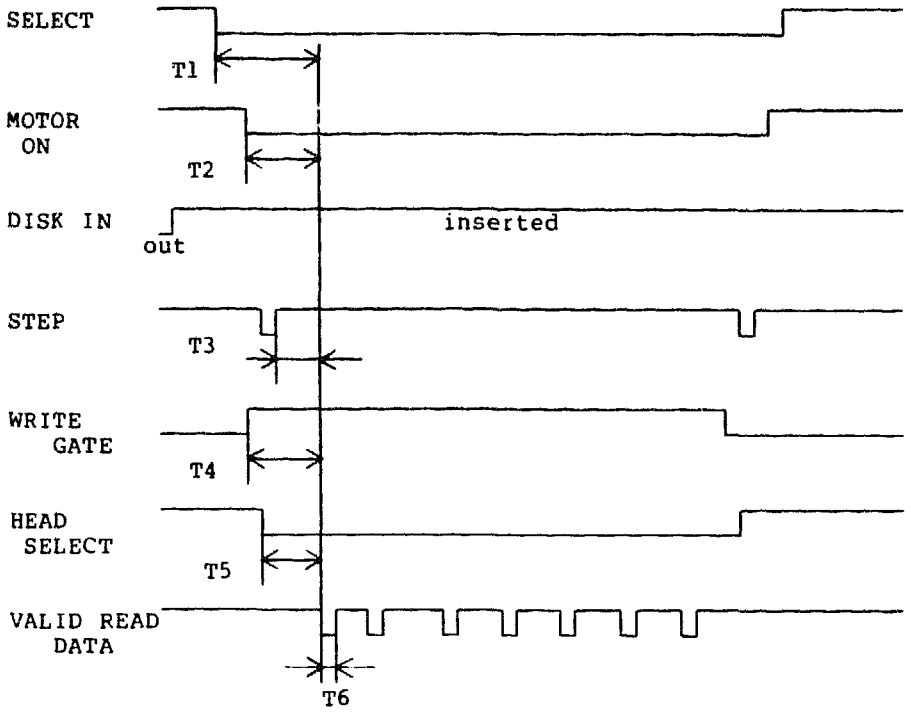


T1	:	0.5 us min.	T6	:	0.5 us min.
T2	:	18 ms min.	T7	:	585 us min. (1020 us min.)
T3	:	500 ms max.**	T8	:	4 us min. (8 us min.)
T4	:	100 us min.	T9	:	150 ns min., 1000 ns max. (150 ns min., 2000 ns max.)
T5	:	4 us max. (8 us max.)	T10	:	See 3.3.4

*NB. DISK IN, the disk-in sensor signal inside the drive, is high when a disk is inserted in the drive.

**NB. When a disk is inserted in the drive, the Motor Start Time will be 700 msec at maximum, but, after that it will be 500 msec max. as long as the disk is kept inserted.

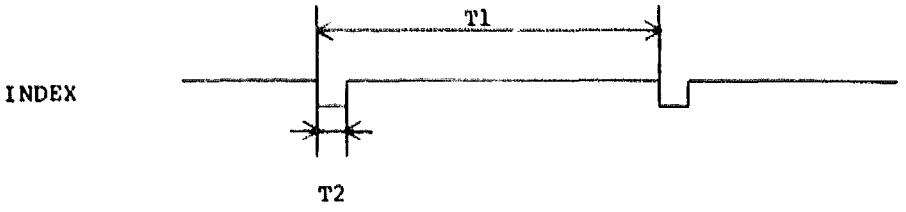
3.4.4 Read Data Timing



T1	:	0.5 us max.	T4	:	615 us max. (1050 us max.)
T2	:	500 ms max.*	T7	:	100 us max
T3	:	18 ms max.	T8	:	350 ns min., 550 ns max.

NB. When a disk is inserted in the drive, the T2, is 700 msec at maximum, but, after that T2 is 500 msec max as long as the disk is kept inserted.

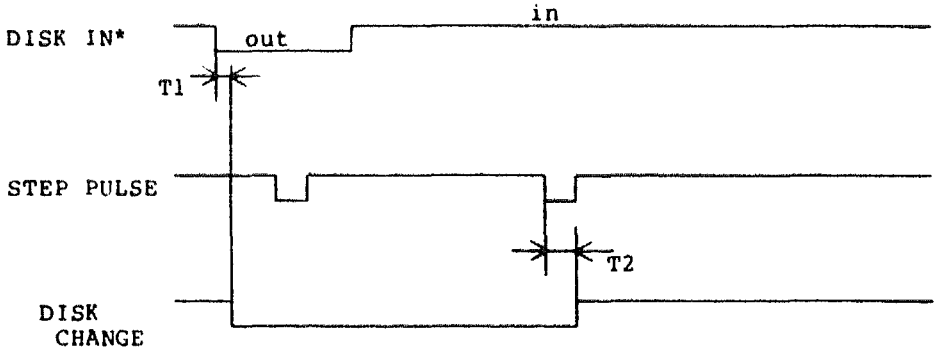
3.4.5 Index Pulse



T1* : 197 ms min., 203 ms max.

T2 : 1.25 ms min., 1.45 ms max.

3.4.6 Disk Change



T1 : 0.5 us max. T2 : 1.6 us max

*DISK IN, the disk-in sensor signal inside the drive, is high when a disk is inserted in the drive.

3.5 Power On and Power off Requirements

3.5.1 Data Protection

Turning power on or off will not cause any damage to recorded data on the disk as long as the drive is not in the midst of writing when the power is shut off or supplied.

3.5.2 Power Supply Sequencing

When the power is turned on, no special power supply sequencing is required. When the power is turned off, although there are no sequencing or timing requirements, both power supplies must fall monotonically to zero volts.

3.5.3 Power-On Reset Timing

Because it takes up to 200 msec to reset the control IC after the power has been turned on, the MP-F73W-70D cannot correctly perform any operations for this period of time after Power-On.

3.6 Disk motor rotation and Disk Insertion.

Even if the MOTOR ON signal is low (true), the disk motor will not rotate until a disk is inserted.

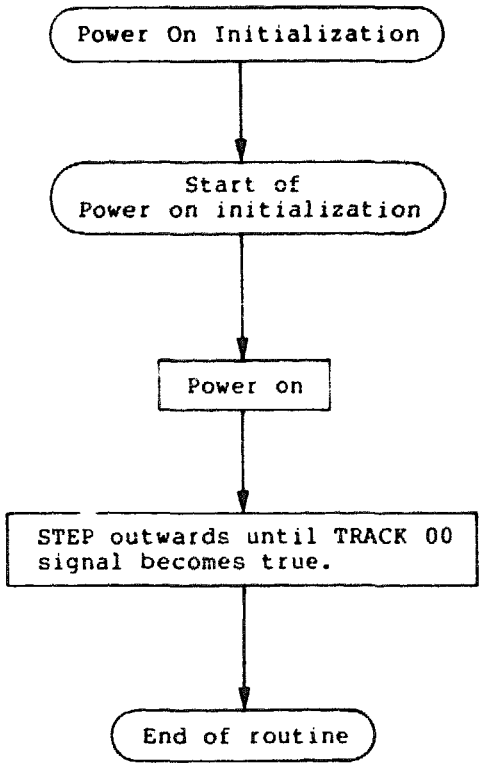
4. Safety Standards

MP-F73W-70D will meet the following product safety regulations:

U.L. 478
C.S.A. C.22.2, No.154
U.L. 94V-0 for Front Bezel

5. Power On Initialization

In order to reduce the peak current requirement when used in a daisy chain, the MP-F73W-70D has been disigned not to seek track 00 automatically. If all the drives connected in the daisy chain sought track 00 simultaneously, this would place a significant power drain on the host system. Thus, the host system must perform the following routine just after power on in order to reset the track counter inside the drive.



Setting the Chip Selector Switch

Set the chip selector switch, S5, according to the first character,"K" or "L", which is printed on the head carriage. See Figures 1 through 3.

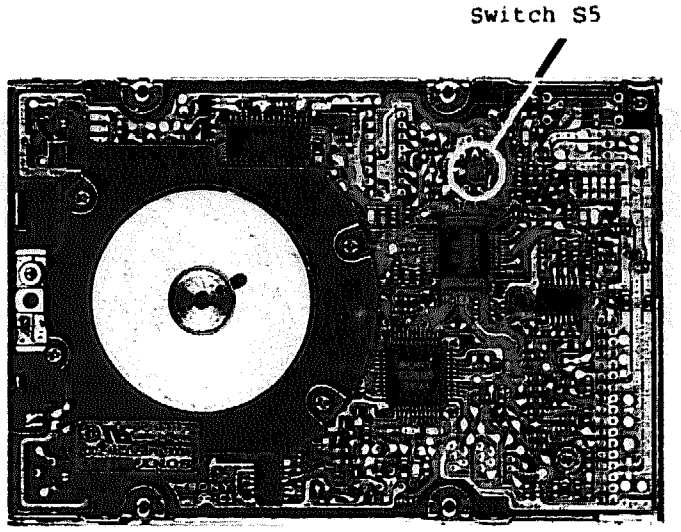


Fig. 1 Bottom view of MP-F73W-70D

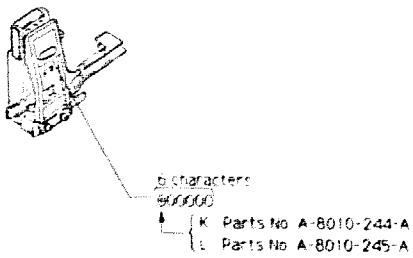
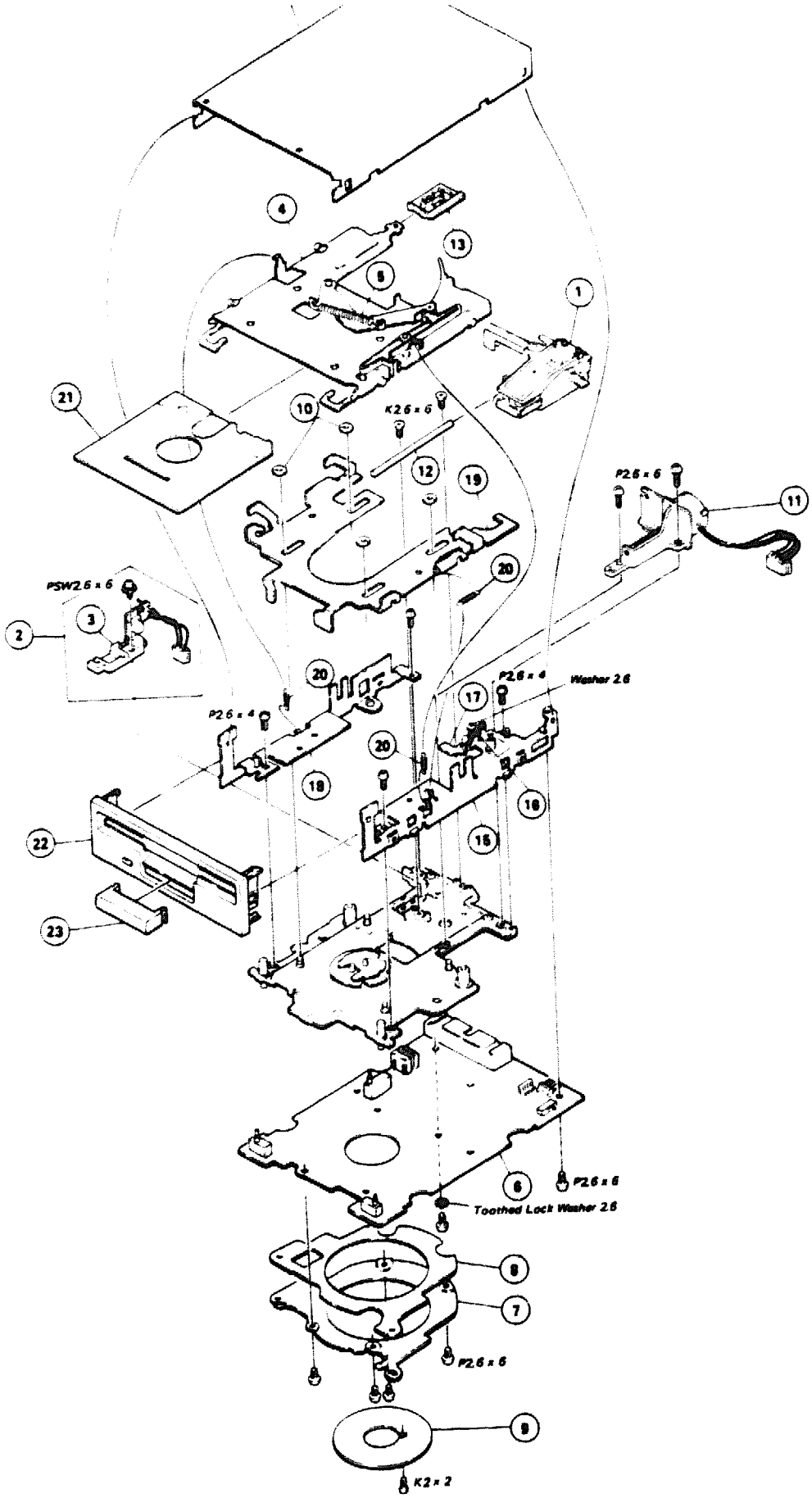


Fig. 2 Head Carriage Ass'y

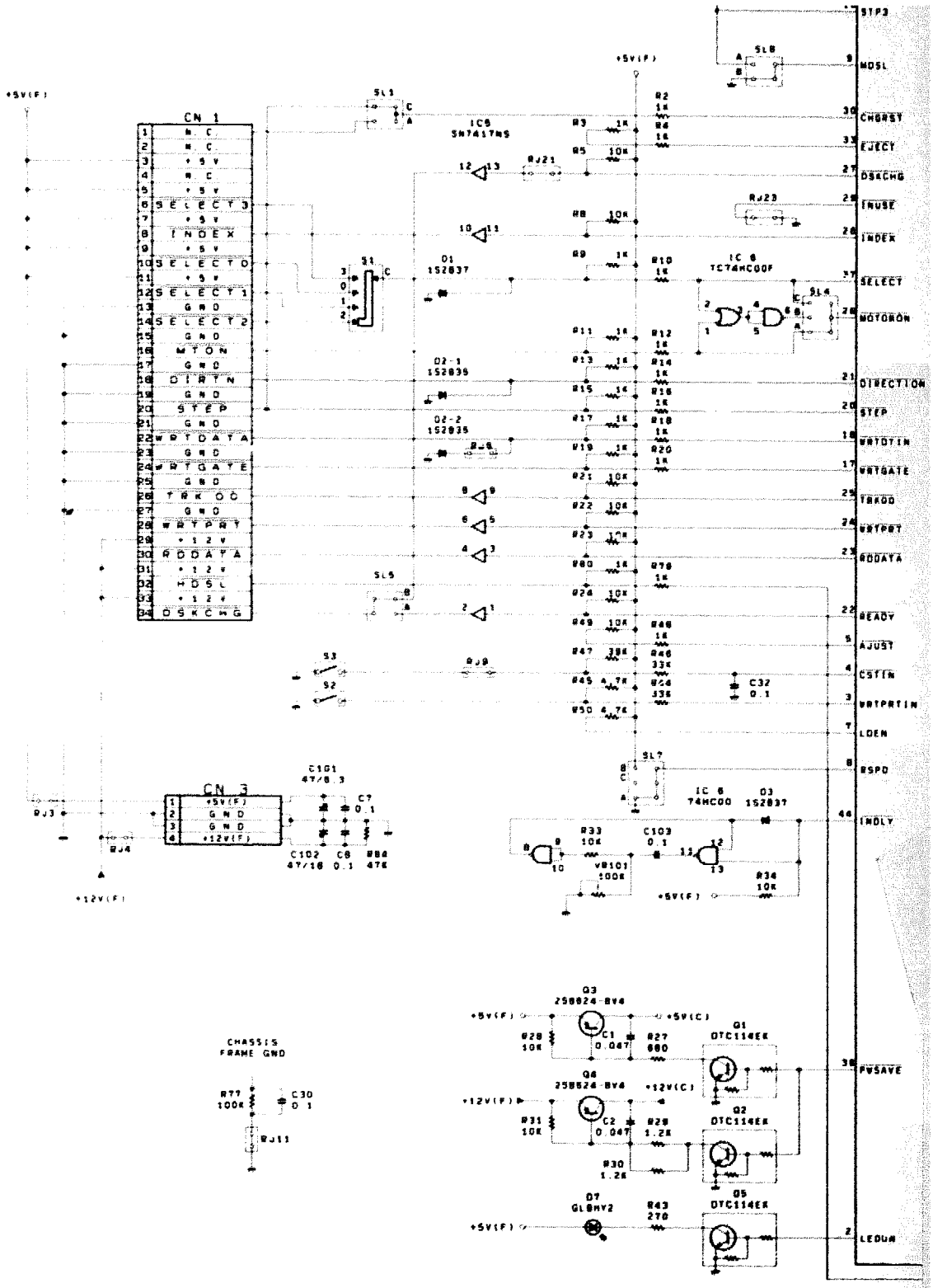


Fig. 3 setting position

Set the position of switch S5 according to the first character, K or L


4
13
5
1
21
10
K2.6 x 6
12
19
P2.6 x 6
11
20
PSW2.6 x 6
3
2
20
P2.6 x 4
Washer 2.6
17
P2.6 x 4
20
18
18
22
16
23
6
P2.6 x 6
Toothed Lock Washer 2.6
8
7
P2.6 x 6
9
K2 x 2

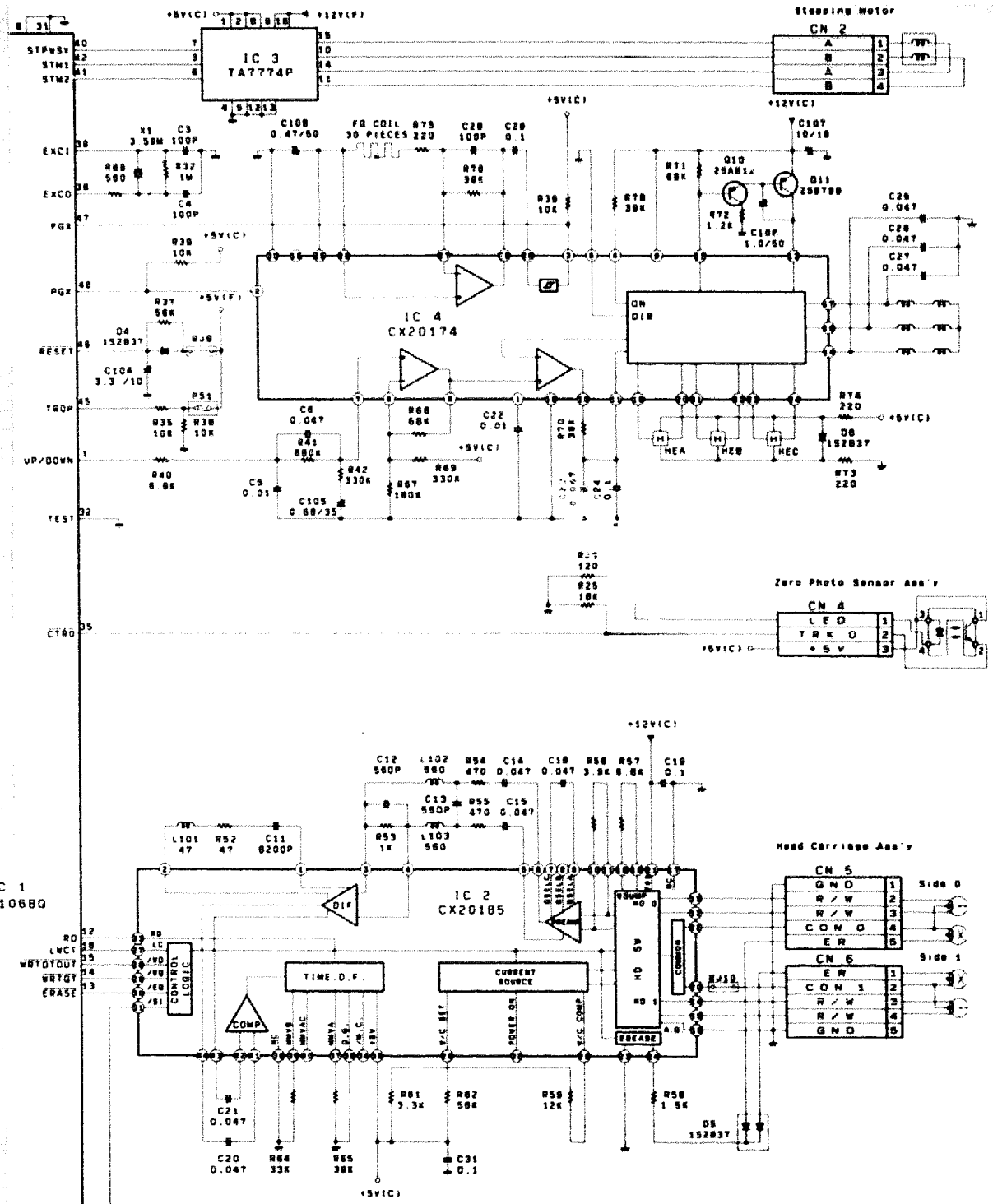
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OPTIONS

VGA Adapter


IC 3
TA7774P
IC 4
CX20174
IC 2
CX20185
IC 1
CXD1068Q
Stepping Motor
CN 2
Zero Photo Sensor Ass'y
CN 4
Head Carriage Ass'y
CN 5
CN 6
Side 0
Side 1
+5V(C)
+12V(C)
+5V(F)
+12V(F)
STPMSY
STM1
STM2
EXCI
EXCO
FGX
PGX
RESET
TROP
UP/DOWN
TEST
CTRO
RD
LWCT
WRTDTOUT
WRTGT
ERASE
CONTROL LOGIC
DIF
TIME.D.F
CURRENT SOURCE
COMP
FREADE
COMMON
FG COIL
30 PIECES

8790142

Hex Mode	Double-Scan	Border
0,1	Yes	No
2,3	Yes	Yes
0*,1*	No	No
2*,3*	No	Yes
0+,1+	No	No
2+,3+	No	Yes
4,5	Yes	No
6	Yes	Yes
7	No	Yes
7+	No	Yes
D	Yes	No
E	Yes	Yes
F	No	Yes
10	No	Yes
11	No	Yes
12	No	Yes
13	Yes	Yes

* = Enhanced EGA Modes
\+ = Enhanced Modes

Border - Double-Scan Support

Alphanumeric Modes

The Alphanumeric modes are modes 0 - 3 and 7. The character font tables are stored in a separate character ROM and consist of three 256 character fonts. When in Alphanumeric mode the BIOS transfers the character patterns to Map 2, the microprocessor transfers character data to Map 0, and the attribute data is stored in Map 1. Maps 0 and 1 can be viewed as a single buffer in any of the Alphanumeric modes. The CRT controller will generate sequential addresses, and will bring in one character code byte and one attribute byte at a time. The character code and row scan information are combined and written to address Map 2 which contains the character generator information. The appropriate character patterns are then sent on to the palette in the attribute section for color assignment.

Two bytes of data are used to define each character on the screen in all alphanumeric modes. The even address is the character code of the character font pattern stored in ROM. The odd address is the attribute byte, which defines the foreground and the background color of the

character. The following chart shows how the attribute byte controls the colors.

Attribute Function	**Attribute Byte**	
	7 6 5 4 B/I R G B Background	3 2 1 0 I/CS R G B Foreground
Normal (White On Black)	B/I 0 0 0	I/CS 1 1 1
Reverse (Black On White	B/I 1 1 1	I/CS 0 0 0
Nondisplay (Black)	B/I 0 0 0	I/CS 0 0 0
Nondisplay (White)	B/I 1 1 1	I/CS 1 1 1
Mono=Underline/Color=Blue	B/I 0 0 0	I/CS 0 0 1

I = Highlighted
B = Blinking Foreground (Character)
CS = Character Select

Table 2 Alphanumeric Mode Attribute Byte Definition

The character box size is dependent on the display mode selected. All modes may be displayed on both monochrome and color VGA displays.

If a color mode is used, the display system supports up to 16 colors. These sixteen colors are defined by combinations of the R, G, B, and I bits as shown in the chart below.

I	**R**	**G**	**B**	**COLOR**
0	0	0	0	BLACK
0	0	0	1	BLUE
0	0	1	0	GREEN
0	0	1	1	CYAN
0	1	0	0	RED
0	1	0	1	MAGENTA
0	1	1	0	BROWN
0	1	1	1	LIGHT GRAY
1	0	0	0	DARK GRAY
1	0	0	1	LIGHT BLUE
1	0	1	0	LIGHT GREEN
1	0	1	1	LIGHT CYAN
1	1	0	0	PINK
1	1	0	1	LIGHT MAGENTA
1	1	1	0	YELLOW
1	1	1	1	WHITE

Table 1 Available Colors

The 40 column modes, Hex 0 and 1, demonstrate the following characteristics:

Display up to 25 rows of 40 columns each.

Requires 2000 bytes of memory per page.

One character code and one attribute code per character.

The 80 column modes, Hex 2, 3, and 7, demonstrate the following characteristics:

Display up to 25 rows of 80 characters each.

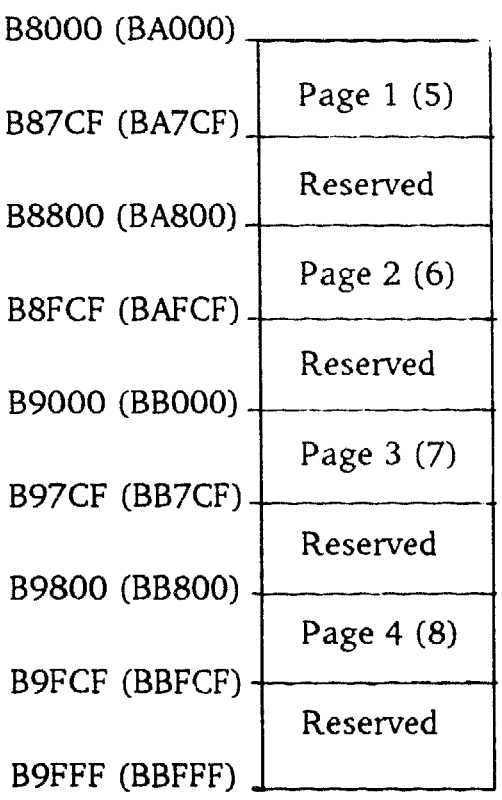
Requires 4000 bytes of memory per page.

One character code and one attribute code per character.

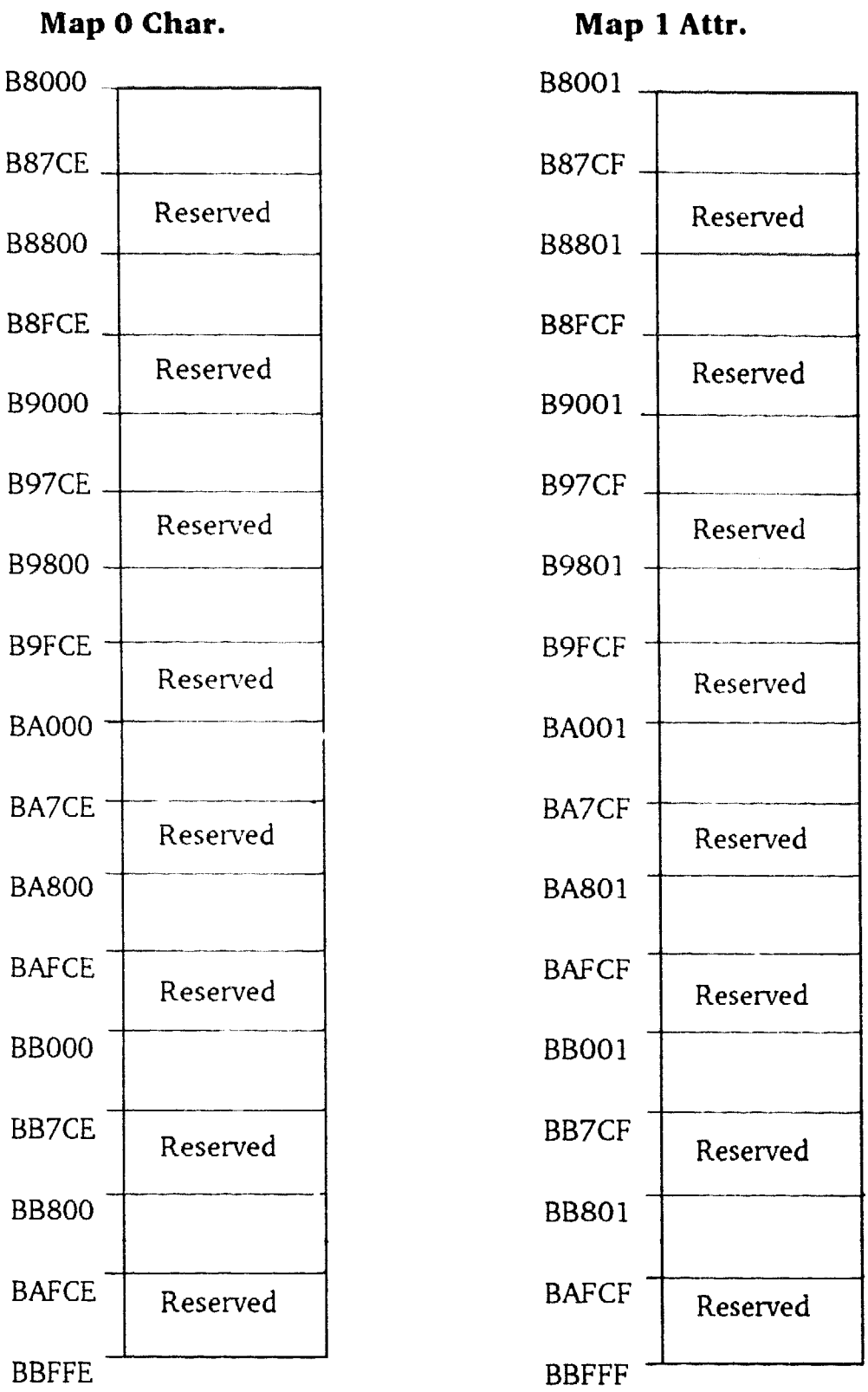
Memory Maps Modes Hex 0, 1, 2, 3, and 7

Modes Hex 0/1

Display Buffer Addresses



Character Map Addresses

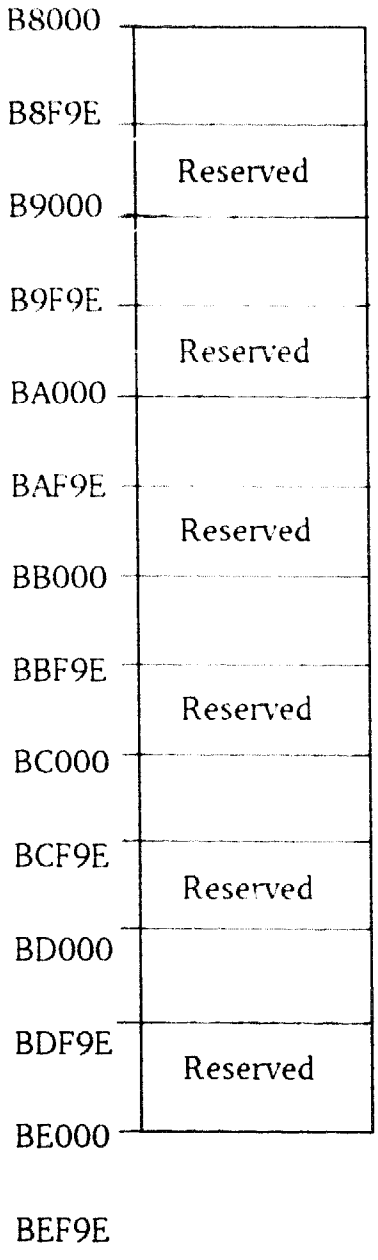


Modes Hex 2/3

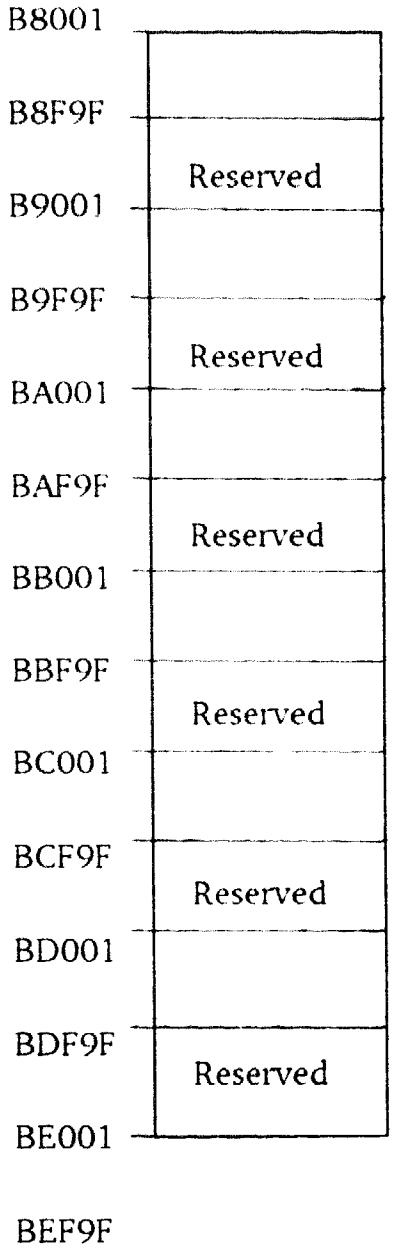
Display Buffer addressing is the same as Mode 0/1.

Character Map Addressing

Map 0 Char.

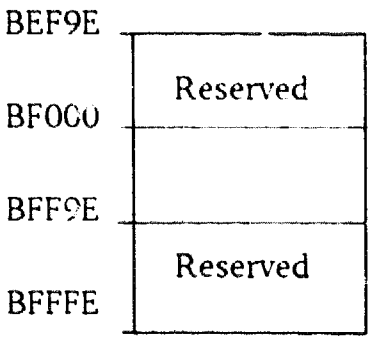


Map 1 Attr.

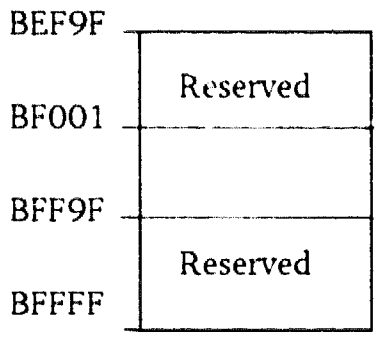


Character Map Addressing (Cont)

Map 0 Char.



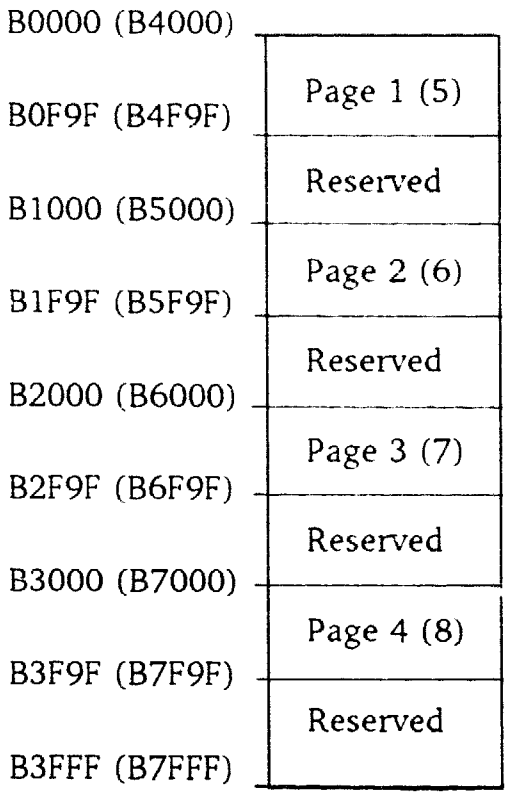
Map 1 Attr.



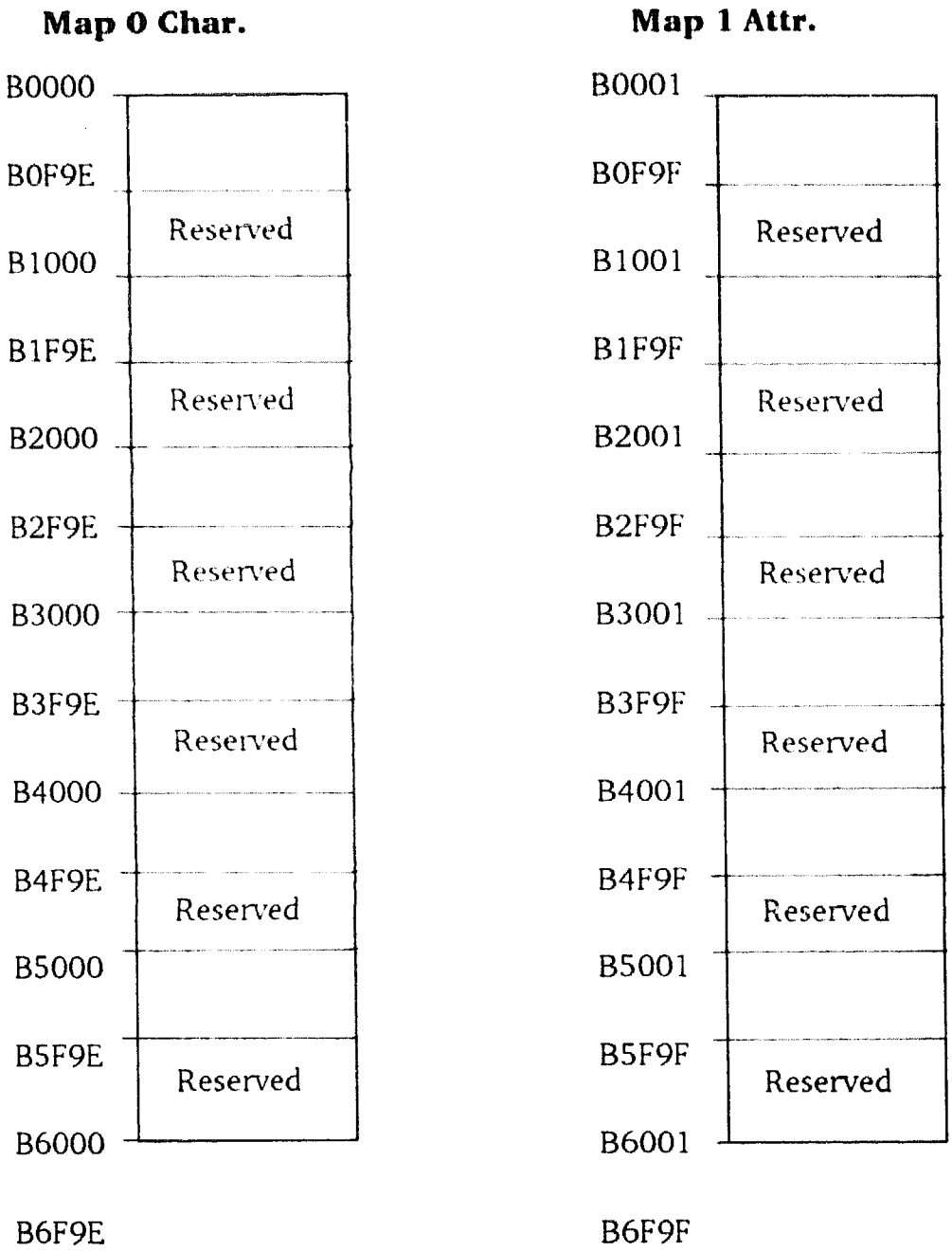
Mode Hex 7

Display Buffer Addressing

Display Buffer

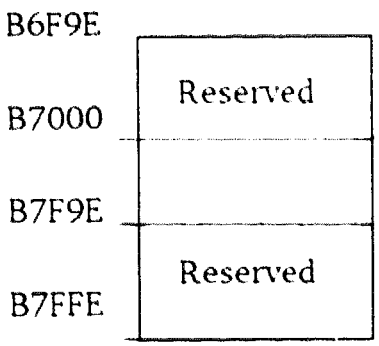


Character Map Addressing

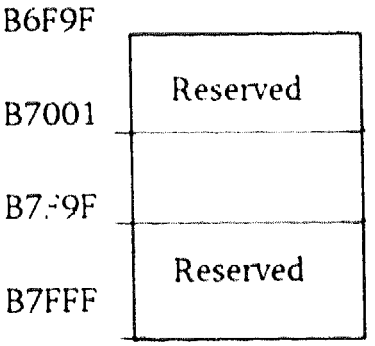


Character Map Addressing (Cont)

Map 0 Char.



Map 1 Attr.



Graphics Modes

All graphics modes may be displayed on both color and monochrome VGA displays. A grey scale is used to represent colors on the monochrome display.

4 Color Graphics Modes Hex 4 and 5

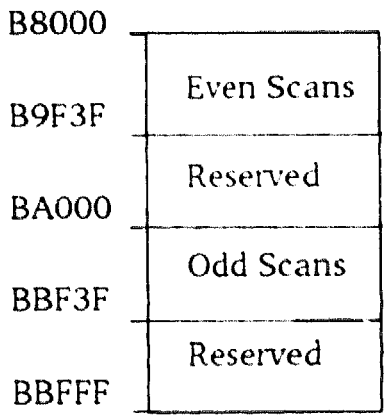
The display buffer is configured at address B8000 hex. Bit image data is kept in memory maps 0 and 1. This mode has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Each pixel selects 1 of 4 colors
Requires 16,000 bytes of read/write memory
Double scanned on display to provide 400 rows
Formats 4 PELs per byte in the following manner:

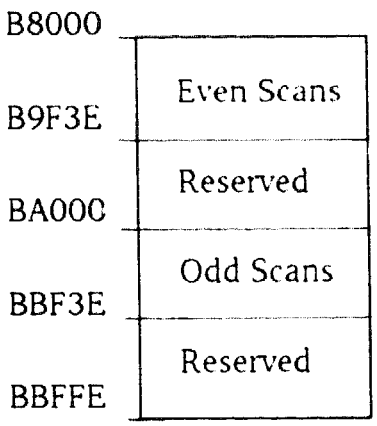
7 PA1	6 PA0	5 PA1	4 PA0	3 PA1	2 PA0	1 PA1	0 PA0
First Display PEL		Second Display PEL		Third Display PEL		Fourth Display PEL	

The memory usage for these modes is as shown below.

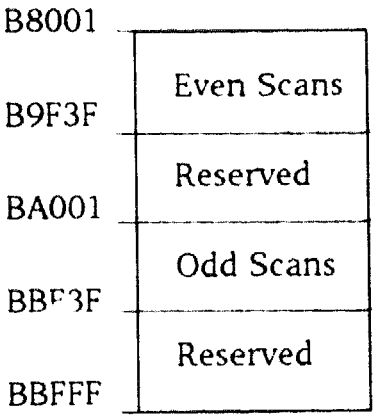
Display Buffer Addressing



Map 0



Map 1



Color selection is determined by the following chart.

PA1	PA0	Color Selected
0	0	Black
0	1	Light Cyan (Green)**
1	0	Light Magenta (Red)**
1	1	Intense White (Brown)**

**The colors in parenthesis represent an alternate palette selectable by BIOS.

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2 Color Graphics Mode Hex 6

The display buffer is configured at address B8000 hex. Bit image data is stored in memory map 0, and comprises a single bit plane. This mode has the following characteristics:

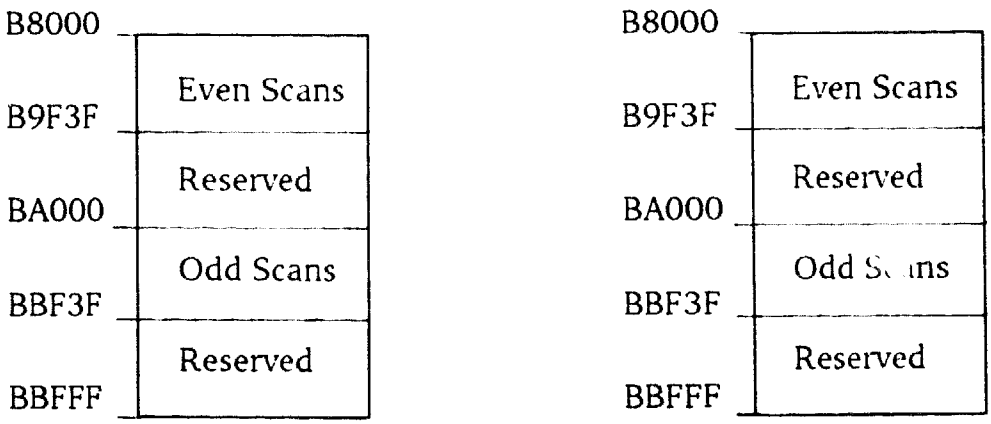
Contains a maximum of 200 rows of 640 PELs.
Can display 2 colors.
Double scanned to display 400 rows.
Requires 16k bytes of read/write memory.
Formats 8 PELs per byte for each byte in the following manner:

7 PA0	6 PA0	5 PA0	4 PA0	3 PA0	2 PA0	1 PA0	0 PA0
First Dsply PEL	Secnd Dsply PEL	Third Dsply PEL	Forth Dsply PEL	Fifth Dsply PEL	Sixth Dsply PEL	Svnth Dsply PEL	Eghth Dsply PEL

The memory usage for this mode is shown below.

Display Buffer Addressing

Map 0
Bit Plane 0



Color selection is determined by the following chart:

PA0-1 – PA0-7	Color
0	Black
1	Intense White

2 Color Graphics Mode Hex 11

Mode 11 maintains 2 color graphics in the same data format as mode 6. Bit image data is stored in map 0 and makes up a single bit plane. The display buffer is configured at address A0000 hex, with the first eight PELs stored at A0000 and the second eight PELs stored at A0001 hex.

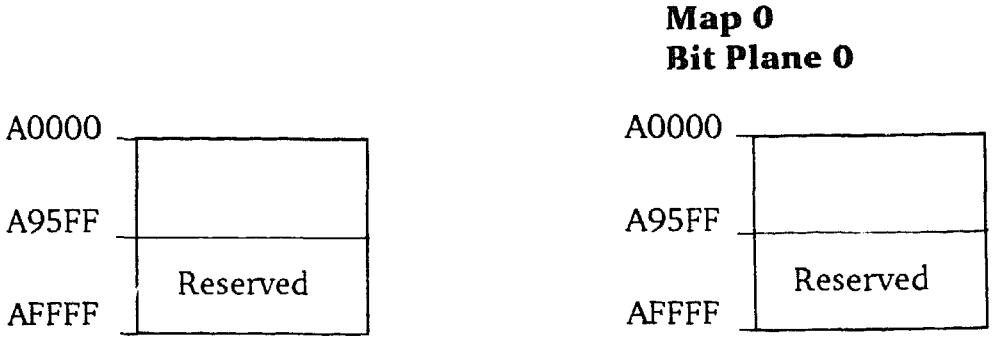
This mode has the following characteristics:

Contains a maximum of 480 rows of 640 PELs.
Can display 2 colors.
Requires 38,400 bytes of read/write memory.
Formats 8 PELs per byte for each byte in the following manner:

7 PA0	**6 PA0**	**5 PA0**	**4 PA0**	**3 PA0**	**2 PA0**	**1 PA0**	**0 PA0**
First Dsply PEL	Secnd Dsply PEL	Third Dsply PEL	Forth Dsply PEL	Fifth Dsply PEL	Sixth Dsply PEL	Svnth Dsply PEL	Eghth Dsply PEL

The memory usage for this mode is shown below.

Display Buffer Addressing



Color selection is determined by the following char

PA0-1 – PA0-7	**Color**
0	Black
1	Intense White

2 Color Graphics Mode Hex F

This mode is used to imitate EGA graphics on an IBM monochrome display. Map 0 is used as the video bit plane, while Map 2 is used for the

intensity bit plane. Both planes occupy memory space beginning at A0000 hex. Picture elements are made up of two bits each, one from each plane. The first eight PELs on the screen are defined by the contents of memory location A0000 hex, the second at location A0001 hex. The first PEL within any one byte is defined by bit 7, the last by bit 0. Since both planes reside at hex address A0000, you must select which plane you wish to update using the Map Mask register of the sequencer. This is covered in detail later in the video subsystem section.

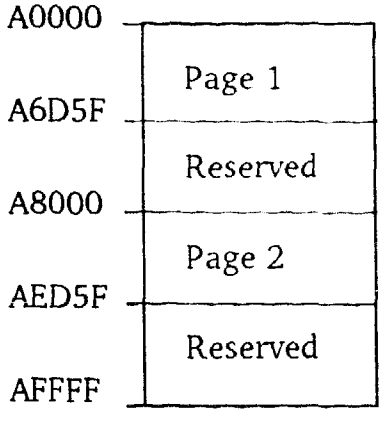
This mode has the following characteristics:

Contains a maximum of 350 rows of 640 PELs.
Can display 2 colors.
Requires 56k bytes of read/write memory.
Formats 8 PELs per byte for each byte in the following manner:

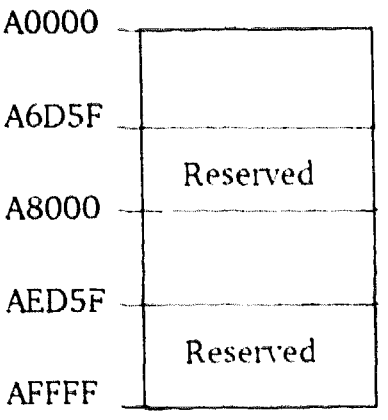
7 **PA0,1**	**6** **PA0,1**	**5** **PA0,1**	**4** **PA0,1**	**3** **PA0,1**	**2** **PA0,1**	**1** **PA0,1**	**0** **PA0,1**
First Dsply PEL	Secnd Dsply PEL	Third Dsply PEL	Forth Dsply PEL	Fifth Dsply PEL	Sixth Dsply PEL	Svnth Dsply PEL	Eghth Dsply PEL

The memory usage for this mode is shown below.

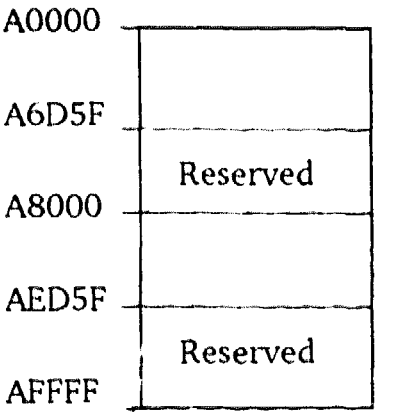
Display Buffer Addressing



Map 0
Video Bit Plane



Map 1
Intensity Bit Plane



PA0-1 – PA0-7 Intensity Bit Plane	PA1-1 – PA1-7 Video Bit Plane	Color Selected
0	0	Black
0	1	White
1	0	Blinking White
1	1	Intense White

16 Color Graphics Modes Hex 10, D, E, and 12

These modes support graphics in 16 colors. The bit image data resides in all four bit planes, and each bit plane represents a color. The display buffer is configured at A0000 hex, and the Map Mask register is used to update any or all maps.

Mode 10 hex has the following characteristics:

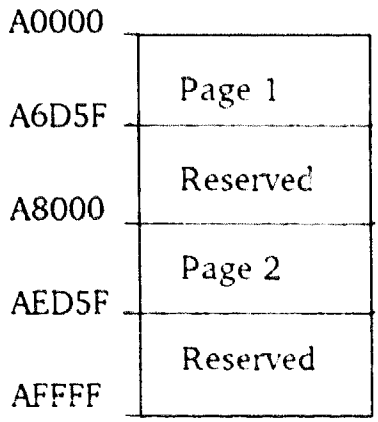
Contains 350 rows of 640 PELs.
Can display 16 of 256K possible colors.
Requires 28,000 bytes of read/write memory.
Formats 8 PELs per byte for each map in the following manner:

7	6	5	4	3	2	1	0
PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
First PEL	←					→	Eighth PEL

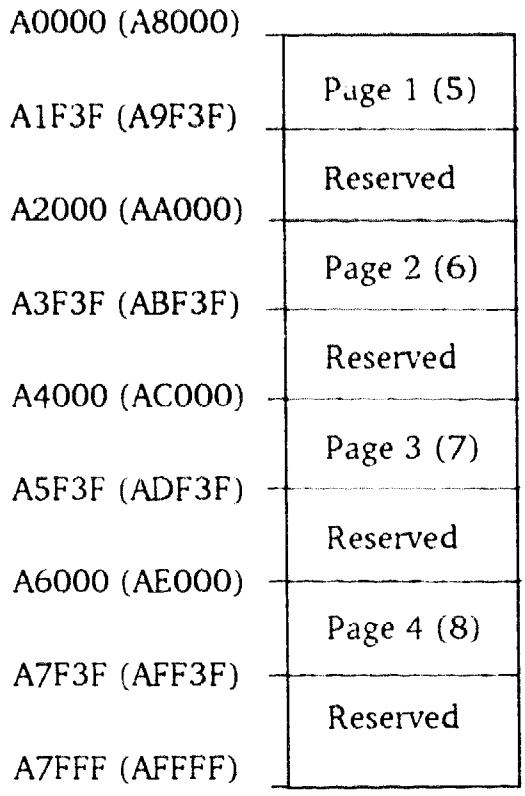
The memory usage for this mode is shown below.

Display Buffer Addressing

Mode Hex 10

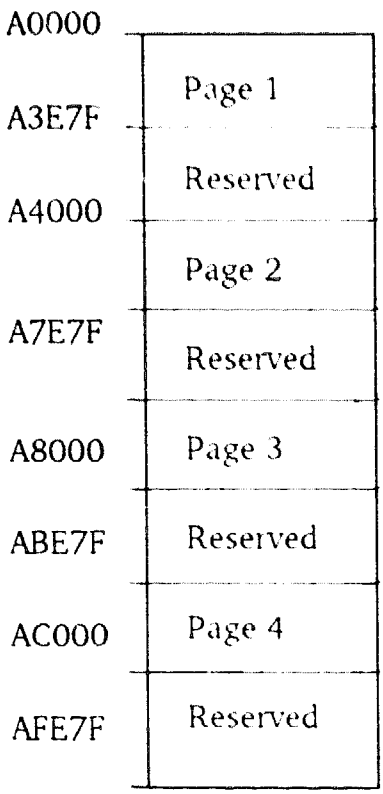


Mode Hex D



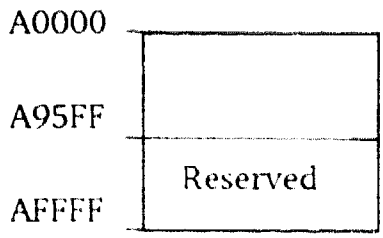
Mode Hex D Requires 8,000 bytes per page and contains 200 rows of 320 PELs

Mode Hex E



Mode Hex E requires 16,000 bytes per page and contains 200 rows of 640 PELs

Mode Hex 12

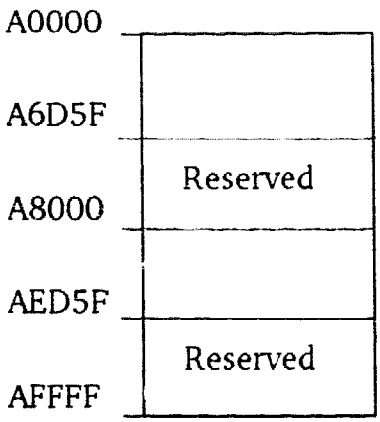


Mode Hex 12 requires 38,400 bytes and contains 480 rows of 640 PELs

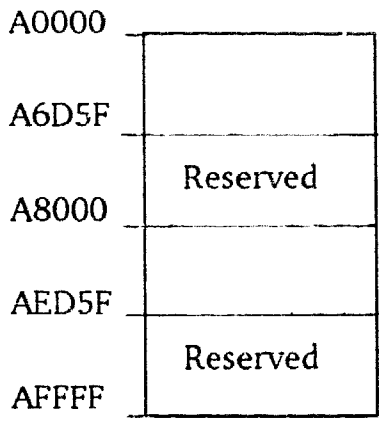
Character Map Addressing

Mode 10

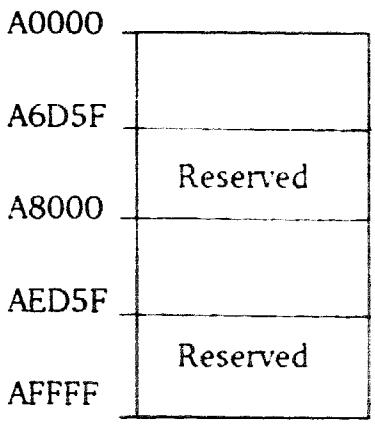
Map 0
Blue Bit Plane



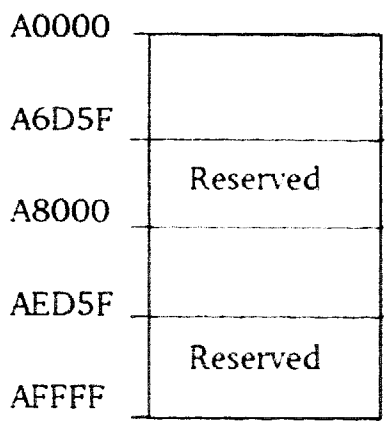
Map 1
Green Bit Plane



Map 2
Red Bit Plane

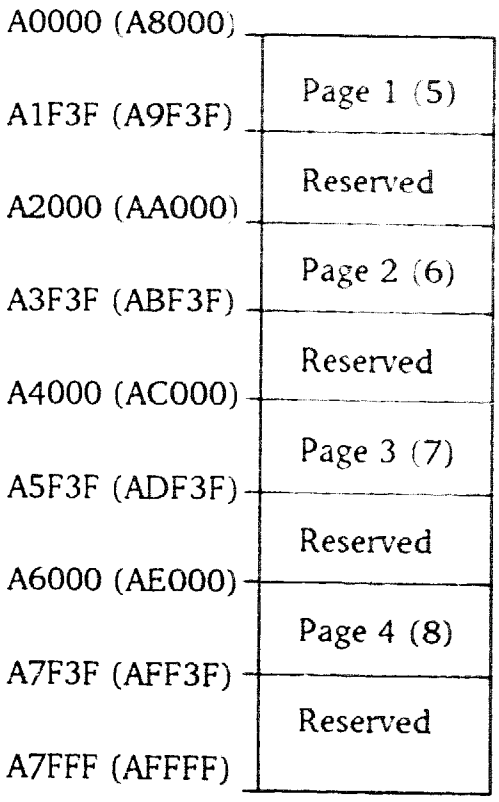


Map 3
Intensity Bit Plane

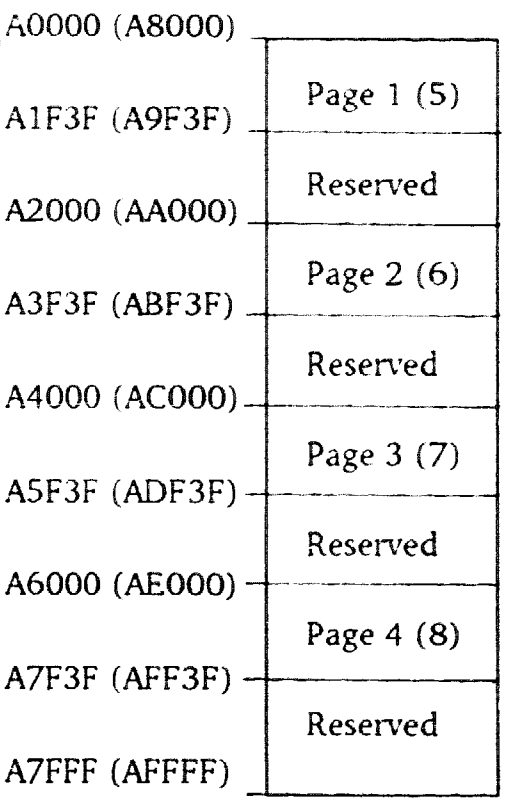


Mode D

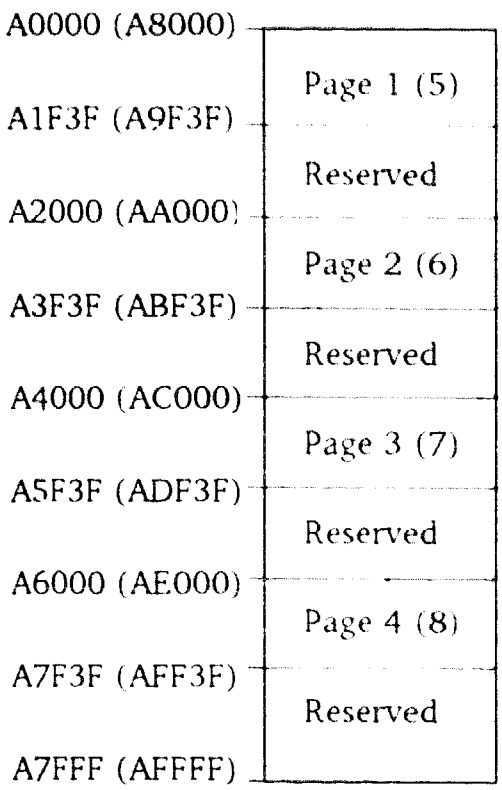
Map 0
Blue Bit Plane



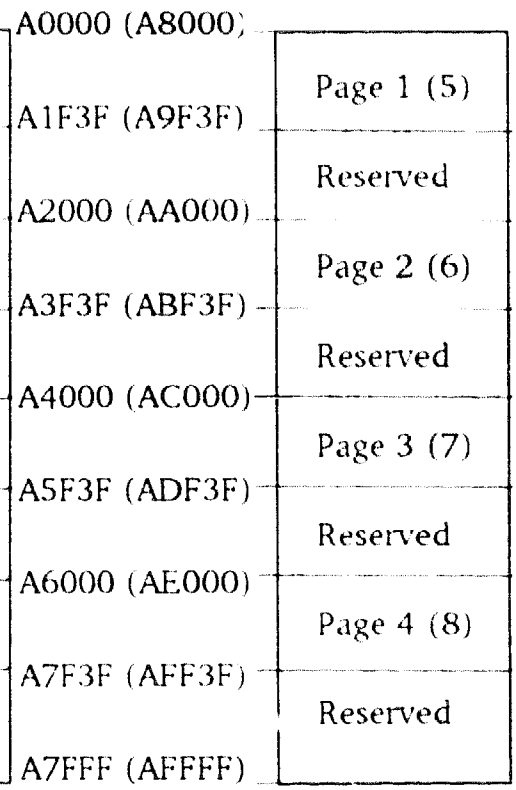
Map 1
Green Bit Plane



Map 2
Red Bit Plane



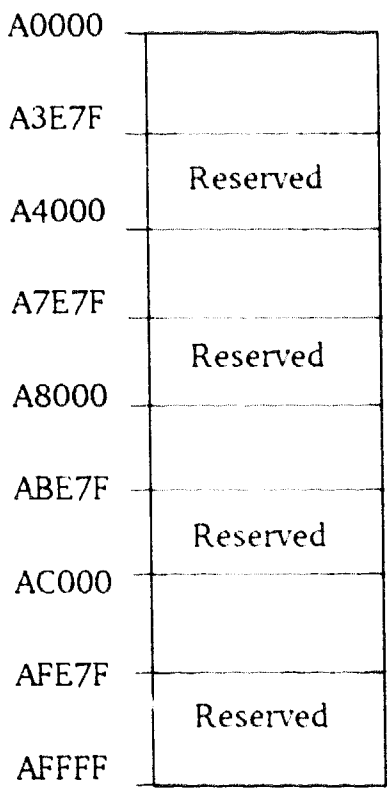
Map 3
Intensity Bit Plane



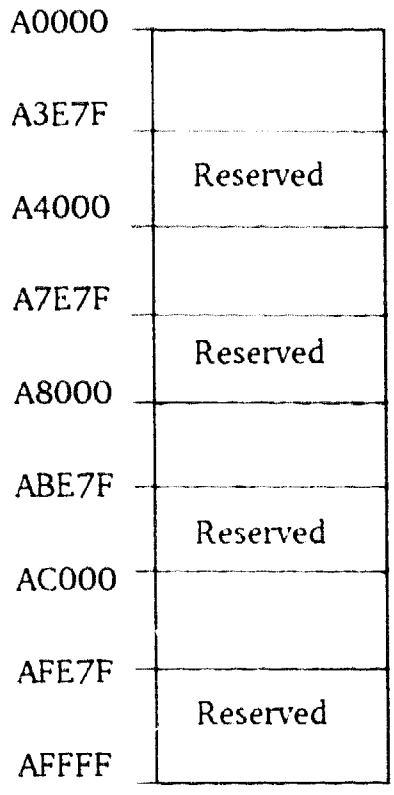
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Mode E

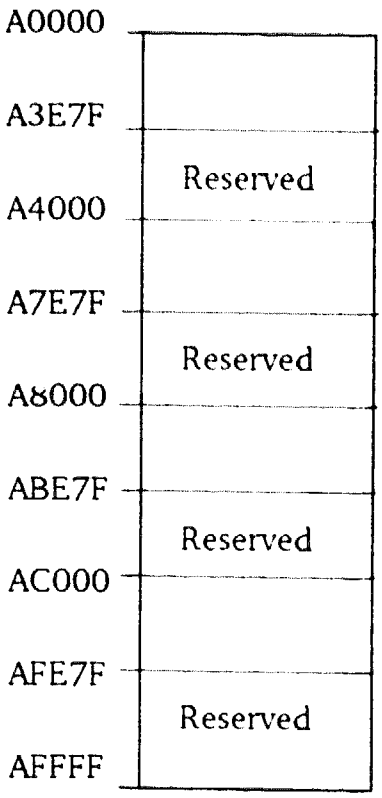
Map 0
Blue Bit Plane



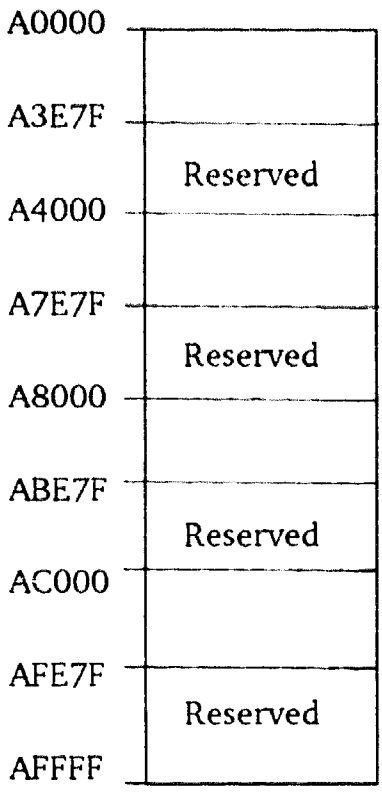
Map 1
Green Bit Plane



Map 2
Red Bit Plane

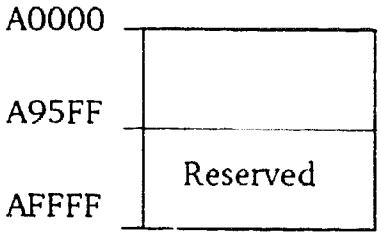


Map 3
Intensity Bit Plane

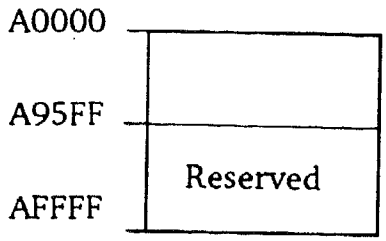


Mode 12

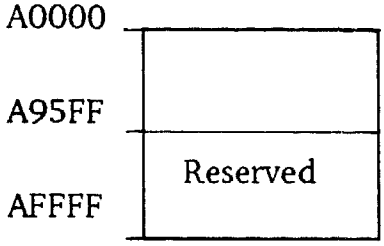
Map 0
Blue Bit Plane



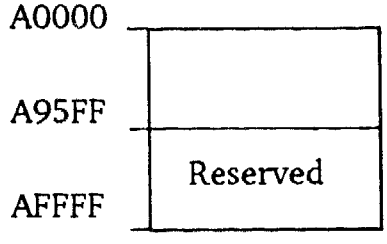
Map 1
Green Bit Plane



Map 2
Red Bit Plane



Map 3
Intensity Bit Plane



Color selection is determined by the following chart.

Map 3	Map 2	Map 1	Map 0	Color
0	0	0	0	BLACK
0	0	0	1	BLUE
0	0	1	0	GREEN
0	0	1	1	CYAN
0	1	0	0	RED
0	1	0	1	MAGENTA
0	1	1	0	BROWN
0	1	1	1	WHITE
1	0	0	0	DARK GRAY
1	0	0	1	LIGHT BLUE
1	0	1	0	LIGHT GREEN
1	0	1	1	LIGHT CYAN
1	1	0	0	LIGHT RED
1	1	0	1	LIGHT MAGENTA
1	1	1	0	YELLOW
1	1	1	1	INTENSIFIED WHITE

256 Color Graphics Mode Hex 13

Mode 13 provides support for 256 colors to be displayed on the screen at any one time. The display buffer is configured at A0000 hex, and is 64,000 bytes long. Bit image data is stored in all four Memory Maps, and is made up of four bit planes. These bit planes are sampled twice to produce eight bit planes that address the video DAC. The internal palette of the video subsystem is not used in this mode. It is set by the BIOS and should not be changed. The external video palette that resides within the video DAC is programmed by the BIOS in a way that allows the first 16 locations to be compatible with colors of other modes. The next 16 locations hold evenly spaced shades of gray, and the remaining 216 locations are programmed based on the hue-saturation-intensity model designed to provide a useable color set that covers a wide range of color values.

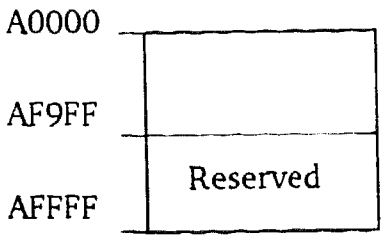
This mode has the following characteristics:

Contains 200 rows of 320 PELs.
Double scanned to 400 rows.
Can display 256 of 256K possible colors.
Requires 64,000 bytes of read/write memory.
Formats 1 PEL per byte for each byte in the following manner:

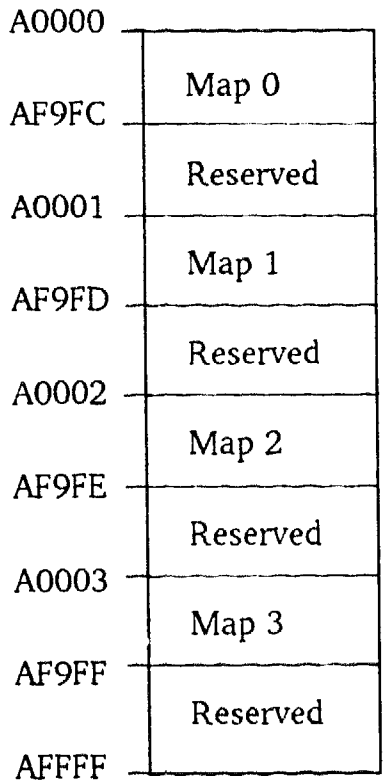
7	6	5	4	3	2	1	0
PA0-7							
Display PEL							

The memory usage for this mode is shown below.

Display Buffer Addressing



Character Map Addressing



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Compatible color selection is determined by the following chart.

PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	COLOR
0	0	0	0	0	0	0	0	BLACK
0	0	0	0	0	0	0	1	BLUE
0	0	0	0	0	0	1	0	GREEN
0	0	0	0	0	0	1	1	CYAN
0	0	0	0	0	1	0	0	RED
0	0	0	0	0	1	0	1	MAGENTA
0	0	0	0	0	1	1	0	BROWN
0	0	0	0	0	1	1	1	WHITE
0	0	0	0	1	0	0	0	DARK GRAY
0	0	0	0	1	0	0	1	LIGHT BLUE
0	0	0	0	1	0	1	0	LIGHT GREEN
0	0	0	0	1	0	1	1	LIGHT CYAN
0	0	0	0	1	1	0	0	LIGHT RED
0	0	0	0	1	1	0	1	LIGHT MAGENTA
0	0	0	0	1	1	1	0	YELLOW
0	0	0	0	1	1	1	1	INTENSIFIED WHITE

Video Memory Read/Write Functions

Video Memory Writes

Memory maps are enabled by a logical decode of the memory addresses sent from the microprocessor and, depending on the video mode selected, the Map Mask register. The Map Mask register resides in the sequencer section and will be covered in detail later in the section on the Video subsystem.

Video Memory Reads

Video memory can be read in one of two ways. The first is by selecting Read Mode 0 with the Graphics Mode register. In this mode the microprocessor reads an eight bit value determined by the logical decode of the memory address and, if applicable, the Read Map Select register. When Read Mode 1 is selected using the Graphics Mode register, the eight bit value read by the microprocessor is the result of a color compare operation controlled by the Color Compare and Color Don't Care registers. The Color Compare and Color Don't Care registers will be covered in detail later in the Video Subsystem section.

Programmable Registers

There are eight sets of registers contained in the video subsystem. The following chart shows their addresses. A more detailed explanation will follow.

Register	Read/Write	Color Address	Mono Address
General Registers			
Miscellaneous Output	Write	03C2H	03C2H
	Read	03CCH	03CCH
Input Status 0	Read Only	03C2H	03C2H
Input Status 1	Read Only	03DAH	03BAH
Feature Control	Write	03DAH	03BAH
	Read	03CAH	03CAH
Sequencer Registers			
Address Register	Read/Write	03C4H	03C4H
Other Sequencer Registers	Read/Write	03C5H	03C5H
CRT Controller Registers			
Index Register	Read/Write	03D4H	03B4H
Other CRT Controller Registers	Read/Write	03D5H	03B5H
Graphics Registers			
Address Register	Read/Write	03CEH	03CEH
Other Graphics Registers	Read/Write	03CFH	03CFH
Attribute Registers			
Address Register	Read/Write	03C0H	03C0H
Other Attribute Registers	Write	03C0H	03C0H
	Read	03C1H	03C1H

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Register	Read/Write	Color Address	Mono Address
Compatibility Registers			
AT&A/M24	Write Only	03DEH	03DEH
Hercules	Write Only	03BFH	03BFH
Mode Control	Write Only	03D8H	03B8H
Color Select	Write Only	03D9H	03D9H
Status	Read Only	03DAH	03BAH
Enhanced Feature Registers			
Address Register	Read/Write	03CEH	03CEH
Address Offset A	Read/Write	03CFH	03CFH
Address Offset B	Read/Write	03CFH	03CFH
Memory Size	Read/Write	03CFH	03CFH
Video Select	Read/Write	03CFH	03CFH
CRT Control	Read/Write	03CFH	03CFH
Video Control	Read/Write	03CFH	03CFH
Lock/Status	Read/Write	03CFH	03CFH
Video DAC			
PEL Address Register (Write Mode)	Read/Write	03C8H	03C8H
PEL Address Register (Read Mode)	Write Only	03C7H	03C7H
DAC State Register	Read Only	03C7H	03C7H
PEL Data Register	Read/Write	03C9H	03C9H
PEL Mask **	Read/Write	03C8H	03C8H

** **Note:** This register must not be written to by application software. Doing so may destroy the color look-up table stored inside the DAC.

General Registers

Miscellaneous Output Register

The Miscellaneous Output register is a read/write register. A hardware reset will cause all of the bits in this register to be cleared to 0. The read address for this register is 03CC hex. The write address for this register is 03C2 hex. The bit definitions for this register are as follows.

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Bit	Function
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page bit for odd/even
4	Reserved = 0
3	Clock Select 1
2	Clock Select 0
1	Enable RAM
0	I/O Address Select

Bits 6-7 — Bits 7 and 6 are selected depending on the vertical size desired as shown in the following chart.

Bit 7	Bit 6	Vertical Size
0	0	Reserved = 0
0	1	400 Lines
1	0	350 Lines
1	1	480 Lines

Bit 5 — This bit selects between two 64K pages in odd or even modes of operation (0-5). A 0 selects the low page of memory, and a 1 selects the high page of memory. This bit should be used for diagnostic purposes only.

Bit 4 — Reserved

Bits 2-3 — These two bits determine clock source selection as shown in the following chart.

Bit 3	Bit 2	Clock Select
0	0	28.322 MHz clock for 720 Horizontal PELs
0	1	Selects external clock
1	0	25.175 MHz clock for 640 Horizontal PELs
1	1	Reserved

Bit 1 — A logical 0 in this position disables the video RAM address decode from the microprocessor. A 1 enables the video RAM to the microprocessor.

Bit 0 — A 0 sets the proper CRTC I/O and Input Status 1 register address maps for Monochrome operation. A 1 in this location sets the maps for color graphics operation. Monochrome addresses are 03Bx for the CRTC I/O addresses and 03BA for the Status 1 register. Color graphics

addresses are 03Dx for the CRTC I/O addresses and 03DA for the Status 1 register.

Input Status Register 0

This is a read only register and is located at address 03C2 hex.

Bit	Function
7	CRT Interrupt
5-6	Reserved = 0
4	Switch Sense Bit
0-3	Reserved = 0

Bit 7 — A 1 in this location denotes that a vertical retrace interrupt is pending. A 0 denotes the vertical retrace interrupt is cleared.

Bits 5-6 — Reserved

Bit 4 — This bit allows the power on self test (POST) to determine if a monochrome or color monitor is attached to the system.

Bits 0-3 — Reserved

Input Status Register 1

This is a read only register and is located at addresses 03BA hex for monochrome emulation and 03DA hex for color graphics emulation.

Bit	Function
6-7	Reserved = 0
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
1-2	Reserved = 0
0	Display Enable

Bits 6-7 — Reserved

Bits 4-5 — Diagnostic usage.

Bit 3 — A 0 in this bit position shows that information is being displayed. A 1 in this location means that a vertical retrace is taking place. This bit can be programmed to interrupt the microprocessor on interrupt level 2 when a vertical retrace is initiated. This is done by programming Bits 4 and 5 of the Vertical Retrace End register, which is covered later in the register descriptions.

Bits 1-2 — Reserved

Bit 0 — A 1 in this bit location signals a horizontal or vertical retrace interval. This bit represents the real-time status of the inverted display enable signal.

Feature Control Register

This is a read/write register. The write address is located at 03BA hex for monochrome graphics and 03DA hex for color graphics. The read address is located at 03CA hex. All bits in this register are reserved. Bit 3 must equal 0.

Video Subsystem Enable Register

This is a read/write register located at address 03C3 hex.

Bit	Function
1-7	Reserved = 0
0	Video Subsystem Enable

Bits 1-7 — Reserved

Bit 0 — When set to 1, this bit enables decoding of memory and I/O addresses. A 0 in this location disables the decode of the memory and I/O addresses.

Sequencer Registers

Sequencer Address Register

This is a read/write register located at address 03C4 hex. It is loaded with the binary value of the sequencer data register where information is to be written. The address is written to 03C4 hex, and the data to be stored in the selected register is then written to 03C5 hex.

Bit	Function
3-7	Reserved = 0
0-2	Sequencer Register Address

Bits 3-7 — Reserved

Bits 0-2 — These bits contain the binary value indicating the register where data is to be written.

Reset Register

This is a read/write register pointed to when the address register is loaded with a value of 00H. Data is written to this register at address 03C5 hex.

Bit	Function
2-7	Reserved = 0
1	Synchronous Reset
0	Asynchronous Reset

Bits 2-7 — Reserved

Bit 1 — A 0 in this bit location causes the sequencer to synchronously clear and halt. Both Bits 0 and 1 of this register must be set to 1 in order for the sequencer to operate. To prevent data loss, this bit must be set to 0 during an active display time, and prior to changing either bit 3 or bit 0 of the Clocking Mode Register, or Bit 3 or Bit 2 of the Miscellaneous Output Register.

Bit 0 — A 0 in this bit location causes the sequencer to asynchronously clear and halt. A 1 causes the sequencer to run unless Bit 1 of this register is set to 0. Resetting the sequencer with this bit can cause data loss in the DRAMs.

Clocking Mode Register

This is a read/write register accessed when the value in Bits 0-2 of the Sequencer Address Register are set to 01H. The data for this register is written to address 03C5 hex.

Bit	Function
6-7	Reserved = 0
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved = 0
0	8/9 Dot Clocks

Bits 6-7 — Reserved

Bit 5 — A 1 in this location turns off the screen. A 0 selects normal video operations. This bit can be used for rapid full screen updates.

Bit 4 — A 0 in this bit causes the video serializers to be loaded every character clock. When set to a 1, the serializers are loaded every fourth character clock.

Bit 3 — A 0 in this bit location causes normal dot clocks derived from the sequencer's master input to be used. A 1 in this location causes the master clock to be divided by 2 to generate the dot click. Dot clock divided by 2 is used for both 320 and 360 horizontal modes.

Bit 2 — When the bit in this location and Bit 4 of this register are set to 0, the video serializers are reloaded every character clock. When this bit is set to 1, they are loaded every other clock.

Bit 1 — Reserved

Bit 0 — A 0 in this location causes the sequencer to produce character clocks that are 9 dots wide. A 1 causes the sequencer to produce character clocks that are 8 dots wide. The 9 dot mode is for alphanumeric modes only.

Map Mask Register

This is a read/write register and is accessed when the value in the address register is 02H. The data is written to this register at address 03C5 hex.

Bit	Function
4-7	Reserved = 0
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits 4-7 — Reserved

Bits 0-3 — A 1 in these bit locations enables the corresponding map to be read or written by the microprocessor. With all bits set to 1, the microprocessor can write one 32-bit wide word of data in one operation.

Character Map Select Register

This is a read/write register that is accessed when the address register is loaded with a value of 03H. Data is written to this register at address 03C5 hex.

Bit	Function
6-7	Reserved = 0
5	Character Map Select High Bit A
4	Character Map Select High Bit B
2-3	Character Map Select A
0-1	Character Map Select B

Bits 6-7 — Reserved

Bit 5 — See bits 2 and 3

Bit 4 — See bits 0 and 1

Bits 2-3 — These bits in combination with Bit 5 selects the part of Map 2 used to generate alphanumeric characters when Bit 3 of the attribute byte is set to 1. The following chart shows the portion of Map 2 selected.

Bit 5	Bit 3	Bit 2	Map Selected	Portion Location
0	0	0	0	First 8K
0	0	1	1	Third 8K
0	1	0	2	Fifth 8K
0	1	1	3	Seventh 8K
1	0	0	4	Second 8K
1	0	1	5	Fourth 8K
1	1	0	6	Sixth 8K
1	1	1	7	Eighth 8K

In alphanumeric modes, Bit 3 is normally used to turn the foreground intensity on or off. This bit can be used as a switch bit between character sets when the following conditions are met.

- Bit 1 of the Memory Mode Register must be set to 1.
- Character Map Select A does not equal Character Map Select B.

If either one of these conditions is not true, the first 16K of Map 2 is used.

Bits 0-1 — These bits in combination with Bit 4 selects the part of Map 2 used to generate alphanumeric characters when Bit 3 of the attribute byte is set to 0. The following chart shows the portion of Map 2 selected.

Bit 4	Bit 1	Bit 0	Map Selected	Portion Location
0	0	0	0	First 8K
0	0	1	1	Third 8K
0	1	0	2	Fifth 8K
0	1	1	3	Seventh 8K
1	0	0	4	Second 8K
1	0	1	5	Fourth 8K
1	1	0	6	Sixth 8K
1	1	1	7	Eighth 8K

Memory Mode Register

This is a read/write register that is accessed when the address register is loaded with a value of 04H. Data is written to this register at address 03C5 hex.

Bit	Function
4-7	Reserved = 0
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved = 0

Bits 4-7 — Reserved

Bit 3 — A 0 in this location causes the microprocessor addresses to sequentially access data in the bit map by using the Map Mask Register. A 1 causes the two low-order bits to select the map that is to be accessed by the following method.

A0	A1	Map Selected
0	0	0
1	0	1
0	1	2
1	1	3

Bit 2 — A 0 in this location causes even microprocessor addresses to access Maps 0 and 2, while odd addresses access Maps 1 and 3. A 1 in this location causes addresses to access data sequentially in the bit map.

The maps are accessed according to the value set in the Map Mask Register.

Bit 1 — A 1 in this location indicates that more than 64K of video memory is available. This bit must be set to allow use of the 256K of video memory and to enable the character map selection discussed earlier in this section.

Bit 0 — Reserved

CRT Controller Registers

CRT Controller Address Register

This is a read/write register located at address 03x4 hex, where x is B or D depending on the value of Bit 0 of the Miscellaneous Output register. It is loaded with the binary value of the CRT controller data register where information is to be written. After the address is written to 03x4 hex, the data to be stored in the selected register is written to 03x5 hex. For the remainder of the examples in this section, addresses will be displayed in the same manner as above.

Bit	Function
7	Reserved = 0
6	Reserved = 0
5	Must = 0
4	CRTC Address
3	CRTC Address
2	CRTC Address
1	CRTC Address
0	CRTC Address

Bits 6-7 — Reserved

Bit 5 — Must be set to 0

Bits 0-4 — These bits are the binary value indicating the data register where information is to be written.

Horizontal Total Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 00H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Horizontal Total (-5)

Bits 0-7 — The value placed in these locations specifies the number of characters in a horizontal scan interval, including the retrace time minus 5. This value also directly controls the interval of the horizontal retrace output signal.

Horizontal Display Enable End Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 01H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Horizontal Display Enable End (-1)

Bits 0-7 — The value placed in these locations specifies the number of character positions displayed per horizontal line minus 1.

Start Horizontal Blanking Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 02H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Start Horizontal Blanking

Bits 0-7 — The value placed in these locations specifies when the horizontal blanking output signal becomes active.

End Horizontal Blanking Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 03H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Must Be set to 1
6	Display Enable Skew Control
5	Display Enable Skew Control
0-4	End Blanking

Bit 7 — This bit must be set to 1

Bits 5-6 — The value of these two bits is used to determine the display enable skew. Skew control is required for the CRT controller to have enough time to access the display buffer, character generator font, and the horizontal PEL panning register located in the Attribute Controller. Each of these accesses necessitates the display enable signal to be skewed one character clock. This is done to allow the video output to remain in synchronization with the horizontal and vertical retrace signals. The following chart shows the bit values and their associated skew amount.

Bit 5	Bit 6	Skew
0	0	0 Character Clock Skew
1	0	1 Character Clock Skew
0	1	2 Character Clock Skew
1	1	3 Character Clock Skew

Bits 0-4 — These bits represent the value of the six least significant bits of the horizontal character counter value at which the horizontal blanking signal becomes inactive. The algorithm used to obtain the proper blanking signal width is as follows:

> Value of the Start Blanking Register + the width of the character blanking signal in character clock units = 6-bit value that should be programmed into the End Horizontal Blanking Register.

Bit number 5 of this value is located in the End Horizontal Retrace Register. This register is located at address index 05.

Start Horizontal Retrace Pulse Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 04H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Start Horizontal Retrace Pulse

Bits 0-7 — The value placed in these locations specifies the character position at which horizontal retrace signal becomes active. This value is used to center the screen horizontally.

End Horizontal Retrace Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 05H. Data is written to this register at address 03x5 hex.

Bit	Function
7	End Horizontal Blanking Bit 5
5-6	Horizontal Retrace Delay
0-4	End Horizontal Retrace

Bit 7 — This is bit number 5 of the End Horizontal Blanking value. Bits 0-4 are located in the End Horizontal Blanking Register.

Bits 5-6 — The value of these bits is used to control the skew of the horizontal retrace signal. A binary 0 is equal to no horizontal retrace delay.

Bits 0-4 — These bits represent the value of the five least significant bits of the count at which the horizontal retrace signal becomes inactive.

The algorithm used to obtain the proper retrace signal width is as follows:

> Value of the Start Retrace Register + the width of the horizontal retrace signal in character clock units = 5-bit value that should be programmed into the End Horizontal Retrace Register.

Vertical Total Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 06H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Vertical Total (-2)

Bits 0-7 — These are the 8 lower order bits contained in a 10 bit register representing the binary value of the number of raster scans on the screen -2, including the vertical retrace period. Bits 8 and 9 of this value are found in the CRT Controller Overflow Register covered next. This 10 bit value is used to control the period of the vertical retrace signal.

CRT Controller Overflow Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 07H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7 — This is Bit 9 of the Vertical Retrace Start Register located at CRT Controller Address 10.

Bit 6 — This is Bit 9 of the Vertical Display Enable End Register located at CRT Controller Address 12.

Bit 5 — This is Bit 9 of the Vertical Total Register located at CRT Controller Address 06.

Bit 4 — This is Bit 8 of the Line Compare Register located at CRT Controller Address 18.

Bit 3 — This is Bit 8 of the Start Vertical Blank Register located at CRT Controller Address 15.

Bit 2 — This is Bit 8 of the Vertical Retrace Start Register located at CRT Controller Address 10.

Bit 1 — This is Bit 8 of the Vertical Display Enable End Register located at CRT Controller Address 12.

Bit 0 — This is Bit 8 of the Vertical Total Register located at CRT Controller Address 06.

Preset Row Scan Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 08H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Reserved = 0
6	Byte Panning Control
5	Byte Panning Control
0-4	Starting Row Scan Count After Vertical Retrace

Bit 7 — Reserved

Bits 5-6 — These bits represent the value used to control panning in multiple shift modes, and are required for PEL panning operations. The PEL panning register in the Attribute controller section allows panning of up to 7 or 8 separate PELs. In single byte shift modes, the CRT controller start address is incremented and attribute panning is reset to 0, in order to pan to the next higher PEL (8 or 9). In multiple shift modes, these bits are used as extensions to the attribute PEL panning register. These bits should normally be set to 0.

Bits 0-4 — These bits represent the starting row scan count after a vertical retrace. The row scan counter is incremented each horizontal retrace time, until a maximum row scan occurs. At this time the row scan is cleared.

Maximum Scan Line Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 09H. Data is written to this register at address 03x5 hex.

Bit	Function
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
0-4	Maximum Scan Line

Bit 7 — When the bit in this location is set to a 1, 200 to 400 line conversion is done. The clock in the row scan counter is divided by 2, effectively causing the 200 line modes to be displayed as 400 lines. When this bit is equal to 0, the clock of the row scan counter is equal to the horizontal scan rate, and no conversion takes place.

Bit 6 — This is Bit 9 of the Line Compare Register located at CRT controller Address 18.

Bit 5 — This is Bit 9 of the Start Vertical Blank Register located at CRT controller Address 15.

Bits 0-4 — These bits represent the binary value of the number of scan lines per character row. The number to be loaded into these bit locations is the maximum row scan number -1.

Cursor Start Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0AH. Data is written to this register at address 03x5 hex.

Bit	Function
6-7	Reserved = 0
5	Cursor Off
0-4	Row Scan Cursor Begins

Bits 6-7 — Reserved

Bit 5 — A 1 in this bit location turns the cursor off. A 0 turns the cursor on.

Bits 0-4 — The value loaded into this register represents the row scan of the character line where the cursor is to begin. This number is one less than the starting cursor row scan.

Cursor End Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0BH. Data is written to this register at address 03x5 hex.

Bit	Function
7	Reserved = 0
5-6	Cursor Skew Control
0-4	Row Scan Cursor Ends

Bit 7 — Reserved

Bits 5-6 — The value loaded into these bit locations are used to control cursor skew. The following chart shows the number of clocks the cursor is delayed.

Bit 5	Bit 6	Skew
0	0	0 Character Clock Skew
1	0	1 Character Clock Skew
0	1	2 Character Clock Skew
1	1	3 Character Clock Skew

Bits 0-4 — These bits represent the row scan of the character line where the cursor is to end.

Start Address High Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0CH. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	High Order Start Address

Bits 0-7 — These are the high order 8 bits of the 16 bit value used for the start address, which is the first address after the vertical retrace on each screen refresh.

Start Address Low Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0DH. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	High Order Start Address

Bits 0-7 These are the low order 8 bits of the 16 bit value used for the start address, which is the first address after the vertical retrace on each screen refresh.

Cursor Location High Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0EH. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	High Order Cursor Location

Bits 0-7 — These bits represent the high order 8 bits of the cursor location.

Cursor Location Low Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 0FH. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Low Order Cursor Location

Bits 0-7 — These bits represent the low order 8 bits of the cursor location.

Vertical Retrace Start Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 10H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Low Order Vertical Retrace Pulse

Bits 0-7 — These bits represent the low order 8 bits of the vertical retrace start position. These values must be programmed in horizontal scan lines. Bit 8 of this value is located in the CRT Controller Overflow Register located at CRT Controller Address 07.

Vertical Retrace End Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 11H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Protect Registers 0-7
6	5 Refresh Cycles
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
0-3	Vertical Retrace End

Bit 7 — A 1 in this bit location disables writing to CRT controller registers 0-7. A 0 in this location enables writing to these registers. The line compare bit in register 07 is not protected.

Bit 6 — A 1 in this bit location causes 5 DRAM refresh cycles for each horizontal line. A 0 in this location selects 3 refresh cycles. The selection of 5 refresh cycles allows the VGA to operate with slow sweep displays.

Bit 5 — A 0 in this bit location enables a vertical retrace interrupt on interrupt level 2 (IRQ2). This can be a shared interrupt level, so Bit 7 of the Input Status Register 0 should be checked to determine if the VGA generated the interrupt. Do not change the value of the other bits in this register.

Bit 4 — A 0 in this bit location clears a vertical retrace interrupt. Do not change the other bits in this register.

Bits 0-3 — These bits represent the count at which time the vertical retrace signal is to become inactive. This value is programmed in units of horizontal scan lines. The following algorithm is used in determining the width of the vertical retrace signal.

> The value of the Start Vertical Retrace Register + the width of the vertical retrace signal in horizontal scan units = 4-bit value that should be programmed into the End Horizontal Retrace Register.

Vertical Display Enable End Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 12H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Low Order Vertical Display Enable End (-1)

Bits 0-7 — These bits represent the lower order 8 bits of a 10 bit value which defines the vertical display end position. This is the position at which the scan line that ends the active video area of the screen is located. It is programmed with the total number of lines minus one.

Bits 8 and 9 of this register is contained in the CRT Controller Overflow Register located at CRT Controller Address 07.

Offset Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 13H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Logical Line Width of the Screen

Bits 0-7 — The value of these bits represents the logical line width of the display screen. The starting memory address for the following character row is usually larger than the current character row by two or four times this value. This register is loaded with a word address. This address can be either a word, or a doubleword address, depending on how the CRT controller is clocked.

Underline Location Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 14H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Reserved = 0
6	Doubleword Mode
5	Count By 4
0-4	Horizontal Scan Line Where Underline Will Appear

Bit 7 — Reserved

Bit 6 — When the bit in this location is set to a 1, memory addresses are doubleword addresses.

Also see the description of the CRT Mode Control Register at CRT Controller address 17.

Bit 5 — When the bit in this location is set to a 1, The character clock used to clock the memory address counter is divided by 4. This bit is set when doubleword addresses are used.

Bits 0-4 — These bits represent the binary value of the row scan where the underline appears. This value is 1 less than the scan line number desired.

Start Vertical Blanking Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 15H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Start Vertical Blanking (-1)

Bits 0-7 — These bits represent the lower order 8 bits of a 10 bit register which is one less than the value of the horizontal scan line where the blanking signal becomes active.

Bit 8 is located in the CRT Controller Overflow Register located at CRT Controller Address 07.

Bit 9 is located in the Maximum Scan Line Register located at CRT Controller Address 09.

End Vertical Blanking Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 16H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	End Vertical Blanking

Bits 0-7 — These bits represent the value of the horizontal scan line where the blanking signal becomes inactive in scan lines. This value is obtained by the following algorithm.

The value of the Start Vertical Blank Register -1 plus the width of the vertical blank signal in horizontal scan lines = 8-bit value that should be programmed into the End Vertical Blank Register.

CRT Controller Mode Control Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 17H. Data is written to this register at address 03x5 hex.

Bit	Function
7	Hardware Reset
6	Word/Byte Mode
5	Address Wrap
4	Reserved = 0
3	Count By Two
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CMS 0

Bit 7 — A 0 in this bit location causes the horizontal and vertical retrace to clear. A 1 causes the horizontal and vertical retrace to be enabled. This bit does not reset any other registers or outputs.

Bit 6 — A 0 in this bit location selects word mode and causes the memory address counter bits to shift down one bit, placing the most significant bit of the counter on the least significant bit of the memory address outputs. A 1 in this bit location selects the byte address mode.

> Bit 6 of the End Vertical Blanking register also controls addressing. When it is 0, Bit 6 of above has control. When set to a 1, the addressing is shifted 2 bits.

Bit 5 — This bit selects whether Bit 13 or Bit 15 of the memory address counter will appear on the memory address Bit 0 output pin in the word address mode. If not in the word address mode, Bit 0 of the address counter appears on the memory address Bit 0 output pin. A 1 in this bit selects Bit 15, and in the odd/even mode, Bit 15 should be selected as 256K of video memory installed on the system board. Bit 13 is selected when only 64K of video memory is available on the system board.

Bit 4 — Reserved

Bit 3 — A 0 in this bit location causes the memory address counter to be clocked by the character clock input. A 1 in this bit location causes the address counter to be clocked by the character clock divided by 2. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 — This bit is used to select horizontal retrace or horizontal retrace divided by 2 as the clock input used to control the vertical timing counter. If the vertical counter is clocked with the horizontal retrace divided by 2, the vertical retrace is doubled to 2048 horizontal scan lines. A 0 in this bit location selects horizontal retrace. A 1 in this location selects horizontal retrace divided by 2.

Bit 1 — A 0 in this bit location selects row scan counter bit 1 on the address counter memory address Bit 14 output pin. A 1 in this bit location selects address counter Bit 14 on the memory address bit address Bit 14 output pin.

Bit 0 — This is a Compatibility Mode Select (CMS) bit. When this bit is equal to 0, row scan address Bit 0 is substituted for memory address Bit 13 during active display times. A 1 in this bit location enables memory address Bit 13 to appear on the memory address output Bit 13 signal of the CRT Controller.

Line Compare Register

This is a read/write register that is accessed when the CRT controller address register is loaded with a value of 18H. Data is written to this register at address 03x5 hex.

Bit	Function
0-7	Line Compare Target

Bits 0-7 — These bits represent the lower order 8 bits of the compare target. When the vertical retrace counter reaches this value, the internal start of the line counter is cleared.

Bit 8 of this value is located in the Overflow Register located at CRT Controller Address 07.

Bit 9 of this value is located in the Maximum Scan Line Register located at CRT Controller Address 09.

Graphics Controller Registers

Graphics Address Register

This is a read/write register located at address 03CE hex. It is loaded with the binary value of the Graphics controller data register where information is to be written. After the address is written to 03CE hex, the data to be stored in the selected register is written to 03CF hex.

Bit	Function
4-7	Reserved = 0
0-3	Graphics Address

Bits 4-7 — Reserved

Bits 0-3 — These bits represent the binary value of the Graphics Controller Register address where data is to be written.

Set/Reset Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 00H. Data is written to this register at address 03CF hex.

Bit	Function
4-7	Reserved = 0
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits 4-7 — Reserved

Bits 0-3 — The bits in these locations represent the value that is written to all 8 bits of the respective memory map, when write mode 0 is selected and the Set/Reset enable bit for that map is set.

Enable Set/Reset Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 01H. Data is written to this register at address 03CF hex.

Bit	Function
4-7	Reserved = 0
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits 4-7 — Reserved

Bits 0-3 — When any of these bits are set to a 1, the respective memory map is written with the value of the Set/Reset Register, when in Write Mode 0. When any of these bits are set to 0, and write mode is 0, the respective map is written with the value of the microprocessor data.

Color Compare Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 02H. Data is written to this register at address 03CF hex.

Bit	Function
4-7	Reserved = 0
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits 4-7 — Reserved

Bits 0-3 — The bits in these locations represent a 4-bit color value to be compared. If the microprocessor sets read mode 1 in the graphics section and performs a memory read, the data that is returned from the memory cycle will be equal to a 1 in each bit position where the 4 maps are equal to the value in the Color Compare Register. This value represents the value that all bits of the corresponding map's byte are compared with. Each of the 8 bits of the selected byte are then compared across the four maps, and a 1 is returned for each bit where all four maps equal their respective color compare values.

Data Rotate Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 03H. Data is written to this register at address 03CF hex.

Bit	Function
5-7	Reserved = 0
4	Function Select
3	Function Select
2	Rotate Count 2
1	Rotate Count 1
0	Rotate Count 0

Bits 5-7 — Reserved

Bits 3-4 — These bits specify what type of logical operation is to be performed on data already present in the microprocessor data latches. Data that is written to the video memory can be operated logically with data already existing in the system microprocessor latches. The data can consist of any of the choices available in the Write Mode Register, except for the system microprocessor latches, which cannot be modified. The following chart shows the logical operations selected by these bits.

Bit 3	Bit 4	Function
0	0	Data Unmodified
1	0	Data ANDed With Latched Data
0	1	Data ORed With Latched Data
1	1	Data XORed With Latched Data

Bits 0-2 — The bits in these locations represent the binary encoded value of how many positions the system microprocessor data bus is to be right rotated during a video memory write. This operation occurs when the write mode is 0. To write data in a non-rotated fashion, the count must be set to 0.

Read Map Select Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 04H. Data is written to this register at address 03CF hex.

Bit	Function
2-7	Reserved = 0
1	Map Select 1
0	Map Select 0

Bits 2-7 — Reserved

Bits 0-1 — The bits in these locations represent the binary encoded value of the memory map from which the microprocessor reads data.

Graphics Mode Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 05H. Data is written to this register at address 03CF hex.

Bit	Function
7	Reserved = 0
6	256 Color Mode
5	Shift Register Mode
4	Odd/Even
3	Read Type
2	Reserved = 0
0-1	Write Mode

Bit 7 — Reserved

Bit 6 — A 0 in this bit position causes Bit 5 to control the loading of the shift registers. A 1 in this bit position causes the shift registers to be loaded in a way that supports the 256 color mode.

Bit 5 — A 1 in this bit position causes the shift registers in the graphics section to format the serial bit stream with even numbered bits from both maps on the even-numbered maps and the odd-numbered bits from both maps on the odd maps. This bit is used for Modes 4 and 5.

Bit 4 — A 1 in this bit position designates the odd/even addressing mode. The value of this bit normally is the same as the value of Bit 2 of the Memory Mode Register in the Sequencer section.

Bit 3 — When this bit is set to 0, the microprocessor reads data from the memory map chosen by the Read Map Select Register, unless Bit 3 of the Sequencer Memory Mode Register equals 1. In this case, the Read Map Select Register has no effect. When this bit is set to a 1, the system microprocessor read the results of a compare of the four memory maps and Color Compare Register.

Bit 2 — Reserved

Bits 0-1 — These bit functions are defined as follows.

Bit 0	Bit 1	Function
0	0	Each of the memory maps is written with the data that has been rotated by the number of counts placed in the Rotate Register, unless the Set/Reset has been enabled for the map. The maps for which the Set/Reset has been enabled are loaded with the 8-bit value contained in the Set/Reset Register for that map.
1	0	Each of the memory maps is loaded with the value in the system microprocessor latches, which are loaded by a microprocessor read operation.
0	1	Memory map *n* (0-3) is loaded with 8 bits of the value of data bit *n*.
1	1	Each map is loaded with the 8-bit value loaded in the Set/Reset Register for that map. Rotated microprocessor data is ANDed with the data in the Bit Mask Register to produce an 8-bit value that performs the same function as the Bit Mask Register does in Modes 0 and 2.

Miscellaneous Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 06H. Data is written to this register at address 03CF hex.

Bit	Function
4-7	Reserved = 0
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits 4-7 — Reserved

Bits 2-3 — The value of these bits is used to control the mapping of the regenerative buffer into the system microprocessor address space. These addresses are defined as follows.

Bit 2	Bit 3	Function
0	0	Hex A0000 for 128K Bytes
1	0	Hex A0000 for 64K Bytes
0	1	Hex B0000 for 32K Bytes
1	1	Hex B8000 for 32K Bytes

Bit 1 — When the value of this bit is set to 1, the system microprocessor address bit 0 is replaced by a high order bit and odd/even maps are selected with odd/even values of the system microprocessor Bit A0, respectively.

Bit 0 — A 1 in this bit location selects the graphics mode. When set in graphics mode, the character generator address latches are disabled.

Color Don't Care Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 07H. Data is written to this register at address 03CF hex.

Bit	Function
4-7	Reserved = 0
3	Map 3 = Don't Care
2	Map 2 = Don't Care
1	Map 1 = Don't Care
0	Map 0 = Don't Care

Bits 4-7 — Reserved

Bits 0-3 — When any of Bits 0-3 respectively are set to a 1, it indicates that the respective map is to participate in the color compare cycle. When any of Bits 0-3 respectively are set to 0, it indicates that the respective map does not participate in the color compare cycle.

Bit Mask Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 08H. Data is written to this register at address 03CF hex.

Bit	Function
0-7	Bit Mask Enable

Bits 0-7 — Any of these bits being set to 0 causes the corresponding bit in each map to be immune to change provided that the location being written was the last location read by the system microprocessor. When any of these bits is set to 1, it allows unrestricted writes to the corresponding bits in the maps. The bit mask applies to Modes 0 and 2, and also applies to all maps simultaneously.

Attribute Controller Registers

Attribute Address Register

This is a read/write register located at address 03C0 hex. It is loaded with the binary value of the Attribute controller data register where information is to be written. After the address is written to 03C0 hex, the data to be stored in the selected register is written to 03C0 hex, and read from 03C1 hex.

Bit	Function
6-7	Reserved = 0
5	Palette Address Source
0-4	Attribute Controller Address

Bits 6-7 — Reserved

Bit 5 — This bit must be cleared to 0 when loading the Color Palette registers. During normal operation this bit is set to a 1. This allows the video memory data to access the palette registers.

Bits 0-4 — These bits represent the binary value of the Attribute Controller Register address where data is to be written.

The Attribute Controller register does not have an address bit input to control selection of the address and data registers. An internal address flip-flop is used to control selection of either the address or data registers. To initialize the flip-flop, an IOR instruction is issued to the Attribute Controller at address 03BA hex or 03DA hex. This action clears the flip-flop and selects the address register. After the address register has been loaded with an Out to address 03C0 hex, the next Out instruction will load the Data register. The flip-flop toggles each time an Out instruction is issued to the Attribute Controller. It does not toggle on In instructions used to read address 0C31 hex.

Palette Registers 00 Through FF

These are read/write registers that are accessed when the Attribute controller address register is loaded with a value of 00H-0FH. Data is written to these registers at address 03C0 hex and read from these registers at address 03C1 hex.

Bit	Function
6-7	Reserved = 0
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 6-7 — Reserved

Bits 0-5 — These bits permit a dynamic mapping between the text attribute or graphic color input and the color being displayed on the screen. A 1 in these bit locations selects the appropriate color. These internal palette register values are sent to the DAC, where they serve as addresses into the DAC registers. These registers should only be modified during the vertical retrace interval.

Attribute Mode Control Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 10H. Data is written to this register at address 03C0 hex and read from address 03C1 hex.

Bit	Function
7	P4,P5 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved = 0
3	Background Intensity or Blink
2	Enable Line Graphics Character
1	Mono Emulation
0	Graphics/Alpha Mode

Bit 7 — When the bit in this location is a 0, P4 and P5 are the outputs of the Palette registers. When this bit is set to a 1, P4 and P5 are Bits 0

and 1 of the Color Select Register. P4 and P5 are the digital video bits that are sent off chip to the DAC.

Bit 6 — When the bit in this location is equal to a 1, the video bit-stream is sampled to allow 8 bits to be available to select colors in the 256 color mode (hex 13). This bit should be set to a 0 in all other modes.

Bit 5 — When the bit in this location is equal to a 0, line compare has no effect on the output of the PEL Panning Register. When this bit is equal to a 1, a successful line compare in the CRT controller causes the output of the PEL Panning Register to be 0 until the Vertical Sync signal becomes active. At this time the output returns to it's programmed value.

Bit 4 — Reserved

Bit 3 — A 0 in this bit location selects the background intensity of the attribute input. A 1 in this bit location enables blink in alphanumeric modes. This bit must be set to 1 for blinking graphics modes.

Bit 2 — When the bit in this location is equal to 0, the ninth dot will be the same as the background. A 1 in this bit position enables special line graphics codes for IBM monochrome emulation. This causes the ninth dot to be equal to the eighth dot of the character.

Bit 1 — A 1 in this bit position indicates that mono emulation mode is set. A 0 in this bit position indicates that color emulation is selected.

Bit 0 — A 0 in this bit position selects the alphanumeric mode. A 1 in this bit location selects the graphics mode.

Overscan Color Register

This is a read/write register that is accessed when the Attribute Address register is loaded with a value of 11H. Data is written to this register at address 03C0 hex and read from address 03C1 hex.

Bit	Function
7	P7
6	P6
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 0-7 — This 8-bit value is used to determine the border (overscan) color to be displayed on the screen.

Color Plane Enable Register

This is a read/write register that is accessed when the Attribute Address register is loaded with a value of 12H. Data is written to this register at address 03C0 hex and read from address 03C1 hex.

Bit	Function
6-7	Reserved = 0
4-5	Video Status Mux
0-3	Enable Color Plane

Bits 6-7 — Reserved

Bits 4-5 — These bits are used to select two of the eight color outputs to be available on the status port. The following chart shows the combinations available.

Color Plane Register		Input Status Register 1	
Bit 4	**Bit 5**	**Bit 4**	**Bit 5**
0	0	P0	P2
1	0	P4	P5
0	1	P1	P3
1	1	P6	P7

Bits 0-3 — When any of these bits is set to a 1, it enables the respective memory color plane.

Horizontal PEL Panning Register

This is a read/write register that is accessed when the Attribute Address register is loaded with a value of 13H. Data is written to this register at address 03C0 hex and read from address 03C1 hex.

Bit	Function
4-7	Reserved = 0
0-3	Horizontal PEL Panning

Bits 4-7 — Reserved

Bits 0-3 — These four bits determine the number of picture elements (PELs) to shift the video data horizontally to the left. In mono emulation alpha modes, and VGA modes 0, 1, 2, and 3 the image can be shifted a maximum of 8 PELs. In 256 color mode, the image can be shifted a maximum of 3 PELs and in all other modes the image can be shifted a maximum of 7 PELs.

PEL Panning Register Value	Number of PELs Shifted to the Left		
	0+, 1+, 2+, 3+, 7, 7+	All Other Modes	Mode Hex 13
0	1	0	0
1	2	1	—
2	3	2	1
3	4	3	—
4	5	4	2
5	6	5	—
6	7	6	3
7	8	7	—
8	0	—	—

Shift Table

Color Select Register

This is a read/write register that is accessed when the Attribute Address register is loaded with a value of 14H. Data is written to this register at address 03C0 hex and read from address 03C1 hex.

Bit	Function
4-7	Reserved = 0
3	Color 7
2	Color 6
1	Color 5
0	Color 4

Bits 4-7 — Reserved

Bits 2-3 — In all modes except for the 256 color mode, these bits are the two high order bits of the 8-bit digital color value sent off-chip to the DAC. In the 256 color mode, the 8-bit attribute contained in video memory becomes the 8-bit digital color value sent to the DAC.

Bits 0-1 — These bits can be used in place of the P4 and P5 bits contained in the Attribute Palette registers. They are used to form the 8-bit digital value sent to the DAC.

Compatibility Registers

The following registers are provided to maintain compatibility with existing CGA, MDA, and Hercules hardware and the software written for those adapters. Except for the Status Register, these are write only registers located at the same addresses as those associated with CGA, MDA, and Hercules adapters.

AT&T/M24 Register

This is a write-only register located at address 03DE hex. It is used to control the 640 x 400 AT&T graphics mode. All bits are set to 0 by reset. This register is enabled by setting Bit 7 of the Video Select register in the Enhanced Feature Registers to a 1.

Bit	Function
7	Reserved
6	Whit/Blue Underline
5	Reserved
4	Reserved
3	Memory Map Displayed
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7 — Reserved

Bit 6 — A 1 in this bit location causes underlined characters to be displayed in white. A 0 in this bit location causes underlined characters to be displayed in blue.

Bits 4-5 — Reserved

Bit 3 — A 1 in this bit location displays 16KB of memory starting at address BC000H. A 0 in this bit location displays 16KB of memory starting at address B8000H.

Bit 2 — Reserved

Bit 1 — A 1 in this bit location selects an alternate character font from RAM plane 3. A 0 in this bit location selects the standard character font from RAM plane 2.

Bit 0 — A 1 in this bit location selects 400 lines to be displayed, if this register is enabled. A 0 in this bit location selects a simulated 200 lines to be displayed.

Hercules Register

The Hercules Register is a 2-bit write-only register located at address 03BF hex. The bits in this register only affect operation in the 6845 Mode. Both bits are set to 0 by reset, or when put in the color mode.

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Force Display Page
0	Force Alpha

Bits 2-7 — Reserved

Bit 1 — A 1 in this bit position allows Bit 7 of the IBM Mode register at 03B8H/03D8H to be set, and upper video memory to be displayed at address B8000 hex. A 0 in this bit location causes Bit 7 of the IBM Mode register at 03B8H/03D8H to be locked, and does not allow it to be set. The second page of video memory cannot be accessed or displayed and the first page of video memory is mapped to address B0000 Hex.

Bit 0 — A 1 in this bit location causes Bit 1 of the IBM Mode register at 03B8H/03D8H to be allowed to be set to a 1, selecting Graphics Mode. A 0 in this bit location will cause Bit 1 of the IBM Mode register at 03B8H/03D8H to be locked at 0, forcing Alpha mode.

Mode Control Register

This is a write-only register that is accessed when the data is written to address 03B8 hex for monochrome, and 03D8 hex for color.

Monochrome Operation Address 03B8H	
Bit	**Function**
7	Reserved
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved
0	High Resolution Mode

Bits 6-7 — Reserved

Bit 5 — A 1 in this bit location enables the character blink, a 0 in this bit location disables the character blink.

Bit 4 — Reserved

Bit 3 — A 1 in this bit location enables video, a 0 in this bit location disables it.

Bits 1-2 — Reserved

Bit 0 — A 1 in this bit location enables high resolution, a 0 in this bit location disables high resolution.

Color Operation Address 03D8H	
Bit	**Function**
7	Reserved
6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bits 6-7 — Reserved

Bit 5 — A 1 in this bit location enables the Blink Attribute. A 0 in this bit location disables the Blink Attribute.

Bit 4 — A 1 in this bit location selects the 640 x 200 B/W Graphics Mode. A 0 in this bit location deselects the 640 x 200 B/W Graphics Mode.

Bit 3 — A 1 in this bit location enables the video signal. A 0 in this bit location disables the video signal.

Bit 2 — A 1 in this bit location selects the B/W mode. A 0 in this bit location selects the color mode.

Bit 1 — A 1 in this bit location selects the 320 x 200 Graphics Mode. A 0 in this bit location selects the Alpha Mode.

Bit 0 — A 1 in this bit location selects the 80 x 25 Alpha Mode. A 0 in this bit location selects the 40 x 25 Alpha Mode.

Color Select Register

This is a write-only register which is accessed by writing to address 03D9 hex.

Bit	Function
7	Reserved
6	Reserved
5	Graphics Mode Color Select
4	Alternate Color Select
3	Border Intensity
2	Red Border In Alpha Mode
1	Green Border In Alpha Mode
0	Blue Border In Alpha Mode

Bits 6-7 — Reserved

Bit 5 — When the bit in this location is set to a 1, the colors in 320 x 200 Graphics Mode are determined as follows:

C1	C0	Set Selected
0	0	Background (Defined by Bits 0-3 of port hex 03D9)
0	1	Cyan
1	0	Magenta
1	1	White

When the bit in this location is set to a 0, the colors in 320 x 200 Graphics Mode are determined as follows:

C1	C0	Set Selected
0	0	Background (Defined by Bits 0-3 of port hex 03D9)
0	1	Green
1	0	Red
1	1	Brown

Bit 4 — A 1 in this bit location selects the alternate color set in the Graphics Mode. A 0 in this bit location selects the background color in the Alpha Mode.

Bit 3 — A 1 in this bit location selects the intensified border in Alpha Mode, intensified background in 320 x 200 Graphics Mode, and intensified foreground in 640 x 200 Graphics Mode.

Bit 2 — A 1 in this bit location selects a red border in Alpha Mode, a red background in 320 x 200 Graphics Mode, and a red foreground in 640 x 200 Graphics Mode.

Bit 1 — A 1 in this bit location selects a green border in Alpha Mode, a green background in 320 x 200 Graphics Mode, and a green foreground in 640 x 200 Graphics Mode.

Bit 0 — A 1 in this bit location selects a blue border in Alpha Mode, a blue background in 320 x 200 Graphics Mode, and a blue foreground in 640 x 200 Graphics Mode.

Status Register

This is a write-only register that is accessed when the data is written to address 03BA hex for monochrome, and 03DA hex for color.

Monochrome Operation Address 03BAH	
Bit	**Function**
7	Vertical Retrace Active
6	Reserved
5	Reserved
4	Reserved
3	B/W Video Active
2	Light Pen Switch
1	Light Pen Trigger
0	Horizontal Retrace Active

Bit 7 — A 1 in this bit location indicates that the vertical retrace in inactive. A 0 in this bit location indicates that the vertical retrace is active.

Bits 4-6 — Reserved

Bit 3 — A 1 in this bit location indicates that the B/W video is active. A 0 in this bit location indicates that the B/W video is inactive.

Bit 2 — A 1 in this bit location indicates that the light pen switch is open. A 0 in this bit location indicates that the light pen switch is closed.

Bit 1 — A 1 in this bit location indicates that the light pen trigger is active, which is set by positive edge or trigger signal. A 0 in this bit location indicates that the light pen has not been triggered.

Bit 0 — A 1 in this bit location indicated that the horizontal retrace signal is active. A 0 in this bit location indicated that the horizontal retrace signal is inactive.

Monochrome Operation Address 03DAH	
Bit	**Function**
7	Vertical Retrace Active
6	Reserved
5	Reserved
4	Reserved
3	Video Retrace Mode
2	Light Pen Switch
1	Light Pen Trigger
0	Display Enable Inactive

Bit 7 — A 1 in this bit location indicates that the vertical retrace in inactive. A 0 in this bit location indicates that the vertical retrace is active.

Bits 4-6 — Reserved

Bit 3 — A 1 in this bit location indicates the video retrace mode is active.

Bit 2 — A 1 in this bit location indicates that the light pen switch is open. A 0 in this bit location indicates that the light pen switch is closed.

Bit 1 — A 1 in this bit location indicates that the light pen trigger is active, which is set by positive edge or trigger signal. A 0 in this bit location indicates that the light pen has not been triggered.

Bit 0 — A 1 in this bit location indicates that the display enable is inactive, and that the border or blanking is active.

Enhanced Feature Registers

The VGA Adapter provides six additional registers that enhance the functions of the basic VGA subsystem. These registers are lock protected and located in the Graphics Controller I/O address space at locations that have not been previously used. To access these registers an index value indicating the register to be written or read is first written to an address register located at I/O address 03CE hex, and data is then read or written from the selected register at address 03CF hex.

The Address Offset, Memory Size, Video Select, CRT Control, and Video Control registers are normally locked on power up. In order to access these registers, the Lock/Status register must be loaded with a value of 05H. These registers then stay unlocked until another value is written to the Lock/Status register.

All registers except for the Memory Size register, Bits 0 and 1, are set to 0 on power up. Bits 0 and 1 of the Memory Size register are latched internally at power on reset from the corresponding video memory data bus pins MD0 and MD1.

Address Offset A Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 09H. Data is written to this register at address 03CF hex. This register contains an offset which gets added to the System Address when accessing 1 megabyte of video memory. Address Offset Register A is the primary Address Offset register and is always enabled.

Bit	Function
7	Reserved
6	Primary Address Offset
5	Primary Address Offset
4	Primary Address Offset
3	Primary Address Offset
2	Primary Address Offset
1	Primary Address Offset
0	Primary Address Offset

Bit 7 — Reserved

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Bits 0-6 — These bits represent the address offset added to the system address when address bit A15 is equal to a 1.

Address Offset B Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0AH. Data is written to this register at address 03CF hex. This register is enabled only when the Memory Size Register Bit 3 is set to a 1. When enabled and the video memory map is A0000H for 128,000 bytes, the system address bit A16 being set to a 1 selects the Alternate Address Offset Register B. Otherwise, system address bit A15 set to a 1 selects the Address Offset Register A.

Bit	Function
7	Reserved
6	Alternate Address Offset
5	Alternate Address Offset
4	Alternate Address Offset
3	Alternate Address Offset
2	Alternate Address Offset
1	Alternate Address Offset
0	Alternate Address Offset

Bit 7 — Reserved

Bits 0-6 — These bits represent the alternate address offset added to the system address when address bit A16 is equal to a 1, the Memory Size Register Bit 3 is equal to a 1, and the Video Memory Map is equal to A0000H for 128,000 bytes.

Memory Size Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0BH. Data is written to this register at address 03CF hex.

Bit	Function
7	Memory Size Select
6	Memory Size Select
5	Memory Map Select
4	Memory Map Select
3	Enable Address Offset Register B
2	Enable Video Memory Bus
1	BIOS ROM Data Path Width
0	BIOS ROM Mapped

Bits 6-7 — These bits are used to define the memory available on the adapter board. The following chart shows the sizes available.

Bit 7	Bit 6	Memory Size
0	0	256 KB VGA
0	1	256 KB PVGA
1	0	512 KB PVGA
1	1	1024 KB PVGA

Bits 4-5 — These bits are used to select the type of memory mapping desired. The following chart shows the mapping options available.

Bit 7	Bit 6	Memory Map
0	0	VGA Mapping
0	1	256 KB in 1 MB space
1	0	512 KB in 1 MB space
1	1	1024KB in a larger space

Bit 3 — This bit is used to enable the Alternate Address Offset Register B. A 1 in this bit location allows system address bit A16 when equal to a 1 to select the Alternate Address Offset Register B, provided video memory map is equal to A0000H for 128,000 bytes. A 0 in this bit location enables the Primary Address Offset Register A.

Bit 2 — A 1 in this bit location selects a 16-bit wide memory bus. A 0 in this location selects an 8-bit wide memory bus.

Bit 1 — A 1 in this bit location selects a 16-bit wide BIOS ROM data path width. A 0 in this bit location selects an 8-bit wide BIOS ROM data path width.

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Bit 0 — A 1 in this bit location allows the BIOS ROM to be mapped out. A 0 in this bit location does not allow the BIOS ROM to be mapped out.

Video Select Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0CH. Data is written to this register at address 03CF hex.

Bit	Function
7	Enable M24 Mode
6	VGA/6845 Mode
5	Character Map Select
4	Character Clock Control
3	Character Clock Control
2	Special Color Underline
1	Third Clock Select
0	Horizontal Sync Timing

Bit 7 — A 1 in this location enables the M24 mode. A 0 in this bit location disables the M24 mode.

Bit 6 — A 1 in this bit location enables the 6845 compatibility mode. A 0 in this bit location enables the VGA mode.

Bit 5 — A 1 in this bit location enables the use of character maps from memory plane 3. A 0 in this bit location enables the use of character maps from memory plane 2.

Bits 3-4 — These bits are used to control the character clock period. The following chart shows the possible selections.

Bit 4	Bit 3	Number Of Dots
0	0	VGA 8 or 9 Dots
0	1	7 Dots For 132 Character Mode
1	0	9 Dots
1	1	10 Dots

Bit 2 — A 1 in this bit location selects a special colored underline using all odd numbered attributes. For example, a 1 causes a blue underline. A 0 in this bit location causes a standard underline.

Bit 1 — A 1 in this bit location allows the selection of a third clock select line, depending on the state of Bit 3 of the configuration register.

If Bit 3 of the power on configuration register is set to 1, the third clock select line is sent to the external clock chip. If Bit 3 is set to 0, the external clock select multiplexor is locked.

Bit 0 — A 1 in this bit location sets horizontal sync timing for 8 or 9 dots per character. A 0 in this bit location sets horizontal sync timing for 16 or 18 dots per character.

CRT Control Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0DH. Data is written to this register at address 03CF hex.

Register locking is controlled by Bits 0, 1, and 5 of this register and Bit 7 of the Vertical Retrace End register. When Bit 7 of the Vertical Retrace End register is equal to a 1, the following CRT Controller registers are write protected as per the VGA definition.

Horizontal Total Register Horizontal
Display Enable End Register
Start Horizontal Blanking Register
End Horizontal Blanking Register
Start Horizontal Retrace Pulse Register
End Horizontal Retrace Pulse Register
Vertical Total Register
CRT Controller Overflow Register

The following chart is provided to give you more information about the five groups of registers that can be locked using the CRT Control Register.

Group 0

These registers are locked if Bit 5 of the CRT Control register is equal to a 1, or Bit 7 of the Vertical Retrace End register is equal to a 1.

Horizontal Total Register
Horizontal Display Enable End Register
Start Horizontal Blanking Register
End Horizontal Blanking Register
Start Horizontal Retrace Pulse Register
End Horizontal Retrace Pulse Register

Group 1

These registers are locked if Bit 1 of the CRT Control register is equal to a 0, and Bit 7 of the Vertical Retrace End register is equal to a 1.

CRT Controller Overflow Register Bit 6
CRT Controller Overflow Register Bit 1

Group 2

These registers are locked if Bit 0 of the CRT Control register is equal to a 1, or Bit 7 of the Vertical Retrace End register is equal to a 1.

Vertical Total Register CRT Controller Overflow Register Bit 7
CRT Controller Overflow Register Bit 5
CRT Controller Overflow Register Bit 3
CRT Controller Overflow Register Bit 2
CRT Controller Overflow Register Bit 0

Group 3

These registers are locked if Bit 0 of the CRT Control register is equal to a 1.

Maximum Scan Line Register Bit 5
Vertical Retrace Start Register
Vertical Retrace End Register Bits 0-3
Start Vertical Blanking Register
End Vertical Blanking Register

Group 4

These registers are locked if Bit 5 of the CRT Control register is equal to a 1.

CRT Controller Mode Control Register Bit 2	
Bit	**Function**
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Convert
3	Bit 8 Convert
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

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Bit 7 — A 1 in this bit location locks the vertical sync. polarity as programmed in the Miscellaneous Output Register Bit 7. A 0 in this bit location does not lock the vertical sync. polarity as programmed in the Miscellaneous Output Register Bit 7.

Bit 6 — A 1 in this bit location locks the horizontal sync. polarity as programmed in the Miscellaneous Output Register Bit 6. A 0 in this bit location does not lock the horizontal sync. polarity as programmed in the Miscellaneous Output Register Bit 6.

Bit 5 — A 1 in this bit location locks the horizontal timing. A 0 in this bit location does not lock horizontal timing. This locks the contents of registers in groups 0 and 4 and prevents applications software from unlocking the group 0 registers by setting Bit 7 of the Vertical Retrace End register to 0.

Bit 4 — A 1 in this bit location converts Bit 9 of the CRT Controller Memory Address High register to Bit 9 of the Cursor Location High register. A 0 in this bit location does not convert these bits.

Bit 3 — A 1 in this bit location converts Bit 8 of the CRT Controller Memory Address High register to Bit 8 of the Cursor Location High register. This bit is used to enable palette registers in 6845 mode. A 0 in this bit location does not convert these bits.

Bit 2 — A 1 in this bit location causes the values found in the Cursor Start, Cursor Stop, Preset Row Scan, and Maximum Scan Line registers to be multiplied by 2. A 0 in this bit location causes the values in these registers not to be multiplied by 2.

Bit 1 — A 1 in this bit location prevents applications software from unlocking the group 1 registers by setting Bit 7 of the Vertical Retrace End register to 1.

Bit 0 — A 1 in this bit location locks the vertical timing. A 0 in this bit location does not lock horizontal timing. This locks the contents of registers in groups 2 and 3 and prevents applications software from unlocking the group 2 registers by setting Bit 7 of the Vertical Retrace End register to 0.

Video Control

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0EH. Data is written to this register at address 03CF hex.

Bit	Function
7	BLINKN Control
6	Tristate HSYNC, VSYNC, BLINKN
5	Tristate VID
4	Tristate Memory Control
3	Disable CGA Bit
2	Lock Palette and Overscan
1	EGA Compatible Mode
0	Mode 13 Enhance

Bit 7 — A 1 in this bit location causes the BLINKN output signal of the VGA chip to supply Display enable. A 0 in this bit location causes the Video DAC to generate the blanking signal.

Bit 6 — A 1 in this bit location causes the output pins HSYNC, VSYNC, and BLINKN of the VGA chip to be tristated. A 0 in this bit location does not cause these output pins to be tristated.

Bit 5 — A 1 in this bit location will cause the Video Output Signal VID0-VID7 to be tristated. A 0 in this bit location causes these signals not to be tristated.

Bit 4 — A 1 in this bit location will cause the VGA chip to tristate the memory control outputs. A 0 in this bit location will cause the VGA chip not to tristate the memory control outputs.

Bit 3 — A 1 in this bit location disables the CGA enable video bit in the Mode Register at address 03D8H. A 0 in this bit location does not disable it. Power on reset causes no override.

Bit 2 — A 1 in this bit location will lock the contents of the Palette and Overscan registers. A 0 in this bit location does not lock the values in the Palette and Overscan registers.

Bit 1 — A 1 in this bit location selects the EGA compatibilty mode. It disables response to registers at I/O addresses 03x8H-03xAH, where x is B or D depending on whether monochrome or color operation is desired. Reading the Input Status Register at I/O address 03C2H high indicates the presence of an EGA monitor. Also, the Attribute Controller Address registers at I/O addresses 03C0H/03C1H change to a write-only mode if the EGA compatibility bit is set. In the VGA mode, Bit 1 of the Video Control register is set to 0, while the Attribute Controller Address register at I/O address 03C0H is write-only, and the Attribute Controller Address register at I/O address 03C1H is read-only. A 0 in this bit location does not select EGA compatibility mode.

Bit 0 — A 1 in this bit location selects the 640 x (480, 400) 256 color mode 13 hex. This is an enhancement of the IBM mode 13 hex which only provides 320 x 200 resolution for mode 13 hex. A 0 in this bit location does not select the mode 13 hex enhancement.

Lock Status Register

This is a read/write register that is accessed when the Graphics controller address register is loaded with a value of 0FH. Data is written to this register at address 03CF hex.

Bit	Function
7	Status Bit
6	Status Bit
5	Status Bit
4	Status Bit
3	Reserved And Set To 0
2	Enhanced Register Unlock
1	Enhanced Register Unlock
0	Enhanced Register Unlock

Bits 4-7 — These are general purpose status bits which are latched on power up reset from the corresponding memory data pins MD4-MD7. They are read-only bits and provided to read the logic states of the configuration register Bits 4-7.

Bit 3 — Reserved and set to 0.

Bits 0-2 — These bits are used to unlock the Enhanced Feature Registers. A value of 05H written to these bit locations unlocks the Enhanced Feature Registers. Any other value written to these bits will lock the Enhanced Feature Registers.

Video Graphics Array Programming Considerations

The following paragraphs list some programming considerations that should be noted when programming the VGA.

Certain internal timings must be guaranteed in order to have the CRT Controller perform properly. This is because of the physical design of the video subsystem. These timings can be guaranteed by being sure the rules listed in the following paragraphs are adhered to when programming the CRT Controller.

1. The Horizontal Total Register must be greater than or equal to a value of 25 decimal.
2. The minimum possible pulse width of the Horizontal Sync output must be four character clock units.
3. The End Horizontal Retrace Register must be programmed such that the Horizontal Sync output goes to a logic "0" a minimum of one character clock time before the Horizontal Display Enable signal goes to a logical "1".
4. The End Vertical Blanking Register must be a minimum of one horizontal scan line greater than the value contained in the Line Compare Register.

   Note: All of the above conditions are met when the video mode is set by the BIOS.

When Bit 5 of the Attribute Mode Control Register equals a logical "1", a successful line compare in the CRT Controller (see the Line Compare Register) forces the output of the PEL Panning Register to logical "0"'s, until vertical sync occurs. When vertical sync occurs, the output returns to the programmed value. This allows the part of the display indicated by the Line Compare Register to be operated on by the PEL Panning Register.

A write to the Character Map Select Register becomes valid on the next whole line. This way no deformed characters are displayed by changing character generators in the middle of a character scan line.

For graphics mode hex 13, the Attribute Controller is configured so the 8-bit attribute stored in video memory for each PEL becomes the 8-bit address (P0-P7) into the DAC. You should not modify the contents of the internal palette registers when using this mode.

The following sequence should be followed when accessing any of the Attribute Data Registers pointed to by the Attribute Index Register.

1. Disable Interrupts.
2. Reset the Read/Write flip-flop.
3. Write to the Index Register.
4. Read from or Write to a data register.
5. Enable interrupts.

The Color Select Register in the Attribute Controller may be used to rapidly switch between sets of colors in the video DAC. When Bit 7 of the Attribute Mode Control Register is equal to a logical "0", the 8-bit color value sent to the Video DAC is made up of 6 bits from the inter-

nal Palette Registers, and Bits 2 and 3 of the Color Select Register. When Bit 7 of the Attribute Mode Control Register is equal to a logical "1", the 8-bit color value sent to the Video DAC is made up of the lower four bits from the internal Palette Registers and the four bits in the Color Select Register. By changing the value in the Color Select Register, software will rapidly switch between sets of colors in the Video DAC. It should be noted that the BIOS does not support multiple sets of colors in the Video DAC. You must load these colors if this function is to be used. Also note that this discussion applies to all video modes except mode hex 13. In mode hex 13 the Color Select Register is not used to switch between sets of colors.

An application that saves the "Video State" must store the four bytes of information contained in the system microprocessor latches in the Graphics Controller subsection. These latches are loaded with the appropriate number of bits from video memory, arranged as 8 bits per map, each time the system microprocessor does a read from video memory. The application needs to do the following steps:

1. Use Write Mode 1 to write the values in the latches to a location in the video memory that is not part of the display buffer. The last location in the address chain is a good choice.
2. Save the values of the latches by reading back from video memory.

It should be noted that if in a chain 4 or odd/even mode it will be necessary to reconfigure the memory organization as four sequential maps prior to performing the above sequence. BIOS provides support for completely saving and restoring the video state.

The description of the Horizontal PEL Panning Register includes a chart which shows the number of PELs shifted left for each value in the PEL Panning Register and each valid video mode. Further panning beyond that which is listed in the chart may be done by changing the start address in the CRT Controller Start Address High and Start Address Low Registers. The steps involved in further panning are listed below.

1. Use the PEL Panning Register to shift the maximum number of bits to the left.
2. Increment the start address.
3. If you are not using modes hex 0+, 1+, 2+, 3+, 7, or 7+, set the PEL Panning Register to a value of 0. If you are using one of the above modes, set the value in the PEL Panning Register to 8. The display will now be shifted one PEL position left of the position it was in at the end of step 1. Step 1 through step 3 can be repeated as many times as desired.

The Line Compare Register in the CRT Controller should be programmed with even values in 200 line modes when used in split screen applications which scroll a second screen on top of the first screen. This is a requirement imposed by the scan doubling logic in the CRT Controller.

If the Cursor Start Register in the CRT Controller is programmed with a value larger than the one in the Cursor End Register, then no cursor is displayed. A split cursor is not possible.

In the 8-dot character modes, the underline attribute produces a solid line across adjacent characters. In 9-dot character modes, the underline across adjacent characters will be dashed. In 9-dot character modes the line graphics characters (C0-DF hex) have solid underlines.

Programming The Registers

Each of the VGA subsections has an Index or Address Register and a number of data registers. The Index or Address Register serves as a pointer to the other registers in the device. These registers are loaded by the system microprocessor by executing an OUT instruction to the I/O address of the Index or Address Register with the value of the desired data register

The data registers in each subsection are accessed through a common I/O address. They are distinguished by the pointer in the Address Register. To write to a data register, the Address Register is loaded with the value of the appropriate data register, then the selected data register is loaded by executing an OUT instruction to the common I/O address.

The General Registers are not accessed through an address register, but are written to directly.

To maintain compatibility with the IBM EGA adapter, the internal VGA palette is programmed the same as the EGA. The Video DAC is programmed by the BIOS so that the compatible values in the internal VGA palette produce a color which is compatible to what was produced by the EGA. Mode hex 13 is programmed so that the first 16 locations in the DAC produce compatible colors.

When the BIOS is used to load the Video DAC palette for a color mode while a monochrome display is connected to the system, the color palette is changed. The colors are summed to produce varying shades of gray, which allows color applications to produce a readable screen.

There are 4 bits which should not be modified unless the sequencer is reset by setting Bit 1 of the Reset Register to a logical "0". These bits are as follows.

Bit 3 or Bit 0 of the Clocking Mode Register.

Bit 3 or Bit 2 of the Miscellaneous Output Register.

RAM Loadable Character Generator

The character generator is RAM loadable and is capable of supporting characters 32 scan lines in height. Three character generators are stored in the BIOS and one is a tomatically loaded into RAM by the BIOS when an alphanumeric mode is selected. The Character Map Select Register can be programmed to define the function of Bit 3 of the attribute byte to be a character generator switch. This allows you to select between any two character sets located in Map 2. This effectively gives you access to 512 characters instead of 256. Character tables can be loaded offline, and up to eight tables can be loaded. The structure of the character tables is described in the following chart. The character generator is in Map 2 and must be protected using the Map Mask function.

Map 2



+0K	Character Generator 0 Character Generator 4
+16k	Character Generator 1 Character Generator 5
+32K	Character Generator 2 Character Generator 6
+48K	Character Generator 3 Character Generator 7
+64K	

Character Table Structure

The following chart shows the structure of each character pattern. If the CRT Controller is programmed to generate a certain number of row scans, the same number of bytes must be filled in for each character in the character generator. This example assumes eight row scans per character.

Address	Byte Image								Data
CC * 32 + 0				X	X				18H
1			X	X	X	X			3EH
2		X	X			X	X		66H
3		X	X			X	X		66H
4		X	X	X	X	X	X		7EH
5		X	X			X	X		66H
6		X	X			X	X		66H
7		X	X			X	X		66H

Character Pattern Example

CC equals the value of the character code. For example, hex 41 equals an ASCII "A".

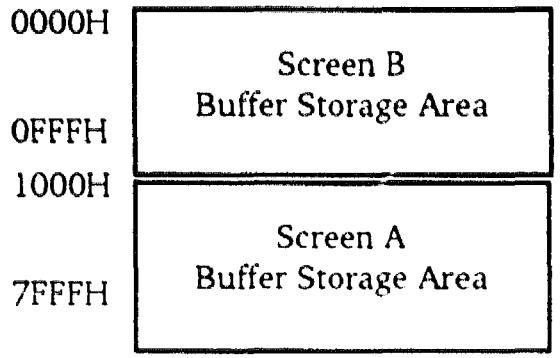
Creating A Split Screen

The VGA hardware will support a dual screen display. The top part of the screen is designated as Screen A, and the bottom part of the screen is Screen B. The following chart shows this layout.

SCREEN A
SCREEN B

Dual Screen Definition

The following chart illustrates the screen mapping for a system containing a 32K byte alphanumeric storage buffer. Note that the VGA has a 32K byte storage buffer in the alphanumeric mode. Information displayed on Screen A is defined by the Start Address High and Start Address Low Registers of the CRT Controller. Information displayed on Screen B always starts at address hex 0000.



The Line Compare Register of the CRT Controller executes the split screen function. The CRT Controller has an internal horizontal scan line counter. The CRT Controller also possesses the logic that compares the line counter value to the Line Compare Register value and clears the memory address generator when a compare occurs. The linear address generator will then sequentially address the display buffer starting at location 0. Each subsequent row address determined by the 16-bit addition of the start of line latch and the Offset Register.

Screen B can be smoothly scrolled onto the display screen by updating the Line Compare in synchronization with the Vertical Retrace signal. The information onXucreen B is not affected by the scrolling operations that utilize the Start Address High and Start Address Low Registers to scroll through the Screen A address map.

When Bit 5 of the Attribute Mode Control Register is equal to a logical "1", a successful line compare forces the output of the PEL Panning Register to a value of 0, until vertical synchronization occurs. When vertical synchronization occurs, the output returns to its programmed value. This feature allows the information on Screen B to remain unaffected by PEL panning operations on Screen A.

Video DAC (Digital to Analog Converter)

PEL Address Register

The PEL Address Register is used to hold an 8-bit value which represents the address used to access a location within the color look-up table. The PEL Address Register can be written to at two different addresses. This is done to establish a read or write mode respectively. Once the PEL Address Register has been written to and an access has been made to the color look-up table, the PEL Address Register automatically increments so that further accesses may occur to successive locations.

Write Sequence

A write sequence is performed by writing to the PEL Address Register at address 03C8 hex. This sequence consists of three successive byte writes to the Data Register located at address 03C9 hex. The least significant 6 bits of each byte are assembled to form the value placed in the 18-bit Data Register. The order is Red byte first, Green byte second, and Blue byte last. Once the third byte has been written, the value in the Data register is written to the location pointed to by the PEL Address Register. The following is a sample of the sequence of events in a write cycle.

1. Write to the PEL Address Register at 03C8 hex.
2. Write three bytes to the Data Register at 03C9 hex.
3. At this time the contents of the Data Register is transferred to the location in the color look-up table pointed to by the PEL Address Register.
4. The PEL Address Register is automatically incremented by 1.
5. Return to Step 2 for the next three bytes of data.

Read Sequence

A read sequence is performed by writing to the PEL Address Register at address 03C7 hex. This sequence consists of three successive byte reads from the Data Register located at address 03C9 hex. The least significant 6 bits of each byte are read from the 18-bit value placed in the Data Register contains the corresponding color value. The order is Red byte first, Green byte second, and Blue byte last. The following is a sample of the sequence of events in a read cycle.

1. Write to the PEL Address Register at 03C7 hex.
2. At this time the contents of the location in the color look-up table pointed to by the PEL Address Registers transferred to the Data Register.
3. The PEL Address Register is automatically incremented by 1.
4. Three bytes are read back from the Data Register at 03C9 hex.
5. Return to Step 2 for the next three bytes of data.

A read from the PEL Address Register at 03C7 hex returns 0's in Bits 0 and 1 if the DAC is in the read mode and 1's if the DAC is in the write mode.

Video DAC Programming

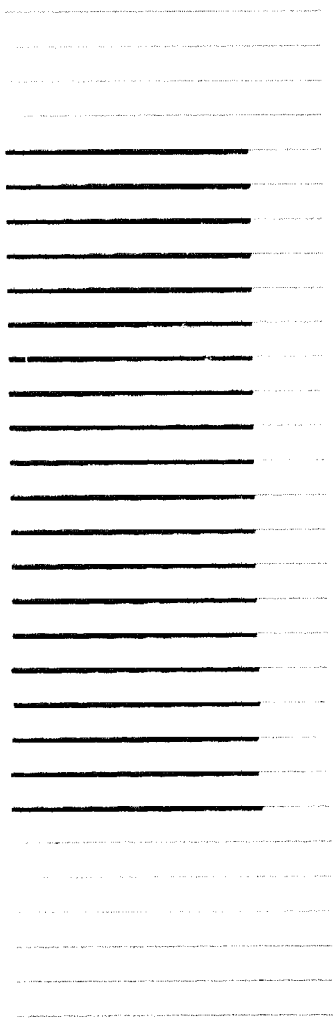
The following sequence of events must be followed when programming the DAC to ensure color look-up table integrity during accesses to it.

1. Write out the address to the PEL address register.
2. Disable interrupts.
3. Write or read three bytes of data.
4. Repeat step three for the desired number of locations.

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AHA-1540 User's Manual
AT-to-SCSI Host Adapter



Preface

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Appendix

Appendix A: AHA-1540 System Timing Diagram A-1

Section One Introduction

1.1 DOCUMENT SCOPE

This manual provides the information required to install and program the AHA-1540 Intelligent Host Adapter in an AT bus-based system.

1.2 PURPOSE

The Adaptec AHA-1540 provides a powerful multitasking interface between the AT bus and the Small Computer System Interface (SCSI) bus. The AHA-1540 is a high performance intelligent host adapter supporting a maximum asynchronous SCSI rate of 2.0 MB/sec and a synchronous transfer rate of 5 MB/sec. The AHA-1540 supports multithreaded I/O operations, allowing simultaneous operations on multiple targets/LUNs. Disconnect/Reconnect support maximizes bus utilization for multiple target systems.

The Adaptec AHA-1540 provides a solution for system applications requiring very high performance, flexibility and multithreaded I/O capability with peripheral devices. The AHA-1540 can also be used in place of a standard hard disk controller.

1.3 AHA-1540 PRODUCT FEATURES

- High performance First Party DMA with programmable data rates of up to 10 MB/sec.
- 16- and 8-bit transfers
- Even or odd starting address transfers
- Maximum synchronous SCSI transfer rate of 5.0 MB/sec.
- Asynchronous and synchronous peripherals supported simultaneously
- Programmable AT bus burst transfer on and off time
- Jumper selectable DMA channel for bus arbitration (channels 0,5,6,7)
- Jumper selectable interrupt channels (IRQ 9, 10, 11, 12, 14, 15)
- True multithreaded operation supporting up to 255 tasks simultaneously
- Programmable mailbox architecture
- Adaptec BIOS for AT hard disk emulation
- Jumper selectable I/O port address
- Internal and external SCSI connectors

1.4 PRODUCT SPECIFICATIONS

- Physical Dimensions:

  Length : 13.25 " Width : 4.75" Height : 0.5"

- Power Requirements:

  +5.0 +/- 0.25 Volts at 2.5 Amps maximum.

• Environmental Requirements:

Temperature 0-70 degrees C (operating or storage)

1.5 REFERENCE DOCUMENTS

- IBM PC/AT technical reference manual
- X3T9.2 Rev 17B SCSI specification

Section Two Host Adapter Architecture

2.1 HARDWARE

2.1.1 First Party DMA

The AHA-1540 controls the host AT bus as a master and transfers data directly to and from main system memory. This implementation is known as First Party DMA. First Party DMA greatly reduces the host software overhead because the host CPU is no longer required to maintain the DMA channel's address pointers and word counts. First Party DMA also reduces the number of interrupts generated per I/O command.

Adaptec's implementation of First Party DMA can achieve a 10 MB/sec burst data rate. This speed is especially valuable in multitasking systems where the tasks execute on a time shared basis. Appendix A shows a diagram of the timing required to achieve the DMA rates that are supported by the AHA-1540.

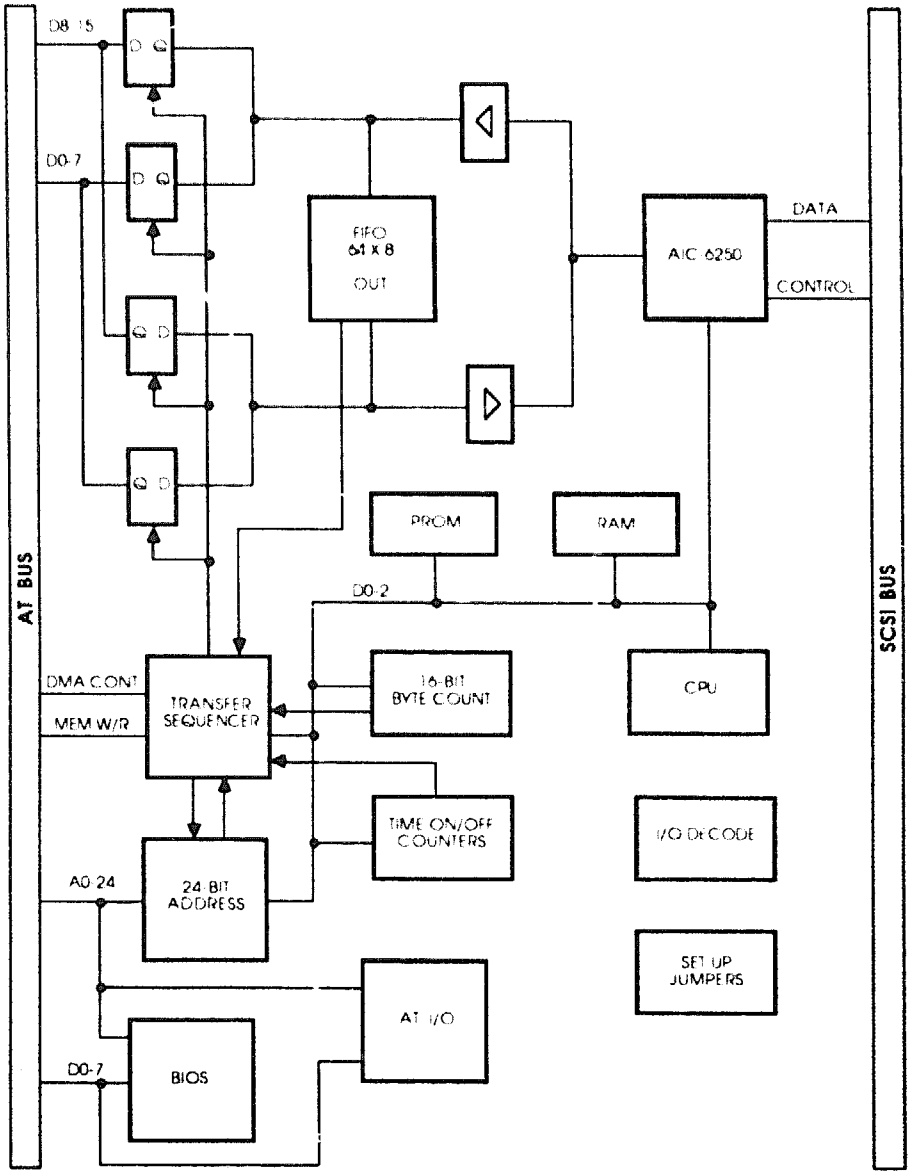
The AHA-1540 DMA hardware will handle both odd-byte and odd-memory address data transfers with no performance degradation.

2.1.2 SCSI Protocol Chip (AIC-6250)

The AHA-1540 utilizes the AIC-6250 SCSI protocol chip to maximize the SCSI bus utilization. The AIC-6250 is an Adaptec VLSI device which allows the AHA-1540 to achieve 2.0 MB/Sec asynchronous SCSI data transfer rates, and 5.0 MB/sec synchronous transfer rates. The AIC-6250 will also enable the AHA-1540 to operate as both an initiator and as a target device. *Note: Target operation is not supported in the first release of this product.*

Through a 16-bit host interface, the AIC-6250 reduces bus busy time during data transfer by bursting data across the AT bus at up to 10 MB/sec. The AIC-6250 has separate data busses for the local microprocessor and for the system data bus. This further increases the performance of the AHA-1540 by reducing the overhead associated with SCSI commands.

2.1.3 Hardware Block Diagram



2.2 FIRMWARE

The AHA-1540 supports both multithreaded SCSI commands and emulated PC/AT BIOS calls. To support multithreaded commands, the firmware accepts and saves multiple task CCB's in local RAM. The firmware controls all of the SCSI activity that a task may require. This includes: Arbitration, Selection, Disconnection, Reconnection, and Command completion.

2.2.1 Multithreaded Operation

A multituser, multitasking operating system issues a large number of I/O tasks in a rapid sequence. The architecture of the AHA-1540 makes management of this activity very easy and straightforward for the operating system. This section briefly explains the interaction between the system and the AHA-1540 required to accomplish an I/O task.

2.2.1.1 Mailboxes

The AHA-1540 uses a mailbox architecture for task communication between the host and host adapter. This allows the host adapter to perform multithreaded operations with a minimum of host intervention.The mailboxes are located in main system memory . Each mailbox entry is four bytes long. At power-up, the host issues an initialization command to inform the host adapter of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). MBIs are located immediately after the MBOs. A typical mailbox structure is shown below:

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example there are four MBOs and four MBIs. The first byte of each MBO contains the command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides additional task information. A MBO is free if the first byte is zero. The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the task. An MBI is free if the Status byte is zero.

2.2.1.2 Command Descriptor Block

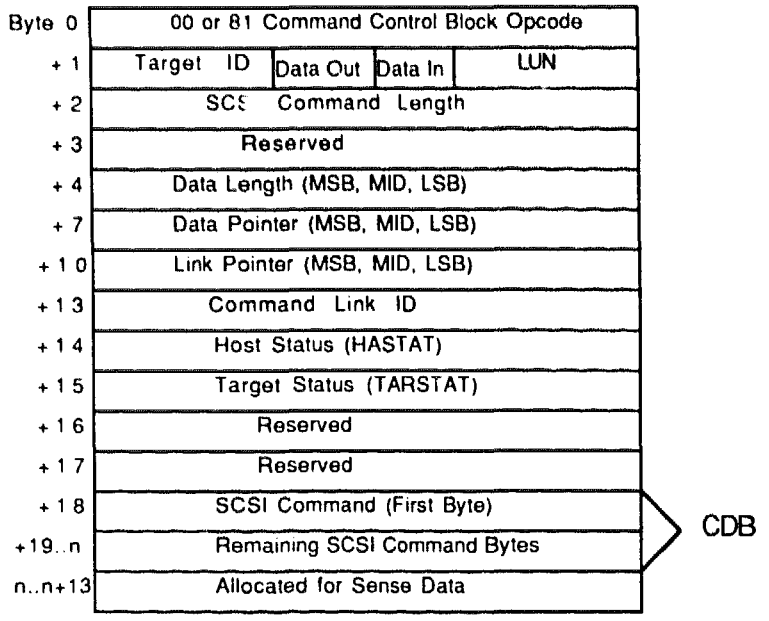
SCSI commands are sent using Command Control Block (CCB) structure. The CCB contains the SCSI Command Descriptor Block (CDB) The CDB contains all of the information about the request that is being sent to a target. The Command Descriptor Block contains the command Operation Code (Opcode) followed by a Logical Unit Number (LUN), command parameters if required, and a control byte. A typical Group 0 six byte CDB is shown below:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Vendor Unique		Reserved				Flag	Link

Please refer to the SCSI specification ANSI X3.131, the Common Command Set (CCS) revision 4B, and the SCSI 2 draft for additional information on Command Descriptor Blocks.

Note: a SCSI CDB is contained within a host adapter CCB. See section 5.3 for details of a CCB.

A typical CCB is shown below:



2.2.1.3 Task Queueing

Multiple tasks may be started against a target/LUN or against multiple targets/LUNs. Since only one task can be active against any one given LUN at a time, all other tasks for the same LUN are queued. Tasks may be directed and be active against multiple targets/LUNs simultaneously.

The host adapter dequeues on a first in, first out (FIFO) basis for each target/LUN combination. However, due to the optimization algorithm used by the host adapter, a task may sometimes be started earlier in spite of it's late entrance in the queue on multiple target/LUN systems.

At power-up, the host informs the host adapter of the location and number of mailboxes. To start a task, the host builds a CCB and stores its memory address into a free mailbox. A non-zero command byte is then written to indicate a full mailbox. If all other MBOs are free, or the state of other MBO's is not known, the host must write to an I/O port (defined in section 4) to force the host adapter to scan the MBO area. When the full MBO is found, the host adapter copies the mailbox's CCB pointer into its internal RAM and writes a zero to the MBO command byte. This frees the MBO so that it can be used to start another task.

After completing a task, the host adapter scans the MBI area for a free mailbox. When one is found, it is updated with the task's completion status and CCB pointer. A host interrupt is also generated to notify the host that a task has been completed. The CCB pointer identifies the completed task. The host scans the MBI area searching for a non-zero Status byte. When one is located, the host obtains the CCB pointer and frees the MBI by writing a zero into the Status byte. The host then examines the contents of the CCB to determine that the command was successfully completed.The freed MBI can now be used to indicate the completion of another task. The host adapter fills the MBI area in a round robin fashion. If the host saves the position of the last active MBI entry, it can determine the MBI of a new entry immediately without searching.

In a heavily loaded system, the host stores new task CCB's in the MBOs and is informed of the completed tasks via the MBI continuously.

2.2.2 Adapter Reporting Command Completion

When a task is completed, the host adapter locates a free MBI entry and stores the task's completion status and CCB pointer. An MBI_STORED interrupt is generated. New interrupts are not generated until a previous one is cleared. The exception to this is if MBI_STORED and MBO_AVAILABLE interrupts are pending, the host adapter will discard any new MBI and MBO interrupts. This will not cause a problem since an interrupt indicates that one or more mailbox events have occurred.

2.2.3 Single-Threaded Operation

The AHA-1540 can also emulate PC/AT BIOS commands. These commands are sent directly to the host adapter via Port I/O, circumventing the mailbox structure. In this mode of operation the host adapter will only accept a single command at a time. A new command sent to the host adapter will be rejected until the first command has been completed.

2.2.4 BIOS

A host adapter BIOS is provided to emulate the AT hard disk BIOS and boot functions. With this BIOS, the host adapter can be used in lieu of a standard hard disk controller on an AT system.
The BIOS is compatible with the PC/AT hard disk BIOS. It allows a standard AT to access a device on the SCSI bus without a driver under PC DOS or MS DOS. All normal I/O functions are supported including system booting. In order to perform system booting from a SCSI drive, the SCSI drive at target 0, LUN 0 must be designated as drive C:.

To perform a system boot, the host adapter BIOS will first attempt to boot from the floppy. If unsuccessful, it determines if there is a hard disk controller attached to the system. If one is found, an attempt is made to boot from that device. If there is no internal hard disk controller, or it has been mapped out through the AT SETUP program, the SCSI device at target ID zero, LUN zero is checked for a copy of the system boot record. See Section 6 for more information on BIOS operation.

Section Three Installation

3.1 UNPACKING AND INSPECTION

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your freight company representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for possible later reuse should return of the equipment to the factory necessary.

NOTE: The AHA-1540, like all electronic equipment is static sensitive. Please take the proper precautions when handling the board. Keep the board in its conductive wrapping until it is configured and ready to be installed in your system.

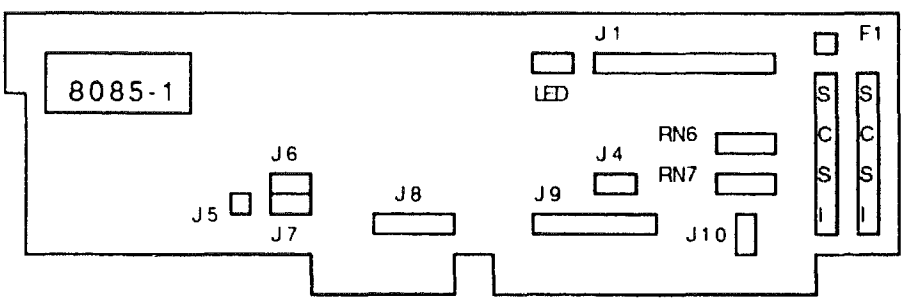
3.2 INSTALLATION

The following section details the installation procedure for the Adaptec AHA-1540 AT to SCSI host adapter. The installation of the board consists of setting the various on-board jumpers, inserting the board into a full-length AT compatible connector, and connecting a SCSI cable from the on-board connector to a SCSI target.

NOTE: The system must be turned off during the installation procedure.

The following diagram shows the approximate location of the various customer configurable items on the AHA-1540. Listed after the diagram are the functions of each item.

Jumper locations:



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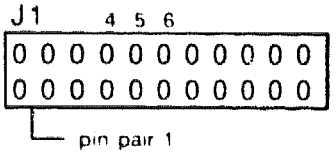
3.2.1 SCSI Jumper Configuration

Jumper set J1, pin pairs 4, 5 and 6, defines the SCSI address. The SCSI address consists of pin pairs 4, 5, and 6 in the large block of jumper pins located in the upper right hand corner of the PCB. Pin pair 1 is the left most pair of pins. The SCSI address is selected according to the following table. **The default address is 7.**

SCSI Address Jumpers

Pin Pair 4	5	6	SCSI Address
X	X	X	0
-	X	X	1
X	-	X	2
-	-	X	3
X	X	-	4
-	X	-	5
X	-	-	6
-	-	-	7

X = Jumper Installed



3.2.2 SCSI Parity

Jumper set J1, pin pair 3, is the parity enable/disable jumper. The SCSI parity jumper, pin pair 3 is located in the large block of jumper pins located in the upper right hand corner of the PCB. Pin pair 1 is the left most pair of pins. The SCSI parity checking is disabled if this jumper is installed. **The default is parity checking enabled.**

3.2.3 SCSI Terminators

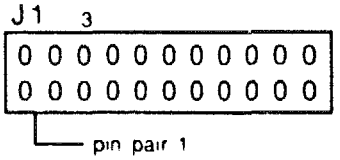
RN6 and RN7 are the SCSI terminators. If the AHA-1540 is not the first or the last SCSI device in a string of SCSI devices, or if in-line terminators are used, then both of these resistor networks must be removed. **Default is terminators installed.**

3.2.4 SCSI Terminator Power

Fuse, F1, controls the terminator power. If another SCSI device is supplying terminator power, then F1 may optionally be removed. No more than 5 SCSI devices should be configured to supply terminator power to a single SCSI bus. **Default is F1 installed** with the AHA-1540 supplying the terminator power.

3.2.5 SCSI Synchronous Negotiation

Jumper set J1, pin pair 1, is the synchronous negotiation enable jumper. This jumper set consists of pin pair 1 in the large block of jumper pins in the upper right hand corner of the printed circuit board. Pin pair 1 is the leftmost pair of pins.



The AHA-1540 will initiate SCSI synchronous negotiation during initialization or after a SCSI reset if this jumper is installed. If the jumper is not installed, the AHA-1540 will still support synchronous SCSI transfers, but the target must initiate the negotiation. **Default is jumper removed, synchronous negotiation initiation disabled.**

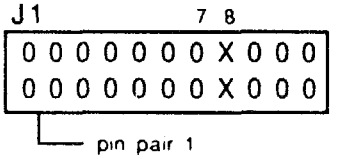
3.3 AT CONFIGURATION

3.3.1 DMA Channel Selection

There are three jumper blocks involved in selecting the DMA channel. These are J1, J6, and J7. The DMA channel selection jumpers consist of pin pairs 7 and 8 located in the large block of jumper pins in the upper right hand corner of the PCB. Pin pair 1 is the left most pair of pins. The DMA channel reported to the AT during the Return Configuration command is set by these jumpers according to the following table. **Default is DMA channel 5.**

DMA Channel Jumpers		
Pin Pair 7	8	DMA Channel
X	X	0
-	X	5
X	-	6
-	-	7

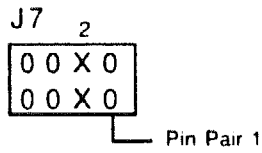
X = Jumper Installed



Jumper set J7 selects the DMA ACK signal to be used by the AHA-1540. This jumper set is located near the left corner of the small AT bus connector. Pin pair 1 is the right most set of pins. **Default is DMA Acknowledge 5.**

DMA ACK Jumpers				
Pin Pair				DMA
4	3	2	1	Channel
-	-	-	X	0
-	-	X	-	5
-	X	-	-	6
X	-	-	-	7

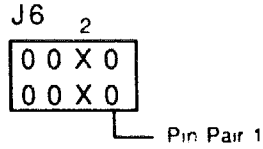
X = Jumper Installed



Jumper set J6 selects the DMA REQ signal to be used by the AHA-1540. This jumper set is located near the left corner of the small AT bus connector. Pin pair 1 is the right most pair of pins. **The default is DMA Request 5.**

DMA REQ Jumpers				
Pin Pair				DMA
4	3	2	1	Channel
-	-	-	X	0
-	-	X	-	5
-	X	-	-	6
X	-	-	-	7

X = Jumper Installed

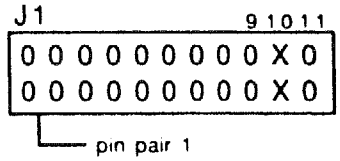


3.3.2 AT Interrupt Channel

There are two jumper blocks involved in selecting the AT interrupt channel. These are J1 and J8. The AT interrupt channel jumpers consist of pin pairs 9, 10, and 11 in the large block of jumper pin pairs located in the upper right hand corner of the PCB. Pin pair 1 is the left most pair of pins. The interrupt channel reported to the AT during the Return Configuration Command is set by these jumpers according to the following table. **The default is interrupt channel 11.**

AT Interrupt Channel			
Pin Pair			Interrupt
9	10	11	Channel
X	X	X	Not Defined
-	X	X	Not Defined
X	-	X	15
-	-	X	14
X	X	-	12
-	X	-	11
X	-	-	10
-	-	-	9

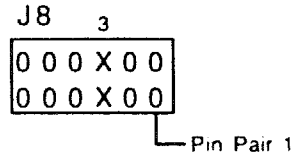
x = Jumper Installed



Jumper set J8 selects the AT interrupt channel to be used by the AHA-1540. This jumper set is located just above the small AT bus connector. Pin pair 1 is the right most pair of pins. The interrupt channel used is set according to the following table. **The default interrupt channel is 11.**

AT Interrupt Channel						
Pin Pair						Interrupt
6	5	4	3	2	1	Channel
-	-	-	-	-	X	9
-	-	-	-	X	-	10
-	-	-	X	-	-	11
-	-	X	-	-	-	12
-	X	-	-	-	-	14
X	-	-	-	-	-	15

X = Jumper Installed

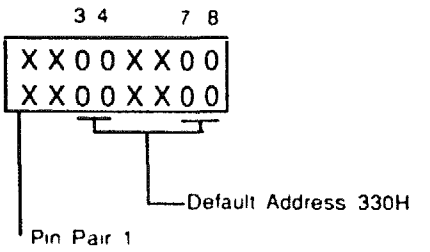


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3.3.3 AT Port Address

The starting address of the block of four I/O ports required by the AHA-1540 is selected by the jumpers in jumper block J9. This jumper set is located just above the left corner of the large AT bus connector. Pin pair 1 is the left most pair of pins. The default address is 0330H and must not be changed unless a new BIOS is supplied. The port address is coded in the BIOS and must match. Valid port addresses are 334H, 330H, 234H, 230H, 134H, and 130. **The default address is 330H.**

	Port Address	
	Pin Pair	Port I/O Address Bit
LSB	1	004H
	2	008H
	3	010H
	4	020H
	5	040H
	6	080H
	7	100H
MSB	8	200H



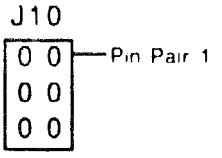
X = Jumper Installed, Jumper Deasserts the Address Bit.
Valid Addresses Are: 334, 330, 234, 230, 134, 130

3.3.4 AT BIOS Address

The starting address of the block of address space reserved for the Adaptec BIOS is selected by the jumper pins located in J10. This jumper set is located just above the large AT bus connector. **The default address is ODCOOOH.** This address must not conflict with any other BIOS in the system.

AT BIOS Address			
Pin Pair			BIOS
1	2	3	Address
X	-	X	0C8000H
-	-	X	0D8000H
X	-	-	0CC000H
-	-	-	0DC000H

X = Jumper Installed



3.3.5 AT BIOS Wait State

Accesses to the Adaptec BIOS can have one wait state added by installing the jumper located at J4. This jumper set is located to the left of the SCSI terminator RN7. **The default is no wait state.**

3.3.6 Reserved Jumpers

The jumper, pin pair 2 located in jumper block J1, is reserved for Adaptec use only and must not have any jumper shunts installed. If this jumper is installed, normal operation is prevented. **Default is no jumper installed.**

3.3.7 LA Enable Jumper

Note: Some computers, especially 80386 based machines, short address lines LA17 and SA17, LA18 and SA18, and LA19 and SA19 together. If your computer system shorts these lines then remove jumper J5. ***Default is jumper installed.***

Warning: Incorrect installation of this jumper may not result in immediate system problems. If it is necessary to change the state of this jumper after the system has been configured, the SCSI hard disk must also be re-formatted. Contact your system manufacturer if in doubt on how your system implements these address lines.

Section Four Hardware Functional Description

4.1 HARDWARE OVERVIEW

This section provides detailed descriptions of the AHA-1540 hardware functional interface to the PC/AT host software.

The hardware consists of a custom SCSI protocol chip, the AIC-6250, a FIFO buffer, a set of I/O ports, and a controlling microprocessor.

The DMA control logic on the host adapter controls the AT bus arbitration and data transfer handshaking. During DMA data transfers, the AHA-1540 becomes a bus master. The DMA logic supports odd starting addresses. In such cases, the first transfer will be an 8-bit transfer. Thereafter, 16 bit transfers will be used to complete the data transfer. Odd-byte transfers, and the the last transfer of an even number of bytes to an odd address are treated in a similar manner.

The SCSI port is controlled by the AIC-6250, an Adaptec SCSI protocol device which supports arbitration, selection, and reselection with a minimum of processor intervention. This VSLI device also supports target mode and synchronous SCSI transfers.

4.2 I/O PORT INTERFACE

The I/O port interface consists of three address locations.

Three port addresses are decoded in the AT I/O address space. They form the primary communications channel between the host and the host adapter. The I/O ports are 8 bits wide. The base port is for control and status, followed by the command and data port, and the interrupt port.

4.2.1 Control and Status Port

Writing to this port initiates host adapter operations, as well as reads and returns host adapter status.

Base+0 Port, Write Host Adapter Control Port.

NOTE: Functions are activated when the indicated bit is asserted. (i.e., high logic level)

bit 7 -- Hard Reset (HRST). Forces the host adapter into a state identical to a power-on reset.
bit 6 -- Soft Reset (SRST). Clears all commands but does not execute diagnostic functions.
bit 5 -- Interrupt Reset (IRST). Clears the host adapter interrupt port.
bit 4 -- SCSI Bus Reset (SCRST).
bit 3 -- Reserved
bit 2 -- Reserved
bit 1 -- Reserved
bit 0 -- Reserved

Base+0 Port, Read Host Adapter Status Port.

bit 7 -- Self testing in progress (STST)
bit 6 -- Internal diagnostic failure (DIAGF)
bit 5 -- Mailbox Initialization required (INIT)
bit 4 -- SCSI host adapter idle (IDLE)
bit 3 -- Command/data (out) port full (CDF)
bit 2 -- Data (in) port full (DF)
bit 1 -- Reserved
bit 0 -- Invalid host adapter command (INVDCMD)

Base+1 Port, Write -- Command and Data-Out Port
Base+1 Port, Read -- Data-In Port

Base+2 Port, Write -- Reserved

Base+2 Port, Read -- Interrupt Flags

bit 7 -- Any interrupt (Set by any other interrupt)
bit 6 -- Reserved
bit 5 -- Reserved
bit 4 -- Reserved
bit 3 -- SCSI reset detected (SCRD)
bit 2 -- Host adapter command complete (HACC)
bit 1 -- MBO empty interrupt (MBOE)
bit 0 -- MBI full interrupt (MBIF)

The STST (Status bit 7) bit indicates when the host adapter is performing initialization and internal diagnostics. This bit is asserted after a power-on or hard reset (Control HRST=1). When diagnostics are completed, the STST bit is reset and either DIAGF (Status bit 6) or INIT (Status bit 5) is set. If DIAGF is asserted, diagnostics have failed and the host adapter must be reset again to clear it. When INIT is asserted, diagnostics have successfully completed and mailbox initialization is required. Initialization consists of specifying the base memory location of the mailboxes and is accomplished through the Mailbox Initialization command. The host can also reset the host adapter without invoking the internal diagnostics by asserting SRST (Control bit 6). Asserting SCRST (Control bit 4) generates a SCSI bus reset.

The status and interrupt ports return information which indicate either when a new command can be accepted, or the source of the host adapter interrupt.

The host adapter will generate an interrupt at the completion of a host command. The state of the HACC and MBIF bits will indicate the interrupt source. An interrupt is also generated when a SCSI Bus Reset is detected. The final interrupt source, MBOE (Interrupt bit 1) is enabled by the host adapter Enable Mailbox-Out Interrupt command (05). This generates an interrupt when one out-bound mailbox is emptied. If all mailboxes are empty, outbound mailboxes will not be scanned until another Start SCSI (02) command is received by the host adapter.

Before starting a host adapter command, the host must check to see if the host adapter is idle. All commands except for Start SCSI (02) and Enable Mailbox-Out Interrupt (05) must wait for the host adapter idle condition. If IDLE (Status bit 4) is set, the host adapter has no outstanding SCSI or host adapter commands and is idle. It is reset otherwise.

The host uses CDF (Status bit 3) to synchronize command and data transfers to the host adapter. Command and data transfer is allowed only if CDF is deasserted. If it is set, the host must wait until it is reset. CDF is automatically set when the host writes to the command/data port and is reset after the host adapter reads the command/data port. After a command has completed, the HACC (Status bit 2) interrupt flag is set. HACC is cleared by setting IRST (Control bit 5).

The DF flag (Status bit 2) is provided to synchronize host adapter to host data transfers. It is asserted when the data is available at the command/data port. It is deasserted after the host removes the data. If a command is aborted, INVDCMD (Status bit 0) or HACC (Interrupt bit 2) is set. In this case, the host adapter may or may not have transferred (in or out) all of the data bytes. While waiting for the host adapter to receive or transmit data, the host should poll HACC since invalid data can prematurely terminate a command sequence.

INVDCMD (Status bit 0) indicates that the last command received was invalid. Therefore, after sending a command, the host software should check the INVDCMD bit before attempting to transfer any data.

4.2.2 Command and Data Port

The second I/O port is used by the host to send a host adapter command. It is also used by the host to send or receive data to or from the host adapter. The command port should not be confused with the command field in the MBO. The command port is used by the host to send commands which can't be sent via the MBO, such as Initialization and Start SCSI commands. Some host adapter commands require additional data transfers.

The host should only write to this port when CDF is deasserted. This allows time for the host adapter to off-load a previously written command byte. CDF is automatically set when the host writes to the port and is reset after the host adapter reads from the port.

If a command needs additional data bytes, the host waits until CDF is deasserted before writing data. Just as in the command transfer case, each host write will set the CDF. The host can write additional data bytes only after CDF is again deasserted. HACC will indicate when the command is done. If INVDCMD is set, the host adapter found either the command or data bytes to be invalid.

If a data transfer is from the host adapter, the host must wait until DF (Status bit 2) is set. After the host reads the Data port, DF is automatically reset. The host should wait until DF is again set before attempting to transfer additional data. After the last data byte, HACC will be set indicating command completion.

Section Five Firmware Functional Description

5.1 HOST ADAPTER COMMAND OVERVIEW

The AHA-1540 supports two types of commands: SCSI and Adapter commands. SCSI commands are issued using the mail boxes. Adapter commands are issued by writing to the second adapter I/O port. Most Adapter commands can not be issued when there are outstanding SCSI commands. When SCSI commands are used, the AHA-1540 is operating in true multithreading mode. In this mode of operation, the AHA-1540 is capable of executing multiple commands for multiple targets concurrently. The AHA-1540 maximizes the I/O transaction throughput by managing SCSI disconnection and reconnection.

Adapter commands are used to initialize the host adapter as well as execute PC/AT commands. PC/AT BIOS functions circumvent the mailbox structure and will only execute in a single-threaded mode. The host writes to the CMD/Data I/O port located at base+1 to start a host adapter command.

5.1.1 Host Adapter Opcodes

Below is a list of the host adapter opcodes.

00 -- No Operation
01 -- Mailbox Initialization
02 -- Start SCSI Command *
03 -- Start PC/AT BIOS Command
04 -- Adapter Inquiry
05 -- Enable Mailbox Out Available Interrupt*
06 -- Set Selection Timeout
07 -- Set Bus-On Time
08 -- Set Bus-Off Time
09 -- Set Transfer Speed
0A -- Return Installed Devices
0B -- Return Configuration Data
1C -- Write Adapter FIFO Buffer
1D -- Read Adapter FIFO Buffer
1F -- ECHO Command Data

Note: This command can be issued when the host adapter is executing a SCSI command.

All host adapter commands except Start SCSI (02) and Enable Mailbox-Out Available Interrupt (05) must be executed only when the IDLE bit (Status bit 4) is asserted. Subsequent bytes of a command sequence may then be written to the second I/O port (base + 1 Command and Data port) if CDF (Status bit 3) is deasserted, indicating that the command port is free.

5.1.1.1 No Operation (Opcode 00)

No host adapter action is taken, but HACC is set indicating command completion.

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5.1.1.2 Mailbox Initialization (Opcode 01)

This command is used to specify the mailbox count and the memory location. The host adapter requires that four bytes of data follow the command byte. Data field definition is shown below.

00 Mailbox count (>0)
01 Mailbox address (MSB)
02 Mailbox address
03 Mailbox address (LSB)

Byte 1 -- Mailbox count must be greater than zero. (A zero value will set the INVDCMD bit. Status bit 0)
Bytes 2, 3, 4 specify memory address of first byte of Mailbox area. (MSB...LSB)

At command completion, HACC will be set and INIT will be reset. HACC will be reset when the host writes to I/O port 1 (Base+0) . (See Section 4.2)

5.1.1.3 Start SCSI Command (Opcode 02)

This command signals the host adapter to scan for active MBO's. This is required only if all of the MBO's are inactive. However, since it is not easy for the host to determine if all of the MBO's are inactive, the host may simply elect to issue this command every time a MBO is filled. This command does not require additional data bytes. To avoid additional interrupts, HACC is NOT set after command completion. HACC will be set if the mailbox was not initialized. In this case, INVDCMD will also be set.

5.1.1.4 Start PC/AT BIOS Command (Opcode 03)

This command signals the host adapter to start a command in the PC/AT emulation mode. (See Section 6.1.3 for details.)

5.1.1.5 Adapter Inquiry (Opcode 04)

After receiving this command, the host adapter returns four bytes of data describing the host adapter firmware revision level. After completing this command HACC is set indicating normal command completion.

5.1.1.6 Enable Mailbox-Out Available Interrupt (Opcode 05)

This command expects one data byte which specifies one of the interrupt options below:

Data Byte 0 -- Enable/Disable MBO Interrupt
(00) -- Disable mailbox out interrupt
01 -- Enable mailbox out interrupt

After completing this command, HACC will NOT be asserted to avoid generating additional interrupts. If the data byte is neither 00 nor 01, INVDCMD will be asserted indicating an invalid command. In this case, HACC will also be asserted.

5.1.1.7 Set Selection Time-out (Opcode 06)

This command sets the SCSI selection time-out value. This command expects four data bytes defined below:

Data Byte 0 -- Enable/Disable Selection Time-out
(00) -- Turn Time-out Off
01 -- Turn Time-out On
Data Byte 1 -- Reserved (00)
Data Byte 2 -- Time-out Value MSB
Data Byte 3 -- Time-out Value LSB

After completing this command, HACC will be asserted, indicating normal completion. INVDCMD will be asserted if the data byte 0 is neither 00 nor 01 indicating an invalid command. The time-out value is specified in milliseconds.

5.1.1.8 Set Bus-On Time (Opcode 07)

Data Byte 0 -- Bus On-Time (2 to 15 us)

This command specifies the time that the host adapter spends on the bus when transferring data. The Bus-on duration is adjustable from 2 to 15 microseconds. The default setting is 11us. After receiving this command, the host adapter expects one byte of data which specifies bus on duration. After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 15.

5.1.1.9 Set Bus-Off Time (Opcode 08)

Data Byte 0 -- Bus-Off Time (.7 to 64 us)

This command sets the time that the host adapter will spend off the bus during a data transfer. The default setting is 5us. After receiving this command, the host adapter expects one byte of data which specifies the bus off time from .7 to 64 microseconds. After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 64.

5.1.1.10 Set Transfer Speed (Opcode 09)

This command sets the maximum AT bus burst rate at one of the following values: 5.0, 6.7, 8, or 10 MB/sec. The selection depends on host memory speed and implementation. Refer to Appendix A for details. The default setting is 5.0 MB/sec. (Word transfer every 400ns)

One data byte follows this command. It specifies the transfer rates as specified below:

Data Byte 0 -- AT Bus Transfer Speed
00 -- 5.0 MB/sec
01 -- 6.7 MB/sec
02 -- 8.0 MB/sec
03 -- 10 MB/sec

After completing this command HACC is set indicating normal completion. INVDCMD will be asserted, indicating an invalid command if the data byte is not between 00 and 03 inclusive.

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5.1.1.11 Return Installed Devices (Opcode 0A)

This command returns information about which target/LUNs are installed on the SCSI bus. The host adapter will issue the SCSI Test Unit Ready command to each target/LUN combination and report the results. This command can be executed once after power-up or any reset. A one signifies that the LUN is installed and ready. The order of significance is bit 7=LUN 7, bit 6=LUN 6, etc.

After receiving this command, the host adapter returns eight bytes of data which specifies configuration data. This is shown below:

Byte 0 -- Target 0
- bit 7 = LUN 7
- bit 6 = LUN 6
- bit 5 = LUN 5
- bit 4 = LUN 4
- bit 3 = LUN 3
- bit 2 = LUN 2
- bit 1 = LUN 1
- bit 0 = LUN 0

1 -- Target 1
2 -- Target 2
3 -- Target 3
4 -- Target 4
5 -- Target 5
6 -- Target 6
7 -- Target 7

Note: One of these bytes has a zero value because this bus ID belongs to the host adapter. After completing this command, HACC will be asserted indicating normal command completion.

5.1.1.12 Return Configuration Data (Opcode 0B)

The DMA channel and Interrupt channel selection will be returned in the registers. After receiving this command, the host adapter returns three bytes of data which specifies the configuration data:

Byte 0 -- DMA channel
bit 0 = ch. 0
5 = ch. 5
6 = ch. 6
7 = ch. 7

Byte 1 -- Interrupt channel
bit 0 = ch. 9
1 = ch. 10
2 = ch. 11
3 = ch. 12
4 = Reserved
5 = ch. 14
6 = ch. 15

Byte 2 -- SCSI ID
bit 7-5, unused
2-0, SCSI ID in Binary

After completing this command, HACC will be set indicating normal completion.

5.1.1.13 Write Adapter FIFO Buffer (Opcode 1C)

After receiving this command, the host adapter expects three bytes of data which point to an area of 54 bytes in system RAM. The most significant address byte is sent first. MSB, MID, LSB. The pointed to area will be fetched to the host adapter FIFO buffer. After completing this command, HACC will be set indicating normal completion. This command is used for host adapter diagnostics.

Data Byte 0 -- MSB Address
Data Byte 1 -- MID Address
Data Byte 2 -- LSB Address

5.1.1.14 Read Adapter FIFO Buffer (Opcode 1D)

After receiving this command, the host adapter expects three bytes of data which point to an area of 54 bytes in system RAM. The most significant address byte is sent first. MSB, MID, LSB. The content of the host adapter FIFO buffer will be sent to the pointed area. After completing this command, HACC will be set indicating normal completion. This command must be used after a write FIFO buffer command. This command is used for host adapter diagnostics.

Data Byte 0 -- MSB Address
Data Byte 1 -- MID Address
Data Byte 2 -- LSB Address

5.1.1.15 ECHO Command Data (Opcode 1F)

This command is used to test host port 1. After receiving this command, the host adapter expects one byte of data. The host adapter sends (ECHOs) this same data back to the host. After completing this command, HACC will be asserted indicating normal completion.

Data Byte 0 -- Echo Data

5.2 MAILBOX OVERVIEW

The AHA-1540 uses a mailbox architecture for task communication between the host and the host adapter when executing SCSI commands. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. At power up, the host issues an initialization command to inform the host of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). The MBIs are located immediately after the MBOs. A typical mailbox structure is shown below.

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example, there are four MBOs and four MBIs. The first byte of each MBO contains the command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides additional task information. A MBO is free if the first byte is zero. The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the task. A MBI is free if the Status byte is zero. One may allocate from 1 to 255 mailboxes. For a multitasking operating system, the number of mailboxes should be proportional to the number of tasks.

5.2.1 Mailbox-Out Structure

MBO Byte 0 -- Status Byte
- 00 -- Mailbox Free
- 01 -- Start SCSI command as described by the CCB
- 02 -- Abort previously started SCSI command.

MBO Byte 1 -- CCB Address MSB
MBO Byte 2 -- CCB Address MID
MBO Byte 3 -- CCB Address LSB

5.2.2 Mailbox-In Structure

When a SCSI command completes, the host adapter scans the first byte of an MBI entry to find a free mailbox. If one is found, it will update the MBI's status byte with a non zero value and update the address pointer to the task's CCB pointer. Valid status codes are shown below:

MBI Byte 0 -- Status Byte
- 00 -- Mailbox free
- 01 -- Completed without error
- 02 -- CCB aborted by the host
- 03 -- CCB for aborted task was not found
- 04 -- CCB completed with error

MBI Byte 1 -- CCB Address MSB
MBI Byte 2 -- CCB Address MID
MBI Byte 3 -- CCB Address LSB

5.2.3 COMMAND BLOCK OVERVIEW

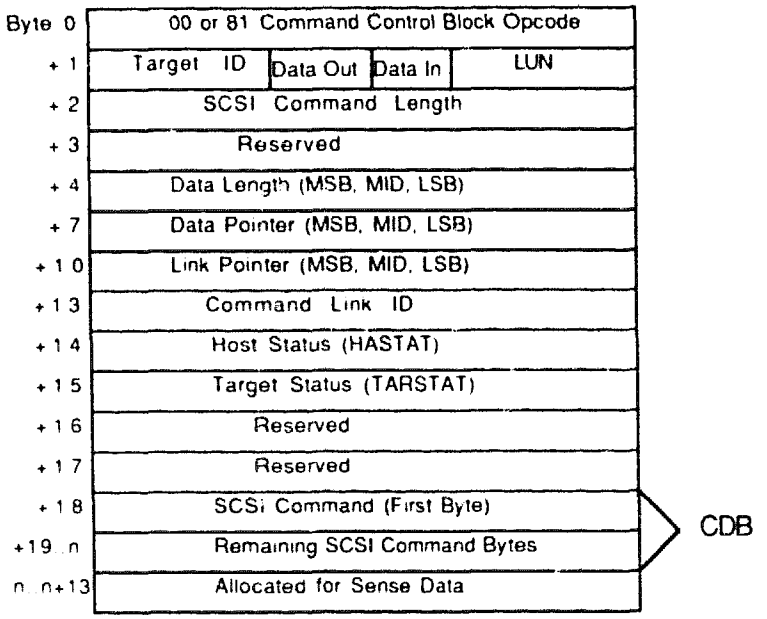
The CCB details information about a SCSI command. The format of a CCB is shown below:

Byte	0	00 or 81-- Command Control Block Opcode
	1	bit 7-5 -- Target ID bit 4 -- Outbound data transfer, length is checked bit 3 -- Incoming data transfer, length is checked bit 2-0 -- LUN
	2	SCSI command length
	3	Reserved
	4	Data length (MSB)
	5	Data length (MID)
	6	Data length (LSB)
	7	Data pointer (MSB)
	8	Data pointer (MID)
	9	Data pointer (LSB)
	10	Link pointer (MSB)
	11	Link pointer (MID)
	12	Link pointer (LSB)
	13	Command link ID
	14	Host status (HASTAT)
	15	Target status (TARSTAT)
	16	Reserved
	17	Reserved
	18	SCSI command, first byte
	19..n	Remaining SCSI Command Bytes

n-n+13: 14 Bytes of Sense Data if target check status is stored in byte 15.

Note: Sense Data is target specific. See your target's manual for details.

A block diagram representation of a CCB follows:



The bytes of the CCB are defined further below:

Byte 0: Command Control Block Opcodes

The AHA-1540 supports two CCB commands. SCSI and Bus Device Reset. The valid command values are shown below:

00	SCSI Command
81	Bus Device Reset

If the command value is zero, the SCSI command specified in the Command Control Block is sent to the addressed Target/LUN. If the value is 81(hex) a Bus Device Reset message will be sent to the addressed target. This command forces the host adapter to abort all outstanding tasks against the selected target. All remaining CCB Bytes are ignored. Any other command value generates a host adapter detected error 16.

Byte 1: Target/LUN

This byte identifies the target SCSI device, the direction of the data transfer if desired, and the LUN. Bits 4 and 3 can be set to determine the direction of data transfer. If bits 4,3 combination is set to 1,0 the AHA-1540 will anticipate a data-out phase. If the bit 4,3 combination is set to 0,1 the AHA-1540 will anticipate a data-in phase. Setting these valid combinations reduces software overhead. The length of the data transfer is also checked when these bits are set. If the amount transferred exceeds the specified amount, the CCB host adapter status field will contain an error code of 12(hex). A target check condition can cause a data underrun. With bit 4 and 3 both set to 0, data transfer direction is determined by the SCSI command. If both bit 3 and bit 4 are asserted, no data transfer is allowed.

Byte 2: SCSI Command Length

This byte establishes the length, in bytes, of the SCSI Command Descriptor Block.

Byte 3: Reserved (must be 0)

Bytes 4, 5, 6: Data Length

These bytes determine the length, in bytes, of the data transfer. CCB host adapter error 12(hex) is posted if a data over run occurs.

Bytes 7, 8, 9 : Data Pointer

These bytes specify the absolute address of the data area.

Bytes 10, 11, 12: Link Pointer

These bytes are used when a SCSI command contains a LINK or LINK WITH TAG bit in the command. When a Linked command is completed, the host adapter will use the contents of this field as a pointer to the next CCB to execute. If the Linked Tag bit is set, an interrupt will be generated before the next command is started. A completed CCB is always reported back in an MBI.

Byte 13 : Command Link ID

This byte is used in conjunction with linked commands. It is set by the host to identify commands in a command chain.

Byte 14 : Host Status

This byte is used to report the host adapter status (HASTAT).
HASTAT has the following definitions:

00 -- No host adapter detected error
0A -- Linked command complete without error
0B -- Linked command complete without error, interrupt generated
11 -- Selection time out
12 -- Data over run/Under run
13 -- Unexpected bus free
14 -- Target bus phase sequence failure
15 -- MBO command was not 00 or 02
16 -- First byte of the CCB was not 00 or 81
17 -- Linked CCB does not have the same status byte codes

Byte 15: Target Status

This byte is used to report the target status (TARSTAT).
TARSTAT has the following definitions:

02 -- Check Status (use Request Sense Command to get details)
08 -- LUN Busy
18 -- Reservation Conflict

Byte 16: Reserved (must be 0)

Byte 17: Reserved (must be 0)

Byte 18: n: SCSI Command

This field holds the SCSI Command Descriptor Block (CDB) as described in the SCSI specification. The length of this command is described in byte 02. When the Command Control Block commands are used, the host adapter is operating in its multithreaded mode. In this mode, the host adapter has the capability to be a task manager, simultaneously handling multiple commands against multiple targets. The host adapter supports SCSI disconnection/reconnection, and arbitration to maximize I/O channel throughput.

Byte n..n+13: Sense Data

This space is filled with up to 14 bytes of sense data when a target check status is detected.

5.2.4 Operation

After finding an active mailbox, the AHA-1540 copies the command field contents and CCB pointer into its internal RAM and clears the command byte, freeing the mailbox. Up to 16 CCB's can be stored in the host adapter's internal RAM concurrently. The AHA-1540 maximizes the SCSI bus utilization by starting the next available CCB as soon as the bus is free. Disconnection and reconnection on the bus are automatically taken care of by the AHA-1540. If the MBO command is to start a SCSI command, the AHA-1540 will first determine if the addressed target/LUN is busy. If the target/LUN is busy, then the command will be placed in the task queue.

Commands are removed from the queue in the order that they were received, establishing a (FIFO) first in first out command execution order. Of course, the order of task completion may vary due to the different amounts of time required to process and complete different commands. If the target/LUN is not busy, the new command is started at the next bus free phase. If busy target status is received by the AHA-1540, the CCB is placed at the end of the FIFO queue to be restarted later.

If a check status is received from the target, the AHA-1540 will issue a Request Sense command to get the sense data. The sense data is stored in the CCB after the SCSI command data. The driver software must reserve 14 bytes at the end of the CCB to hold the sense data which is returned as result of a receiving a check status.

If the MBO command is to abort a SCSI command, the host adapter first searches the active and queued CCBs. If the CCB is found, the task is aborted at the earliest possible moment. If the CCB is not found among the active or queued CCBs, the AHA-1540 completes the command and reports an error in MBI status. It is possible to send an Abort command and find that the CCB has completed. In this case the host adapter will report that the CCB was not found.

The AHA-1540 scans the MBOs in a round robin fashion. This is to ensure that all of the mailboxes will be scanned with equal probability. A host can minimize the AHA-1540 MBO scan time by using MBO's sequentially.

When executing a START SCSI command, the AHA-1540 does not verify that the new CCB is currently active or queued. Therefore, the host must not restart a CCB before it is completed. CCB addresses are used by the AHA-1540 as task identifiers.

5.3 SINGLE THREADED HARD DISK I/O COMMANDS

PC/AT BIOS commands are provided to support single-threaded PC/MS DOS hard disk I/O. This mode of operation allows the system to access SCSI peripherals one at a time without the use of the Mailboxes.The BIOS issues adapter command (03) Start PC/AT BIOS command, to the host adapter. If there are outstanding SCSI commands, the AHA-1540 will assert INVDCMD, invalid command, to reject the command. If there are not any outstanding SCSI commands, the AHA-1540 expects the following ten bytes of command data from the BIOS:

byte	0	Command Value (see Section 5.3.7)
	1	Drive Number (Target/LUN)
	2	High Order Cylinder Number
	3	Low Order Cylinder Number
	4	Head Number (4 bits only)
	5	Sector Number (5 bits only)
	6	Sector Count
	7	Buffer Address (MSB)
	8	Buffer Address (MID)
	9	Buffer Address (LSB)

5.3.1 Drive Number

Normally only hard disks C: and D: are accessed by the AT. Using this byte, the BIOS or device driver can access any target or LUN that is attached to the host adapter. However, the BIOS design limits access to target 0 and 1, LUN 0 only. Bits 7 to 5 form the target address, and bits 2 to 0 form the LUN. The remaining bits are reserved and should be deasserted.

5.3.2 Cylinder Number

The BIOS generates this number from the CL and CH registers.

5.3.3 Head Number

The BIOS generates this number from the DH register.

5.3.4 Sector Number

The BIOS generates this number from the CL register.

5.3.5 Sector Count

The BIOS generates this number from the AL register.

*Note: To provide BIOS compatibility with DOS PC/AT commands, which use DOS physical parameters rather than SCSI logical addresses, a translation algorithm is used. The SCSI logical address is formed by concatenating cylinders, heads, and sector values. The algorithm is (16 heads * 32 sectors * n cylinders) in all cases. Refer to Section 5.4.6 and 5.4.15 for more information. This translation results in all drives appearing as having 16 heads, 32 sectors per track, and a number of cylinders that does not match the physical parameters of the drive.*

5.3.6 Data Buffer Pointer

This pointer is generated from ES:BX registers. The 80286 and 80386, in the real mode, support a 20-bit address. However, SCSI commands can utilize the full 24-bit address space of the AT bus. PC commands will always assume that the address space is limited to 20 bits, and will force the upper address bits to 0. SCSI commands must have all 24 bits defined. This means that in protected mode, or with some other processor, it is the hosts responsibility to build a 24-bit pointer to the CCB and data areas, and to use the mailboxes for 24-bit addresses.

After sending ten bytes of data, the host BIOS will wait for the assertion of HACC and then read the completion status from the data port. Completion status is one byte long. Valid PC/AT command and status values are defined in Section 6.1.4.

5.3.7 Command Byte -- Similar to the PC/AT BIOS Function Codes

00H -- Reset SCSI Bus
01H -- Sense
02H -- Read Sectors
03H -- Write Sectors
04H -- Verify Sectors
08H -- Return Drive Parameter
09H -- Initialize Drive Pair
0CH -- Seek
0DH -- Alternate SCSI Reset
0EH -- Read Buffer
0FH -- Write Buffer
10H -- Test Drive Ready
11H -- Recalibrate
14H -- Self Diagnostics
15H -- Get Disk Type

Status Byte -- Provided after command completion

00 -- Completed without error
01 -- Invalid PC/AT Command
02 -- Error Status From Target
04 -- Selection Timeout (Target Not Online)
08 -- Selected Target is Busy
10 -- Host Adapter Detected Bus Phase Error
18 -- Addressed Target or Sector is Reserved

Note: The AHA-1540 BIOS PC/AT commands are identical to the BIOS function codes. However, the BIOS must generate the proper BIOS status from the host adapter return status byte and the target sense data. The BIOS will return one of the status values, to the host software, as defined below:

BIOS Status Codes

FFH - Sense Failed
CCH - Write Error
BBH - Unknown Target Sense Data
AAH - Not Ready
80H - Selection Timeout
40H - Bad Seek
20H - Bad Controller
10H - Uncorrectable ECC Error
11H - Correctable ECC Error
07H - Drive Parameter Activity Failed (command 09)
04H - Read Error
01H - Bad Command

5.4 COMMAND BYTE DESCRIPTIONS

5.4.1 Reset SCSI Bus (00)

The AHA-1540 asserts the SCSI Reset line. The remaining nine bytes of data are not used.

5.4.2 Sense (01)

The AHA-1540 issues a SCSI Request Sense (03) command to the selected target/LUN. The command returns 4 bytes of data to the specified data area. These are defined as follows:

Byte 0 -- Sense code, extended sense data byte 12.
Byte 1, 2, 3 -- Sector address, extended sense data byte 4-6, cylinder, head, sector address, and sector count are not used.

5.4.3 Read Sectors (02)

The AHA-1540 issues a SCSI Read command (08) to the addressed target/LUN. The sector address is generated by concatenating cylinder, head (4 bits) and sector addresses (5 bits). A 512 byte sector size is assumed. The DMA channel is set up to transmit to the host.

5.4.4 Write Sectors (03)

The AHA-1540 issues a SCSI Write command (0A) to the addressed target/LUN. The sector address is generated by concatenating cylinder, head (4 bits) and sector addresses (5 bits). A 512 byte sector size is assumed. The DMA channel is set up to transfer from the host.

OPTIONS (CONT'D)

5.4.5 Verify Sectors (04)

The AHA-1540 issues a SCSI Verify command (2Fh) to the addressed target/LUN. The sector address is generated by concatenating cylinder, head (4 bits), and sector addresses (5 bits). No data is transferred by this command.

5.4.6 Return Drive Parameters (08)

The AHA-1540 sends a SCSI Read Capacity command (25h) to the addressed target/LUN. It returns six bytes of data to the specified data area. These are defined below:

Byte 0-3, Total number of sectors on the LUN
Byte 4-5, Block size

The BIOS will return the number of cylinders to be the value in bytes 0 and 1. The BIOS will also report back the number of sectors per track as being 32, and the heads per cylinder as being 16. This information is used by the AHA-1540 to concatenate cylinder, head, and sector numbers back to the SCSI logical sector number.

5.4.7 Initialize Drive Pair (09)

This command works like a Reset command since all SCSI devices are self configuring.

5.4.8 Seek (0C)

The AHA-1540 issues a SCSI Seek command (0B) to the addressed target/LUN. The sector address is generated by concatenating cylinder, head (4 bits), and sector addresses (5 bits).

5.4.9 Reset SCSI Bus (0D)

The AHA-1540 asserts the SCSI Reset line. The remaining nine bytes are not used.

5.4.10 Read Buffer (0E)

The AHA-1540 issues a SCSI Read Buffer command (3Ch) to the addressed target/LUN. The data transfer size is the (Sector Count * 512)+4. The DMA channel is set up to transfer to the host. The cylinder, head, and sector addresses are not used.

5.4.11 Write Buffer (0F)

The AHA-1540 issues a SCSI Write Buffer command (3Bh) to the addressed target/LUN. The data transfer size is the (Sector Count * 512)+4. The DMA is set up to transfer from the host. Cylinder, head, and sector addresses are not used.

5.4.12 Test Unit Ready (10)

The AHA-1540 sends a SCSI Test Unit Ready command (00) to the addressed target/LUN. The remaining 8 data bytes are not used.

5.4.13 Recalibrate (11)

The AHA-1540 sends a SCSI Recalibrate command (01) to the addressed target.LUN. The remaining 8 data bytes are not used.

5.4.14 Self Diagnostics (14)

This causes the AHA-1540 to perform self diagnostic functions. A check status is returned if the diagnostic functions failed.

5.4.15 Get Disk Type (15)

The AHA-1540 issues two SCSI commands, Read Capacity (25h), and Inquiry (12h) to the addressed target/LUN. It returns six bytes of data to the specified data area. These are defined as shown below:

Bytes 0-3: Total number of sectors on an LUN
Bytes 4-5: First two bytes of Inquiry data. (command 12h)

The BIOS will return the proper media data to the host.

6.1 PC/AT BIOS

The PC/AT BIOS is provided to allow the user to use the AHA-1540 in lieu of, or in addition to, a standard PC/AT hard disk controller. This compatibility includes booting from a SCSI device. Hard disk requests are sent to the BIOS via an INT 13 software interrupt. CPU register contents specify the desired I/O function and associated parameters. The BIOS then uses host adapter commands to emulate PC/AT functions. Again, since the mailbox architecture is circumvented, PC/AT BIOS functions run in a single-threaded mode.

The BIOS consists of three major functional components. These are:

1. Initialization Routine
2. System Boot Routine
3. Hard Disk I/O Routine

6.1.1 Initialization

The Initialization routine is called at power-up. This routine performs all of the necessary initialization functions and will display the following message if the system successfully recognizes the AHA-1540 BIOS.

ADAPTEC AHA-1540 HOST ADAPTER BIOS
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ALL RIGHTS RESERVED.

If any subsequent initialization of the AHA-1540 fails, the following message is displayed:

HOST ADAPTER NOT FOUND AT PORT 330H.

Otherwise, the AHA-1540 BIOS chooses a course of action based upon the number and types of hard disks already installed. In each case, the number of hard disks already installed is displayed along with the ID numbers of any SCSI devices that are successfully used by the BIOS.

Possible Messages:

HARD DISK #0 ALREADY INSTALLED.
HARD DISK #1 ALREADY INSTALLED.
HOST ADAPTER DIAGNOSTIC FAILURE.
SCSI DEVICE 0 : 0 NOT FOUND.
USING SCSI DEVICE 0 : 0 AS HARD DISK #0.
USING SCSI DEVICE 0 : 0 AS HARD DISK #1.
USING SCSI DEVICE 0 : 1 AS HARD DISK #1.
USING SCSI DEVICE 1 : 0 AS HARD DISK #1.

NOTE: No error message is displayed if a second SCSI drive is not available.

If the system reports an initial number of hard drives greater than 2, the following message is displayed:

SYSTEM CONFIGURATION ERROR.

The AHA-1540 BIOS allows the use of 0, 1, or 2 hard disks on the SCSI bus under DOS without a device driver.

If 2 hard disks are attached to an internal hard disk controller, and are already recognized by the system, the BIOS does nothing. A device driver will be needed to access SCSI devices.

If 1 hard disk is attached to an internal hard disk controller, and is already recognized by the system, the BIOS attempts to assign the SCSI device (Target : LUN) 0 : 0 as the second drive. (drive D:) If this is unsuccessful, an initialization error is reported to the system.

If there are 0 hard disks attached to an internal controller, the BIOS attempts to assign the first SCSI device (Target : LUN) 0 : 0 as the first drive. (drive C:) If this is unsuccessful an initialization error is reported to the system. If successful, the BIOS attempts to assign another SCSI device as the second drive. (drive D:) Device 0 : 1 is tried first, and if that fails, device 1 : 0 is tried. There is no initialization error reported if a second drive is not available.

6.1.2 System Boot

This routine is called to boot an operating system when drive C: is a SCSI drive. It performs the system boot from devices in the following order:

1. Floppy drive A:
2. Device attached to the AHA-1540 Target 0 LUN 0, (drive C:)

6.1.3 Hard Disk I/O

The BIOS enables up to two SCSI drives to be accessed via interrupt 13. This allows two drives to be used under DOS since PC DOS and MS DOS or their application programs use a INT 13h instruction.

The hard disk I/O routine checks the device address specified in the DL register for the following actions:

DL = 0 or 1, invoke floppy BIOS.
DL = 80 or 81, send a PC/AT command through the AHA-1540 to device at target 0, LUN 0.

If an INT. 13 call is directed to the AHA-1540 and a check status is received from the target, a SCSI REQUEST SENSE command is issued and translated into the proper BIOS completion codes.

Command parameters are passed in the 80286 and 80386 registers as described below:

AH BIOS Function
AL Number of Sectors
CH Low Order Cylinder Number
CL bits 7, 6 High Cylinder Number bits
bits 5, 0 Sector Number
DH Head Number
DL Drive Number (80 or 81)
ES:BX Data Buffer Pointer

The BIOS intercepts the INT. 13h calls. When the selected drive is a SCSI device, the BIOS builds a single threaded host adapter PC/AT command.

6.2 XENIX/UNIX Drivers

SCO XENIX support will be available at production release. Generic (non-bootable) Xenix and Unix drivers are available for OEM integration.

6.3 DOS Driver

An optional DOS Driver is available that enables the AHA-1540 to access additional SCSI devices on the SCSI bus. When operating under DOS, a device driver is needed to access more than two hard disks, tape devices or other types of SCSI peripherals. If all DOS operations will be confined to two SCSI disks or one internal and one SCSI disk, a device driver is not needed because of the on-board BIOS.

The DOS driver is installed by creating a DOS configuration (CONFIG.SYS) file that calls the device driver at boot time. Please refer to your DOS manual for information on creating a CONFIG.SYS file. At initial system loading, the AHA-1540 device driver will determine the number of hard disks attached to the system. The device driver is normally only installed if one of the following cases is true.

1) There are two internal hard disks and one or more SCSI disks.
2) There is one internal hard disk and two or more SCSI disks.
3) There are no internal hard disks and more than two SCSI disks.

The following table shows how hard disks in a system are addressed:

Configuration	C:	D:	Device Driver
TWO INTERNAL HARD DISKS	1st Int Disk	2nd Int Disk	SCSI Devices
ONE INTERNAL HARD DISK	Internal Hard Disk	SCSI 0/0 Disk	Other SCSI Devices
NO INTERNAL HARD DISK	SCSI 0/0 Disk	SCSI 0/1 or 1/0	Other SCSI Devices

The SCSI disk drives that are accessed by the device driver are divided into 32 MB logical disks. There can be multiple logical disks on one physical SCSI disk drive. A utility program is also provided that performs the functions of the DOS FDISK and FORMAT utilities. This utility will perform FDISK and FORMAT to SCSI disks that can only be accessed through the device driver. These utility programs partition the disks and create file directories so that DOS files may be copied and accessed from SCSI drives. Please refer to your DOS manual for details of FDISK and FORMAT.

SCSI II compatible and QIC 104 command set 1/4" tape drives are also be supported by the DOS device driver. The user accesses a SCSI tape drive by building a CCB as described in Section Five. The device driver passes the CCB to the AHA-1540 and instructs the AHA-1540 to complete the command.

6.4 VIRTUAL MEMORY/VIDEO MEMORY DRIVER

The use of high performance 16-bit first party DMA on the AHA-1540 SCSI host adapter may result in incompatible operation with two types of application programs.

The first category includes any programs that transfer screen images directly from disk to video memory. The host adapter supports only high performance 16-bit data transfers, while video memory uses an 8-bit interface.

The second category includes DOS programs that use the virtual mode, V86, mode of operation on 80386 based AT machines. In real mode, the host adapter BIOS is passed a physical address. This is necessary since the host adapter controls all SCSI I/O without CPU intervention. This physical address may not be passed to the host adapter when the system is in the V86 mode. Programs that use the V86 mode can only be run on 80386 machines.

A software driver is available that will allow these two types of application programs to run under DOS.

To install the driver into your boot routine, you must create, or edit the DOS configuration file named CONFIG.SYS. You can use any file editor to do this, or you can create it through the "COPY CON: CONFIG.SYS" DOS command. Refer to your DOS manual for more information on this command. Once installed, the driver operates transparently to the user.

6.5 AHA-1540 On-board Utilities

The AHA-1540 BIOS contains a utility program that allows the user to perform the following functions:

1) A list of all devices installed on the SCSI bus may be requested. This information is retrieved via a RETURN INSTALLED DEVICES host adapter command, followed by INQUIRY commands to all available targets.

2) A low level, or primary, format of any Target/LUN can be requested. A MODE SELECT is issued first to set the block size at 512 bytes per sector. Then a FORMAT command is issued which will format the drive with factory as well as grown defects. *Note: Only one SCSI drive can be formatted at a time.*

3) Integrity of a target can be checked by verifying an entire drive. Any correctable errors found will automatically be handled through the SCSI Reassign Blocks Command. If any uncorrectable errors are found the user will first be asked via a screen prompt if reassignment of this block should be performed.

Utilities are invoked through DOS debug. Once in Debug, type G=XXXX:6 where XXXX is the BIOS base address. Default = DC00:6. Once invoked, the utilities are menu driven.

Section Seven Advanced Features

7.1 LINKED SCSI COMMANDS

The AHA-1540 supports linking of SCSI commands. When the link bit in the SCSI command control byte is set, the target will present either a 0A or 0B message at command completion. The AHA-1540 uses the the link pointer in a CCB to fetch another CCB. At the same time, the completed CCB status and address are stored in an MBI. If the target returns the 0B status, the AHA-1540 generates an interrupt to inform the host of the full MBI. The linked CCBs must address the same target and LUN since the target is not re-selected.

7.2 ZERO LATENCY READ OPERATION

The AHA-1540 implements Zero Latency operation through the use of modify data pointer messages. Zero Latency can eliminate rotational latency, depending on the length of the data transfer, by supporting out of order data transfers. This advanced feature is currently only implemented on the ACB-4525Z SCSI to ESDI controller, and is supported transparently to the user.

7.2.1 Zero Latency Implementation Notes

Since the Adaptec AHA-1540 is the first SCSI host adapter to support Zero Latency Read operation, this section is intended to briefly explain the required target support. Please refer to the Adaptec ACB-4525Z SCSI to ESDI controller manual for complete details of Zero Latency Read operation.

After seeking to the target track, the ACB-4525Z (ACB-4525Z is assumed since it is the first SCSI controller to implement this feature) will begin reading block IDs. If the first block ID is within range of the data transfer, but not the last block of the the data transfer, the ACB-4525Z will begin reading the subsequent blocks into its buffer. Before transferring data the ACB-4525Z will issue a MODIFY DATA POINTER message to the AHA-1540. This supplies a positive argument that is added to the value of the current data pointer. The ACB-4525Z will now send this portion of the data transfer to the host. The ACB-4525Z will resume reading data into its buffer as soon as the first block of the data transfer is detected. Before sending this data to the host, the ACB-4525Z will issue a second MODIFY DATA POINTER message to the AHA-1540 which supplies a negative argument. This returns the data pointer to its original position. This guarantees that a data transfer of one track or less will never require more than a single revolution since data can now be transferred out of order.

7.3 EXTENDED SCSI MESSAGE SUPPORT

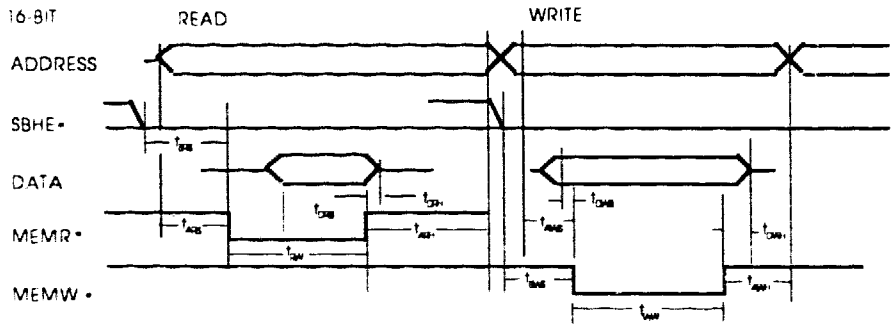
The AHA-1540 supports both the Synchronous Negotiation and Modify Data Pointer extended messages.

7.4 SELF DIAGNOSTICS

The AHA-1540 will execute self diagnostics upon power up, or after a hard reset. These test will check the CPU operation, do a sum check on the EPROM, and check the data path on the board. The host has the option of exercising more extensive diagnostics involving reads and writes to memory. These diagnostics require participation by the host.

Appendix A AHA-1540 System Timing Diagram

AHA-1540 MEMORY CYCLE TIMING



t_{ARS} Address Setup to MEMR Leading Edge
t_{ARH} Address Hold from MEMR Trailing Edge
t_{BRS} SBHE Setup to MEMR Leading Edge
t_{DRS} Data Setup to Leading Edge of MEMR
t_{DRH} Data Hold from MEMR Trailing Edge
t_{RW} Read Pulsewidth

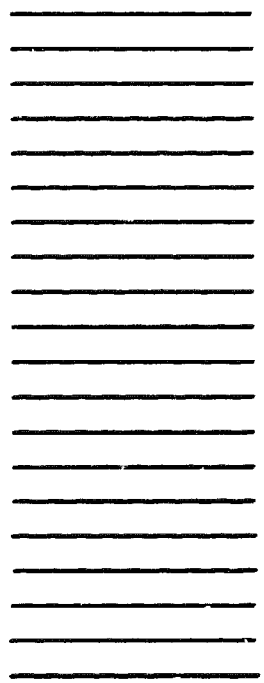
t_{AWS} Address Setup to MEMW Leading Edge
t_{AWH} Address Hold from MEMW Trailing Edge
t_{BWS} SBHE Setup to MEMW Leading Edge
t_{DWS} Data Setup to MEMW Leading Edge
t_{DWH} Data Hold from MEMW Trailing Edge
t_{WW} Write Pulsewidth

NOTE: All single-byte transfers use the slowest speed.

SPEED	5.0 MB (nanoseconds)	6.7 MB (nanoseconds)	8 MB (nanoseconds)	10 MB (nanoseconds)
t_{RW}	300	200	150	100
t_{ARS}	69	69	69	69
t_{ARH}	-8	-8	-8	-8
t_{BRS}	100	100	100	100
t_{DRS}	15	15	15	15
t_{DRH}	0	0	0	0
t_{WW}	250	150	100	100
t_{AWS}	69	69	119	69
t_{AWH}	42	42	-8	-8
t_{BWS}	100	100	100	100
t_{DWS}	-8	-8	-8	-8
t_{DWH}	36	36	36	36

adaptec

AHA-1540A/1542A
User's Manual



Preface

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Additional information may be obtained from:

Adaptec
Literature Department
691 South Milpitas Blvd.
Milpitas, CA 95035

Preface

FCC Compliance

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television equipment reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to Identify and Solve Radio-TV Interference Problems"

This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

Warning: This equipment has been certified to comply with the limits for Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception. Also this equipment must be used with shielded power cables and shielded I/O cables.

AHA-1540A and AHA-1542A Industry PC/AT-to-SCSI Host Adapter
User's Manual and Specification

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Section One Introduction

1.1 DOCUMENT SCOPE

This manual provides the information required to install and program the AHA-1540A and the AHA-1542A Intelligent Host Adapters in AT bus-based systems.

1.2 PURPOSE

The Adaptec AHA-1540A and AHA-1542A provide a powerful multitasking interface between the Industry Standard Architecture (PC/AT compatible) bus and the Small Computer System Interface (SCSI) bus. The AHA-1540A/1542A are high performance intelligent host adapters supporting a maximum asynchronous SCSI rate of 2.0 MBytes/second and a synchronous transfer rate of 5 MBytes/second. The AHA-1540A/1542A support multithreaded I/O operations, allowing simultaneous operations on multiple targets/LUNs. Disconnect/Reconnect support maximizes bus utilization for multiple target systems. Target mode operation allow the AHA-1540A and AHA-1542A to receive information from other host adapters. Scatter-gather allows high-performance even in systems with fragmented memory buffers.

The Adaptec AHA-1540A/1542A provides a solution for system applications requiring very high performance, configuration flexibility and multithreaded I/O capability, and system redundancy. The Adaptec BIOS also allows the AHA-1540A/1542A to be used in place of a standard hard disk controller. The AHA-1540A host adapter provides only the high performance host adapter circuitry. The AHA-1542A host adapter provides identical host adapter circuitry, but adds an IBM compatible flexible diskette controller to the circuit board.

1.3 AHA-1540A/1542A PRODUCT FEATURES

- High performance Bus Master DMA with selectable or programmable data rates of up to 10 MBytes/second.
- 16- and 8-bit transfers
- Odd and Even starting address transfers and odd or even data lengths
- Maximum synchronous SCSI transfer rate of up to 5.0 MBytes/second
- Asynchronous and synchronous peripherals supported simultaneously
- Programmable AT bus burst transfer on and off time
- Jumper selectable DMA channel for bus arbitration (channels 0,5,6,7)
- Jumper selectable interrupt channels (IRQ 9, 10, 11, 12, 14, 15)
- True multithreaded operation supporting up to 255 tasks simultaneously
- Programmable mailbox architecture
- Adaptec BIOS for standard hard disk emulation
- Jumper selectable I/O port address
- Internal and external SCSI connectors
- Initiator and Target modes of operation fully supported
- On-board flexible diskette controller (AHA-1542A only)
- Scatter-gather

1.4 PRODUCT SPECIFICATIONS

- Physical Dimensions:

  Length : 13.25 " Width : 4.125" Height : 0.5"

  Standard PC/AT™ compatible form factor

- Power Requirements:

  +5.0 +/- 0.25 Volts at 2.1 Amps maximum.

- Environmental Requirements:

  Temperature 0-60 degrees C (operating or storage)

- Reliability Information

  Mean Time Between Failures: 15000 hours
  (calculated per Mil Handbook 217E, ground benign, 40 °C)

  Mean Time Between Failures: TBD hours
  (experimental)

  Mean Time to Repair: 30 minutes

- Industry Standard Architecture Interface

  Standard PC/AT bus electronic and physical interface.

  Driver output:

V_{OL}:	min:	0 volts	max.	0.4 volts	I_{OL}:	24 ma.
V_{OH}:	min:	2.4 volts	max.	5.25 volts	I_{OH}:	8 ma.

  Receiver Input

  V_{IL}: 0.8 volts
  V_{IH}: 2.0 volts

  Connector configuration as specified by IBM PC/AT Technical Reference Manual or manual of Industry Standard Architecture host computer.

- SCSI Interface:

Electrical Interface:

As specified by ANSI X3.131-1986 for single-ended operation.

Minimum driver output: 48 milliamps, sinking @ 0.5 volts

Signal true:	min:	0 volts	max:	0.8 volts
Signal false:	min:	2.0 volts	max:	5.25 volts
Input hysteresis:	min:	0.2 volts		
Terminator Power voltage:	min:	4.25 volts	max:	5.25 volts
Terminator Power current:	min:	800 ma.	max:	1.5 amp (fused)

Internal connector:

Unshrouded 50-pin header, compatible with unshielded alternative 1 connector as specified in ANSI X3.131-1986 Figure 4-1

For connector pin out, see Appendix B.

Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3425-6000
T&B Ansley	N.A.	609-5000M
Molex	N.A.	15-29-8505

Cable for internal SCSI connector should be good quality 50 conductor flat cable with 26 or 28 gauge conductors and a characteristic impedance (Z_0) of 100 ± 10 Ω. Cable shielding is necessary if extremely noisy circuitry or extremely noise sensitive circuitry is present inside the host computer frame.

External connector:

Shielded 50-pin connector as specified in ANSI X3.131-1986, Figure D-4.

For connector pin out, see Appendix B.

Partial list of compatible connector plugs or cable assemblies (for reference only):

Manufacturer	Model	Part Number
Amphenol	N.A. (Mates with 57-BC50B-AM200)	200-1M115-02003
AMP	Champ	
	Plug	554953-1
	Cover	554946 - x(1-2)
	Ferrule	554725 - x(1-6)

Cable for external SCSI connector should be good quality 100% shielded round cable with 25 twisted pairs. Each pair should have a characteristic impedance (Z_0) between 90 and 135 Ω. Wire gauge may be 26 or 28 AWG. All pairs should have the same impedance and should have the same delay per length of cable. Cables meeting these requirements will normally operate correctly in any SCSI configuration and should normally meet all FCC requirements.

- Floppy Disk Interface

Standard Floppy Disk electronic and physical interface:

Driver output:

V_{OL}:	min: 0 volts	max.	0.5 volts	I_{OL}:	60 ma.
V_{OH}:	open collector	max.	5.25 volts	I_{OH}:	.1 ma.

Receiver Input

Tied to +5 volt supply through 150 Ω resistors.
Schmidt Trigger with 0.8 volts hysteresis

V_{T-}:	max	1.0 volts
V_{T+}:	min	1.4 volts

Connector:

Unshrouded 34-pin header.

For connector pin out, see Section 9.1

Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3414-6000
T&B Ansley	N.A.	609-3400M

Cable for floppy connector should be good quality 34 conductor flat cable with 28 gauge conductors. Addressing of the second drive may be generated by twisting connector signals 10 through 16 or by changing jumpers in the floppy disk drives.

- Meets radiation limits specified for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. See FCC Compliance notes and recommendations in preface of this document.

1.5 REFERENCE DOCUMENTS

- IBM PC/AT Technical Reference Manual
- Small Computer System Interface, ANSI X3.131-1986, American National Standards Institute
- Adaptec AHA-1540A/AHA-1542A Host Adapter Installation Guide
- Adaptec AHA-1540 Programming Guide

2.1 HARDWARE

2.1.1 Bus Master DMA

The AHA-1540A/1542A controls the host AT bus as a master and transfers data directly to and from main system memory. This implementation is known as Bus Master DMA. Bus Master DMA greatly reduces the host software overhead because the host CPU is no longer required to maintain the DMA channel's address pointers and word counts. Bus Master DMA also reduces the number of interrupts generated per I/O command. The Adaptec AIC-560L is the DMA controller.

Adaptec's implementation of Bus Master DMA can achieve a 10 MB/second burst data rate. This speed is especially valuable in multitasking systems where the tasks execute on a time shared basis. Appendix A shows a diagram of the timing required to achieve the DMA rates that are supported by the AHA-1540A/1542A.

The AHA-1540A/1542A DMA hardware will handle both odd-byte and odd-memory address data transfers with no performance degradation.

2.1.2 SCSI Protocol Chip (AIC-6250)

The AHA-1540A/1542A utilizes the AIC-6250 SCSI protocol chip to maximize the SCSI bus utilization. The AIC-6250 is an Adaptec VLSI device which allows the AHA-1540A/1542A to achieve greater than 2.0 MBytes/Sec asynchronous SCSI data transfer rates, and up to 5.0 MBytes/second synchronous transfer rates. The AIC-6250 will also enable the AHA-1540A/1542A to operate as both an initiator and as a target device.

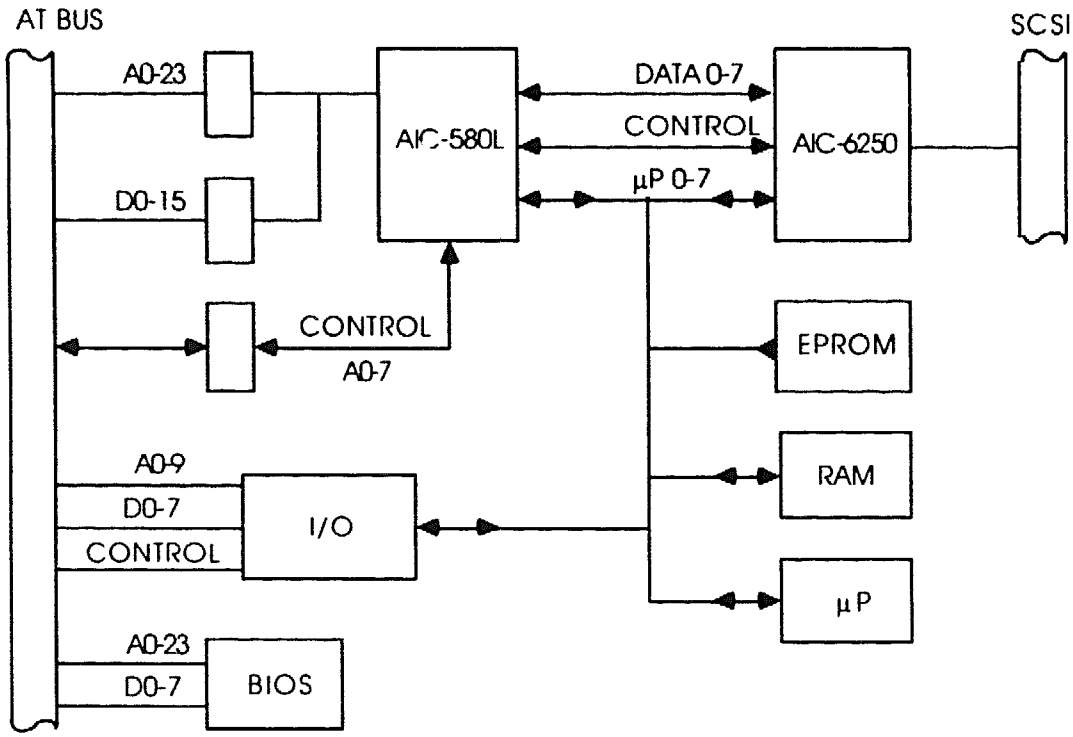
Through a 16-bit host interface, the AIC-6250 reduces bus busy time during data transfer by bursting data across the AT bus at up to 10 MBytes/second. The AIC-6250 has separate data busses for the local microprocessor and for the system data bus. This further increases the performance of the AHA-1540A/1542A by reducing the overhead associated with SCSI commands.

2.1.3 8 Bit Memory

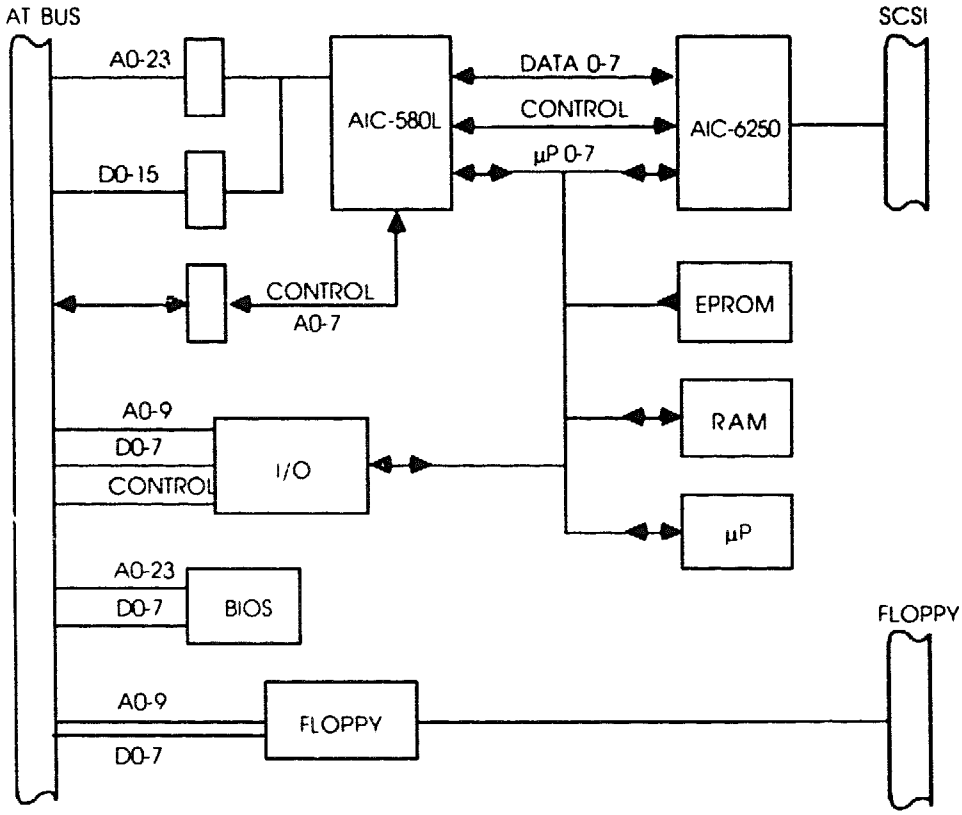
During normal DMA operations, nearly all transfers to and from memory are 16 bit transfers. At the very end, or the very beginning of an odd address boundary, an 8 bit transfer on the upper data bits (D8-D15) will occur according to the AT bus architecture. Some memory in the I/O space, such as video RAM, is 8 bits only and always transfers data only on the lower data bits (D0-D7). The AHA-1540A/1542A will transfer 16 bit or 8 bit memory in the address space between 0A0000 hex and 0BFFFF hex depending on the signal line MEM16 on the AT bus. If this signal is active, 16 bit memory is assumed, and if inactive 8 bit memory is assumed. Outside of this address space 16 bit memory is always assumed.

2.1.4 Hardware Block Diagram

BLOCK DIAGRAM OF AHA-1540A



BLOCK DIAGRAM OF AHA-1542A



2.2 FIRMWARE

The AHA-1540A/1542A supports multithreaded SCSI initiator operation through a simple mailbox protocol. The firmware accepts as many Command Control Blocks (CCB's) as required and executes them from its local RAM. The firmware controls all of the SCSI activity that a task may require. This includes: Arbitration, Selection, Disconnection, Reconnection, and Command completion.

Using the same mailbox protocol, the AHA-1540A/1542A can operate as a Processor type device serving as a multitasking target to other initiators. This feature allows high bandwidth communication between multiple hosts.

In addition, the AHA-1540A/1542A firmware cooperates with the BIOS installed on the host adapter to emulate the standard DOS BIOS calls. This allows booting operations and the execution of standard DOS operations from attached SCSI disks, allowing the SCSI subsystem to completely replace the usual internal disk functions.

2.2.1 Multithreaded Operation

A multiuser, multitasking operating system issues a large number of I/O tasks in a rapid sequence. The architecture of the AHA-1540A/1542A makes management of this activity very easy and straightforward for the operating system and its associated I/O drivers. This section briefly explains the interaction between the system and the AHA-1540A/1542A required to accomplish an I/O task.

2.2.1.1 Mailboxes

The AHA-1540A/1542A uses a mailbox architecture for task communication between the host and host adapter. This allows the host adapter to perform multithreaded operations with a minimum of host intervention.The mailboxes are located in main system memory . Each mailbox entry is four bytes long. After power up sequencing, host initialization procedures, and the boot procedure are completed, the host issues an initialization command to inform the host adapter of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). MBIs are located immediately after the MBOs. A typical mailbox structure is shown below:

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example there are four MBOs and four MBIs. The first byte of each MBO contains the MBO Command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides all the rest of the information needed to complete a task. A MBO is available to accept a new entry if the first byte is zero.

The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the completed task. An MBI is free if the Status byte is zero. Mailboxes may point to CCB's controlling initiator tasks, controlling target tasks, or controlling error recovery tasks.

2.2.1.2 Command Control Block

A Command Control Block provides the information required to control a SCSI command sequence. The block contains pointers to the data area to be used by the command. It contains areas for presenting status of both the host adapter and the addressed SCSI device. In addition, it contains the SCSI Command Descriptor Block defining the action to be taken by the addressed SCSI device. An error information buffer area is also provided.

A Command Control Block is also used to service an operation requested by another initiator when the AHA-1540A/1542A is being addressed as a SCSI Processor device.

The CCB is defined completely in Section 5.

A typical CCB is shown below:

Byte					
0	Command Control Block Opcode				
+1	Tar/Init	Data Out	Data In		LUN
+2	SCSI Command Length = m				
+3	Returned Sense Info Length = n				
+4	Data Length (MSB,MID,LSB)				
+7	Data Pointer (MSB,MID,LSB)				
+10	Link Pointer (MSB,MID,LSB)				
+13	Command Link ID				
+14	Host Status				
+15	Target Status				
+16	Reserved				
+17	Reserved				
+18	SCSI Command Bytes (m Bytes)				
18+m	Allocated for Sense Data (n Bytes)				

2.2.1.3 Command Descriptor Block

The Command Descriptor Block (CDB), a part of the Command Control Block, is a standard format command packet that is transmitted to the addressed SCSI device. It contains all the command information required by the SCSI device to perform the desired operation. The Command Descriptor Block contains the command Operation Code followed by a Logical Unit Number (LUN), command parameters if required, and a control byte. A typical Group 0 six byte CDB is shown below:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	LUN			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Vendor Unique		Reserved				Flag	Link

Please refer to the SCSI specification ANSI X3.131, the Common Command Set (CCS) revision 4B, and the SCSI 2 draft for additional information on Command Descriptor Blocks.

2.2.1.4 Principles of Operation

At power-up, the host must inform the host adapter of the location and number of mailboxes. To start a task, the host builds a CCB and stores its memory address into a free mailbox. A non-zero Mailbox Out command byte is then written to indicate that the mailbox entry is full and valid. The host then writes to an I/O port (defined in section 4) to indicate that the host adapter should scan the MBO area. When a full MBO is found, the host adapter copies the mailbox's CCB pointer into its internal RAM and clears the Mailbox entry by writing a zero to the MBO command byte. This frees the MBO so that it can be used to start another task.

After completing a task, the host adapter scans the MBI area for a free mailbox. When one is found, it is updated with the task's completion status and CCB pointer. The CCB pointer identifies the completed task. A MBI Stored interrupt is generated to notify the host that a task has been completed. The host scans the MBI area searching for a non-zero Status byte. When one is located, the host obtains the CCB pointer and frees the MBI by writing a zero into the Status byte. The host then examines the contents of the CCB to determine that the command was successfully completed. The freed MBI can now be used to indicate the completion of another task. The host adapter fills the MBI area and scans the MBO area in a round robin fashion. If the host saves the position of the last active MBI entry, it can determine the MBI of a new entry immediately without searching, since a new entry will be in the next MBI location.

The host adapter transmits a new MBO Available or MBI Full interrupt to the host whenever all non-Mailbox interrupts have been cleared and serviced by the host. The host should analyze the interrupts and clear them as soon as possible so that the host adapter can post any new interrupts quickly. The host adapter will not wait until an interrupt can be transmitted to the host before processing an MBO entry or creating a new MBI entry. Thus, in processing a single MBI

interrupt, the host may find several MBI entries waiting by the time the interrupt processing is finished. Similarly, a later MBI interrupt for the last of the later MBI entries may find nothing to service because the MBI entry was examined and processed as a result of the first MBI Full interrupt. If the interrupts are reset quickly by the host, the probability of an interrupt occurring when no MBI entry is available is much lower, providing an important performance improvement. If the MBI entries are emptied by the host in a round-robin order, the scan for the next full entry is very simple, since it is always the next MBI entry in the Mailbox area.

2.2.1.5 Task Queueing

Multiple tasks may be started against a target/LUN or against multiple targets/Logical Units. Since only one task can be active against any one given LUN at a time, all other tasks for the same LUN are queued. Other LUN's may have active tasks at the same time.

The host adapter dequeues on a first in, first out (FIFO) basis for each target/LUN combination. However, due to the optimization algorithm used by the host adapter, a task may sometimes be started earlier in spite of it's late entrance in the queue on multiple target/LUN systems. Task queueing should not be used where changes in the order of command execution may cause data integrity failures.

2.2.2 Single-Threaded Operation

A host adapter BIOS is provided to emulate the standard hard disk BIOS and boot functions. With this BIOS, the host adapter can be used in lieu of a standard hard disk controller on any ISA compatible system.

The BIOS is compatible with the standard hard disk BIOS. This allows DOS to access up to two hard disk devices on the SCSI bus without a driver. All normal I/O functions are supported including system booting. Single threaded operation and multithreaded operation do not operate simultaneously. Single threaded operation cannot be requested until all multithreaded operations are completed. Similarly, all multithreaded operations must be complete before a single threaded operation can be requested. For most multitasking operating systems, such as Xenix and OS/2, single threaded operation is normally used only for the early part of the boot operation, after which multithreaded drivers take over all control of the SCSI operations.

Section Three Installation

3.1 UNPACKING AND INSPECTION

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your freight company representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for possible later reuse should return of the equipment to the factory necessary.

CAUTION: THE AHA-154XA IS CAREFULLY DESIGNED TO RESIST THE EFFECTS OF STATIC ELECTRICITY. HOWEVER, LIKE ALL ELECTRONIC EQUIPMENT , IT CAN BE DAMAGED OR ITS LIFE CAN BE SHORTENED BY UNUSUAL STATIC DISCHARGES. PLEASE TAKE THE PROPER PRECAUTIONS WHEN HANDLING THE BOARD. KEEP THE BOARD IN ITS CONDUCTIVE WRAPPING UNTIL IT IS READY TO BE INSTALLED IN YOUR SYSTEM. BE SURE THAT THE HOST COMPUTER AND THE PERSONNEL HANDLING THE BOARD ARE PROPERLY GROUNDED WHILE INSTALLING THE BOARD.

3.2 INSTALLATION

The following section details the installation procedure for the Adaptec AHA-1540A/1542A AT to SCSI host adapter. The installation of the board consists of setting the various on-board jumpers, preparing the SCSI devices, installing the correct terminations, inserting the board into a full-length AT compatible connector, and connecting a SCSI cable from the on-board connector to a SCSI target.

NOTE: The system must be turned off during the installation procedure.

3.2.1 System Configuration

The DOS operating system and the standard AT BIOS support two hard disk drives, drive C: and drive D:. If two standard hard disk drives are installed, they are the only hard disk drives accessible from the operating system. If one standard hard disk drive is installed, the AHA-154XA BIOS allows DOS to access the SCSI drive with the Target:LUN address of 0:0 as the second of the two supported drives (drive D:). If no standard hard disk drives are installed, the AHA-154XA BIOS allows DOS to access the SCSI drive with the address of 0:0 as the first of two supported drives (drive C:) and the SCSI drive with the address of 0:1 or 1:0 as the second of the drives (drive D:). System booting is performed from the floppy drive if a floppy diskette is installed. If no floppy is installed, system booting is attempted from the drive chosen as drive C: through the above process, whether the drive is a standard hard disk or a SCSI hard disk. The AHA-154XA BIOS fully supports the extended partitioning capabilities of DOS 3.3 for up to two drives. The AHA-154XA BIOS only supports the AHA-154XA if its I/O Port Address is set to 330h.

Adaptec provides a special DOS driver for the AHA-154XA that allows the support of up to 24 physical or logical devices under DOS. Many other operating systems, including SCO Xenix and Unix, do not have this limitation and will allow the access of any number of attached SCSI devices.

The term "standard hard disk" refers to the disks attached to the system by a standard ISA disk controller. These standard hard disks can be set to the "Installed" or "Not Installed" state by the SETUP program that is supplied with each ISA host computer. The SETUP program allows the user to select the number of standard hard disks that are recognized by the system regardless of whether or not they are physically installed.

3.2.2 Hardware Setup

Several preparatory steps must be taken to install the host adapter in the host computer. The initialization jumpers must be correctly placed in the AHA154XA. The SCSI Bus terminators must be installed in the correct SCSI devices. Finally, the correct SCSI addresses must be assigned to each peripheral device.

The Adaptec AHA-1540A/1542A 16-Bit AT bus to SCSI bus Host Adapter has been designed to operate as shipped in the majority of AT class computers. The host adapter's jumper settings should almost always remain in their original default positions. Refer to section 3.3 if conflicting memory or port assignments require that the host adapter jumpers be reconfigured. The AHA-1540A/1542A is shipped with the following default settings:

SCSI Address	7
SCSI Parity	Enabled
Terminators	Installed
Terminator Power	Supplying
Synchronous Negotiation	Disabled
DMA Channel	5
Interrupt Channel	11
AT Port Address	330H
AT BIOS Address	ODCOOOH
LA Enable Jumper	Installed

Termination

The SCSI bus must be terminated correctly to assure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed. All other SCSI devices must have terminators removed. The host adapter is shipped with terminators already installed at locations RN3, RN4, and RN5. The internal and external connectors connect to the same SCSI bus, so both internal and external cabling must be considered in determining where terminators are installed.

If only one cable (either internal or external) is connected to the host adapter, the terminators must remain installed in the host adapter. Terminators must also be installed on the device at the farthest end of the cable from the host adapter. Terminators must be removed from all other attached SCSI devices.

If both an internal and an external cable are connected to the host adapter, remove the terminators on the host adapter and install terminators on the devices at the farthest end of each cable. Terminators must be removed from all devices except the device at the end of each cable. The instruction manuals for each SCSI device will indicate how the terminators can be removed or replaced.

Addressing

The SCSI target address for each SCSI device to be attached must be selected by setting the proper jumpers or switches on the device. If the SCSI device is a hard disk that is to be used as the boot disk, it must have the Target Identifier (SCSI Address) set to zero and the Logical Unit Number set to zero. SCSI Addresses 0 and 1 should be reserved for SCSI hard disk drives. SCSI Address 2 is often used for tape devices. Each installed peripheral must have a different Target Identifier. The host adapter's default address is 7. Duplicate SCSI Addresses will cause errors that are extremely difficult to identify. Any jumpers that control operating modes must also be properly set. If there is a jumper that enables synchronous transfer negotiation, the jumper should be set to enable negotiation. Check the SCSI drive or controller to ensure that Parity Checking is enabled. If Parity checking on the device is disabled or not supported, the jumper at location J8 of the host adapter should be removed. Parity checking should only be enabled if all SCSI devices support it.

Installation Procedure

Now that the host adapter and the devices to be installed have been properly prepared, the devices should be installed in the following manner:

1) **Turn OFF the power to the computer system.**

2) Remove the system cover according to the directions of the computer manufacturer.

3) If only an external SCSI subsystem is to be used, no internal cabling is required. If an internal SCSI peripheral is to be used, install a 50 pin SCSI ribbon cable to the host adapter. This cable must be oriented correctly. Pin 1 of the SCSI cable is designated by a red stripe. Multi-color 50 pin ribbon cables signify pin 1 with a brown color. Pin 1 on the host adapter 50 pin SCSI header is located on the left hand side, farthest from the installation bracket and is designated by the words PIN 1 on the board adjacent to the header. After locating pin 1 on the host adapter and on the SCSI cable, carefully insert the connector located at the end of the long end of the cable into the host adapter connector. After ensuring that all pins are lined up and that the pin 1 orientation is correct, firmly seat the connector to the board. If it is ever necessary to remove the cable, gentle prying with a small thin-bladed screwdriver may be required.

4) After installing the SCSI cable, the host adapter can be installed in any one of the adapter slots in the host computer.

5) If an internal SCSI device is to be used, it should be installed in the drive bays in accordance with the directions on the peripheral. The proper power supply must be connected to the SCSI peripheral device.

6) The 50 pin SCSI ribbon cable can now be attached to each SCSI device. Refer to the device's installation instructions to ensure proper pin 1 orientation. Pin 1 orientation must be consistent throughout the system. Keep the ribbon cable neatly dressed away from the ventilation slots in the computer system. Keep the ribbon cable dressed away from possible electrical noise sources or noise sensitive components, particularly large microprocessors, memory boards, switching power supplies, and analog data acquisition boards. If the internal

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configuration requires the cable to come near noise sensitive circuits , make sure that the cable crosses the boards at right angles and is near the noise sensitive circuits for the shortest distance possible.

7) Carefully reinstall the cover of the computer.

8) If an external SCSI subsystem is to be installed, it can now be cabled to the External SCSI Connector projecting from the shielding bracket on the back of the AHA-154XA Host Adapter. The proper shielded SCSI cable must be used for proper operation. The external connector on the AHA-1540A/1542A is a D shell connector that ensures correct pin 1 orientation on the host adapter. The subsystem, cables, and SCSI terminators must be installed in accordance with the directions provided with the external SCSI subsystem. The addresses selected for external SCSI devices must not overlap with the addresses of the host adapter or any other SCSI devices attached internally.

3.2.3 Checklist

Before applying power to your system, the following items should be completed and checked:

1. 50 pin SCSI ribbon cable is connected to the host adapter with proper pin 1 orientation.
2. The host adapter is firmly seated in the host computer's adapter slot.
3. The correct SCSI addresses are selected on all attached SCSI devices. Address 0 is reserved for the boot hard disk and address 1 is used for a second hard disk.
4. The correct operating modes are selected on all attached SCSI devices.
5. Terminators are installed or removed on the drives and host adapter as required.
6. External SCSI devices are properly installed and cabled.

3.2.4 Operation Using the BIOS Under DOS

To bring up the system for the first time with the host adapter installed, insert a bootable system diskette in drive A:, and close the door. After the system initialization and power-up diagnostics have completed, system error messages, such as "SYSTEM CONFIGURATION CHANGED, RUN SETUP" and prompts on how to continue, may be displayed. After following the instructions displayed on the screen, the system will boot from the flexible diskette drive.

Run your SETUP program to configure the system as required. **Remember that a SCSI drive can only be used as a boot device if both standard hard disks are mapped out.** When the SETUP parameters have been defined, follow the directions on the screen to re-initialize the system.

Most SCSI drives are shipped from the factory with a complete low-level format. A few SCSI drives and most bridge controllers, including the CCS compatible Adaptec ACB-4525Z, require a low-level SCSI format operation before they will operate. Section 7.4 describes how the low-level format utility that is available in the Adaptec BIOS Utilities should be used to format such SCSI devices.

Run the DOS FDISK program to partition the disk for the number of cylinders to be used by DOS. When using DOS 3.2 or under, it is generally a good idea to select 1 less cylinder than the maximum allowable per partition according to DOS. This eliminates the possibility of exceeding the 32 MB limit. Activate the first DOS partition before leaving the FDISK program if it is to be the boot partition. If you are not sure if a DOS partition exists, use the menu entry in FDISK to display partition data.

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After the DOS partition has been created and activated, the drive is ready for a DOS FORMAT. Refer to the DOS manual for the format options that are available. If the system is going to boot from a SCSI disk, it is usually easiest to transfer the hidden system files to that disk during the FORMAT.

CAUTION: IF THE DRIVE YOU ARE USING WAS PREVIOUSLY FORMATTED OR PARTITIONED WITH A DIFFERENT HOST ADAPTER OR DISK CONTROLLER, A DOS PARTITION MAY ALREADY EXIST. IF SUCH A PARTITION DOES EXIST IT SHOULD BE DELETED AND RE-CREATED USING THIS HOST ADAPTER. IF THIS PRECAUTION IS NOT FOLLOWED, ERRATIC SYSTEM OPERATION MAY RESULT.

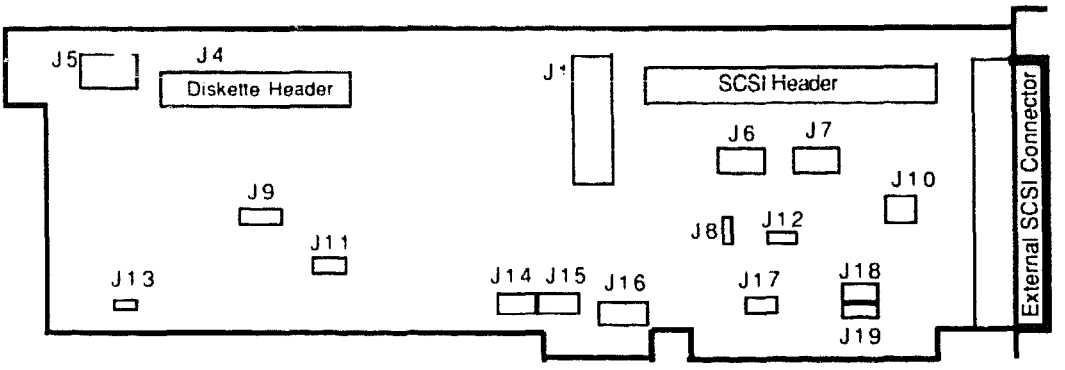
The host adapter and SCSI disks are now ready for normal operation. The host adapter's BIOS performs the necessary initialization procedures during the boot operation. This procedure is described in section 6.1.1

3.3 Jumper Configuration

All of the jumpers have been preset at the factory to ensure proper system operation with the majority of AT bus systems. This information is provided to help the OEM or system integrator to configure the system properly if other option boards present conflicts.

The following diagram shows the approximate location of the various customer configurable items on the AHA-1540A/1542A. Listed after the diagram are the functions, defaults, and set-up options for each jumper.

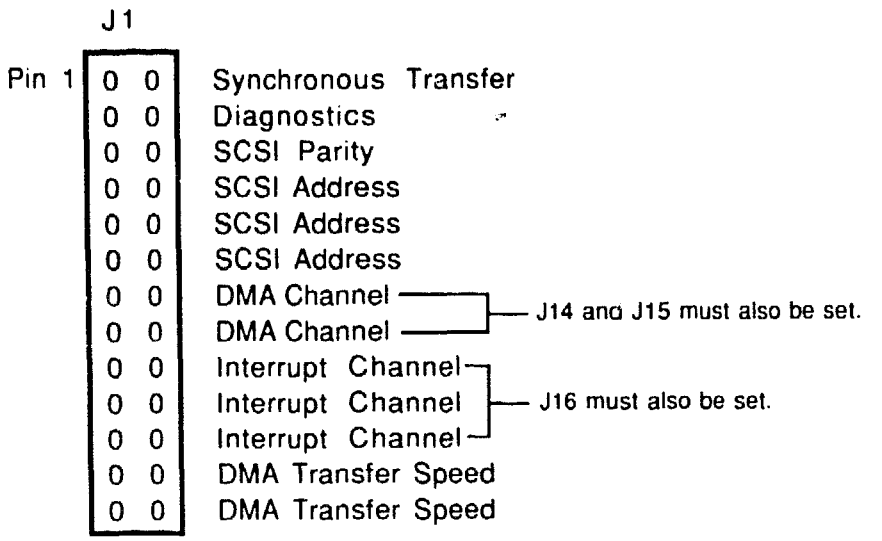
Jumper locations:



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3.3.1 Jumper Block J1

Jumper block J1 is shown below:



Jumper block J1 is the large vertically oriented block of jumpers located near the center of the host adapter. Pin pair 1 is the topmost pair of pins.

3.3.1.1 SCSI Synchronous Negotiation

Pin-pair 1 of jumper block J1 is the synchronous negotiation enable jumper. The AHA-1540A/1542A will initiate SCSI synchronous negotiation during initialization, or after a SCSI reset if this jumper is installed. If the jumper is not installed, the AHA-1540A/1542A will still support synchronous SCSI transfers, but a different SCSI device must initiate the negotiation. **Default is jumper removed, synchronous negotiation initiation disabled.** If any attached SCSI devices support synchronous transfer, the initiation of negotiation should be enabled by both the AHA-154XA and the attached devices to fully implement the SCSI synchronous negotiation protocol.

3.3.1.2 Diagnostic Jumper

Pin-pair 2 of jumper block J1 is a factory diagnostic jumper. This jumper is reserved for Adaptec use and must not have a jumper shunt installed. If this jumper is installed, the firmware will loop through the power on diagnostics, preventing normal operation. **Default is jumper removed.**

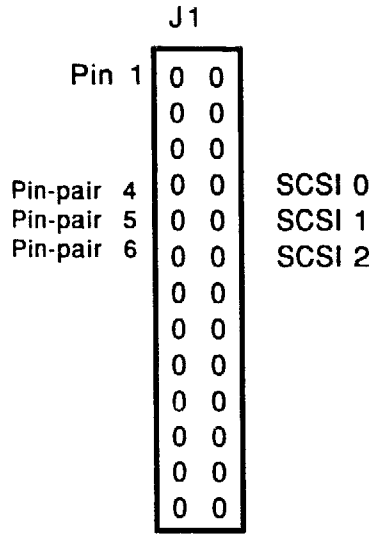
3.3.1.3 SCSI Parity

Pin-pair 3 of jumper block J1 is the parity enable/disable jumper. The SCSI parity checking is disabled if this jumper is installed. **The default is parity checking enabled.**

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3.3.2 SCSI Address

Pin-pairs 4, 5, and 6 of jumper block J1 define the SCSI address. The SCSI address is selected according to the following table. **The default address is 7.**



Pin-pair 4 5 6	SCSI Address	
O O O	7	Default
X O O	6	
O X O	5	
X X O	4	
O O X	3	
X O X	2	
O X X	1	
X X X	0	

X = Jumper Installed

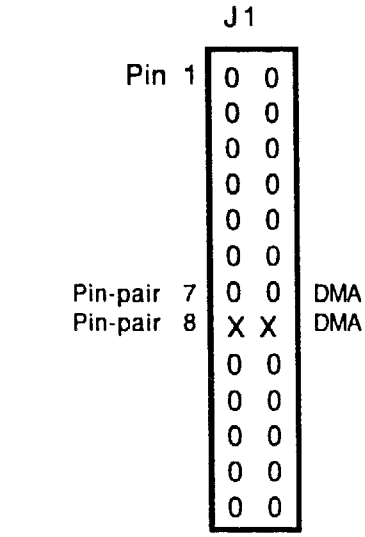
3.3.3 DMA Channel

There are three jumper blocks involved in selecting the DMA channel. These are J1, J14, and J15. The DMA channel selection jumpers consist of pin pairs 7 and 8 located in the large block of jumper pins J1. The DMA channel reported to the AT during the Return Configuration command is set by these jumpers according to the following table. **Default is DMA channel 5.**

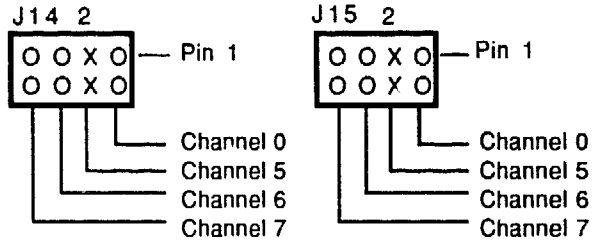
Jumper set J14 selects the DMA REQ signal to be used by the AHA-1540A/1542A according to the following table. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most pair of pins.
The default is DMA Request 5.

Jumper set J15 selects the DMA ACK signal to be used by the AHA-1540A/1542A according to the following table. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most set of pins. **The default is DMA Acknowledge 5.**

There are four DMA channels that may be chosen for use by the AHA-1540A/AHA-1542A, channels 0, 5, 6, and 7. The DMA channel is set up by using the three jumper blocks and pin-pairs previously described. The jumper settings for each channel are shown below:



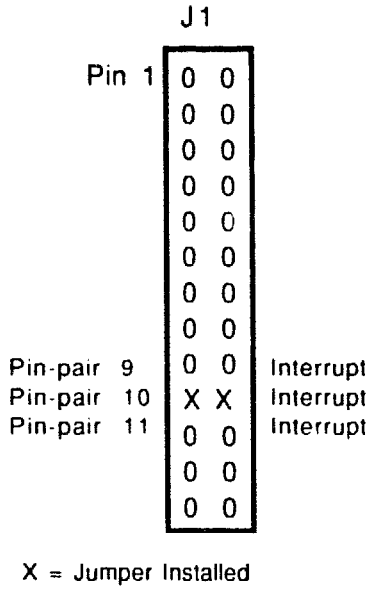
J1 DMA CHANNEL JUMPERS	
Pin-pair 7 8	DMA Channel
O O	7
X O	6
O X	5 Default
X X	0



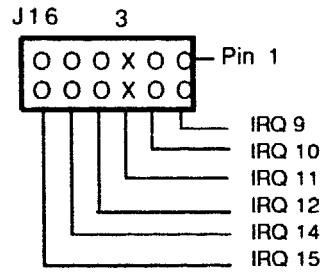
3.3.4 AT Interrupt Channel

There are two jumper blocks involved in selecting the AT interrupt channel. These are J1 and J16. The AT interrupt channel jumpers consist of pin pairs 9, 10, and 11 in the large block of jumper pin pairs J1. The interrupt channel reported to the AT during the Return Configuration Command is set by these jumpers according to the following table. **The default is interrupt channel 11.**

Jumper set J16 selects the AT interrupt channel to be used by the AHA-1540A/1542A. This jumper set is located near the bottom center of the host adapter. Pin pair 1 is the right most pair of pins. The interrupt channel used is set according to the following table. **The default interrupt channel is 11.**

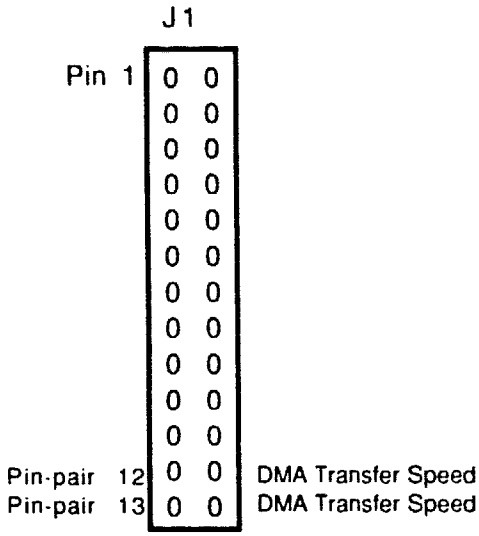


J1 INTERRUPT CHANNELS	
Pin-pair 9 10 11	Interrupt Channel
O O O	9
X O O	10
O X O	11
X X O	12
O O X	14
X O X	15



3.3.5 DMA Transfer Speed Default

Pin-pairs 12 and 13 of jumper block J1 set the default DMA transfer speed. Installing jumper shunts as shown below will set any of 4 default DMA transfer speeds. (See Appendix A for system timing requirements.) The default speed is selected after power on or after a hard reset occurs. This speed may also be tuned to allow for the fastest possible transfer (minimum bus on time) for any particular system by using the Host Adapter command Set Transfer Speed. The Host Adapter Command overrides the jumper settings. This command is detailed in section 5. **The default is no jumper installed.**

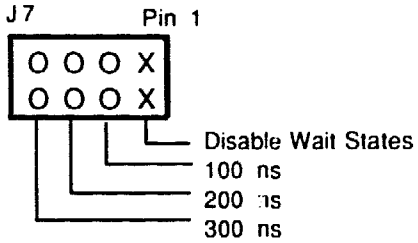


Pin-pair 12 13	DMA Speed	
O O	5.0 MB/s	Default
X O	5.7 MB/s	
O X	6.7 MB/s	
X X	8.0 MB/s	

X = Jumper Installed

3.3.6 AT BIOS Wait State

Jumper block J7 allows IOCHRDY on the AT bus to be driven not active during BIOS reads. The time may be set to 100ns, 200ns, 300ns, or the function may be disabled. **The default is Wait State Disabled.**

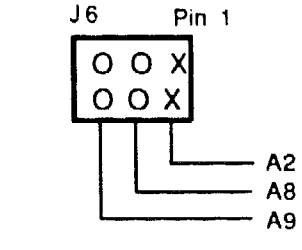


X = Jumper installed

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3.3.7 AT Port Address

The starting address of tne block of four I/O ports required by the AHA-1540A/1542A is selected by the jumpers in jumper block J6. Pin pair 1 is the right most pair of pins. The default address is 0330H. That port address is required by the BIOS. Other valid port addresses are 334H, 330H, 234H, 230H, 134H, and 130. These port addresses may be used by device drivers and operating systems that support multiple host adapters. **The default address is 330H.**

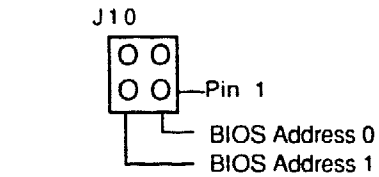


Default is 330H
X Jumper Installed

AT Port Address				
A9	A8	A2	Address	
O	O	O	334H	
O	O	X	330H	Default
O	X	O	234H	
O	X	X	230H	
X	O	O	134H	
X	O	X	130H	

3.3.8 AT BIOS Address

The starting address of the block of address space reserved for the Adaptec BIOS is selected by the jumper pins located in J10. **The default address is ODCOOOH.** This address must not conflict with any other BIOS or decoded address space in the system.

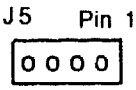


DEFAULT ADDRESS = 0DC000H
X = Jumper Installed

BIOS Address	
Jumpers 0 1	BIOS Address
O O	0DC000H
X O	0CC000H
O X	0D8000H
X X	OC8000H

3.3.9 Front Panel LED Connector

J5 is the front panel LED header. Pins 1 and 4 are connected to the same 220 ohm pull up resistor and pins 2 and 3 are pulled low by the same LED driver whenever the on board LED is on. This allows the Front Panel LED cable to be plugged in with either orientation. The driver is specified to pull 24 milliamps through the LED. J5 is located near the top left of the host adapter.



3.3.10 LA Enable Jumper (AHA-W1542A Only)

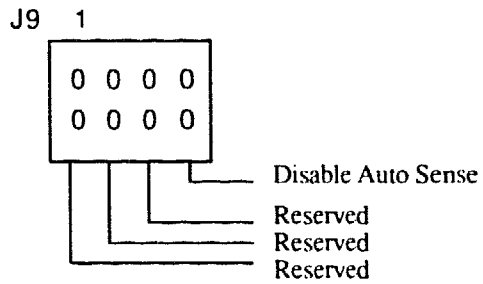
Note: This jumper exists only on the early production units. These are easily identified by a label on the board that has a model number of AHA-W1542A. Standard production AHA-1540A and AHA-1542A boards do not have this jumper.

When J8 is installed, address drivers LA17 - LA19 are enabled. When not installed these address lines are not driven. Some computers, especially 80386 based machines, short address lines LA17 and SA17, LA18 and SA18, and LA19 and SA19 together. If your computer system shorts these lines then remove jumper J8. Default is jumper installed.

CAUTION: INCORRECT INSTALLATION OF THIS JUMPER MAY NOT RESULT IN IMMEDIATE SYSTEM PROBLEMS. IF IT IS NECESSARY TO CHANGE THE STATE OF THIS JUMPER AFTER THE SYSTEM HAS BEEN CONFIGURED, THE SCSI HARD DISK MUST ALSO BE RE-FORMATTED. CONTACT THE COMPUTER SYSTEM MANUFACTURER IF THERE IS ANY DOUBT ON HOW THE SYSTEM IMPLEMENTS THESE ADDRESS LINES.

3.3.11 Auxiliary Jumpers

Installation of a jumper shunt on pin pair 1 of jumper block J9 will disable the automatic request sense function on the AHA-1540A/1542A. If the automatic Request Sense function is enabled, it may additionally be disabled on a command by command basis using the Request Sense Allocation Length Field of the CCB (see Section 5.3). All other pins-pairs on jumper block J9 are reserved for future use.



3.3.12 BIOS Enable/Disable

Only one host adapter BIOS should be enabled in any host system. That BIOS allows DOS to access up to two SCSi drives on the host adapter having a port address of 330H. Any other host adapters installed in the system must have their BIOS disabled. In addition, certain operating systems may require that the BIOS be disabled. The enabling of the BIOS is controlled by jumper J11, near the bottom left of the host adapter. When the jumper is installed on J11 the BIOS is enabled. When the jumper is removed, the BIOS is disabled and will not respond to host reads. **The default is jumper installed.**

3.3.13 SCSI Terminators

RN3, RN4, and RN5 are the SCSI terminators. If the AHA-1540A/1542A is not the first or the last SCSI device in a string of SCSI devices, or if in-line terminators are used, then all of these resistor networks must be removed. More information is provided in section 3.2.2 about the proper use of the SCSI terminators. **The default is terminators installed.**

3.3.14 SCSI Terminator Power

Fuse F1 controls the terminator power. If another SCSI device is supplying terminator power, then F1 may optionally be removed. No more than 5 SCSI devices should be configured to supply terminator power to a single SCSI bus. **The default is F1 installed** with the AHA-1540A/1542A supplying terminator power. The terminator power is protected with a 1.5 amp fuse to prevent short circuits from burning SCSI cables. The terminator power is additionally protected from terminator power back-flow with a low voltage-drop diode so that the SCSI bus will continue to operate even if one or more SCSI host adapters is powered down.

3.4 FLEXIBLE DISKETTE CONTROLLER CONFIGURATION JUMPERS (AHA-1542A ONLY)

3.4.1 Flexible Diskette Controller Secondary Address

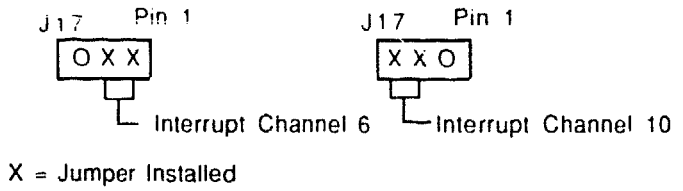
Jumper J12, located near the center right of the host adapter, controls the selection of the flexible diskette controller secondary address. When J12 is installed, the flexible diskette controller will respond to I/O addresses 370-377. When not installed, the flexible diskette controller will respond to I/O addresses 3F0-3F7. **The default is no jumper installed.**

3.4.2 Flexible Diskette Controller Enable

Jumper J13, located near the bottom left of the host adapter, enables or disables the flexible diskette controller. When this jumper is installed, the flexible diskette controller will respond to host reads and writes. When not installed, the flexible diskette controller will not respond to any signal. **The default is jumper installed.**

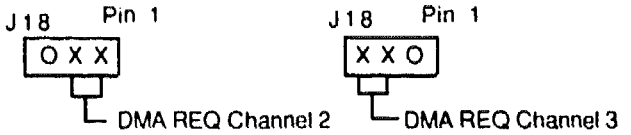
3.4.3 Flexible Diskette Controller Interrupt Channel

Jumper block J17, located near the bottom right of the host adapter, sets the interrupt channel for the flexible diskette controller. **The default is interrupt channel 6.**



3.4.4 Flexible Diskette Controller DMA Request Channel

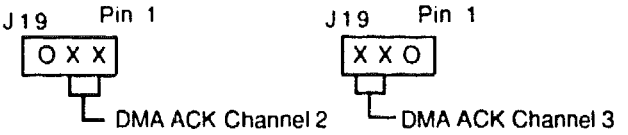
Jumper J18, located near the bottom right of the host adapter, selects the DMA Request channel for the flexible diskette controller. Jumper J19, the DMA Acknowledge jumper, must be set to the same position. **Default is DMA channel 2.**



X = Jumper Installed

3.4.5 Flexible Diskette Controller DMA Acknowledge Channel

Jumper J19, located near the bottom right of the host adapter, selects the DMA acknowledge channel for the flexible diskette controller. Jumper J18, the DMA Request jumper, must be set to the same position. **Default is DMA channel 2.**



X = Jumper Installed

4.0 HARDWARE FUNCTIONAL DESCRIPTION

4.1 HARDWARE OVERVIEW

This section provides a description of the AHA-1540A/1542A hardware functional interface to the PC/AT host software.

The hardware consists of a custom SCSI protocol chip, the AIC-6250, a FIFO buffer, a set of I/O ports, and a controlling microprocessor.

The DMA control logic on the host adapter controls the AT bus arbitration and data transfer hand shaking. During DMA data transfers, the AHA-1540A/1542A becomes a bus master. The DMA logic supports both odd and even starting addresses. For odd starting addresses, the first transfer will be an 8-bit transfer. Thereafter, 16 bit transfers will be used to complete the data transfer. Odd-byte transfers, and the the last transfer of an even number of bytes to an odd address are treated in a similar manner.

The SCSI port is controlled by the AIC-6250, an Adaptec SCSI protocol device which supports arbitration, selection, and reselection with a minimum of processor intervention. This VSLI device also supports target mode and synchronous SCSI transfers.

4.2 I/O PORT INTERFACE

The I/O port interface consists of three address locations. These three port addresses are decoded in the AT I/O address space. They form the primary communications channel between the host and the host adapter. The I/O ports are 8 bits wide. The base port is for control and status, the second port for command and data transfer, and the third port for interrupt flags.

I/O PORT INTERFACE BIT DEFINITION

PORT ADDRESS = BASE + 0

WRITE: Control Register		**READ: Status Register**	
Bit 7	Hard Reset (HRST)	Bit 7	Self Test in Progress (STST)
Bit 6	Soft Reset (SRST)	Bit 6	Internal Diagnostic Failure (DIAGF)
Bit 5	Interrupt Reset (IRST)	Bit 5	Mailbox Initialization Required (INIT)
Bit 4	SCSI Bus Reset (SCRST)	Bit 4	SCSI Host Adapter Idle (IDLE)
Bit 3	Reserved (0)	Bit 3	Command/Data Out Port Full (CDF)
Bit 2	Reserved (0)	Bit 2	Data In Port Full (DF)
Bit 1	Reserved (0)	Bit 1	Reserved (Undefined)
Bit 0	Reserved (0)	Bit 0	Invalid H A Command (INVDCMD)

PORT ADDRESS = BASE + 1

WRITE: Command / Data Out **READ: Data In**

Bit 7	Command/Data Out	Bit 7	Bit 7	Data In	Bit 7
Bit 6	"	Bit 6	Bit 6	"	Bit 6
Bit 5	"	Bit 5	Bit 5	"	Bit 5
Bit 4	"	Bit 4	Bit 4	"	Bit 4
Bit 3	"	Bit 3	Bit 3	"	Bit 3
Bit 2	"	Bit 2	Bit 2	"	Bit 2
Bit 1	"	Bit 1	Bit 1	"	Bit 1
Bit 0	"	Bit 0	Bit 0	"	Bit 0

PORT ADDRESS = BASE + 2

WRITE: Reserved, do not write **READ: Interrupt Flags**

Bit 7	Bit 7	Any Interrupt
Bit 6	Bit 6	Reserved
Bit 5	Bit 5	Reserved
Bit 4	Bit 4	Reserved
Bit 3	Bit 3	SCSI Reset Detected (SCRD)
Bit 2	Bit 2	HA Command Complete (HACC)
Bit 1	Bit 1	MBO Empty (MBOA)
Bit 0	Bit 0	MBI Full (MBIF)

4.2.1 Control and Status Port

Writing a one to the bits of the Control Port initiates certain special host adapter operations. There is no requirement to return the bits to the zero state, since they are reset automatically after the requested operation is initiated. Read operations to the Status port address return host adapter status information.

Base+0 Port, Write: Host Adapter Control Port.

Bit 7 Hard Reset (HRST): The setting of the Hard Reset bit to one forces the host adapter into a state identical to a normal power on state. Diagnostic functions are executed and all status for ongoing SCSI operations is lost. A Reset Condition is generated on the SCSI bus. While the reset is being processed, the Self Testing in Progress bit (Host Adapter Status Port bit 7) is set. When the reset is complete, that bit is reset and the Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set, indicating that the AHA-154XA mailbox structure must be re-initialized and that no other operations are active on the host adapter. See section 4.3, describing the overall reset structure.

Bit 6 Soft Reset (SRST): The Soft Reset bit clears all ongoing SCSI and host adapter commands. All Command Control Blocks are abandoned and all queued commands are abandoned. Mailbox In and Mailbox Out entries must be cleared by the host. No diagnostic functions are executed. No Reset Condition is generated on the SCSI bus. The Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set when the reset processing is completed. This indicates that the AHA-154XA Mailbox structure must be re-initialized and that no other operations are active on the Host Adapter. See section 4.3, describing the overall reset structure.

Bit 5 Interrupt Reset (IRST): The setting of this bit clears the interrupt port of all bits that have been set and resets the interrupt line. The host adapter manages the interrupt presentation to minimize the possibility of incorrectly resetting an interrupt. MBOE and MBIF interrupts are presented immediately unless an SCRD or HACC interrupt has not yet been cleared. An SCRD or HACC will only be presented after any interrupt bit has been cleared and DF is zero, indicating an operation is fully completed. The prompt resetting of MBOE and MBIF interrupts minimizes the chance of a reset of one also resetting the other. Host programs should, however, be aware that there is a small chance of falsely resetting a new MBIF reset while clearing an MBOE interrupt. This can be resolved by periodically scanning the MBI entries when activity is expected on the host adapter or by not enabling the MBOE interrupt.

Bit 4 SCSI Bus Reset (SCRST): The setting of this bit causes a SCSI Bus Reset to be generated on the SCSI bus. The SCSI Bus Reset is triggered at the time the SCRST bit is set to one and raises the RST line on the SCSI Bus for the architected 25 microsecond period. The reset is managed as a SCSI Soft Reset and will allow partially completed operations to continue after the reset occurs. See section 4.3, describing the overall reset structure.

Bits 0-3 Reserved: Reserved bits must be set to zero to avoid compatibility problems with future extensions of the Control Register.

Base+0 Port, Read: Host Adapter Status Port

Bit 7 Self Testing in progress (STST): This bit, when one, indicates that the host adapter is performing self-initialization and internal diagnostics. The bit is asserted after a power-on or hard reset (Control Port Bit 7 HRST = 1). When diagnostic operation is complete, the STST bit is set to zero and bit 5 or bit 6 is set to indicate the successful or unsuccessful completion of the diagnostics. If bit 7 remains on, it indicates that the initialization or diagnostic could not be completed. The error condition can be determined as described in section 10. In most cases, bit 6 (DIAGF) will be set to indicate that an internal diagnostic failure occurred.

Bit 6 Internal Diagnostic Failure (DIAGF): This bit, when one, indicates that the self-testing process has completed and that an error was detected. The host adapter must be reset by setting the Hard Reset bit (bit 7 of the Control Port) to clear the error. If the AHA-154XA again detects an error, troubleshooting procedures must be performed to identify and correct the error condition. The diagnostic LED will usually present a flash code that indicates the nature of the failure. Section 10 describes the corrective procedures.

Bit 5 Mailbox Initialization Required (INIT): This bit, when one, indicates that the self-testing process has completed successfully and that the AHA-154XA is ready for mailbox initialization to be performed. The base memory address of the Mailbox area must be established by execution of the Mailbox Initialization command. After execution of the Mailbox Initialization command and any other desired initialization operations, the AHA-154XA is ready for full operation.

Bit 4 SCSI Host Adapter Idle (IDLE): This bit, when one, indicates that the host adapter is in the idle state. The host adapter has no outstanding Adapter Commands or SCSI commands. The host processor must wait for the idle state before executing any Adapter Command except the Start SCSI (02) and Enable Mailbox Out Interrupt (05) commands.

Bit 3 Command / Data Out Port Full (CDF): The host uses the CDF bit to synchronize command and data transfers to the host adapter. An Adapter Command byte or an outbound parameter byte can be placed in the Command / Data Out Port when the port is empty, indicated by the CDF bit being zero. When a byte is placed in the Command / Data Out Port, the CDF bit is set to one and remains one until the host adapter has obtained and processed the byte. When the CDF bit returns to zero, the next Command or parameter byte can be placed in the port.

Bit 2 Data In Port Full (DF): The host uses the DF bit to synchronize transfers of data from the host adapter to the host. When the DF bit is set to one, the host adapter has placed a byte in the Data In Port for the host to remove and process. When the host performs a read to the Data In Port address, the DF bit is set back to zero automatically and not set to one again until a new data byte has been placed in the Data In Port by the host adapter for the host.

Bit 1 Reserved: This bit is zero.

Bit 0 Invalid Host Adapter Command (INVDCMD): The Invalid Host Adapter Command bit is set to one if an invalid command or parameter byte was received in the Command / Data Out Port . After sending a command byte or data byte, the host software determines that the next byte is ready to send by waiting for the CDF bit to be reset. If the command byte or parameter byte is not valid, the command sequence will instead be terminated by the host adapter. The host adapter always terminates a command by raising the Host Adapter Command Complete (HACC) interrupt. If the HACC interrupt is set to one and the INVDCMD bit is not set, the command terminated normally. If the INVDCMD bit is also set to one, the command or parameter bytes were determined to be invalid and the command terminated abnormally. The INVDCMD bit is only valid from the time the HACC interrupt is set until the HACC interrupt is reset. The bit's value is not predictable until a new HACC interrupt is set for a new Adapter Command.

4.2.2 Command/Data Out and Data In Port

The second I/O port address is used by the host to write Adapter Command bytes and accompanying parameter data bytes to the host adapter. It is also used by the host adapter to send parameters back to the host to be read. The Command / Data Out Port is used by the host to send host adapter initialization and management commands and parameters that cannot be sent by the standard Mailbox protocol. Information requested by the Adapter Commands placed in the Command / Data Out Port is returned through the Data In Port. The host should understand the format and number of bytes to be transmitted for each command so that extra invalid bytes are not passed across the interface. Bytes in addition to those required by the particular command are

likely to be interpreted as invalid, although they may instead cause the execution of valid commands that were not supposed to be performed.

The host should only write to the Command / Data Out Port when CDF is zero. This allows time for the host adapter to process a previously written command or parameter byte. CDF is automatically set to one when the host writes to the port and is reset to zero after the host adapter removes the byte from the port.

If an Adapter Command needs additional data bytes, the host waits until CDF is zero before writing the additional bytes to the Command / Data Out Port. Just as in the command transfer case, each parameter byte written will set the CDF. The host can write additional data bytes only after CDF is again zero. The HACC interrupt will indicate when the command has terminated, normally or abnormally. If INVDCMD is also set, the host adapter found either the command or data bytes to be invalid and terminated abnormally. The use of CDF as a hand-shaking bit is required to prevent the transfer of invalid data.

If an Adapter Command requires data transfer from the host adapter, the host adapter will place the data bytes in the Data In Port and set the DF bit (Status Port bit 2) to indicate that the requested parameter is ready for the host to read. When the host reads the Data port, DF is automatically reset. The host should wait until DF is again set before attempting to transfer the next parameter byte. The use of the DF bit to control the hand-shaking process is required to prevent the transfer of invalid data. After the last data byte has been transferred, the HACC interrupt bit will be set indicating command completion. If the Adapter Command was invalid, the HACC interrupt will occur before all data bytes have been transmitted and the INVDCMD bit will be set.

4.2.3 Interrupt Flag Port

The Interrupt Flag Port contains bits that indicate the reason that an interrupt was provided to the host from the host adapter. The host adapter uses the interrupt to notify the host that the host adapter is ready for immediate service from the host. The Interrupt Flag Port is a read-only port. When an interrupt bit is set by the host adapter to indicate that the host should respond, the Any Interrupt bit and the interrupt line are both also set. When the host begins to examine the returned registers and mailboxes to determine the cause of the interrupt and to perform the operations needed to service the interrupt, the host will first read the Interrupt Flag Port to record which interrupts must be serviced. The host will then clear the interrupts by setting the IRST bit (Host Adapter Control Port bit 5). The host adapter presents MBOA and MBIF interrupts immediately unless there is already an SCRD or HACC interrupt present. If the SCRD or HACC is present, the MBOA and/or MBIF interrupt will be posted after the SCRD or HACC interrupt is cleared. An SCRD or HACC interrupt will only be presented if the Any Interrupt signal is zero and the DF signal is zero, indicating the completion of all pending interrupt presentation. It is recommended that the MBOA interrupt be enabled only when required by the host. This prevents the possible presentation and resetting of MBIF interrupts before they are processed. Other reset operations will also reset the Interrupt Flag Port and the interrupt line, including the Hard Reset bit (HRST), the Soft Reset bit (SRST), and the power on reset issued by the motherboard.

Base+2 Port, Read only: Interrupt Flag Port

Bit 7 Any Interrupt: This bit, when one, indicates that the interrupt to the host has been established. The actual identify of the interrupting condition is provided in bits 0 to 3.

Bit 6 Reserved: Returned as zero.

Bit 5 Reserved: Returned as zero.

Bit 4 Reserved: Returned as zero.

Bit 3 SCSI Reset Detected (SCRD): This bit, when one, indicates that a SCSI Reset has been received on the SCSI bus. The Any Interrupt bit and the AT interrupt signal will also be set. The host adapter supports SCSI Soft Reset (see section 4.3). Any ongoing target or initiator activities will continue normally after first clearing the SCSI bus. In some rare cases, host intervention will be required to restart a SCSI command that was aborted by the reset operation. The host can convert the SCSI Soft Reset to a SCSI Hard Reset by setting the Control Register Soft Reset (Bit 6) to one, clearing all ongoing operations in the host adapter. In this case, the host must recognize that any operations not yet completed will never be completed and must perform appropriate error recovery operations. See section 4.3, describing the overall reset protocol. The SCRD bit is not set for host initiated SCSI Reset conditions caused by the setting of the HRST bit or the SCRST bit, since the host is already aware of the actions it has requested. If the Any Interrupt signal or DF signal is present, the SCRD interrupt will not be presented until the interrupts already present are cleared.

Bit 2 Host Adapter Command Complete (HACC): This bit, when one, indicates that an Adapter command has been completed, normally or abnormally. The Any Interrupt bit and the AT interrupt signal will also be set. If the command was completed normally, only the HACC bit will be on. If the command was completed abnormally or was aborted before it was completed, the HACC bit will be one and the Invalid Command Bit (Status Register bit 5) will also be one. During parameter transfers to or from the host adapter, the HACC bit should be examined to verify that the command is still being processed and has not been ended abnormally. If the Any Interrupt signal or DF signal is set, the HACC interrupt will not be presented until the interrupts already presented are cleared.

Bit 1 Mailbox Out Available (MBOA): This bit, when one, indicates that an outbound Mailbox entry is now available for use by the host. The Any Interrupt bit and the AT interrupt signal will also be set. Most operating systems will choose to leave this interrupt disabled to avoid the generation of extra interrupts. The host adapter will normally empty Mailbox Out entries to its local RAM so rapidly that round robin filling of the Mailbox Out entries will assure that a Mailbox Out entry will already be empty by the time that the host is ready to fill it again.

If the host finds that all Mailbox Out entries are full, it can enable the Mailbox Out Available interrupt by executing an Enable Mailbox Out Interrupt command through the I/O Command Port. The Enable Mailbox Out Interrupt command is one of the two commands that can be executed without waiting for the IDLE state of the host adapter. As soon as any Mailbox Out entry is cleared by the host adapter, an MBOA interrupt will be generated to indicate to the host that an MBO entry is available. An MBOA interrupt is generated after that each time a Mailbox Out entry is cleared by the host adapter until an Enable Mailbox Out Interrupt command is executed to force the reporting of MBOA interrupts to be disabled. If the SCRD or HACC interrupts are present, the MBOA interrupt is not presented until they are cleared. At all other times, MBOA is presented immediately.

Bit 0 Mailbox In Full (MBIF): This bit, when one, indicates that an entry has been placed by the host adapter in the Mailbox In. The interrupt should be reset as soon as possible so that any subsequent interrupts can be detected. The host adapter may return information in other Mailbox In entries, so the host should check the next

entry to determine if more than one set of information has been provided. The MBI entries are filled in round-robin order, so the host should simply check the next MBI entry after the last one that was found when a new MBIF interrupt occurs.

If an MBIF interrupt is set and other Mailbox In entries are made before the interrupt is cleared, then all the entries can be scanned as found. The new MBIF interrupt will be presented if the SCRD and HACC interrupts are cleared. A new MBIF interrupt will be presented regardless of the state of the MBOA interrupt bit. It is important to clear and record each interrupt as soon as possible to avoid the possible accidental resetting of a valid interrupt. In addition, it is desirable to enable the MBOA interrupt as rarely as possible. The host system software must be ready to scan for MBI entries even if no MBIF interrupt occurred.

4.3 RESET OVERVIEW

The reset functions provided by the AHA-154XA are extensive to allow the fullest flexibility and architectural consistency, both with SCSI and with the Industry Standard Architecture.

4.3.1 Hard Reset Operations

Resets may be generated by the hardware through two mechanisms. The RESET signal from the ISA socket is generated by the system board to reset or initialize all installed adapters upon power on or during a low line voltage condition. The system can also activate this signal under host program control. In addition to the RESET signal, the setting of the HRST bit (bit 7 of the Host Adapter Control Port) will force a hardware reset to the AHA-154XA. Regardless of the source, a Hard Reset forces the following actions on the AHA-154XA.

- All internal registers of the AHA-154XA are returned to their reset condition.
- The host adapter's microprocessor returns all internal information and parameters to their initial state.
- The host adapter performs all required internal diagnostics.
- A standard SCSI Reset condition is generated to all other attached SCSI devices.

During the Hard Reset process, the AHA-154XA will indicate to the attached host that self-testing is in process by raising the STST bit in the Host Adapter Status Port. After the Hard Reset process is complete, the AHA-154XA will indicate that initialization parameters are required from the host by raising the INIT bit in the Host Adapter Status Port.

4.3.2 SCSI Reset Operations

The SCSI Reset condition is defined in the SCSI Standard, X3.131-1986, section 5.2.2. A SCSI Reset condition may be forced by any SCSI device on the bus. The condition is forced by the assertion of the SCSI Reset signal.

The AHA-154XA has four mechanisms which may force a SCSI Reset condition. The SCSI Reset condition may be invoked from the host software if the software sets the SCRST bit (Bit 4 of the Host Adapter Control Port). In this case, the normal SCSI Reset operations will be performed by the Host Adapter and the SCSI Reset signal will be asserted on the SCSI bus. In this case, the SCRD bit (Interrupt Flag Port bit 3) will not be set, since the host itself caused the reset.

The SCSI Reset is invoked if a hard reset is generated, either by the system board RESET signal or by the setting of the HRST bit. This reset is described in Section 4.3.1.

The SCSI Reset condition may be invoked by the AHA-154XA as part of the recovery mechanism for a bus phase error. Bus phase errors may include detection of an invalid information transfer phase or detection of an impossible phase sequence (Command Phase after a Data Phase in the same command). In this case, the normal SCSI Reset operations will be performed and the SCSI Reset signal will be asserted on the SCSI bus. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate interrupt signal to be presented.

The SCSI Reset condition may be invoked by another SCSI device attached to the AHA-154XA as part of the other device's recovery mechanism or initialization procedure. In this case, the normal SCSI Reset operations will be performed. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate ISA interrupt signal to be presented.

4.3.2.1 SCSI "Soft" Reset Option

The SCSI standard indicates two optional methods of handling the normal SCSI Reset operations. The AHA-154XA implements the "Soft" Reset Option, described in section 5.2.2.2 of the SCSI specification. The "Soft" Reset Option is designed to allow a SCSI Reset signal to correctly clear the SCSI bus, but to allow ongoing system operations to continue without any major interruptions. When the SCSI Reset occurs, any activity on the SCSI bus is immediately halted and all bus lines are cleared from the bus. After the Reset condition ends, any operations in progress are again allowed to start up in the normal manner. No status or pointer information is destroyed. All disconnected commands are allowed to reselect and continue in the normal manner. This "Soft" Reset function allows a multiple initiator system to use reset to clear certain types of bus failures without damaging ongoing tasks from any initiator.

The SCSI "Soft" Reset option is useful in multitasking systems that cannot tolerate the overhead of a complex reconfiguration and reinitialization after a normal reset operation. For the SCSI "Soft" Reset option to operate correctly, all SCSI devices that communicate on the SCSI bus must support the "Soft" Reset option. If any SCSI devices support the "Hard" Reset option, it is likely that operations will be terminated without warning and the system will have to time out and monitor the requirement to restart some activities.

4.3.2.2 SCSI "Hard" Reset Option

The "Hard" Reset Option is designed to restore all attached SCSI devices, including both hosts and peripheral devices, to their power on reset state. All system activities that have not been recorded on a non-volatile memory device or through another SCSI path are completely lost and must be restarted. The system must be completely re-initialized. For certain types of systems that frequently do back-up or check point their transactions, that re-initialize quickly and easily, or that infrequently do resets, the "Hard" Reset Option is appropriate. The AHA-154XA responds to a SCSI Reset Condition by executing only the "Soft" Reset Option, but it notifies the host whenever a SCSI Reset condition has been established by causing an interrupt to the host. The host then has the option of converting the "Soft" Reset to a "Hard" Reset by forcing the host adapter to clear all the ongoing operations and return to its initial state. The host requests this by raising the SRST bit (bit 6 of the Host Adapter Control Port). The host must raise the SRST bit within 300 microseconds to disable the restarting of operations according to the rules of "Soft" Reset. The raising of the SRST bit causes the host adapter to abandon all CCB's and prepare itself to begin accepting new instructions from the host. No secondary SCSI Reset signals are activated. The Mailbox initialization and all normal SCSI initial conditions are reset by the SRST bit, so that reinitialization is required to restart the system. Of course the system still has the right at any time that the IDLE bit (bit 4 of the Host Adapter Status Port) is on to execute any of the Adapter Commands and modify the Mailbox Address or the SCSI initial conditions.

If the host requires that the SCSI be reset according to the SCSI "Hard" Reset option, the host raises the HRST bit. The host adapter will then set a SCSI Reset Condition on the SCSI Bus ar ' clear all its CCB and status information, thus performing a SCSI "Hard" Reset with a single load to the Host Adapter Control Port. Reinitialization will be required.

5.1 HOST ADAPTER COMMAND OVERVIEW

The AHA-1540A/1542A supports two types of commands: SCSI and Adapter Commands. SCSI commands are issued using the mail box protocol and a Command Control Block. When SCSI commands are used, the AHA-1540A/1542A is operating in true multithreading mode. In this mode of operation, the AHA-1540A/1542A is capable of executing multiple commands for multiple targets concurrently. The AHA-1540A/1542A maximizes the I/O transaction throughput by managing SCSI disconnection and reconnection.

Adapter Commands are issued by writing to the Command / Data Out port. Most Adapter commands can not be issued when there are outstanding SCSI commands. Adapter commands are used to initialize the host adapter and to establish control conditions within the host adapter. Adapter commands are also used to transmit the special parameters for communication between the BIOS and the host adapter for the execution interrupt 13 operations.

5.1.1 Adapter Command Operation Codes

Below is a list of the Adapter Command operation codes.

00 -- No Operation
01 -- Mailbox Initialization
02 -- Start SCSI Command *
03 -- Start PC/AT BIOS Command
04 -- Adapter Inquiry
05 -- Enable Mailbox Out Available Interrupt*
06 -- Set Selection Time-out
07 -- Set Bus-On Time
08 -- Set Bus-Off Time
09 -- Set Transfer Speed
0A -- Return Installed Devices
0B -- Return Configuration Data
0C -- Enable Target Mode†
0D -- Return Setup Data†
1A -- Write Adapter Channel 2 Buffer†
1B -- Read Adapter Channel 2 Buffer†
1C -- Write Adapter FIFO Buffer
1D -- Read Adapter FIFO Buffer
1F -- ECHO Command Data

**Note: This command can be issued when the host adapter is executing a SCSI command.*
† These commands are not supported by the AHA-1540.

All Adapter Commands except Start SCSI (02) and Enable Mailbox-Out Available Interrupt (05) must be executed only when the IDLE bit (Status bit 4) is one. Many commands require additional parameter bytes which are then written to the Command / Data Out I/O port (base + 1). Before each byte is written by the host to the host adapter, the host must verify that the CDF bit (Status bit 3) is zero, indicating that the command port is ready for another byte of information. The host adapter usually clears the Command / Data Out Port within 100 microseconds. Some commands require information bytes to be returned from the host adapter to the host. In this case, the host monitors the DF bit (Status bit 2) to determine when the host adapter has placed a byte in the Data In I/O port for the host to read. The DF bit is reset automatically when the host reads the byte. The format of each Adapter Command is strictly defined, so the host adapter and host system can always agree upon the correct number of parameter bytes to be transferred during a command.

All Adapter Commands except Return Installed devices, Start SCSI, and Start PC/AT BIOS typically require less than 200µs to complete. Return installed devices will typically complete in less than 3 seconds. Start SCSI and Start PC/AT commands completion times will vary with the SCSI device and the command issued.

5.1.1.1 No Operation (Operation Code 00)

No host adapter action is taken, but HACC is set indicating command completion. No additional information bytes are exchanged.

5.1.1.2 Mailbox Initialization (Operation Code 01)

This command is used to specify the number of mailbox locations used by the host adapter and to specify the base memory location of the mailbox area. The host adapter requires that four bytes of outbound data follow the command byte. The definition of those four bytes is shown below.

00	Mailbox count	(>0)
01	Mailbox address	(MSB)
02	Mailbox address	
03	Mailbox address	(LSB)

Byte 0	Mailbox Count:	The Mailbox count must be greater than zero.
Byte 1,2,3	Mailbox Address:	The Mailbox address specifies the location of the first byte of the Mailbox area. Byte 1 is the most significant byte.

When the Mailbox Initialization command and parameters are received, the host adapter will then assume that the specified number of Mailbox Out entries and the same number of Mailbox In entries will be assigned beginning at the Mailbox address. The total number of bytes reserved for the Mailbox area will be eight times the Mailbox count. If the Mailbox Count is zero, the INVDCMD bit will be set with HACC to indicate that the parameter is invalid.

At command completion, HACC will be set to one and INIT will be reset to zero. HACC will be reset as specified by section 4.2.3.

5.1.1.3 Start SCSI Command (Operation Code 02)

This command indicates that the host has made at least one Mailbox Out entry and that the host adapter should begin to scan for active MBO entries. Once scanning has been started, it continues until all MBO entries have been serviced, either by beginning the requested operations or by queueing the activities for later execution. Since it is not easy for the host to determine that scanning is still taking place, the host should normally issue this command every time a Mailbox Out is filled. This command does not require additional data bytes. To avoid unnecessary interrupts, HACC is NOT set after command completion. HACC will be set with INVDCMD if the mailbox was not yet initialized.

5.1.1.4 Start PC/AT BIOS Command (Operation Code 03)

This command is used by the Adaptec BIOS to communicate with the host adapter firmware. The command is not available for use by programs other than the Adaptec BIOS.

5.1.1.5 Adapter Inquiry (Operation Code 04)

After receiving this command, the host adapter returns four bytes of data describing the host adapter firmware revision level. After completing the transfer of the four bytes of inbound data, the HACC interrupt is set indicating normal command completion. The bytes contain the following information:

00	Board Identification
01	Special Options Identification
02	Hardware Revision Level
03	Firmware Revision (ASCII)

Byte 0 Board ID: The value in this byte allows software supported on both the PC/AT and on the Microchannel™ to distinguish the type of supporting host adapter.

Value	Meaning
00H	Board is an AHA-1540 with 16 Head BIOS
30H ('0' ASCII)	Board is an AHA-1540 with 64 Head BIOS
41H ('A' ASCII)	Board is an AHA-1540A/1542A, 64 Head BIOS
42H ('B' ASCII)	Board is an AHA-1640, 64 Head BIOS
All Others	Reserved

Byte 1 Special Options ID: The value in this byte indicates what special options are supported on the AHA-154XA host adapter. Other host adapters use other values in this byte.

Value	Meaning
41H ('A' ASCII)	Board is standard model
All Others	Reserved

Byte 2	Firmware Revision:	This value indicates an ASCII value from 0-9,A-Z that indicates the firmware revision installed in the AHA-154XA.
Byte 3	Firmware Revision:	This value indicates an ASCII value from 0-9,A-Z that indicates the firmware revision installed in the AHA-154XA.

After completing this command, HACC will be asserted, indicating normal completion.

5.1.1.6 Enable Mailbox-Out Available Interrupt (Operation Code 05)

The Enable Mailbox Out Available Interrupt command specifies that a Mailbox Out Available Interrupt should be generated whenever a Mailbox Out entry has been cleared by the host adapter. One byte of outbound data is transmitted to indicate whether the interrupt should be enabled or disabled.

Byte 0	Enable/Disable Parameter:	The Enable/Disable parameter byte must be either 00H or 01H. If the Enable/Disable parameter byte is 00H, the Mailbox Out Available interrupt is not returned. If the Enable/Disable parameter byte is 01H, the Mailbox Out Available interrupt is returned as soon as a Mailbox Out has been cleared by the host adapter.

After completing this command, HACC will NOT be asserted to avoid generating additional interrupts. If the data byte is neither 00 nor 01, INVDCMD will be asserted indicating an invalid command. In this case, HACC will also be asserted.

The Mailbox Out Available interrupt is normally intended to be used by the host as an indicator that a Mailbox Out entry is available. This function should only be enabled if all Mailbox Out entries have been found full by the host. It should be disabled soon afterward. If used in other ways, the interrupt may generate a large number of relatively useless interrupt handling activities.

5.1.1.7 Set Selection Time-out (Operation Code 06)

This command sets the SCSI selection time out value. The SCSI Selection time out value is used to determine whether or not a SCSI selection was successful. If the SCSI BSY signal is not returned within the specified time out value, the selection will be terminated and an appropriate error message posted with the returned CCB. This command expects four outbound data bytes to be provided as defined below:

00	Enable/Disable Selection Time Out	
01	Reserved (00)	
02	Time Out Value	(MSB)
03	Time Out Value	(LSB)

Byte 0	Enable/Disable Selection Time Out:	This parameter byte specifies whether or not the Selection Time-out will be used. If the byte is set to 00H, no time-out will be performed. If the byte is set to 01H, the time specified in bytes 02 and 03 will be used as the Selection Time Out by the SCSI. The default value established by the reset process is 01H, indicating the time out is enabled.
Byte 1	Reserved:	This byte must be zero.
Byte 2,3	Time Out Value:	This two-byte value specifies the time in milliseconds that will be used for the Selection Time Out. The default value is 250 milliseconds.

After completing this command, HACC will be asserted, indicating normal completion. INVDCMD will be asserted if the data byte 0 is neither 00 nor 01 or if byte 1 is not zero, indicating an invalid command.

5.1.1.8 Set Bus-On Time (Operation Code 07)

This command specifies the time that the host adapter spends on the bus when transferring data. The Bus-On duration is adjustable from 2 to 15 microseconds. The default setting is 11us. One data byte is passed out to the host adapter to indicate the Bus-On duration in microseconds.

Data Byte 0 -- Bus On-Time (2 to 15 us)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 15. The valid range is 2 to 15 decimal.

5.1.1.9 Set Bus-Off Time (Operation Code 08)

This command sets the time that the host adapter will spend off the bus during a data transfer. The Bus-On duration is adjustable from 1 to 64 microseconds. The default setting is 4us. After receiving this command, the host adapter expects one byte of data which specifies the bus off time in microseconds.

Data Byte 0 -- Bus-Off Time (1 to 64 us)

After completing this command, HACC will be asserted indicating normal completion. INVDCMD will be asserted, indicating an invalid command, if the data byte is greater than 64. The valid range is 1 to 64 decimal. The actual time implemented by the host adapter is rounded down to the next four microsecond step at or below the specified value. The minimum value is approximately one microsecond.

5.1.1.10 Set Transfer Speed (Operation Code 09)

This command adjusts the Bus Master DMA circuitry to a specified maximum AT bus transfer speed to and from the host memory. Several speeds may be selected by setting the jumper configuration as explained in section 3.3. The selected jumper speeds are overridden if the Set Transfer Speed command is executed. The single data byte transmitted after the command byte either sets the read and write speed together, or establishes separate values for each. Appendix A gives the timings that result from the selected values. The default setting is the value set by the jumpers. The I/O Channel Ready signal automatically slows the system further if required by the host memory.

Data Byte 0 -- AT Bus Transfer Speed
00 -- 5.0 MB/second
01 -- 6.7 MB/second
02 -- 8.0 MB/second
03 -- 10 MB/second
04-- 5.7 MB/second
80-FF -- See Table

Custom Transfer Speed		
bit 7	1	
bit 6-4		Read pulse width (ns)
	000	100
	001	150
	010	200
	011	250
	100	300
	101	350
	110	400
	111	450
bit 3	0	Strobe off time = 100ns
	1	Strobe off time = 150ns
bit 2-0		Write pulse width (ns)
	000	100
	001	150
	010	200
	011	250
	100	300
	101	350
	110	400
	111	450

After completing this command HACC is set indicating normal completion.

5.1.1.11 Return Installed Devices (Operation Code 0A)

This command returns information about which SCSI Targets and Logical Units (LU's) are installed on the SCSI bus. The host adapter issues the SCSI Test Unit Ready command to each target/LUN combination and reports the results using eight bytes of data returned through the Data In Register. A bit having a value of one indicates that the associated LU is installed. Each byte is associated with the corresponding target. Each bit within a target byte is associated with a particular Logical Unit, bit 7 indicating the presence of LU 7 and so forth. The state of the target is analyzed using the SCSI TEST UNIT READY command, analyzing the returned data to determine if the addressed LU is available.

After receiving this command, the host adapter returns eight bytes of information which specify the installed configuration as shown below:

Byte 0	Target 0 Configuration:	
	Bit 7	LU 7 Installed
	Bit 6	LU 6 Installed
	Bit 5	LU 5 Installed
	Bit 4	LU 4 Installed
	Bit 3	LU 3 Installed
	Bit 2	LU 2 Installed
	Bit 1	LU 1 Installed
	Bit 0	LU 0 Installed
Byte 1	Target 1 Configuration	
Byte 2	Target 2 Configuration	
Byte 3	Target 3 Configuration	
Byte 4	Target 4 Configuration	
Byte 5	Target 5 Configuration	
Byte 6	Target 6 Configuration	
Byte 7	Target 7 Configuration	

The byte associated with the SCSI Device Identifier of the host adapter will always be zero. After completing the information transfer, the HACC bit will be set to indicate normal completion.

5.1.1.12 Return Configuration Data (Operation Code 0B)

The DMA arbitration priority, the Interrupt channel, and the SCSI ID of the adapter are returned by this command. The three bytes of information are returned in the following format:

Byte 0 DMA Arbitration Priority:

Bit 7	Channel 7
Bit 6	Channel 6
Bit 5	Channel 5
Bits 4-1	Reserved (0)
Bit 0	Channel 0

Byte 1 Interrupt Channel:

Bit 7	Reserved (0)
Bit 6	Interrupt channel 15
Bit 5	Interrupt channel 14
Bit 4	Reserved (0)
Bit 3	Interrupt channel 12
Bit 2	Interrupt channel 11
Bit 1	Interrupt channel 10
Bit 0	Interrupt channel 9

Byte 2 SCSI Identifier

Bits 7-3	Reserved (0)
Bits 2-0	Binary value of SCSI Identifier

After completing this command, HACC will be set indicating normal completion.

5.1.1.13 Enable Target Mode Command (Operation Code 0C)

A special host adapter command (0C) enables and disables target mode. The host adapter requires that two bytes of outbound information follow the command byte. The information bytes contain the following information:

Byte 0 Enable/Disable Target Mode: This parameter specifies which operating modes the host adapter will use. If the byte is set to 00H, the AHA-1540A/1542A will operate only in Initiator Mode. If the byte is set to 01H, the host adapter will operate both as an initiator and as a Processor type Target SCSI Device. Any other value is invalid. The default value after a Hard Reset, Soft Reset, or Power On Reset is 00H (Initiator only).

Byte 1 Logical Unit Mask: This parameter byte contains an eight bit bit-significant mask indicating the Logical Units which will respond in Target Mode. Bit 7 corresponds to LU 7, and so forth. If the bit is one, the corresponding LU will be treated as installed. If the bit is zero, the LU will be treated as not installed.

If the AHA-1540A/1542A does not have the Target Mode feature installed, the host adapter will indicate an invalid host adapter command. If an attempt is made to change from target mode while there are still target mode CCB's being processed by the host adapter, the host adapter will post an invalid host adapter command indication.

If the command disables Target Mode, the Logical Unit Mask byte will be ignored. If the command enables Target Mode, the Logical Unit Mask byte must contain at least one bit, indicating the presence of at least one Logical Unit.

The SCSI INQUIRY command will provide an indication to other initiators that the Logical Unit is installed or not installed in byte 1 of the returned inquiry data.

If target mode is not enabled, the host adapter will behave on the SCSI interface as if it were an ordinary SCSI initiator. Any attempt to select the host adapter will result in a SCSI selection time out. Most Reset Operation, including Soft Reset, Hard Reset, and Power-On Reset will return the AHA-1540A/1542A Target Mode to the disabled state. SCSI Resets, generated either by the host or by other SCSI Devices, will not change the previously established enabled or disabled state of Target Mode.

5.1.1.14 Return Setup Data (Operation Code 0D)

This command returns information describing the setup of the host adapter. The information returned reflects either the values supplied by previous host adapter commands or default values. The command is followed by an outbound data transfer and an inbound data transfer. The outbound transfer is a one byte parameter indicating the length of the required inbound data transfer. The inbound data transfer contains from zero to 255 bytes of information describing the setup of the host adapter. The inbound information normally transferred will be truncated or padded with zeros as necessary to transfer the requested number of bytes. The number of bytes normally transferred by the AHA-154XA is 16.

Outbound Data Byte:

Byte 0	Data In Length:	The number of data bytes requested can be from 0 to 255. A value of zero will be accepted and 256 bytes will be returned.

Inbound Data Summary:

00	SDT and Parity Status
01	Transfer Speed
02	Bus On Time
03	Bus Off Time
04	Number of Mailboxes
05	Mailbox Address (MSB)
06	Mailbox Address
07	Mailbox Address (LSB)
08-0F	Synchronous Transfer Agreements
10-FF	Reserved (00)

Inbound Data Bit Assignments:

Byte 0	SDT and Parity Status:	
	Bit	Meaning
	0	If this bit is zero, Synchronous Data Transfer negotiation will not be initiated by the host adapter, but will be responded to if requested by an attached SCSI Device. If the bit is one, Synchronous Data Transfer negotiation will be initiated by the host adapter under those conditions which require such negotiation. The state is set from jumper J1.
	1	If this bit is zero, parity checking on inbound SCSI transfers has been disabled. If this bit is one, parity checking on inbound SCSI transfers is enabled. The state is set from jumper J1
	2-7	Reserved (0)
Byte 1	Transfer Speed	This byte returns the value passed in to the host adapter by the Set Transfer Speed command (See Section 5.1.1.10)
Byte 2	Bus On Time:	Indicates the Bus On Time in microseconds (See Section 5.1.1.8)
Byte 3	Bus Off Time:	Indicates the Bus Off Time specified by the Bus Off Time Value in microseconds. (See Section 5.1.1.9)

Byte 4	Number of Mailboxes:	The number of Mailboxes established by a previous Mailbox Initialization command will be returned in this byte. This number will be 00H if the Mailbox Initialization command has not yet been successfully completed.
Byte 5-7	Mailbox Address:	The base address of the Mailbox area established by a previous Mailbox Initialization command will be returned in these bytes. The Most Significant byte is byte 5. These bytes have no meaning if Mailbox Initialization has not yet been successfully completed.
Byte 8	Sync Neg, Target 0	Returns information about the synchronous negotiation with Target 0. The byte will be 00H for the address of the host adapter.
	Bit 7	Set to one if synchronous transfer is negotiated. Set to zero if asynchronous transfer is being performed.
	Bits 6-4	These bits contain a value between 0 and 7 that defines the synchronous transfer period according to the following equation. Period = 200 + 50 (value) nanoseconds
	Bits 3-0	These bits contain the negotiated offset value. The value will normally be between 1 and 7.
Byte 9	Sync Neg, Target 1	Same as byte 8, for target 1
Byte 10	Sync Neg, Target 2	Same as byte 8, for target 2
Byte 11	Sync Neg, Target 3	Same as byte 8, for target 3
Byte 12	Sync Neg, Target 4	Same as byte 8, for target 4
Byte 13	Sync Neg, Target 5	Same as byte 8, for target 5
Byte 14	Sync Neg, Target 6	Same as byte 8, for target 6
Byte 15	Sync Neg, Target 7	Same as byte 8, for target 7

If the command completes normally, the HACC interrupt will be set to one. If the Mailbox area has not been properly initialized, all 16 bytes are still requested by the host. If byte 4, the Number of Mailboxes, is zero, bytes 5-7 must be ignored.

5.1.1.15 Write Adapter Channel 2 Buffer (Operation Code 1A)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be transferred to the host adapter's Channel 2 Buffer using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Channel 2 Buffer command for host adapter diagnostics The Channel 2 Buffer is used for transmission of all information except the actual data field between the host adapter and the host system.

Byte 0	Buffer area address, Most significant byte
Byte 1	Buffer area address
Byte 2	Buffer area address, Least significant byte

5.1.1.16 Read Adapter Channel 2 Buffer (Operation Code 1B)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to will be used as a buffer to receive 64 bytes of information transferred from the host adapter's Channel 2 Buffer to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the Channel 2 Buffer to the indicated host memory area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Channel 2 Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.17 Write Adapter FIFO Buffer (Operation Code 1C)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be transferred to the host adapter's FIFO buffer using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the indicated buffer area to the host adapter, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Read Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.18 Read Adapter FIFO Buffer (Operation Code 1D)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to will be used as a buffer to receive 54 bytes of information transferred from the host adapter's FIFO to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the FIFO to the indicated buffer area, the HACC interrupt will be set indicating normal completion. This command is used in conjunction with the Write Adapter FIFO Buffer command for host adapter diagnostics.

Byte 0 Buffer area address, Most significant byte
Byte 1 Buffer area address
Byte 2 Buffer area address, Least significant byte

5.1.1.19 ECHO Command Data (Operation Code 1F)

This command is used to test the Command / Data Out Port, the Data In Port, and the associated control bits in the other I/O Ports. After receiving this command, the host adapter expects one byte of outbound information to be transferred through the Command / Data Out Port. The host adapter then sends (Echos) the same data value back to the host through the Data In Port. After the host has read the data value provided on the Data In Port, the host adapter will generate the HACC interrupt to indicate normal command completion.

Byte 0, Out Outbound Echo Value

Byte 0, In Returned Echo Value

5.2 MAILBOX OVERVIEW

The AHA-1540A/1542A uses a mailbox architecture for task communication between the host and the host adapter when executing SCSI commands. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. At power up, the host issues an initialization command to inform the host of the mailbox location. There are always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). The MBIs are located immediately after the MBOs. Initiator operations and target operations use the same mailboxes. Both initiator and target operations may be in process at the same time. A typical mailbox structure is shown below.

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example, there are four MBOs and four MBIs. The Mailbox Count in the Mailbox Initialization command was set to four. The base address is the address specified by the Mailbox Address field.

Note: The Adaptec BIOS initializes the AT DMA controller to accommodate Bus Master DMA. If the host adapter BIOS is removed or disabled, the host DMA controller must be initialized, via software, for Bus Master DMA operation. See section 5.5.

5.2.1 Mailbox Out Definition

The first byte of each MBO contains the Mailbox status byte. The remaining three bytes contain an address pointer to the first byte of a Command Control Block (CCB). The CCB provides additional task control information. A MBO is free if the first byte is zero. The host can make an entry in any free MBO and indicate that it is filled out or completed by placing the proper MBO command in the first byte of the MBO. After the MBO has been examined by the host adapter and all relevant information obtained by the host adapter, the host adapter sets the MBO command byte back to zero to allow the host to fill it again. For a multitasking operating system, it is desirable that the number of mailboxes be sufficient to allow at least one mailbox for each active independent task or activity.

The MBO format is described in detail below:

Byte 0	MBO Command	This byte specifies the state of the MBO entry.
	Value	Definition
	00H	Mailbox Out is free
	01H	SCSI or Host Adapter command is to be started. CCB pointer indicates location of CCB to be processed.
	02H	SCSI or Host Adapter command is to be aborted. CCB pointer indicates location of CCB to be terminated.
Byte 1	CCB Pointer (MSB)	
Byte 2	CCB Pointer	
Byte 3	CCB Pointer (LSB)	

The use of Mailbox Out (MBO) entries to pass pointers to CCB's is identical for target and initiator modes. The appropriate target mode CCB may be prepared early and posted to the host adapter in preparation for an operation that is expected to happen. If a SCSI operation occurs before the CCB is prepared, the host adapter processes as much of the transaction as possible, then requests a CCB from the host through the MBI. The host is fully responsible for preparing the correct CCB from the information provided through the MBI.

In target mode, one CCB may be presented for each unique combination of LUN, Initiator, and direction. If a second CCB to the same LUN and initiator with the same direction bit is sent to the AHA-1540A/1542A, the CCB will be returned with a host status of 19H, Duplicate CCB Received.

Initiator type CCB's may be queued for an LUN and Target. The host adapter will always search for new MBO entries in a round-robin order, beginning with the entry after the last MBO entry that was processed. By always placing the MBO entries in the MBO area consecutively, the host can assure that the SCSI commands will be started with a minimum scan overhead. Initiator CCB queueing must be used with caution, since under some circumstances it is possible for CCB's to be executed out of order.

If the Mailbox Out Available Interrupt is enabled by execution of Adapter Command 05 (Enable Mailbox Out Available Interrupt), the host adapter will take one of the following actions after each MBO entry is freed by the host adapter:

1) If the Any Interrupt bit in the Interrupt Flag Port is zero, indicating that there are no interrupts pending, the host adapter will set the Mailbox Out Available Interrupt and the Any Interrupt bit and indicate a hardware interrupt to the host.

2) If the Mailbox Out Available Interrupt has been set to one by the previous clearing of a Mailbox Out entry and the interrupt has not yet been cleared by the host, the host adapter will not change the MBOA interrupt bit and will continue to scan for other stored MBO entries.

3) If interrupts other than the Mailbox Out Available Interrupt are pending, the host adapter will wait for the pending interrupts to be cleared before setting the Mailbox Out Available Interrupt. This guarantees that the MBO Available Interrupt will not be cleared accidentally by clearing another interrupt.

5.2.2 Mailbox In Definition

The Mailbox In entries are used to pass completion information concerning a task from the host adapter to the host. In addition, requests for Target Mode CCB's are passed to the host using MBI entries. The first byte of each MBI contains the MBI Status byte, summarizing the type of information being passed from the host adapter to the host. The remaining three bytes contain specialized information that provides more detail about the information. In the case of a CCB Completed MBI, the bytes contain a pointer to the completed CCB. In the case of a CCB Required MBI, the bytes contain the information necessary for the host to prepare an appropriate CCB. Only those MBI's with a MBI Status that is non-zero have information for the host. When the host returns the MBI Status byte to zero, the MBI Free state, the host adapter is allowed to place a new set of information in the MBI entry.

When a SCSI command completes or if a new CCB is required, the host adapter scans the first byte of an MBI entry to find a free mailbox. If one is found, the host adapter will update the MBI's status byte with a non zero value and update the following bytes with the appropriate required pointers or parameters. The valid MBI formats are defined below:

Mailbox In Format for CCB Complete

Byte 0	MBI Status	This byte specifies the state of the MBI entry.
	Value	Definition
	00H	Mailbox In is free
	01H	CCB completed without error. CCB pointer indicates location of successfully completed CCB.
	02H	CCB aborted by host. CCB pointer indicates location of CCB that was aborted.
	03H	Aborted CCB not found. CCB pointer indicates the supposed location of the CCB that was to have been aborted. It is likely that the CCB was already presented to the host before the Abort CCB MBO entry was completed.
	04H	CCB Completed with Error. The CCB fields indicate the details of the error condition. This code allows normal CCB completion to be processed without bothering to examine the completion codes in the CCB.
Byte 1	CCB Pointer (MSB)	
Byte 2	CCB Pointer	
Byte 3	CCB Pointer (LSB)	

Mailbox In Format for CCB Required

Byte 0	MBI Status	This byte specifies the state of the MBI entry.
	Value	Definition
	10H	SCSI Target Command received with no CCB available. The host must prepare an appropriate CCB and place it in the MBO to complete the SCSI command. The remaining three bytes of the MBI specify the information necessary to prepare a SCSI command.
Byte 1	Initiator and LUN	
	Bit 7-5	Binary address of initiator that selected the host adapter in Target Mode.
	Bit 4	The SCSI Target Command received was a RECEIVE command. A CCB must be prepared to transmit data to the Initiator.
	Bit 3	The SCSI Target Command received was a SEND command. A CCB must be prepared to transmit data from the Initiator.
	Bits 2-0	Binary address of the logical unit of the Target Mode host adapter that was addressed by the Initiator.
Byte 2-3	Data Length	The high order two bytes of the data length specified in the SEND or the RECEIVE command. A CCB must be prepared to transmit this amount of data plus up to 256 more bytes. It is assumed that the data fields are self-defining or of a known length in such protocols.

The CCB Required Mailbox In entries are only generated when a command has been received by the host adapter in target mode. For the CCB Required Mailbox In entries, byte 0 takes on a distinctive value of 10H, indicating both that the MBI entry is filled and that the MBI entry is being presented to request a CCB appropriate to service a SCSI transaction for which no CCB was available. The host adapter will have disconnected on the SCSI after receiving the initiator and LU addresses and after having received either a SCSI SEND or a RECEIVE command. If the LU address is enabled by the Logical Unit Mask, the MBI will provide the addresses in bits 7-5 and bits 2-0 and will indicate by setting either bit 3 or bit 4 that a SCSI SEND or RECEIVE command was accepted from the initiator. The host system is then expected to prepare a CCB suitable for processing the Send or Receive command. The information in bytes 2 and 3 is a copy of bytes 2 and 3 of the Send or Receive command CDB. This provides the host an approximation of the length of the requested data transfer. This length is used by the host to allocate the correct amount of buffer to accept data in a SEND command or to control the maximum amount of data that can be transferred in a RECEIVE command. If the LU address received is disabled, no MBI will be presented and a check condition will be posted to the Initiator. A subsequent REQUEST SENSE command will recover an Invalid LUN error indication.

After each Mailbox In entry is stored by the host adapter, it will indicate that Mailbox In scanning must be performed in the following manner:

1) If the Any Interrupt bit is not set to one in the Interrupt Flag port, indicating that no interrupts are pending, the host adapter will set the Mailbox In Full interrupt bit, the Any Interrupt bit, and raise the hardware interrupt line to indicate that there is at least one Mailbox In entry to be examined by the host system.

2) If the Mailbox In Full interrupt bit has already been set to indicate that an entry was made in the Mailbox In area and if that interrupt has not yet been cleared by the host, no further notification is provided by the host adapter.

3) If interrupts other than the Mailbox In Full interrupt are pending, the host adapter will wait for all pending interrupts to be cleared before setting the Mailbox In Full interrupt.

Note that careful host Target Mode software design is necessary to prevent ambiguity in the notification process. If a CCB was just prepared but the MBO has not yet been searched by the host adapter at the time the MBI entry is made to the host, the host may choose to examine the MBI entry and not act on it, having already provided the needed CCB. The host should also examine the entire MBI space to be sure that a previously supplied CCB which should have been able to service the notification MBI entry was not already used for a previous operation that had been posted by the host adapter but not yet serviced by the host. Proper care in host system design will prevent these overlapping operations from becoming a problem.

5.3 COMMAND BLOCK DEFINITION

The CCB specifies detailed information about a SCSI command. The format of a CCB is shown below. Each of the fields is separately explained following the table.

COMMAND CONTROL BLOCK FORMAT

Byte 0	Command Control Block Operation Code	
	Value	Definition
	00H	SCSI Initiator Command
	01H	Target Mode Command
	02H	SCSI Initiator Command with Scatter/Gather
	81H	Bus Device Reset
Byte 1	Address and Direction Control	
	Bits 7-5	CCB Op Code = 00, 02: SCSI Target Id CCB Op Code = 01: SCSI Initiator Id
	Bit 4	Outbound data transfer, length is checked.
	Bit 3	Inbound data transfer, length is checked.
	Bit 2-0	Logical Unit Number
Byte 2	SCSI Command Length	
Byte 3	Request Sense Allocation Length/Disable Auto Sense	
Byte 4-7	Data Length (Byte 4 most significant)	
Byte 7-9	Data Pointer (Byte 7 most significant)	
Byte 10-12	Link Pointer (Byte 10 most significant)	
Byte 13	Command Linking Identifier	
Byte 14	Host Adapter Status (HASTAT)	
Byte 15	Target Device Status (TARSTAT)	
Byte 16-17	Reserved (00)	
Byte 18-n	SCSI Command Descriptor Block (Length specified by byte 2)	
Byte n-m	Reserved for REQUEST SENSE information bytes (Length of reserved space in byte 3)	

The standard format of the Command Control Block is shown in the following diagram:

Byte 0	Command Control Block Opcode			
+1	Tar/Init	Data Out	Data In	LUN
+2	SCSI Command Length = m			
+3	Request Sense Allocation			
+4	Data Length (MSB,MID,LSB)			
+7	Data Pointer (MSB,MID,LSB)			
+10	Link Pointer (MSB,MID,LSB)			
+13	Command Link ID			
+14	Host Status			
+15	Target Status			
+16	Reserved			
+17	Reserved			
+18	SCSI Command Bytes (m Bytes)			
18 + m	Allocated for Sense Data (n Bytes)			

The bytes of the CCB are defined further below:

Byte 0: Command Control Block Operation Codes

The AHA-1540A/1542A supports four CCB Operation Codes. The valid command values are shown below:

00	SCSI Initiator Command Control Block
01	SCSI Target Command Control Block
02	SCSI Initiator Command Control Block with Scatter/Gather
81	SCSI Bus Device Reset

If the Operation Code value is 00H, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target / LUN. The other fields of the CCB support the required Initiator functions of the AHA-1540A/1542A.

If the Operation Code value is 01H, the CCB is intended to service a SEND or RECEIVE command sent to the host adapter as a target from another initiator. The values in the other fields are used to service the Target Mode operation. If an Operation Code of 01H is specified to a host adapter that has not had its Target Mode enabled, the host adapter returns a Host Status indication of 18H, Invalid CCB Parameter.

If the Operation Code value is 02H, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed Target / LUN. The definition of the Data Length and the Data Pointer is modified to support the Scatter/Gather function. Refer to section 5.2.4.

If the value is 81(hex) a Bus Device Reset message will be sent to the addressed target. This command forces the host adapter to abort all outstanding tasks against the selected target. All remaining CCB Bytes are ignored. The host adapter will generate a Bus Device Reset message out to the specified target.

Any other command value generates a Host Adapter Detected Error (Host Status byte of 16H).

Byte 1: Address and Control Byte

This byte identifies the address of the devices that will be serviced and provides information about the expected direction of data flow.

If the CCB is an Initiator CCB, this byte identifies the target SCSI device in bits 7,6, and 5. If the CCB is a Target CCB, the byte identifies the initiator which the CCB will serve.

Bits 4 and 3 are optionally set to determine the direction of data transfer. For an Initiator CCB, if neither bit is set, the direction of data transfer will be established by the SCSI command being executed. For a Target CCB, if neither bit is set, the CCB will be returned with an indication of Invalid CCB Parameters (18H) in the Host Status field, since each Target CCB must be identified as to whether it will service a SEND or a RECEIVE command. If both bits are set for either type of CCB, the command must perform no data transfer. If only bit 3 is active, the data transfer will be to the host adapter and from the external SCSI device. If the CCB is a target CCB, the data transfer will be required to be a Data Out phase, while if the CCB is an initiator CCB, the data transfer will be required to be a Data In phase. If only bit 4 is active, the data transfer will be from the host adapter and to the external SCSI device. If the CCB is a target CCB, the data transfer must be a Data In phase, while if the CCB is an initiator CCB, the data transfer will be a Data Out phase.

If bits 3 or 4 are set for an Initiator CCB, the data length will be checked. If the amount of data transferred exceeds the specified amount, the CCB Host Status field will contain an indication of Data Over/Under Run (12H). For a Processor Target mode CCB, the handling of incorrect lengths is described in Section 8.2.4.

If the CCB is an initiator CCB, bits 2,1, and 0 define the target Logical Unit which will be addressed. If the target accepts an IDENTIFY message out, the value in bits 2,1, and 0 will be provided in the LUN field of the message byte. The LUN field in the SCSI Command Descriptor Block (CDB) is expected to be zero. If the target does not accept an IDENTIFY message out, the LUN field in the SCSI CDB must contain the correct Logical Unit address. SCSI devices with conformance level 2, including Common Command Set (CCS) disk drives and all SCSI-2 devices will always accept the IDENTIFY message out. The few SCSI devices not meeting those requirements must be examined on a case by case basis to determine whether the Logical Unit Address should be placed in CCB Byte 1 or in the CDB.

Byte 2: SCSI Command Length

This byte establishes the length, in bytes, of the SCSI Command Descriptor Block.

Byte 3: Request Sense Allocation Length

When a SCSI device terminates an operation with CHECK CONDITION status, it means that the device has error or status information as a result of execution of the operation. The SCSI specification indicates that a REQUEST SENSE command must be executed before any other command is executed in order for the host initiator to be sure of obtaining the error information. Since the AHA-154XA host adapter has the capability of queueing commands for execution, the host adapter itself must take charge of generating the Request Sense command. The automatic generation of Request Sense is inconvenient for some specialized operating systems, so the function can be disabled by installation of a jumper in J9 (See section 3.3.11). If the jumper is not installed, the function can also be disabled by specifying a value of 01H for the Request Sense Allocation Length.

This byte indicates the length, in bytes, of the area reserved for information that may be obtained by a REQUEST SENSE command. A value of 00H indicates that an allocation length of 14 bytes is to be used, sufficient to capture the sense key and error code of all normal extended sense type devices. A value of 01H requests that no automatic REQUEST SENSE be executed. The values from 02H to 07H are reserved. Values from 08H to FFH are valid allocation lengths. The value is used to notify the host adapter that the specified number of bytes have been reserved at the end of the CCB to receive possible Request Sense data bytes. The REQUEST SENSE also uses the indicated allocation length as its byte count in the Command Descriptor Block generated by the host adapter.

If an operation that treats the AHA-1540A/1542A as a Target Mode device fails and presents a Check Condition status byte, the Initiator should return a REQUEST SENSE command. The AHA-1540A/1542A will return appropriate sense information in response to the command. If the command that originally failed was a SEND or a RECEIVE command, the same REQUEST SENSE information bytes that will later be sent to the Initiator are also sent to the host when the CCB is returned. The sense information is placed in the specified Request Sense Allocation area with a length not exceeding the Request Sense Allocation Length.

Bytes 4, 5, 6: Data Length

These bytes determine the length, in bytes, of the data transfer. CCB host adapter error 12(hex) is posted if a data over run occurs.

If the CCB specifies a Scatter/Gather operation, the Data Length field contains the total number of bytes in the Data Segment List.

Bytes 7, 8, 9 : Data Pointer

These bytes specify the real address of the first byte of the data area to be used during the data phase of the SCSI command.

If the CCB specifies a Scatter/Gather operation, the Data Pointer field contains the pointer to the first byte of the Data Segment List.

Bytes 10, 11, 12: Link Pointer

These bytes are used when a SCSI command contains a LINK or LINK WITH TAG bit in the command. When a Linked command is completed, the host adapter will use the contents of this field as a pointer to the next CCB to execute. If the Linked Flag bit is set, an interrupt will be generated before the next command is started. A completed CCB is always reported back in an MBI, but MBIF interrupts are only reported if the linked set of commands is finished or if a Link with Flag message is presented. There must be enough MBI entries to receive the entire set of linked commands.

Target Mode does not support the linking function.

Byte 13 : Command Link ID

This byte is used in conjunction with linked commands. It is set by the host to identify commands in a command chain.

Linking is not supported in Target Mode.

Byte 14 : Host Status

This byte is used to report the host adapter status (HASTAT).

HASTAT has the following definitions:

00 H	No host adapter detected error The CCB was completed normally.
0A H	Linked command complete without error The SCSI command completed and linked normally.
0B H	Linked command complete without error, interrupt generated. The SCSI command completed and linked with a LINKED COMMAND COMPLETE WITH FLAG message.
11 H	Selection time out The initiator selection or target reselection was not complete within the Set SCSI Selection Time-out period.
12 H	Data over run/Under run The target attempted to transfer more data than was allocated by the Data Length field or the sum of the Scatter / Gather Data Length fields.
13 H	Unexpected bus free The target dropped the SCSI BSY at an unexpected time.
14 H	Target bus phase sequence failure An invalid bus phase or bus phase sequence was requested by the target. The host adapter will generate a SCSI Reset Condition, notifying the host with a SCRD interrupt.
15 H	MBO command was not 00, 01, or 02 The first byte of the MBO command was invalid. This usually indicates a software failure.
16 H	Invalid CCB Operation Code The first byte of the CCB was invalid. This usually indicates a software failure.
17 H	Linked CCB does not have the same LUN A subsequent CCB of a set of linked CCB's does not specify the same logical unit number as the first.
18 H	Invalid Target Direction received from Host The direction of a Target Mode CCB was invalid.
19 H	Duplicate CCB Received in Target Mode More than once CCB was received to service data transfer between the same target LUN and initiator SCSI ID in the same direction.
1A H	Invalid CCB or Segment List Parameter A segment list with a zero length segment or invalid segment list boundaries was received. A CCB parameter was invalid.

Byte 15: Target Status

For an initiator CCB, this byte is used to return the SCSI status byte sent to the host adapter from the initiator. If a SCSI command returns with BUSY status, the normal recovery process is to execute the command again. The AHA-154XA takes that burden off the host and periodically restarts the command automatically until the command completes with a status other than Busy.

For a target mode CCB, this byte is used to indicate to the host what status the host adapter returned to the initiator.

Target Status may have the following values in target mode

00 -- Good Status
02 -- Check Status (See REQUEST SENSE byte area)
08 -- LUN Busy

Byte 16: Reserved (must be 0)

Byte 17: Reserved (must be 0)

Byte 18: n: SCSI Command Descriptor Block

This field holds the SCSI Command Descriptor Block (CDB) as described in the SCSI specification. The length of this command is described in byte 02. For initiator mode CCB's, the CDB provided by the host is transmitted to the target. For target mode CCB's, the CDB provided from the initiator is returned to the host in this space.

Byte 18+n - 18+n+m : Allocated for Sense Data

If a Check Status condition is detected by the AHA-154XA as it completes an operation on the SCSI bus, the host adapter automatically executes a REQUEST SENSE command with the data length specified by Request Sense Allocation Length. The actual bytes returned, up to the maximum indicated by the Request Sense Allocation Length, are placed in the area Allocated for Sense Data. If the Request Sense Allocation Length was 01h, no REQUEST SENSE command is executed.

If a check condition is detected by the AHA-154XA while it is operating in Processor Target Mode, the same information that will later be recovered by the initiator that received the Check Status is also placed in the area Allocated for Sense Data so that the host processor is also aware of the failure.

5.3.1 SCATTER/GATHER LIST DEFINITION

Using the normal CCB Operation Codes of 00 and 01 (SCSI Initiator and SCSI Target CCB's), the CCB itself contains a pointer to the first byte of a contiguous area of data of a specified length. The direction of transfer with respect to the data area and the checking of the length of the data transfer to the data area are both managed by the AHA-1540A/1542A according to the requirements of the particular mode and control bit set-up.

Using the Scatter/gather Operation Code of 02, the CCB instead contains a pointer to a list of data segments and an indication of the length of the list of data segments. The data segment list contains pointers to the actual location in host memory of the data segments to be transferred as well as a precise indication of the length of each data segment. Each data segment list entry contains a three-byte pointer to the location of a data segment and three-byte length indicator telling how long that particular data segment shall be. The data segment list is arranged in the order in which data will be gathered or distributed, the first pointer in the list being used first.

A typical data segment list is shown in the following table. The data segment list describes the distribution of 4096 bytes distributed in four separate locations within the memory. The beginning of the data segment list is indicated by the data segment list pointer. The length of the data segment list (24 bytes) will be contained in the data segment list length field of the CCB.

	3 bytes	3 bytes
	(MSB) (LSB)	(MSB) (LSB)
Data Segment List Pointer →	Segment 0 L = 1024	Data Segment 0 Pointer
	Segment 1 L = 2	Data Segment 1 Pointer
	Segment 2 L= 2046	Data Segment 2 Pointer
	Segment 3 L= 1024	Data Segment 3 Pointer

A data segment list can have from one to sixteen segments. A list with 0 segments or a list with more than 16 segments causes an Invalid Segment List error to be posted in the host status field.

The AHA-154XA has certain constraints in the data segment address boundaries and lengths that are allowed. If these boundaries are violated, an Invalid Segment List error will be posted in the host status field of the CCB. The simplest way to assure that these boundaries are not violated is to require all boundaries between segments to be on even word boundaries. The first segment may begin on any boundary and the last segment may end on any boundary. All segments but the first and last should have even byte counts.

The actual boundary limitation is somewhat less restrictive. If the binary values of the starting address of a segment, the byte count of that segment, and the starting address of the next segment are all exclusive OR'd together, and the result of that exclusive or is an even number, the boundary between those two segments is valid. Another way to express the limitation is to require that the ending boundary of one segment must be the same as the beginning boundary of the next segment. If a segment ends on a word boundary, the next segment must begin on a word boundary. Similarly, if a segment ends on an odd-byte boundary, the next segment must begin on an odd-byte boundary.

5.4 DESCRIPTION OF OPERATION

This section describes the interface operations required to invoke the desired SCSI behavior. The AHA-1540A/1542A must be properly initialized before any of these operations can be performed.

After system initialization is done, the I/O Command Port initialization commands must be executed. The Mailbox Initialization command must be executed to assign the Mailbox area. The Enable Target Mode command may optionally be executed if Target Mode is to be allowed.

5.4.1 Execution of Initiator Mode operations

To begin an Initiator Mode SCSI command, the host first allocates a data buffer area. A CCB is then created to perform the desired operation to the correct peripheral device and a pointer to the data buffer area is placed in the CCB. Once the CCB is completely defined, the host places a pointer to the CCB in an empty MBO location, places an MBO full status in the MBO status byte, and transmits a Start SCSI Command to the I/O Command Port. If it is not already scanning the MBO for an active MBO entry, the Start SCSI Command to the I/O Port causes the host adapter to begin scanning for such an entry.

After finding an active MBO entry, the AHA-1540A/1542A copies the MBO Command field contents and CCB pointer into its internal RAM and clears the MBO Command byte, freeing the mailbox. Up to 16 initiator CCBs and 16 target CCBs can be stored in the host adapter's internal RAM concurrently. The AHA-1540A/1542A maximizes the SCSI bus utilization by starting the next available CCB as soon as the bus is free. Disconnection and reconnection on the bus are automatically taken care of by the AHA-1540A/1542A. As the host adapter starts the SCSI operation, it will first determine if the addressed target/LUN is busy. If the target/LUN is busy, then the command will be placed in the task queue to be tried again later.

Commands are removed from the queue in the order that they were received, establishing a (FIFO) first in first out command execution order. Of course, the order of task completion may vary due to the different amounts of time required to process and complete different commands. If the target/LUN is not busy, the new command is started at the next bus free phase. If BUSY status is received by the AHA-1540A/1542A, the CCB is placed at the end of the FIFO queue to be restarted later.

If a CHECK CONDITION status is received from the target, the AHA-1540A/1542A will issue a Request Sense command to get the sense data. The sense data is stored in the CCB after the SCSI command data. The driver software must reserve the allocated number of bytes at the end of the CCB to hold the sense data which is returned as result of a receiving a check status. Automatic Request Sense can be optionally disabled by jumpers or by using the CCB.

If the MBO Command is to abort a SCSI command, the host adapter first searches the active and queued CCBs. If the CCB is found, the task is aborted at the earliest possible moment and an MBI entry is made to indicate that the CCBs execution was successfully terminated. If the CCB is not found among the active or queued CCBs, the AHA-1540A/1542A completes the command and reports that fact in the MBI Status byte. The CCB may not be found because it has previously been aborted, because an intervening reset occurred, or because the CCB was already finished normally and returned.

The AHA-1540A/1542A scans the MBOs in a round robin fashion. This is to ensure that all of the mailboxes will be scanned with equal probability. A host can minimize the AHA-1540A/1542A MBO scan time by using MBO's sequentially.

When executing a START SCSI command, the AHA-1540A/1542A does not verify that the new CCB resides in an unused memory area. Therefore, the host must not reuse a CCB location until it has been returned through a Mailbox In entry and the host has examined all the pertinent information in the CCB. CCB addresses are used by the AHA-1540A/1542A as task identifiers.

5.4.2 Execution of Target Mode Operations

5.4.2.1 Target Mode with a Prepared CCB

Typical target operation is managed in the following way by the host software. After power-on initialization is complete, the host sends an Enable Target Mode command to the host adapter to enable Processor Target mode. After that, the host, from previous configuration knowledge, generates a pair of CCB's for each likely initiator and for each LUN supported by the host. One CCB is for outbound data from the initiator using the SEND command, while the other is for inbound data from the target to the initiator using the RECEIVE command. The SEND command CCB defines a data buffer for the expected network type command from the initiator. The RECEIVE command CCB defines a set of data which is known and expected by the initiator, typically a welcome or configuration type message packet. The host adapter tests to be sure that duplicate CCBs are not provided by the host.

As the initiator finishes its initialization procedure, it requests availability and configuration information using the TEST UNIT READY, REQUEST SENSE, and INQUIRY commands. Finally, it may choose to address SEND and RECEIVE commands to the targets it has located to transmit or request information packets.

When the initiator executes a SEND or a RECEIVE command, the target accepts the selection on the SCSI bus, accepts the command from the initiator, and executes the proper data transfer to or from the area specified by the proper CCB. When all SCSI activity is finished successfully, the CCB is posted back to the host program by an entry in the MBI. The host adapter updates the CCB byte count and CDB field contents to correctly reflect the operation performed. The host is notified that there is an entry in the MBI by an interrupt from the host adapter. The host then prepares a new CCB to control the target's next activity expected from the initiator.

5.4.2.2 Target Mode without a Prepared CCB

Alternatively, the processor type device may be addressed by an initiator when no CCB has yet been prepared for use by the host adapter. If the host adapter command enabling target mode has not yet been executed, the host adapter will act like any initiator. It will not accept any selection sequence and any attempts to select it by its target ID will cause the initiator to detect a selection time-out.

If the host adapter has been enabled as a Processor Target by a host adapter command, any selection to the host adapter's target address will be accepted. The availability commands and identification commands (TEST UNIT READY, REQUEST SENSE, and INQUIRY) will be executed completely and normally. If a SEND or RECEIVE command is received and if a CCB is not active, either because the host has not completed its program initialization or because the host has not finished analyzing the results of previous data transfers and has not generated a new CCB, the Processor Target will accept the selection, obtain the IDENTIFY Message Out to determine what Logical Unit has been selected, request the CDB from the SCSI, and then disconnect. The CDB will be partially interpreted so that the proper MBI can be generated to notify the host that a new CCB with a certain address, direction, and data length must be generated. When the new CCB is passed to the host adapter by an MBO entry, the CCB is filled up with the command information, the SCSI is reconnected, and the command is completed as described above.

5.5 DMA CHANNEL INITIALIZATION WITH THE HOST ADAPTER BIOS DISABLED

The DMA circuitry must be set to a special state to allow the Bus Master operation of the AHA-154XA to operate correctly. This state is normally established by the BIOS during initialization so that no other activity is required. If a DMA channel other than the default channel is being used or if the DMA channel is manipulated by other programs, the circuitry must be initialized in the following way before the AHA-154XA can be used.

For the DMA channel being used, 2 bytes of data must be written to the DMA controller port specified to initialize the Host DMA controller for Bus Master DMA operation. The following table specifies these values in HEX.

DMA Channel	DMA Controller Port	Data
0	0B	0C
	0A	00
5	D6	C1
	D4	01
6	D6	C2
	D4	02
7	D6	C3
	D4	03

5.6 INTERRUPT INITIALIZATION

This setup procedure is normally completed by the BIOS during initialization so that no other activity is required. If modifications to the interrupt handler are required, this information together with the programming information provided by the host system should be sufficient to properly set up the interrupt vectors.

The host adapter will drive one of several interrupts in the AT system. The particular interrupt used must be set up on power up initialization and be properly managed during usage. The AT interrupts of interest to the host adapter driver along with their corresponding vector locations are summarized below. All these interrupst are handled by a slave interrupt controller. The master controller handles all system interrupts such as keyboard, timer, etc. and is assumed to be correctly initialized to allow interrupts by the slave controller. Upon receiving an interrupt, the processor will be vectored to the contents of the corresponding vector location.

Hardware interrupt		Software interrupt vector location (hex)
int 9	--	INT71
int 10	--	INT72
int 11	--	INT73
int 12	--	INT74
int 13	--	INT76
int 14	--	INT77
int 15	--	INT78

The interrupt is initialized by clearing the corresponding interrupt mask bit in the slave controller. The mask register is a read/write register, and only the bit of interest should be cleared. The port address is A1 hex, and bit definitions follow.

Interrupt mask bit definition (port address A1 hex)

bit 0 -- int 8
bit 1 -- int 9
bit 2 -- int 10
bit 3 -- int 11
bit 4 -- int 12
bit 5 -- int 13
bit 6 -- int 14
bit 7 -- int 15

6.1 SINGLE THREADED BIOS COMMAND INTERFACE

The AHA-1540A/1542A BIOS resides on the host adapter board. It provides support for up to two SCSI Common Command Set disk drives under DOS. If SCSI devices other than CCS disk drives or if support for more than two disk drives is required under DOS, the Adaptec DOS Driver, ASW-1110 must be used. The BIOS provides a very simple single threaded capability that does not make use of the Mailbox Interface used by more sophisticated programs. This capability allows the host system to boot from a SCSI disk drive and to support standard DOS calls from any standard program.

The BIOS communicates with the host adapter through a special set of commands passed under the I/O Command Port command 02H (Start Bios Command). These commands are not available to any programs except the Adaptec BIOS. The Adaptec BIOS provides a standard BIOS interface. The DOS interface to the standard BIOS is described in this section.

On an AT compatible machine, up to two hard disks are supported by the BIOS resident on the mother board. Any other drives must be managed through the Mailbox Interface using an appropriate driver. The operation of the AHA-1540A/1542A BIOS on attached SCSI devices depends on the number of standard hard disks installed directly on the system.

No standard hard disks installed:

> In this case, two SCSI drives can be supported by the AHA-1540A/1542A BIOS. SCSI Device 0 Logical Unit Number 0 is designated as drive 0 (Drive C:). Either SCSI Device 0 LUN 1 or SCSI Device 1 LUN 0 may be designated as drive 1 (Drive D:). This set of addresses allows the use of two drives with either embedded controllers or bridge controllers. Booting is only performed from SCSI Device 0 LUN 0. When no standard hard disks are installed, the AHA-1540A/1542A BIOS is operating in non-concurrent mode.

One standard hard disk installed:

> In this case, the internally installed hard disk is designated as drive 0 (Drive C:). SCSI Device 0 LUN 0 is designated as drive 1 (Drive D:). Booting is performed from the internally installed hard disk. This mode of operation is called concurrent operation, indicating that the internally installed drive and one SCSI drive can operate together under the BIOS.

Two standard internal hard disks installed:

> In this case, all the disks that can be supported by the BIOS are directly installed. The AHA-1540A/1542A BIOS will not support any SCSI drives. Therefore a device driver will need to be installed to access the SCSI drives.

6.2 BIOS COMMAND EXECUTION USING INTERRUPT 13

On IBM compatible systems, disk I/O requests are passed from the operating system to the BIOS through software interrupt 13H. CPU registers are used to pass information about the desired operation and the associated parameters.

The AHA-1540A/1542A BIOS provides SCSI support by intercepting each interrupt and managing the request according to the drive address. If the drive is a floppy or internally installed fixed disk, the call is managed by the mother board BIOS with no changes. If the selected drive is a SCSI disk drive, the request is handled by the Adaptec BIOS resident on the AHA-1540A/1542A. For concurrent operation, only calls to drive 81H (D:) are handled by the AHA-1540A/1542A BIOS. For nonconcurrent operation, calls to both drive 80H (C:) and 81H (D:) are managed by the AHA-1540A/1542A BIOS.

On each Interrupt 13 call, the correct host microprocessor registers are set by the operating system program to provide the required parameters to both the Adaptec BIOS and the mother board BIOS. Most commands use the registers as indicated in the following table.

Register	Function
AH	BIOS Function Code
AL	Number of Sectors
CH	Low Order Byte of Cylinder Number
CL	Cylinder and Sector Numbers
	Bits 7,6 High Order Cylinder Bits
	Bits 5-0 Sector Number
DH	Head Number
DL	Drive Number
ES:BX	Data Buffer Address

6.2.1 Physical to Logical Address Translation

As shown above, the starting sector address for read, write and verify requests is passed as a physical address including a 10 bit Cylinder Number, an 8 bit Head Number, and a 6 bit Sector Number. SCSI devices are addressed by logical block address without regard to the physical layout of the drive. For this reason, all SCSI devices are defined as drives with 64 heads and 32 sectors per track and with the appropriate number of cylinders to provide the full capacity of the drive using this physical to logical translation. The SCSI logical address is formed by the BIOS by concatenating the values as show below:

Cylinder (10 bits) || Head (6 bits) || Sector (5 bits)=SCSI Logical Block Address

6.2.2 BIOS Command Return Codes

The BIOS command, when complete, returns control to the requesting program at the next instruction after the software interrupt. A return code is set in the Carry Flag (CF) and a status code is placed in register AH for examination by the requesting program. The expected return codes placed in the Carry Flag are shown below.

CF Contents at Return	Return Code
CF = 1	Status is non-zero. Unusual condition or error detected.
CF = 0	Status is zero. Normal command completion occurred.

AH Contents at Return	Status of Operation
AH = 00H	No error: The operation completed successfully.
AH = 01H	Invalid Function Request: The operation code or an associated parameter provided by the Interrupt 13 operation was not valid.
AH = 02H	Unable to Read Address Mark: One of the following additional sense codes (SCSI ASC) was presented in the sense information returned by the REQUEST SENSE command: 12H (No AM Found on Data Field) 21H (Illegal Logical Block Address)
AH = 03H	Write Protect Error: Returned SCSI ASC was: 27H (Data Protect)
AH = 04H	Read Error: Returned SCSI ASC during a read operation was: 14H (No Record Found) 16H (Data Sync Error)
AH = 10H	Uncorrectable ECC Error in Data: Returned SCSI ASC during a read operation was: 10H (ID ECC Error) 11H (Unrecovered Read Error)
AH = 11H	ECC Corrected Data Error: Returned SCSI ASC during a read operation was: 17H (Recovered Read Error w/o ECC) 18H (Recovered Read Error w/ ECC)

AH = 20H	General Controller Failure: A host adapter detected failure occurred or one of the following SCSI ASC's was returned: 01H 08H 40H 46H 03H 09H 41H 47H 05H 1BH 42H 48H 06H 1CH 43H 49H 07H 1DH 44H
AH = 40H	Seek Operation Failed: Returned SCSI ASC was: 15H (Seek Positioning Error) 02H (No Seek Complete)
AH = 80H	Selection Time-out: A host adapter does not respond to BIOS.
AH = AAH	Device Not Ready: Returned SCSI ASC was: 04H (LUN Not Ready) 28H (Unit Attention, Ready) 29H (Unit Attention, Power On) 2AH (Unit Attention, Mode Select Change)
AH = BBH	Unknown Target Sense Error Occurred: A SCSI ASC other than those specified above was returned from the selected SCSI device.
AH = CCH	Write Error: Not Returned
AH = FFH	Sense Operation Failed: BIOS unable to retrieve sense information from target.

6.3 BIOS DISK COMMANDS

The commands that can be accepted from the operating system by the BIOS include all those commands required for normal DOS operation, for booting of the DOS operating system, for the booting of other operating systems, and for basic maintenance and verification of normal disk operation. The command set is summarized in the following table and each command is described in more detail in the sections following.

AH Register	Meaning
00 H	Reset Disk System
01 H	Read Status of Last Operation
02 H	Read Desired Sectors into Memory
03 H	Write Desired Sectors from Memory
04 H	Verify Desired Sectors
06 H	Identify SCSI Devices
08 H	Read Drive Parameters
09 H	Initialize Drive Pair Characteristics
0C H	Seek
0D H	Alternate Disk Reset
10 H	Test Drive Ready
11 H	Recalibrate
15 H	Read DASD Type

The Format commands (AH = 05, 06, 07, and 1AH) are not supported by the AHA-1540A/1542A BIOS. The format operation is performed under a special format utility installed in ROM and initiated through the DEBUG program.

The Diagnostic Reserved commands (AH = 0A, 0B, 0E, 0F, 12, and 14H) are not supported by the AHA-1540A/1542A BIOS.

The Park Heads command (AH = 19H) is not supported by the AHA-1540A/1542A BIOS.

The Reserved for Diskette commands (AH = 16, 17, 18) and the commands from 1BH up to FFH are not supported by the AHA-1540A/1542A BIOS. Any attempt to execute any of these unsupported commands will be ended by the BIOS and an error code of 01H (Invalid Function Request) will be returned in the AH register.

6.3.1 Reset Disk System

The BIOS is requested to reset the disk subsystem. A SCSI Reset operation is performed on the SCSI bus if the bus is busy at the time the Reset Disk System command is received by the host adapter. No other SCSI or host adapter activity occurs. The BIOS command is then passed on to the standard BIOS so that any internally installed hard disks and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed hard disk, the drive number is decremented by the AHA-1540A/1542A BIOS so that the standard BIOS does not attempt to reset the drive that is not installed.

Input Parameters: AH = 00H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.2 Read Status of Last Operation

The status of the last operation performed to the specified disk is returned. No SCSI activity occurs. The disk status is reset to zero.

Input Parameters: AH = 01H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.3 Read Desired Sectors Into Memory

The sectors requested by the parameters are read from the disk to the system memory. The SCSI command is executed as a READ (EXTENDED) command (SCSI Operation Code 28H). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time. If a 11 Error (ECC Corrected Data Error) is returned, the data returned has been corrected and may be used with confidence.

Input Parameters:
AH = 02H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Read
ES:BX = Address of buffer area

Output Parameters:
AH = Status of Operation
CF = Return Code

6.3.4 Write Desired Sectors from Memory

The sectors requested by the parameters are written from the system memory to the indicated disk. The SCSI command is executed as a WRITE (EXTENDED) command (SCSI Operation Code 2AH). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters:
AH = 03H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Write
ES:BX = Address of buffer area

Output Parameters:
AH = Status of Operation
CF = Return Code

6.3.5 Verify Desired Sectors

The sectors defined by the parameters are verified to be correctly written on the SCSI disk. The SCSI command is executed as a VERIFY command (SCSI Operation 2F) with the Byte Check bit set to zero. If the VERIFY command is not supported by the selected disk, the Verify Desired Sectors will perform a SCSI READ command (SCSI Operation Code 28H) and throw away the received data. If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters: AH = 04H
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder and Sector
AL = Number of Sectors to Verify

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.6 Identify SCSI Devices

This is a special AHA-1540A/1542A BIOS call that is used to return the number of the first supported SCSI drive. In the nonconcurrent case (2 SCSI drives), the returned value will be 80H. If only one SCSI drive is installed, the returned value will be 81H.

Input Parameters: AH = 06H

Output Parameters: AH = Status of Operation
AL = First Drive Supported
80H Nonconcurrent operation
81H Concurrent operation
CF = Return Code

6.3.7 Read Drive Parameters

A SCSI READ CAPACITY command is used to determine the maximum logical block of the selected drive. This information is then used to calculate the proper number of cylinders to be returned to the host system. The number of heads returned will always be 64 and the number of sectors per track will always be 32. The number of drives returned will include both internally installed drives and SCSI drives.

Input Parameters: AH = 08H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
DL = Number of BIOS accessible drives attached (1 or 2)
DH = Maximum value for head number (3FH)
CH = Maximum value for Cylinder Range (Low Byte)
CL = Maximum value for Sector, High Cylinder Bits
Bits 7,6 High Order Cylinder Bits
Bits 5-0 Sector Number Maximum Value (20H)
CF = Return Code

6.3.8 Initialize Drive Pair Characteristics

This command performs no operation, since SCSI CCS drives are self configuring.

Input Parameters: AH = 09H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.9 Seek

A seek to the logical block address defined by the physical parameters is performed. The seek is performed using the SEEK (EXTENDED) command (SCSI Operation 2BH). The SEEK commands are not mandatory CCS commands and are not required for proper functioning of SCSI devices. If the addressed disk drive reports an error indicating that the SEEK (EXTENDED) command is not supported, the BIOS command will complete normally anyway. Since the seek operation is performed automatically by a Read or a Write operation, there is no need to generate a separate seek operation to access data.

Input Parameters: AH = 0CH
DL = Drive Number (80H or 81H)
DH = Head
CH = Cylinder
CL = High Cylinder. (Sector bits = 0)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.10 Alternate Disk Reset

The BIOS is requested to reset the disk subsystem. A SCSI Reset operation is performed on the SCSI bus if the bus is busy at the time the Reset Disk System command is received by the host adapter. No other SCSI or host adapter activity occurs. The BIOS command is then passed on to the standard BIOS so that any internally installed hard disks and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed hard disk, the drive number is decremented by the AHA-1540A/1542A BIOS so that the standard BIOS does not attempt to reset the drive that is not installed.

Input Parameters: AH = 00H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.11 Test Drive Ready

The BIOS command determines that the specified drive is available and ready by executing a TEST UNIT READY command (SCSI Operation Code 00H) to the SCSI device. The command may have to be executed a second time if a Unit Attention condition was detected in the first execution of the TEST UNIT READY.

Input Parameters: AH = 10H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.12 Recalibrate

The BIOS command transmits a REZERO UNIT command (SCSI Operation Code 01H) to the specified drive. Since the REZERO UNIT command is not a mandatory command and is not required for proper functioning of the SCSI device, the BIOS command will complete without indicating an error even if the SCSI device indicates that the command is invalid.

Input Parameters: AH = 11H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation
CF = Return Code

6.3.13 Read DASD Type

The AHA-1540 BIOS executes this command by performing an INQUIRY (SCSI Operation Code 12H) and a READ CAPACITY (SCSI Operation Code 25H) to the selected SCSI drive. The INQUIRY command is used to verify that the device is a Direct Access Storage Device. The READ CAPACITY is used to determine the number of logical blocks available. A special return format is used to obtain the required information.

Input Parameters: AH = 15H
DL = Drive Number (80H or 81H)

Output Parameters: AH = Status of Operation (Special Format)

00H Drive not present or DL invalid
01H Reserved
02H Reserved
03H Fixed Disk installed

CX,DX Number of 512 byte blocks available on disk
CF = Return Code

7.1 PC/AT BIOS

The PC/AT BIOS is provided to allow the user to use the AHA-1540A/1542A in lieu of, or in addition to, a standard PC/AT hard disk controller. This compatibility includes booting from a SCSI device. Hard disk requests are sent to the BIOS via an INT 13 software interrupt. CPU register contents specify the desired I/O function and associated parameters. The BIOS then uses host adapter commands to emulate PC/AT functions. Again, since the mailbox architecture is circumvented, PC/AT BIOS functions run in a single-threaded mode.

The BIOS consists of three major functional components. These are:

1. Initialization Routine
2. System Boot Routine
3. Hard Disk I/O Routine

7.1.1 Initialization

The Initialization routine is called at power-up. This routine performs all of the necessary initialization functions and will display the following message if the system successfully recognizes the AHA-1540A/1542A BIOS.

ADAPTEC AHA-1540A/1542A HOST ADAPTER BIOS
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If any subsequent initialization of the AHA-1540A/1542A fails, the following message is displayed:

HOST ADAPTER NOT FOUND AT PORT 330H.

Otherwise, the AHA-1540A/1542A BIOS chooses a course of action based upon the number and types of hard disks already installed. In each case, the number of hard disks already installed is displayed along with the ID numbers of any SCSI devices that are successfully used by the BIOS.

Possible Messages:

HARD DISK #0 ALREADY INSTALLED.
HARD DISK #1 ALREADY INSTALLED.
HOST ADAPTER DIAGNOSTIC FAILURE.
SCSI DEVICE 0 : 0 NOT FOUND.
USING SCSI DEVICE 0 : 0 AS HARD DISK #0.
USING SCSI DEVICE 0 : 0 AS HARD DISK #1.
USING SCSI DEVICE 0 : 1 AS HARD DISK #1.
USING SCSI DEVICE 1 : 0 AS HARD DISK #1.

NOTE: No error message is displayed if a second SCSI drive is not available.

If the system reports an initial number of hard drives greater than 2, the following message is displayed:

SYSTEM CONFIGURATION ERROR.

The AHA-1540A/1542A BIOS allows the use of 0, 1, or 2 hard disks on the SCSI bus under DOS without a device driver.

If 2 hard disks are attached to an internal hard disk controller, and are already recognized by the system, the BIOS does nothing. A device driver will be needed to access SCSI devices.

If 1 hard disk is attached to an internal hard disk controller, and is already recognized by the system, the BIOS attempts to assign the SCSI device (Target : LUN) 0 : 0 as the second drive. (drive D:) If this is unsuccessful, an initialization error is reported to the system.

If there are 0 hard disks attached to an internal controller, the BIOS attempts to assign the first SCSI device (Target : LUN) 0 : 0 as the first drive. (drive C:) If this is unsuccessful an initialization error is reported to the system. If successful, the BIOS attempts to assign another SCSI device as the second drive. (drive D:) Device 0 : 1 is tried first, and if that fails, device 1 : 0 is tried. There is no initialization error reported if a second drive is not available.

7.1.2 System Boot

System boot is invoked by execution of an Interrupt 19. No interception of this interrupt is necessary, as the PC/AT BIOS manages the boot process. When the boot procedure attempts to read the boot track from drive C:, the AHA-154XA BIOS will respond if drive C: is a SCSI Drive. Only SCSI drive 0:0 can be assigned as a SCSI C: drive. Mother board BIOS's that use interrupt 13 to perform booting should boot normally from SCSI drives using the AHA-154XA.

7.1.3 Hard Disk I/O

The BIOS enables up to two SCSI drives to be accessed via interrupt 13 as described in Section 6.

7.2 XENIX/UNIX Drivers

SCO Xenix and Unix, Interactive Systems Unix, and Microport Unix all support the AHA-1540A/1542A at the time of this publication. Please consult with these Operating System companies for more information on their products.

7.3 DOS Driver

An optional DOS Driver is available that enables the AHA-1540A/1542A to access additional SCSI devices on the SCSI bus. When operating under DOS, a device driver is needed to access more than two hard disks, tape devices or other types of SCSI peripherals. In addition, DOS applications that use the virtual memory mode of the 80386 processor require this driver. If you are not running DOS programs that operate in the virtual 80386 mode, or if all DOS operations will be confined to two SCSI disks or one internal and one SCSI disk, a device driver is not needed because of the on-board BIOS.

The DOS driver is installed by creating a DOS configuration (CONFIG.SYS) file that calls the device driver at boot time. Please refer to your DOS manual for information on creating a CONFIG.SYS file. At initial system loading, the AHA-1540A/1542A device driver will determine the number of hard disks attached to the system. The device driver is normally only installed if one of the following cases is true.

1) There are two internal hard disks and one or more SCSI disks.
2) There is one internal hard disk and two or more SCSI disks.
3) There are no internal hard disks and more than two SCSI disks.

The following table shows how hard disks in a system are addressed:

Configuration	C:	D:	Device Driver
TWO INTERNAL HARD DISKS	1st Int. Disk	2nd Int. Disk	SCSI Devices
ONE INTERNAL HARD DISK	Internal Hard Disk	SCSI 0/0 Disk	Other SCSI Devices
NO INTERNAL HARD DISK	SCSI 0/0 Disk	SCSI 0/1 or 1/0	Other SCSI Devices

The SCSI disk drives that are accessed by the device driver are divided into 32 MB logical disks. There can be multiple logical disks on one physical SCSI disk drive. A utility program is also provided that performs the functions of the DOS FDISK and FORMAT utilities. This utility will perform FDISK and FORMAT to SCSI disks that can only be accessed through the device driver. These utility programs partition the disks and create file directories so that DOS files may be copied and accessed from SCSI drives. Please refer to your DOS manual for details of FDISK and FORMAT.

SCSI 2 compatible and QIC 104 command set 1/4" tape drives are also be supported by the DOS device driver. The user accesses a SCSI tape drive by building a CCB as described in Section Five. The device driver passes the CCB to the AHA-1540A/1542A and instructs the AHA-1540A/1542A to complete the command. Software products such as Sytron Corporations SYTOS Tape Operating System automatically interface to the Adaptec AHA-1540A/1542A DOS driver.

To install the driver into your boot routine, you must create, or edit the DOS configuration file named CONFIG.SYS. You can use any file editor to do this, or you can create it through the "COPY CON: CONFIG.SYS" DOS command. Refer to your DOS manual for more information on this command. Once installed, the driver operates transparently to the user.

7.3.1 DOS Driver Support of Virtual Mode

The use of high performance 16-bit Bus Master DMA on the AHA-1540A/1542A SCSI host adapter may result in incompatible operation with application programs that use the 80386 virtual memory mode of operation.

In real mode, the host adapter BIOS is passed a physical address. This is necessary since the host adapter controls all SCSI I/O without CPU intervention. This physical address may not be passed

to the host adapter when the system is in the V86 mode. Programs that use the V86 mode can only be run on 80386 machines.

The AHA-1540A/1542A DOS driver also allows this type of application program to run under DOS.

7.4 AHA-1540A/1542A On-board Utilities

The AHA-154XA BIOS contains a utility program that allows the user to perform the several important functions. The utility programs are accessed using a self explanatory menu.

The utilities are accessed using the DOS Debug function. To access the utilities, boot using a standard DOS system disk or diskette. When the DOS prompt symbol appears on the screen, enter the debug program by typing **debug** and pressing Enter. The debug program will load and present a new cursor, the - symbol. Enter the following line and press enter to invoke the On-board Utility program.

G=dc00:6

If a BIOS base address other than DC000H is being used on the adapter to be tested, replace the dc00 parameter with the actual BIOS base segment. The segment is the upper 16 bits of the 20 bit BIOS base address.

The menu options include the following items which are selected by pressing the index number of the menu function.

(1) A list of all devices installed on the SCSI bus may be requested. This information is retrieved via a RETURN INSTALLED DEVICES host IOCP command, followed by INQUIRY commands to all available targets.

(2) A device may be selected for execution of the following two functions. Pressing the '2' key toggles the selection from one installed device to the next.

(3) A low level, or primary, format of the selected Target/LUN can be requested. A MODE SELECT is issued first to set the block size at 512 bytes per sector. Then a FORMAT command is issued which will format the drive with factory as well as grown defects. Only one SCSI drive can be formatted at a time.

(4) Integrity of a target can be checked by verifying an entire drive. Any correctable errors found will automatically be handled through the SCSI Reassign Blocks Command. If any uncorrectable errors are found the user will first be asked via a screen prompt if reassignment of the effected block should be performed.

(5) The user can leave the AHA-154XA On-board Utility functions and return to normal DOS operation.

In addition to the On-Board Utilities, a DMA channel test also resides on the AHA-154XA BIOS. The test verifies that all DOS-available memory can be accessed correctly from the host adapter using first party DMA. The test takes from 2 to 10 minutes to execute, depending on the CPU speed and the amount of memory available. The test is invoked by entering the debug program as above and entering:

G=DC00:9

The program then is activated and verifies each segment of the memory, indicating with screen messages as each segment is verified. The test runs indefinitely or until an error is detected. In most cases of error, the error information cannot be presented since the host operating system is likely to be compromised. The error symptom is usually a system crash. The test is halted by rebooting.

8.0 SCSI FEATURES

8.1 SCSI DESCRIPTION, INITIATOR MODE

The AHA-1540A/1542A provides a very high performance SCSI interface connection. The host adapter meets the ANSI Standard X3.131-1986, describing the SCSI. The host adapter additionally meets conformance level 2 of the specification by implementing the following SCSI options:

Accepts or manages the following messages:

Command Complete
Disconnect
Message Reject
Identify
Save Data Pointer

Performs arbitration

The following alternatives are selected for the AHA-1540A/1542A SCSI interface connection from those described by X3.131-1986.

Single-ended SCSI driver/receivers are used.

The Termination Power is supplied through a removable fuse, allowing the user to select whether or not termination power is provided by the host adapter at installation time.

Parity is always generated. Parity checking can be disabled through the jumper selection.

The "Soft" Reset option is always performed by the AHA-1540A/1542A. If the user desires the "Hard" Reset, an interrupt servicing program that detects the SCSI Reset Detected interrupt in the Interrupt Flags Port must set the Soft Reset bit in the Control Port. This bit forces the host adapter to clear all SCSI related operations, but does not require execution of the diagnostic functions. If the Soft Reset bit has been set, the host software must re-initialize the AHA-1540A/1542A.

Synchronous data transfer is supported. Negotiation for the synchronous transfer initiated by another SCSI device will be accepted by the AHA-1540A/1542A at any time. If the jumper has been set to allow it, the AHA-1540A/1542A will also initiate synchronous data transfer negotiation when it has detected that such negotiation may be required.

Multitasking is fully supported.

Modify Data Pointers is supported to allow Zero Latency Read operations.

In addition to these SCSI functions, the SCSI Common Command Set at level 4B is also supported. While this document was never made a standard, it describes a widely available set of disk drive functions which are supported by the host adapter. The Host Adapter BIOS commands are all mapped in to SCSI CCS commands to allow the proper support of all the most common SCSI disk drives. The Adapter Command "Return Installed Devices" also uses CCS commands to determine which devices are available.

The draft ANSI standard for SCSI-2 has been used as a reference for the implementation of all SCSI functions with the expectation that the host adapter will be fully compatible with the final version of the SCSI-2 standard. In particular, the Processor type device command set has been selected from the SCSI-2 manual for Target Mode operation.

8.1.1 Linked SCSI Commands

The AHA-1540A/1542A supports linking of SCSI commands in initiator mode. When the link bit in the SCSI command control byte is set, the target will present either a 0A or 0B message at command completion. The AHA-1540A/1542A uses the the link pointer in a CCB to fetch another CCB. At the same time, the completed CCB status and address are stored in an MBI. If the target returns a 0B or 00 message, the AHA-1540A/1542A generates an interrupt to inform the host of the full MBI. If the target returns a 0A message, the MBIF interrupt is not posted until all linked commands are completed. The linked CCBs must address the same target and LUN since the target is not re-selected.

8.1.2 Zero Latency Read Operation

The AHA-1540A/1542A implements Zero Latency operation through the use of modify data pointer messages. Zero Latency can eliminate rotational latency, depending on the length of the data transfer, by supporting out of order data transfers. This advanced feature is currently only implemented on the ACB-4525Z SCSI to ESDI controller, and is supported transparently to the user.

Since the Adaptec host adapter family is the first to support Zero Latency Read operation, this section is intended to briefly explain the required target support. Please refer to the Adaptec ACB-4525Z SCSI to ESDI controller manual for complete details of Zero Latency Read operation.

After seeking to the target track, the ACB-4525Z (ACB-4525Z is assumed since it is the first SCSI controller to implement this feature) will begin reading block IDs. If the first block ID is within range of the data transfer, but not the last block of the the data transfer, the ACB-4525Z will begin reading the subsequent blocks into its buffer. Before transferring data the ACB-4525Z will issue a MODIFY DATA POINTER message to the AHA-1540A/1542A. This supplies a positive argument that is added to the value of the current data pointer. The ACB-4525Z will now send this portion of the data transfer to the host. The ACB-4525Z will resume reading data into its buffer as soon as the first block of the data transfer is detected. Before sending this data to the host, the ACB-4525Z will issue a second MODIFY DATA POINTER message to the AHA-1540A/1542A which supplies a negative argument. This returns the data pointer to its original position. This guarantees that a data transfer of one track or less will never require more than a single revolution since data can now be transferred out of order.

8.1.3 SCSI Messages

The AHA-154XA host adapter supports a number of special messages in addition to the messages required by meeting conformance level 2. Those messages are described in detail in the SCSI specification, X3.131-1986, and in this section where they are used. The messages are summarized in this table:

FUNCTION	MESSAGE	CAUSED BY
Standard Messages	Command Complete	Normal Sequencing
Error Management	Message Reject	Invalid Messages
	Bus Device Reset	Special CCB
	Abort	Special MBO
Disconnect / Reconnect	Identify	Normal Sequencing
	Disconnect	Normal Sequencing
	Save Data Pointer	Normal Sequencing
	Restore Pointers	Special Sequencing/ZLR
Synchronous Transfer	Synchronous Data Transfer Request	Initialization Sequencing
Zero Latency Operation	Modify Data Pointers	ZLR Sequencing
Linked Commands	Linked Command Complete	Command Linking
	Linked Command Complete With Flag	Command Linking

8.2 SCSI DESCRIPTION, TARGET MODE

8.2.1 Initiator Conformance Level Requirements

Initiators that execute commands against an AHA-1540A/1542A operating in Target Mode are required to have the following conformance levels, as described in Appendix E of the SCSI Specification, ANSI X3.131-1986. Conformance must be present with respect to each of the following items:

The initiator must use single-ended drivers.

Termination power may optionally be provided by the initiator, but must meet the SCSI specification in both its over-current protection and its reverse current diode protection. The terminators may be installed on the AHA-1540A/1542A board or installed as in-line terminators at the cable connectors.

The implementation of parity is optional, but desirable.

The initiator may support either "hard" reset or "soft" reset. All attached devices must support the same type of reset.

The initiator must meet the requirements of conformance level two. In particular, all LUN addressing must be performed by the IDENTIFY message, not by the LUN field in the CDB. Disconnection and reconnection must be supported.

The initiator and target functions have the same SCSI ID.

8.2.2 Support of Synchronous Transfer

Synchronous transfer is supported by the AHA-1540A/1542A in target mode without any instruction or support from the system processor. If an initiator invokes a synchronous transfer negotiation, the AHA-1540A/1542A will complete the negotiation of the required transfer offset and period. If the proper jumper has been set, the AHA-1540A/1542A will also attempt to negotiate synchronous transfer during the initial selection period of the first command after an initialization or after a SCSI reset.

8.2.3 SCSI Target Operation in Processor Target Mode

When the AHA-1540A/1542A has been set to respond in Processor Target Mode, the host adapter appears on the SCSI bus as a normal processor type device as defined by the SCSI specification. From one to eight LUN's may be supported, depending on the LUN mask byte in the Enable Target Mode command. Five SCSI commands are accepted:

TEST UNIT READY
REQUEST SENSE
INQUIRY
SEND
RECEIVE

All other commands are rejected with CHECK CONDITION status. The sense information will indicate a Sense Key of 05H (Illegal Request) with a Sense Code of 20H (Invalid Command Operation Code).

The commands that do not perform data transfer to or from the host are handled completely by the AHA-1540A/1542A with no CCB communication with the host system. Those commands are the TEST UNIT READY, REQUEST SENSE, and INQUIRY commands. The SEND and RECEIVE commands must have a CCB from the host with the proper direction bits, the proper initiator address, and the proper LUN number to complete the SCSI operation. The SEND and RECEIVE CCBs may be provided to the host adapter before a command is received on the SCSI or may be requested after the command is received.

Each time an initiator activates a command to the AHA-1540A/1542A, an internal sub-channel is activated to manage the command. The sub-channel is dedicated to that particular LUN-Initiator transaction until all operations associated with the command are completed. Such operations include disconnection to obtain a CCB, pending error conditions, and linked operations. If all sub-channels are busy, a selection to the AHA-1540A/1542A will result in the AHA-1540A/1542A accepting the command and then generating BUSY status immediately. If this occurs, the initiator must re-issue the command later.

8.2.3.1 TEST UNIT READY

BIT / BYTE	7	6	5	4	3	2	1	0
0	Test Unit Ready Operation Code (00)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Reserved (00)							
5	Reserved (00)						Flag	Link

The TEST UNIT READY command follows the SCSI specification in all respects. If the AHA-1540A/1542A has been initialized by the Enable Target Mode command to the Processor Target Mode, the command will finish normally with GOOD status and a COMMAND COMPLETE message. The host adapter supports the normal definition of UNIT ATTENTION on the first operation after power on, after a SCSI Reset, or after a BUS DEVICE RESET.

If a TEST UNIT READY command is executed against an LUN which was not allowed by the Enable Target Mode command, then CHECK CONDITION status will be presented with sense data of Sense Key 5 (Invalid Request) and an Error Code of 25H (Invalid LUN).

8.2.3.2 REQUEST SENSE

BIT / BYTE	7	6	5	4	3	2	1	0
0	Request Sense Operation Code (03h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

If the AHA-1540A/1542A has returned CHECK CONDITION status to a previous command, the REQUEST SENSE command will obtain the sense information associated with the error. The sense information will be sent in the extended sense format according to the SCSI standard. The data format is given in the following figure:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Error Code (70h or Foh)							
1	Reserved (00h)							
2	00		ILI	0	Sense Key			
3 - 6	Information Bytes (Residue)							
7	Additional Sense Length (06h)							
8 - 11	Reserved (00000000h)							
12	Additional Sense Code							
13	Additional Sense Code Qualifier (00h)							

The following errors are detected and presented by the AHA-1540A/1542A while operating in Processor Target Mode:

Error	Sense Key	Additional Sense Code
No Sense Data	00	00
Invalid Command Operation Code	00	20
Invalid LUN	05	25
Invalid Command Parameter	05	26
Power Up Attention	06	29
Reset Attention	06	29
Interface Parity Error	0B	47
Initiator Detected Error	0B	48
Dumb Initiator	05	2B

One set of error data may be buffered for each initiator - LU association possible, up to a total of 56 sets of sense data. No Contingent Allegiance or Extended Contingent Allegiance state is established.

The Error Code (Byte 0) will be F0h if the residue field is valid and 70h if the residue field has no information.

The Incorrect Length Indicator (ILI) will be set if an incorrect data transfer length is executed as described in Section 8.2.4.

The residue is set equal to the transfer length requested in the initiator CDB minus the target host's specified data length specified as a four-byte two's complement number.

8.2.3.3 INQUIRY

BIT / BYTE	7	6	5	4	3	2	1	0
0	Inquiry Operation Code (12h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

The INQUIRY command provides the information necessary to uniquely identify the Adaptec AHA-1540A/1542A as a Processor-type device. The information is returned in the SCSI-2 format. The following information is returned to any selecting initiator from any selected AHA-1540A/1542A Logical Unit:

BIT / BYTE	7	6	5	4	3	2	1	0
0	Peripheral Qualifier			Processor Device Type (03h)				
1	Reserved (00h)							
2	Reserved (00h)					ANSI Version (02)		
3	Response Data Format (02h)							
4	Additional Length (1Dh)							
5	Reserved (00h)							
6	Reserved (00h)							
7	0	0	0	Sync =1	Lnk=1	0	0	0
8 - 15	Vendor Identification (ASCII) ADAPTEC *bbb*							
16 - 31	Product Identification (ASCII) AHA-1540*bbbbbbbb*							
32 - 35	Product Revision Level (ASCII)							

If the INQUIRY command is attempted against a Logical Unit that has not been enabled as a target, byte 0 is returned as 23h, indicating that the LUN is not installed, but would be a Processor Device if it were installed. The remaining bytes are returned normally.

If a length shorter than the required 36 bytes is specified by the INQUIRY command, the number of bytes specified by the command is transferred. If a length longer than 36 bytes is specified, the command will only transmit 36 bytes.

8.2.3.4 SEND

BIT / BYTE	7	6	5	4	3	2	1	0
0	Send Operation Code (0Ah)							
1	LUN (unused = 00)			Reserved (00)				
2	Transfer Length (MSB)							
3	Transfer Length							
4	Transfer Length (LSB)							
5	Reserved (00)						Flag	Link

The SEND command has the format specified by the SCSI standard.

The SEND command transfers data from the initiator to the target. The information is placed in the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter by the host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the SEND command specifies the length in bytes of data that is sent during the DATA OUT phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in Section 8.3.2.6.

The CDB information is included in the returned CCB so that the receiving host programming can determine whether or not the information transmitted by the SEND command was application data or asynchronous event notification data.

8.2.3.5 RECEIVE

BIT / BYTE	7	6	5	4	3	2	1	0
0	Receive Operation Code (08h)							
1	LUN (unused = 00)			Reserved (00)				
2	Allocation Length (MSB)							
3	Allocation Length							
4	Allocation Length (LSB)							
5	Reserved (00)						Flag	Link

The RECEIVE command has the format specified by the SCSI standard

The RECEIVE command transfers data from the target to the initiator. The information is taken from the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to th host adapter through the MBO protocol. An appropriate CCB must have the same initiator address, target LUN, and direction as is required to complete the command.

The transfer length in the RECEIVE command specifies the length in bytes of data that is sent during the DATA IN phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in section 8.3.2.6.

8.2.4 Incorrect Length Management for Target Mode Operation

The messages transmitted using the SEND and RECEIVE commands are normally expected to have a length that has previously been agreed to by the initiator system software and by the target system software. If the transfer length specified by the command is equal to the transfer length specified by the CCB, normal operation takes place and no errors are posted.

If the transfer length specified by the initiator's command is shorter than the space defined by the target CCB, all data bytes expected and required by the initiator will be transmitted. The target AHA-1540A/1542A will indicate GOOD status on the SCSI at the end of the transfer. The target system's software however must be notified that the entire area of data defined by the CCB was not transmitted. A Target Status of GOOD will be presented in the returned CCB. At the same time, the Incorrect Length Indication bit (bit 5 of byte 2) will be set in the CCB Request Sense data area. Bytes 3 through 6 of the Request Sense data area will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the CCB. In this case, the residue will be a negative number, since the requested length was less than the area specified by the CCB. The HA status stored in the CCB will be 12h, indicating a Data Over/Under Run. The MBI Status Byte will be set to 04 to indicate that the CCB was completed with an error.

If the transfer length specified by the initiator's command is longer than the space defined by the target CCB, only those bytes contained within the CCB's data transfer area will be transmitted. The target AHA-1540A/1542A must indicate with an error condition to the initiator that not all the requested bytes could be transferred. The target AHA-1540A/1542A presents a SCSI status of CHECK CONDITION at the end of the data transfer. The Request Sense information transmitted to the initiator as a result of an immediately following REQUEST SENSE command indicates that an Incorrect Length Indication is present by setting bit 5 of byte 2. Bytes 3 through 6 of the Request Sense information transmitted to the initiator will contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the target CCB. In this case, the residue will be a positive number, since the requested length was greater than the available area. The target system's software must also be notified that the transfer length requested by the initiator exceeded the assigned buffer area. A Target Status of CHECK CONDITION will be presented in the returned target CCB. A Host Status of '12'h will be returned indicating a Data Over/Under Run. At the same time, the information that will later be posted to the initiator by the REQUEST SENSE command will be posted to the target system in the CCB Request Sense data area. This includes both the Incorrect Length Indicator and the Residue. The MBI Status Byte will be set to 04 to indicate that the CCB was completed with an error.

Section Nine Flexible Disk Controller Specification

9.1 FLOPPY DISK INTERFACE

The floppy disk controller allows the attachment of any standard IBM compatible floppy disk drive to the AHA-1542A. The floppy disk controller is accessed by the standard IBM compatible BIOS through the standard IBM compatible floppy diskette program interface. The floppy disk controller section of the host adapter is completely independent of the host adapter function. The floppy disk controller section can be disabled by removing jumper J13 as described in section 3.4.2. The base address and interrupt and DMA channels can be modified by jumpers as described in section 3.4.

A floppy disk is attached to the host adapter using a 34 pin ribbon cable connector as specified in section 1.4. The pin out of the cable is described here, although that is usually not necessary, since all standard floppy disk drives have the same pin out. Some systems choose to use the same address for all floppy disk drives and to twist the cable, pins 10-16, to switch the address lines at the drive.

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-LD
Ground	3	4	Reserved
Ground	5	6	Reserved
Ground	7	8	-INDEX
Ground	9	10	MOTOR ENB DRIVE A
Ground	11	12	DRIVE SELECT B
Ground	13	14	DRIVE SELECT A
Ground	15	16	MOTOR ENB DRIVE B
Ground	17	18	DIRECTION
Ground	19	20	-STEP
Ground	21	22	-WRITE DATA
Ground	23	24	-WRITE ENABLE
Ground	25	26	-TRACK 0
Ground	27	28	-WRITE PROTECT
Ground	29	30	-READ DATA
Ground	31	32	-HEAD SELECT
Ground	33	34	-DSKCHNG

10.0 PROBLEM DETERMINATION

10.1 SELF DIAGNOSTIC CAPABILITY

The AHA-1540A/1542A executes self diagnostics upon power up or after a hard reset. These diagnostics test the CPU operation, perform a sum check on the EPROM, and check the data transfer paths on the board. The host system has the option of exercising more extensive diagnostics involving reads and writes to memory.

The red light emitting diode (LED) on the host adapter indicates the result of the self diagnostic process. When power is first applied to the board, the LED turns on. If the board is operating normally, the light will soon go off and stay off until SCSI or I/O port activity is requested by the host. If the board is not operating correctly, a flash code number is flashed on the LED to indicate which test failed. The flash code number is indicated by a series of 1 to 6 closely spaced flashes followed by a longer pause. The flash code is repeated continuously until the board is powered off, reset, or repaired. The SCSI interface should be disconnected if these diagnostic tests are being run for fault isolation purposes. At least one set of terminators must remain installed or the LED will stay on, indicating that the AHA-154XA is receiving an active RST signal. Continuous execution of the diagnostics can also be forced by inserting the diagnostic jumper (pin-pair 2 in jumper J1). The flash code and associated failure modes are indicated in the following table.

TABLE OF FLASH CODES

FLASH CODE	POSSIBLE MEANINGS OF FLASH CODE
LED Remains On	Host Adapter Control Processor inoperative/terminators missing or not powered.
1 Flash	Firmware EPROM check sum failed.
2 Flashes	RAM test failed.
3 Flashes	AIC-6250 SCSI protocol chip verification failed
4 Flashes	FIFO read data path test failed.
5 Flashes	FIFO write data path test failed.
6 Flashes	Channel 2 test failed.

If any of these failure conditions is identified, the host computer should be powered down, the host adapter removed, and the host adapter inspected for physical damage. Such damage can include EPROM's that are not correctly installed or not firmly seated, broken wires, missing or damaged components, or conductive debris on the board. If no such physical damage is found, the AHA-154XA should be returned for repair.

All boards are fully tested, burned in, cleaned, and inspected before they are shipped. Care should be taken to keep the board in its protective conductive wrapping until it is installed. With these simple precautions, mechanical damage can normally be avoided.

10.2 INDICATORS

The red light emitting diode (LED) on the AHA-154XA is used to provide the fault isolation information described above. In addition, the LED indicates when the host adapter is performing activities on the host interface and the SCSI interface. The LED is such a useful activity indicator that a connector is made available on the host adapter to allow the cable to an externally visible LED to be attached. (See Section 3.3.9).

As an activity indicator the LED is turned on from the time that an Adapter Command is transmitted to the host adapter until the HACC interrupt is generated to indicate that the Adapter Command is complete. In addition, the LED will be turned on whenever SCSI bus activity is occurring. This is roughly the same period of time that the SCSI BSY signal is present on the SCSI bus. If the light stays on when no activity is expected to be present on the bus, it is possible that the bus is hung, the processor has failed, that unexpected activity is occurring, or that the SCSI cables are incorrectly installed. If the SCSI cables are installed reversed, the host adapter is forced in to a solid SCSI reset state which halts normal operation.

10.3 PROBLEMS DETECTED DURING OPERATION

The information in section 10.3 is not intended for routine users of the AHA-1502A/1542A. It is intended to provide a reference for programmers preparing device drivers, error recovery procedures, and error information presentation programs.

Operation of the I/O Port interface is controlled and monitored by host system software. Two bits in the Status Port (Base + 0), described in section 4.2.1, are provided to indicate unusual conditions in the host adapter.

Internal Diagnostic Failure (Status Port, bit 6): This bit indicates that the self testing process after either a hard reset or a power on operation was terminated by an error condition. The error indicates that a critical failure was found in the AHA-154XA control circuitry or data paths. The error should be presented to the host video display to indicate that diagnostic actions are required. The diagnostic action uses the host adapter diagnostic flash codes to determine if the AHA-154XA is failing. The host system should be powered off, then opened so that the LED can be observed. All SCSI cables, both external and internal, should be removed from the host adapter. The system should then be powered on. If the LED flashes once and turns off, the host adapter has passed its diagnostics and should be accessible again. If the LED flashes one of the error flash codes, the AHA-154XA should be replaced. If the LED remains on and does not turn off, the host adapter is not able to begin operation at all. The host system may be holding the AHA-154XA in the reset state or the host adapter may have failed. To distinguish these two cases, the AHA-154XA should be replaced and the new host adapter operation should be verified. Be sure to power down the host system when removing or replacing the host adapter. If the diagnostics

indicate that the AHA-154XA must be replaced, it should be sent to an authorized service facility for repair.

Invalid Host Adapter Command (Status Port, bit 0): This bit is set to indicate that a command or parameter transmitted to the host adapter was invalid. This is an indication that the host software, usually an operating system, special application program, or device driver, has generated an invalid request. The responsible programming organization should be notified so that the invalid sequence or parameter can be corrected.

10.3.1 HA Status Error Indications and Corrective Actions

The Host Adapter Status indications, in addition to indicating several normal completion states, indicate three general groups of errors. One set describes software errors in the requests made to the host adapter. Even though most of these errors are caused by software design problems, the AHA-154XA may need to be replaced as an isolation step, since there exists a small chance that hardware failures in the AHA-154XA cause the appearance of a software error.

A second set describes errors detected by the host adapter firmware in the host adapter hardware. The most likely failing component in this case is the AHA-154XA, although certain system or cable failures may generate the appearance of a host adapter hardware error.

A third set describes the appearance of unexpected or incorrect sequences executed by the attached SCSI devices. In this case, the cables are the most likely failure point, with the peripheral device second and the AHA-154XA third. The host adapter status code should be returned to the host video display to indicate to the operator what errors have occurred and under what conditions the errors occurred. The following section describes those Host Adapter Status indications that indicate an error.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
11	SCSI	NO	Selection Time Out: The SCSI attempted to select a device that was not installed or that did not respond to selection due to a power, parity or addressing failure. Verify correct address values set to SCSI devices. Verify that SCSI cable routing includes the required devices. Verify SCSI cable integrity by replacement of cables. Verify that SCSI Selection Time Out value has been correctly established by Adapter Command.
12	HOST	NO	Data Over Run / Under Run: Data length or direction specified by CCB did not agree with the data length actually provided by the attached peripheral device. Often a normal error or accompanied by a check condition indicating transfer truncation. Verify program requested correct length or direction. Verify peripheral provided expected data length, number of blocks, or block length.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
13	SCSI	YES	Unexpected Bus Free: The target dropped BSY without executing the proper messages first. This normally indicates that the BSY and/or other portions of the SCSI bus failed or that the target encountered such an invalid sequence that no recovery was possible. Some targets may have sense information available to qualify the error condition. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-154XA.
14	SCSI	YES	Target bus phase sequence failure: The initiator detected an invalid phase or an invalid phase sequence. If this occurs, it is likely that the host adapter forces a SCSI reset on the bus as the first phase of the recovery process. Verify SCSI cable integrity. Verify SCSI cables are all properly connected. Replace SCSI cables. Replace peripheral. Replace AHA-154XA
15	HOST	YES	MBO Command Byte invalid: This indicates a software failure or bug in the host's development of the MBO entry. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
16	HOST	YES	Invalid CCB Operation Code: This indicates a software failure or bug in the host's development of the CCB. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
17	HOST	YES	Linked CCB does not have same LUN: This indicates that the host software generated an invalid combination of link commands. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.

NUMBER	TYPE	ERROR	DESCRIPTION AND CORRECTIVE ACTION
18	HOST	YES	Invalid Target Direction Parameters received from Host: This indicates that the host software generated an invalid Target Direction Parameter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
19	HOST	YES	Duplicate CCB Received in Target Mode: This indicates that the host system was not keeping correct management information for target mode operation and incorrectly generated a second CCB identical to one already active. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.
1A	HOST	YES	Invalid CCB Parameter or Segment List: A segment list was presented to the host adapter with a zero length segment or invalid segment boundaries. An invalid CCB parameter was presented to the host adapter. Generally, this indication will only occur during initial debug processes of new operating systems. Replace the AHA-154XA. Replace the host computer system. Contact the software developer for design support.

10.3.2 SCSI Error Indications and Corrective Actions

Error conditions detected by SCSI peripherals usually cause a CHECK CONDITION Status byte to be presented. When this is presented, the host adapter automatically retrieves the sense information from the SCSI peripheral by executing a REQUEST SENSE command according to the SCSI standard. The information returned is mapped for single-threaded BIOS operation into the categories of error conditions described in section 5.2.2. For multitasking (mailbox) operation, the information returned is made available in the area allocated for Sense Data. In either case, an intelligent attempt is made by most operating systems to retry the operation at least one time. Such retry operations may require the management of queued operations that have already started execution. This attempt to retry the operation is rarely successful, since SCSI peripheral devices have very extensive automatic retry and correction mechanisms designed to be executed before the error information is returned in the first place.

Since it is rare that such an operation is successful, the host software and operating systems should make every attempt to make available key information about the error which can be analyzed by the system operator or customer engineer. In small systems, it may be sufficient to present the important Sense Data together with the command that created the error. Some simpler systems may perform a preliminary analysis of the error information and generate a code or descriptive text that describes the error and indicates the corrective action. In very complex systems, a logging process may take place, allowing a customer engineer to analyze the data at some future time. In all systems, such information is very important for host program verification and for system integrity

verification, even if the designers choose not to make the information available to any system users other than the design and maintenance engineers.

The SCSI Sense Data is generally self descriptive. The errors can be mapped in to four major categories, each category with its own diagnostic procedure.

The first category includes those errors caused by incorrect command or parameter bytes or by incorrect sequences of commands. These errors typically are presented only during the early development stages of an operating system or device driver, since a properly operating program will not generate invalid commands.

The second category includes those sense codes associated with peripheral status presentation. Such sense codes are not truly errors, in that they inform the host program of an unusual but not unexpected condition. Such sense codes include indications that a device is not ready, that the device has just become ready, that a device has reached the end of its media (End of Tape or Blank Check), or that the expected data length and actual data length differed. These sense codes are normally used by the device driver to execute the correct operation in response to the condition. Such sense codes are not normally presented to the system user except as text that requests some action. As one example, an End Of Tape condition may require the system user to replace the tape cartridge.

The third category of errors points to a particular hardware failure in the peripheral device or its supporting electronics. Such error conditions usually require the adjustment, repair, or replacement of the peripheral device or some of its components. In some cases, the error condition may also indicate possible cable or host adapter failures. These errors must be exposed to the system user so that the proper actions can be taken.

The fourth category of errors points to a media failure in the peripheral device. Such errors include bits that cannot be recovered from magnetic media and imperfections in the surface of optical media. Most such errors are recovered using the extensive retry and correction algorithms programmed into the peripheral device. In some peripheral device technologies, the errors may be caused by noise conditions or by marginal electronic failures in the read or write path. Those rare errors that cannot be recovered usually indicate that some data important to the operating system or application has been lost. The system must make this error information available to the system user so that the system user can replace the media or recover the data from a back up copy as required. In addition, logging of errors that were successfully recovered by the peripheral device is often useful as an indicator of the overall reliability of the device or of the requirement for periodic maintenance.

10.4 PROBLEMS DETECTED DURING INSTALLATION

This section may be useful to correct problems related to installation. The information in this section is included in the Host Adapter Installation Guide.

If the system will not boot from the flexible diskette drive after initial hardware installation the following items should be checked:

- AHA-1540A/1542A internal diagnostics: The LED on the AHA-1540A/1542A should come on briefly at system power up. If the LED begins to blink at regular intervals then the host adapter has detected an internal failure and should be returned for repair or replacement to the place of purchase. A message may also be posted to the screen.

- If the AHA-1540A/1542A LED and the SCSI drive LED are always on, the SCSI cable's pin 1 orientation has probably been reversed between the host adapter and the drive. See section 3.2.

- Is the AHA-1540A/1542A BIOS message displayed on the screen? If not, the AHA-1540A/1542A BIOS is not being recognized by the system.

  a) Check for BIOS address conflicts between the AHA-1540A/1542A and other option boards.
  b) Try a different BIOS address. See section 3.3.
  c) Change the BIOS wait state jumper. See section 3.3.

- If the HOST ADAPTER NOT FOUND AT PORT 330H message is displayed check the AT port address jumper setting. Also verify that the SCSI cable is correctly installed. A forced SCSI reset caused by an inverted or displaced internal SCSI cable may cause the problem. See Section 3.3.

Problems Booting the System from a SCSI drive:

- Make sure that both standard hard disks are mapped out of the system by using the AT SETUP program.

- Make sure that the SCSI boot drive address is set to SCSI ID 0:0. Check the drive installation manual for information about setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.

- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.

- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Section 3.

- Power should be cycled off and on after changing any values on a HA, Setup program, or SCSI device to be sure that a DOS format operation has been successfully completed.

- Make sure that the SCSI bus is properly terminated.

- Make sure that the intended boot disk has an active DOS partition and a DOS format. See section 3.0 and the DOS manual for more information.

Problems using a SCSI drive as drive D: with a standard hard disk as drive C:

- Make sure that the second hard disk is mapped out of the system with the AT SETUP program.
- Make sure that the SCSI drive to be used as drive D: is set to SCSI ID 0:0. Check the drive manual for information on setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.
- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.
- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing Section 3.
- Power should be cycled off and on after changing any values on an HA, Setup program or SCSI device to be sure that the new initial values are loaded.
- Make sure that the SCSI bus is properly terminated. See Section 3.
- Make sure that the disk has a DOS partition and a DOS format. See section 5.0 and the system DOS manual for more information.

Problems using a SCSI drive as drive D: with another SCSI drive as drive C:

- Make sure that both standard hard disks are mapped out of the system with the AT SETUP program.
- Make sure that the SCSI drive to be used as drive D: is set to SCSI ID 0:1 or 1:0. Check the drive manual for information on setting the SCSI ID for that device. The Return Installed Devices utility in the Onboard Utilities can also be used to determine the SCSI addresses of peripherals on the SCSI bus.
- Power should be cycled off and on after changing any values on an HA, Setup program or SCSI device to be sure that the new initial values are loaded.
- Make sure that SCSI parity is consistently enabled or disabled on all devices on the SCSI bus.
- Verify that the host adapter and the SCSI devices are properly configured and installed by referencing section 3.
- Make sure that the SCSI bus is properly terminated. See section 3.
- Make sure that the disk has a DOS partition and a DOS format. See section 3.0 and the DOS manual for more information.

System works erratically. Hangs or the host adapter can't always find the drives.

- Check SCSI parity for consistency.
- Check Termination.
- Check cable length and integrity.
- If host adapter and drive light remain on during a hang condition, make sure that the SCSI drive conforms to the Common Command Set revision 4B. (CCS 4B)
- If only the host adapter LED remains on during a hang, it is probably a host adapter, system interface problem. The system may not be capable of First Party DMA transfers. Check with the System manufacturer for information.

Adapter Command — A command transmitted to the host adapter using the Command/Data Out Port and the Data In Port. The commands are sequenced using the Control Port, the Status Port, and the Interrupt Flag Port. Abbreviated as IOCP command.

AEN — See Asynchronous Event Notification

AHA-1540 — Adaptec Host Adapter for connecting SCSI devices to the PC/AT backplane bus. The AHA-154XA is an enhancement of the AHA-1540 (see Appendix C)

AHA-1540A — The enhanced high performance Adaptec Host Adapter for connecting SCSI devices to the PC/AT backplane bus.

AHA-1542A — The enhanced high performance Adaptec Host Adapter for connecting SCSI devices and standard IBM compatible floppy disk devices to the PC/AT backplane bus.

AHA-154XA — Either the AHA-1540A or the AHA-1542A or both.

AHA-1540A/1542A — Either the AHA-1540A or the AHA-1542A or both.

Asynchronous Event Notification — A process by which a target can send unsolicited sense information to an initiator using the SEND command in order to inform the initiator about the occurrence of an important unusual occurrence.

Asynchronous Data Transfer — Data transfer performed by the SCSI interface involving the interlocking of a signal to the initiator (REQ) and a signal to the target (ACK) such that each step of the data transfer protocol must occur before the next step can begin. Characterized by a low data rate and independence of external timing constraints, including cable length and circuit response times.

AT Bus — The Industry Standard Architecture bus.

Bus Device Reset — A SCSI message that clears all activity in the target to which it is addressed.

Byte — An 8 bit unit of data. An octet. A byte is normally the smallest addressable unit of a memory and the unit of transfer on the SCSI.

CCB — See Command Control Block

CCS — See Common Command Set

CDB — See Command Descriptor Block

Command Control Block — A software object prepared by the host microcomputer software for the host adapter to provide it all the control information it needs to execute a SCSI command. Abbreviated CCB.

Command Descriptor Block — A block of information passed across the SCSI bus to provide the command, parameter, and address information necessary for the target to execute the desired functions. Prepared by the host software and placed in the CCB to be passed to the target by the host adapter. Abbreviated CDB.

Common Command Set — A defacto standard SCSI command set for communication with hard disk drives. The Common Command Set (CCS) is the basis for the SCSI-2 command set for all types of peripheral devices.

Control Microprocessor — An integrated circuit computer used to execute the software that controls the host adapter's operation.

Device Driver — A program that is linked with or attached to an operating system to map the software interface of the operating system to the requirements of attached peripheral devices and host adapters.

DMA — See Direct Memory Access

Direct Memory Access — A mechanism that allows hardware control of the transfer of streams of data to or from the main memory of a computing system. The mechanism may require set up the host software. After initialization, it automatically sequences the required data transfer and provides the necessary address information.

EPROM — Erasable Programmable Read Only Memory. An integrated circuit used to store the host adapter firmware and the host adapter BIOS.

FIFO — First In / First Out.

A queueing order in which items are removed from the queue for execution in the same order in which they are placed in the queue.

An integrated circuit that buffers data in such a manner that the each byte placed in the buffer is removed from the buffer in the same order.

Firmware — The software that controls and manages the host adapter. It is 'firm' as opposed to 'soft' because it is designed in to the host adapter and cannot be modified by the user.

IBM PC/AT Compatible — Any computer system that emulates exactly the IBM PC/AT and that uses an ISA backplane bus.

ISA — The Industry Standard Architecture

Industry Standard Architecture — The IBM PC/AT functions have been duplicated by a number of manufacturers. All the IBM PC/AT™ compatible machines use a backplane bus that very closely emulates the function of the backplane bus of the PC/AT™. Because of the broad usage of this bus structure, it has become known as the Industry Standard Architecture bus, even though there is no presently accepted standard for the bus.

initiator — A SCSI device that requests an operation to be performed by another SCSI device (the target). The initiator provides all the command information and parameters required to perform the operation, but the details of the operation are actually sequenced by the target.

host — A microcomputer in which a host adapter is installed. The host uses software to request the services of the host adapter in transferring information to and from peripheral devices attached to the SCSI bus connector of the host adapter.

host adapter — A hardware printed circuit board that installs in a standard microcomputer backplane and provides a SCSI bus connection so that SCSI devices can be connected to the microcomputer. A host adapter is "intelligent" if it has a simple high-level software interface to the microcomputer. A host adapter is "dumb" if the microcomputer must directly manage the SCSI protocol using the microcomputer processor.

Logical Unit — A physical or virtual device addressed through a target.

Logical Unit Number — An encoded three-bit identifier for a logical unit.

LU — See Logical Unit

LUN — See Logical Unit Number

Mailbox In — An area in main memory assigned by the host microcomputer software for communication with the host adapter. The host adapter places status and pointer information in entries in the Mailbox In (MBI) to indicate to the host microcomputer what operations have been completed or what information must be obtained from the host microcomputer.

Mailbox Out — An area in main memory assigned by the host microcomputer software for communication with the host adapter. The microcomputer software places commands and pointer information in entries in the Mailbox Out (MBO) to indicate what operations should be started by the host adapter.

MBI — See Mailbox In.

MBO — See Mailbox Out.

Multi-tasking Operation — The execution of commands in such a way that more than one command is in progress at the same time, allowing the system to take advantage of overlapping activities by using resources that are temporarily not required for other operations. More than one program or more than one portion of a program may be operating in parallel.

PC/AT — A family of small computers sold by IBM, also called the Personal Computer /AT family of computers. The name is trademarked by IBM.

RAM — Random Access Memory. Memory of which any byte can be accessed directly in a single memory cycle. Information can be read from and written to the memory.

SCSI — Small Computer System Interface.

SCSI ASC — SCSI Additional Sense Code. Byte 12 of the extended sense information. Provides a standardized description of the condition described by the sense information.

SCSI Device — A device attached to a Small Computer System Interface bus cable. The device may be an initiator, a target, or capable of both types of operation. The device may be a peripheral device, a host device, or a device mixing both roles.

Single Threaded Operation — Operation of the computing system such that only one program can be operating or active at a time. The computing system must wait until all resources are available before starting an operation and cannot start another operation until the first one is completed. No overlapping of latencies or program operation occurs.

Synchronous Data Transfer — A method of data transfer on the SCSI bus involving clocking data on to the bus with a fixed-length fixed-frequency strobe pulses. The acknowledgements may be delayed several clock periods from the data requests. Synchronous Data Transfer can be used only for data transmission on the SCSI bus. It is prohibited for command, message, and status transmission.

Synchronous Data Transfer Negotiation

The message exchange between the initiator and the target that allows the negotiation of the data transfer frequency and delay between requests and acknowledgements required for synchronous data transfer. Once negotiated, synchronous data transfer parameters remain unchanged until certain reinitialization activities occur.

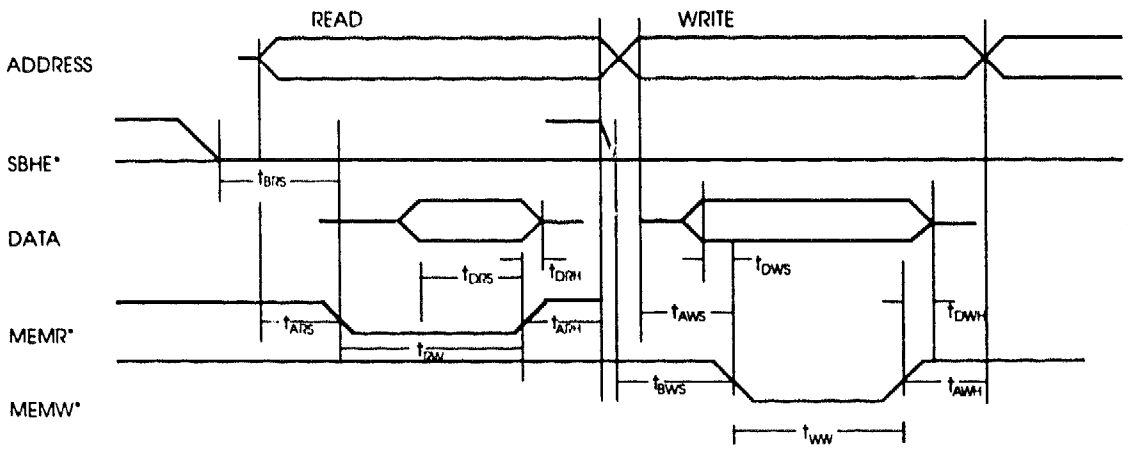
Target

A SCSI device that performs an operation requested by an initiator. The target may be a peripheral device performing a service for an initiator. The target may also be a host adapter performing a Processor type device service for an initiator.

Word

A two byte (16 bit) unit of data.

AHA-1540A/1542A MEMORY CYCLE TIMING



STANDARD SPEEDS	t_{RR} t_{WW}	TIMING
5.0 MB	250	A
5.7 MB	200	A
6.7 MB	200	A
8.0 MB	150	A
10.0 MB	100	B

SPEED	TIMING A	TIMING B
t_{ARS}	73	23
t_{ARH}	55	55
t_{BRS}	73	23
t_{DRS}	32	32
t_{DRH}	26	26
t_{AWS}	73	23
t_{AWH}	55	55
t_{BWS}	73	23
t_{DWS}	13	13
t_{DWH}	60	60

t_{ARS} Address Setup to MEMR Leading Edge
t_{ARH} Address Hold from MEMR Trailing Edge
t_{BRS} SBHE Setup to MEMR Leading Edge
t_{DRS} Data Setup to Trailing Edge of MEMR
t_{DRH} Data Hold from MEMR Trailing Edge
t_{RW} Read Pulsewidth

t_{AWS} Address Setup to MEMW Leading Edge
t_{AWH} Address Hold from MEMW Trailing Edge
t_{BWS} SBHE Setup to MEMW Leading Edge
t_{DWS} Data Setup to MEMW Leading Edge
t_{DWH} Data Hold from MEMW Trailing Edge
t_{WW} Write Pulsewidth

Note: I/O Channel Ready may slow the actual transfer rate

Appendix B

CONNECTOR PINOUT

Internal Connector Pin Assignments

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-DB(0)
Ground	3	4	-DB(1)
Ground	5	6	-DB(2)
Ground	7	8	-DB(3)
Ground	9	10	-DB(4)
Ground	11	12	-DB(5)
Ground	13	14	-DB(6)
Ground	15	16	-DB(7)
Ground	17	18	-DB(P)
Ground	19	20	Ground
Ground	21	22	Ground
Ground	23	24	Ground
Open	25	26	Term Power (Fused)
Ground	27	28	Ground
Ground	29	30	Ground
Ground	31	32	-ATN
Ground	33	34	Ground
Ground	35	36	-BSY
Ground	37	38	-ACK
Ground	39	40	-RST
Ground	41	42	-MSG
Ground	43	44	-SEL
Ground	45	46	-C/D
Ground	47	48	-REQ
Ground	49	50	-I/O

External Connector Pin Assignments

Signal Name	Pin	Pin	Signal Name
Ground	1	26	-DB(0)
Ground	2	27	-DB(1)
Ground	3	28	-DB(2)
Ground	4	29	-DB(3)
Ground	5	30	-DB(4)
Ground	6	31	-DB(5)
Ground	7	32	-DB(6)
Ground	8	33	-DB(7)
Ground	9	34	-DB(P)
Ground	10	35	Ground
Ground	11	36	Ground
Ground	12	37	Ground
Open	13	38	Term Power (Fused)
Ground	14	39	Ground
Ground	15	40	Ground
Ground	16	41	-ATN
Ground	17	42	Ground
Ground	18	43	-BSY
Ground	19	44	-ACK
Ground	20	45	-RST
Ground	21	46	-MSG
Ground	22	47	-SEL
Ground	23	48	-C/D
Ground	24	49	-REQ
Ground	25	50	-I/O

Appendix C AHA-1540/1640 FAMILY COMPATIBILITY INFORMATION

Brief summary of board characteristics:

AHA-1540:

High performance SCSI to ISA Bus Master host adapter. Most revisions support synchronous data transfer. Separate user's manual. Subset of AHA-154XA Adapter Commands available.

W AHA-1542A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Supports floppy disk drives. Higher level of host adapter integration.

AHA-1542A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Supports floppy disk drives. Higher level of host adapter integration. Improved SCSI connection pattern and jumper controls. Supports Target Mode operation.

AHA-1540A:

High performance SCSI to ISA Bus Master host adapter. Supports synchronous data transfer. Does not support floppy disk drives. Higher level of host adapter integration. Improved SCSI connection pattern and jumper controls. Supports Target Mode operation.

AHA-1640:

Very high-performance SCSI-to-Micro Channel Bus Master host adapter. Supports synchronous data transfer. Does not support floppy disk drives. High level of host adapter integration. Supports Target Mode Operation. See Adaptec's AHA-1640 User's Manual for details, including POS management, differences in interrupt presentation, differences in reset management and improvements in Adapter commands.

COMPATIBILITY CHART

Function	1540	W1542A	1542A	1540A	1640
Floppy Disk Controller	No	Yes	Yes	No	No
Synchronous Transfer	No	Yes	Yes	Yes	Yes
Selectable DMA Speeds	No	Yes	Yes	Yes	POS
Programmable DMA Speeds	Yes	Yes	Yes	Yes	Yes
Internal SCSI Connectors	Straight	Rt Angle	Rt Angle	Rt Angle	Straight
Scatter Gather	No	Yes	Yes	Yes	Yes
64 Head BIOS	Option	Yes	Yes	Yes	Yes
16 Head BIOS	Yes	No	No	No	No
LED Connector	No	Yes	Yes	Yes	Yes
Target Mode	No	No	Yes	Yes	Yes
LA 17-19 Jumper	Yes	Yes	No	No	NA
Micro Channel	No	No	No	No	Yes
PC/AT	Yes	Yes	Yes	Yes	No

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Quantum ProDrive Series™ Intelligent Disk Drives

ProDrive™ 40S/80S

Product Manual

Quantum Corporation
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PREFACE

Quantum reserves the right to make changes and/or improvements to its products without incurring any obligation to incorporate such changes or improvements in units previously sold or shipped.

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VDE certification granted per File No. 11342-3250-2003/A1A

WARRANTY

Quantum ***ProDrive*** disk drives are warranted against defects in material and workmanship for a period of two years from the date of shipment. The warranty includes parts and labor. This is a limited warranty; further details can be obtained from your Quantum sales representative. All requests for service should be directed to the Quantum service center in your area.

PATENTS

Product covered or licensed under the following U.S. Patents: 4,538,193; 4,593,194; 4,639,798; 4,647,769; 4,647,997; 4,661,696; 4,669,004; 4,703,176. Other patents pending.

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SECTION 1
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 GENERAL DESCRIPTION

The Quantum ***ProDrive Series***™ is a family of ten hard disk drives using non-removable 3 1/2-inch rigid disk platters as storage media. These drives feature formatted capacities ranging from 42 to 168 megabytes and a variety of interfaces. This manual covers the ***ProDrive***™40S and ***ProDrive*** 80S, which feature the industry-standard Small Computer System Interface (SCSI) host interface. The ***ProDrive*** 40S has 42 megabytes of formatted capacity on two disks with three movable heads; the ***ProDrive*** 80S has 84 megabytes of formatted capacity on three disks with six movable heads. These drives make optimum use of powerful SCSI commands to provide maximum system performance. Media defects and error recovery are efficiently managed within these products and can be fully transparent to the user. The ***ProDrive Series*** drives feature an innovative design using an integrated controller, minimum number of parts, and close control of product quality during manufacture. The result is low cost, high reliability products.

NOTE: Throughout this manual, ***ProDrive*** 40S/80S or ***ProDrive*** will refer to either the ***ProDrive*** 40S or the ***ProDrive*** 80S. ***ProDrive*** 40S and ***ProDrive*** 80S will be used to refer specifically to the 42 and 84 megabyte versions, respectively.

1.1.1 APPLICABLE DOCUMENTS

This document provides a general description of the ***ProDrive*** 40S/80S, including installation, principles of operation, interface command implementation, and maintenance. Additional information pertaining to the SCSI interface may be found in the ANSI X3.131-1986, Small Computer System Interface Specification Common Command Set, Rev 4B, (by an ANSC X3T9.2 working group).

1.2 SPECIFICATIONS

Key features of the ***ProDrive*** 40S/80S include:

- Formatted storage capacity of 42 or 84 megabytes
- Industry-standard (ANSI) SCSI host interface, CCS, Rev 4B
- Fully integrated SCSI controller
- Industry standard 3 1/2-inch form factor
- Data transfer rate of up to 2.0 megabytes/second asychronous, 4.0 megabytes/second synchronous
- Full disconnect/arbitrate/reconnect capability
- 64 KB look-ahead, programmable DisCache®
- 19 msec average access time
- 48 bit computer generated cyclic ECC (Error Correcting Code) with 11-bit burst correction capability
- Automatic retry for read disk errors
- Transparent defect mapping
- High-performance in-line defective sector skipping and reassignment of new defective sectors without need to reformat
- Buffer memory parity and SCSI bus parity
- Patented AIRLOCK® automatic shipping lock and dedicated landing zone
- Read/Write with 1:1 interleave operation
- Support for 512, 1024, and 2048 byte logical block sizes
- Multiple block data transfer up to 64K blocks

1.2.1 PHYSICAL SPECIFICATIONS

Environmental Limits

Ambient Temperature -	Non-Operating:	-40°F to 140°F (-40°C to 65°C) 42°F/hr (20°C/hr) gradient
	Operating:	39°F to 122°F (4°C to 50°C) 23°F/hr (10°C/hr) gradient
Ambient Relative Humidity -	Non-Operating:	5% to 95% without condensation Maximum wet bulb = 115°F (46°C)
	Operating:	8% to 85% without condensation Maximum wet bulb = 79°F (26°C)
Altitude (relative to sea level) -	Non-Operating: Operating:	-200 (-60M) to 40,000 ft. (12 km) -200 (-60M) to 10,000 ft. (3 km)

Mechanical Dimensions (Exclusive of Faceplate)

Height	=	1.625 in.	(41.3 mm)
Width	=	4.0 in.	(101.6 mm)
Depth	=	5.75 in.	(144.9 mm)
Weight	=	1.9 lb.	(0.88 kg)

Heat Dissipation

Average Power Consumption (idle):	8 Watts (27.3 BTU/Hr)
Typical Power Consumption (30% Seeking):	9 Watts (30.7 BTU/Hr)

Power consumption includes power dissipated by drive's SCSI bus terminators.

Shock and Vibration

Table 1-1 lists specified levels for shock and vibration applied to any of the three mutually perpendicular axes (the principal drive base axes). The term "operating" implies that the drive will be fully functional while being subjected to the shock or vibration level listed during operation. "Non-operating" implies that there will be no change in performance once the drive is powered up after being subjected to the listed shock or vibration in the powered-down (non-operating) condition.

TABLE 1-1 Vibration and Shock Specification

	Operating	Non-Operating
VIBRATION:		
5-500 Hz Sine Wave (Peak to Peak) 1 Oct/Min Sine Sweep	0.50 G	2.00 G
SHOCK:	10 G (1 soft error/shock)	
1/2 Sine Wave of 11 msec Duration (10 hits maximum)	(6 G No soft errors)	60 G

In addition, the ***ProDrive*** as packaged in the shipping container will withstand drops onto a concrete surface from 48 inches on all surfaces, six edges and three corners. It will withstand vibration applied to the container of 0.5 G, 5-100 Hz (0 to Peak) and 1.5 G, 100-500 Hz (0 to Peak).

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1.2.2 PERFORMANCE SPECIFICATIONS

Capacity

	ProDrive 40S	ProDrive 80S
Formatted capacity (MB) *	40	80
Number of 512 byte sectors	82,029	164,058

* One megabyte is defined as 2^{20} bytes

Data Transfer Rates

Buffer to SCSI Bus - Up to 2.0 Mbytes/second asynchronous, 4.0 Mybtes/seconds synchronous

Disk to Buffer - Up to 1.25 Mbytes/second in bursts

Seek Times/Miscellaneous Times

DESCRIPTION	TYPICAL NOMINAL CONDITION	MAXIMUM NOMINAL CONDITION	MAXIMUM WORST CASE CONDITION
Single Track Seek (msec)	6	7	7
Average Seek (msec)	19	21	23
1/3 Stroke Seek (msec)	30	23	25
Full Stroke Seek (msec)	35	40	45
Average Rotational Latency (msec)	8.3	8.3	8.3
Sequential Head Switch (msec)	3.0	3.0	3.0
Power Up Time (sec)	13	15	18

NOTES Quoted seek times include head settling time but do not include command overhead or latency time. Seek time is the time required for the actuator to seek and settle on track.

Seek times are measured by averaging 1000 seeks of the indicated length. Average seek time is the average of 1000 random seeks. In the rare occurrence of a seek error, any individual seek may take up to 5 seconds for recovery.

Sequential head switch time is the time required for the head to move from the end of the last sector on a track to the beginning of the next sequential sector, located on the next track, same cylinder. This time is fixed by the track skewing feature of the drive. (See Appendix B.)

Power-up time is the time from the supply voltages reach operating range to the time the drive is able to accept all commands.

Nominal conditions are defined as 25°C ambient temperature, nominal supply voltages, and no applied shock or vibration. Worst case conditions are defined as worst case extremes of temperature and supply voltages.

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Media Quality

The ***ProDrive*** features defect management, which eliminates the need to manually identify defects. Defect management is completely transparent to the user. See Appendix C for a detailed description of the ***ProDrive*** defect handling procedure and ECC (Error Correcting Code) capability.

Error Rates

Random Data Errors (2):	1 error per 10^{10} bits read (maximum)
Defect Data Errors (3):	1 error per 10^{12} bits read (maximum)
Unrecoverable Data Errors (4):	1 error per 10^{14} bits read (maximum)
Seek Errors (5):	1 error per 10^{6} seeks (maximum)

Error rates are defined by Quantum as follows:

1) A data error is one (1) sector read incorrectly. Data error rates are defined as average rates measured over at least 1000 different sectors under any of the specified operating conditions except applied shock or vibration.

2) Random errors are those which do not exhibit a repeating error pattern, i.e., the error does not occur twice in a row within a specified number of retry reads; the default is eight. (Retries are terminated once data is read correctly.) The sectors will not be automatically reallocated since the errors are probably not due to media defects. See Appendix C for information on defect handling.

3) Defect errors are those which exhibit a repeating error pattern, i.e., the error occurs twice in a row within eight retry reads, and cannot be read without error up to that point. Such errors are likely due to media defects. The sectors will be automatically reallocated if the Automatic Read Reallocation Enabled bit in page 1H and the Reallocate Uncorrectable Error Enabled bit in page 39H of the MODE SELECT command are set to 1. (The default is 0: automatic reallocation is not performed.) See Appendix C for a description of error correction options.

4) Unrecoverable errors are those whose final retry error pattern is uncorrectable using ECC; retry reads are terminated by either a repeating error pattern, or eight attempts without reading correctly.

5) A seek error is any seek in which the drive does not locate the desired cylinder, or any seek in which the drive must go through a full recalibration routine to locate the desired cylinder. A full recalibration takes approximately five seconds.

1.2.3 FUNCTIONAL SPECIFICATIONS

	ProDrive 40S	ProDrive 80S
Nom Rotational Speed (RPM)	3,662 ±0.3%	3,662 ±0.3%
Max Recording Density (bpi)	22,055	22,055
Max Flux Density (fci)	14,700	14,700
Track Density (tpi)	1,000	1,000
Data Cylinders	834	834
Data Tracks	2,502	5,004
R/W Heads	3	6
Disks	2	3
Encoding Scheme	RLL 2,7	RLL 2,7

1.2.4 RELIABILITY SPECIFICATIONS

MTBF:	50,000 POH typical usage
PM:	Not required
MTTR:	30 minutes
Start/Stop:	10,000 cycles

1.2.5 ACOUSTICS

Idle Mode: 45 dBa maximum at 1 foot in any direction

1.2.6 STANDARDS AND REGULATIONS

The ***ProDrive*** disk drives satisfy the following standards and regulations:

a) U.L.: Standard 478, Standard for Safety, Electronic Data Processing Units and Systems

b) CSA: Standard C22.2-154 Data Processing Equipment
SDA: Standard C22.2-143 Office Equipment

c) VDE: VDE 0806, (IEC 380), Standard for Office Appliances and Machines

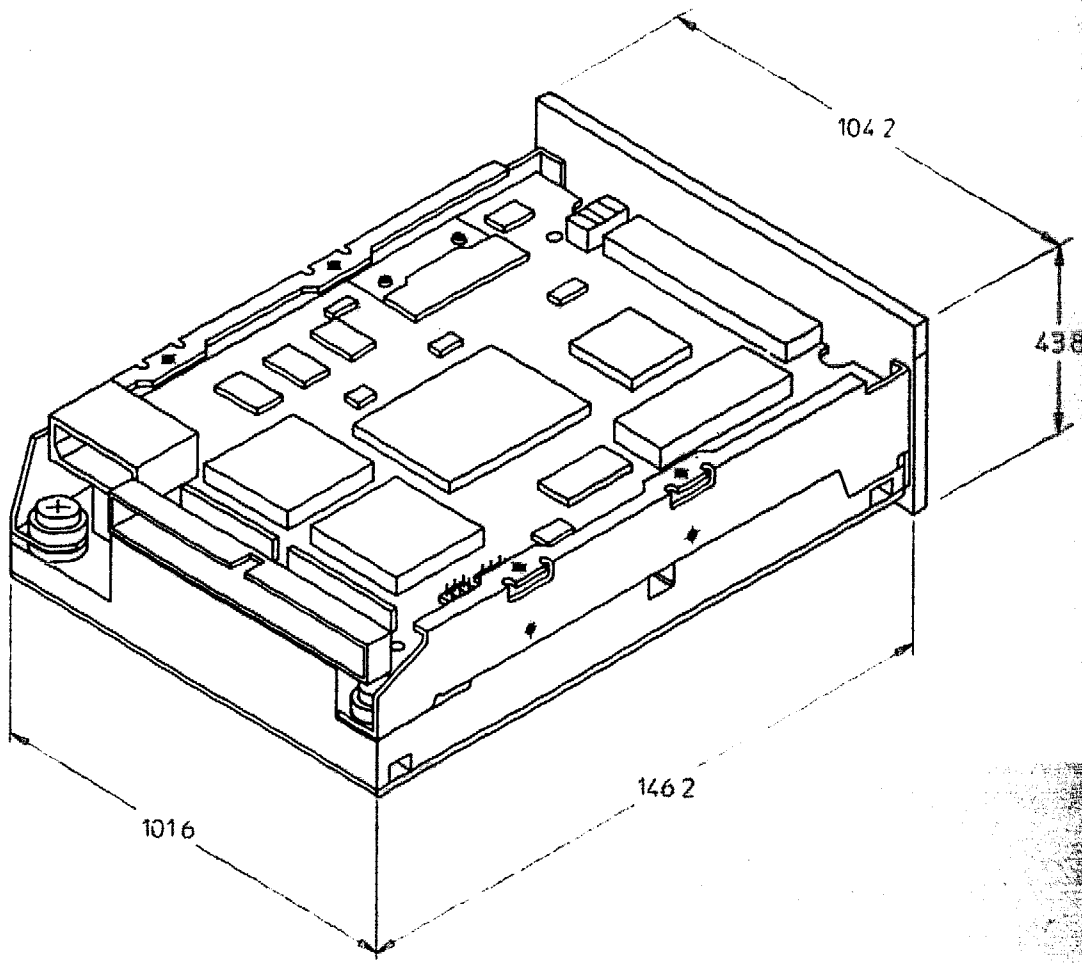
d) FCC: FCC Rules for Radiated and Conducted Emissions, Part 15, Sub Part J, For Class B Equipment

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2.1 INSTALLATION

2.1.1 SPACE REQUIREMENTS

The ***ProDrive*** disk drives are shipped with a faceplate installed and shock mounts mounted directly to the base casting. Figure 2-1 shows the external dimensions of the drives.



All dimensions in millimeters

FIGURE 2-1 ProDrive Mechanical Dimensions

2.1.2 UNPACKAGING INSTRUCTIONS

a) Open the shipping container.
b) Lift shipping container material and remove drive.

Figure 2-2 illustrates the 8-pack packing assembly for the ***ProDrive***. The list following the figure identifies each item.

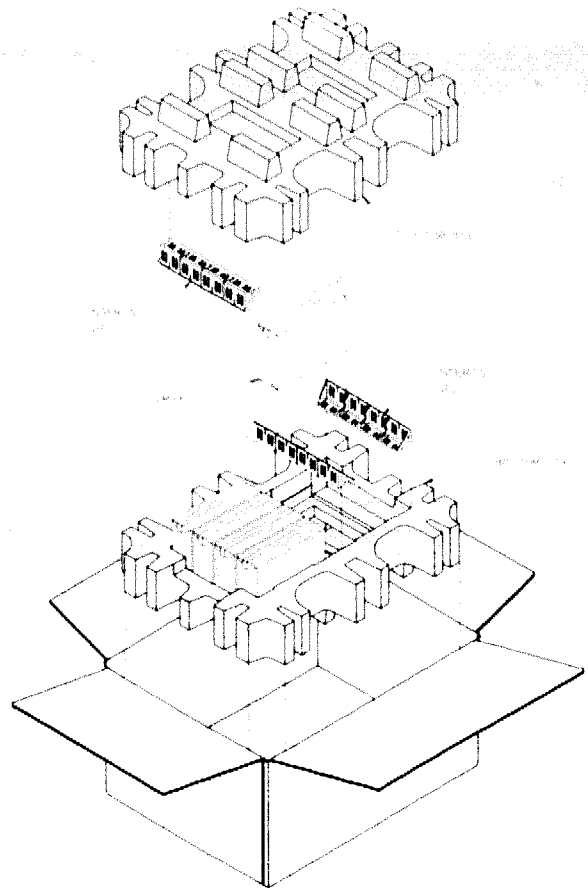


FIGURE 2-2 ProDrive Packing Assembly

Packing Assembly Item Description:

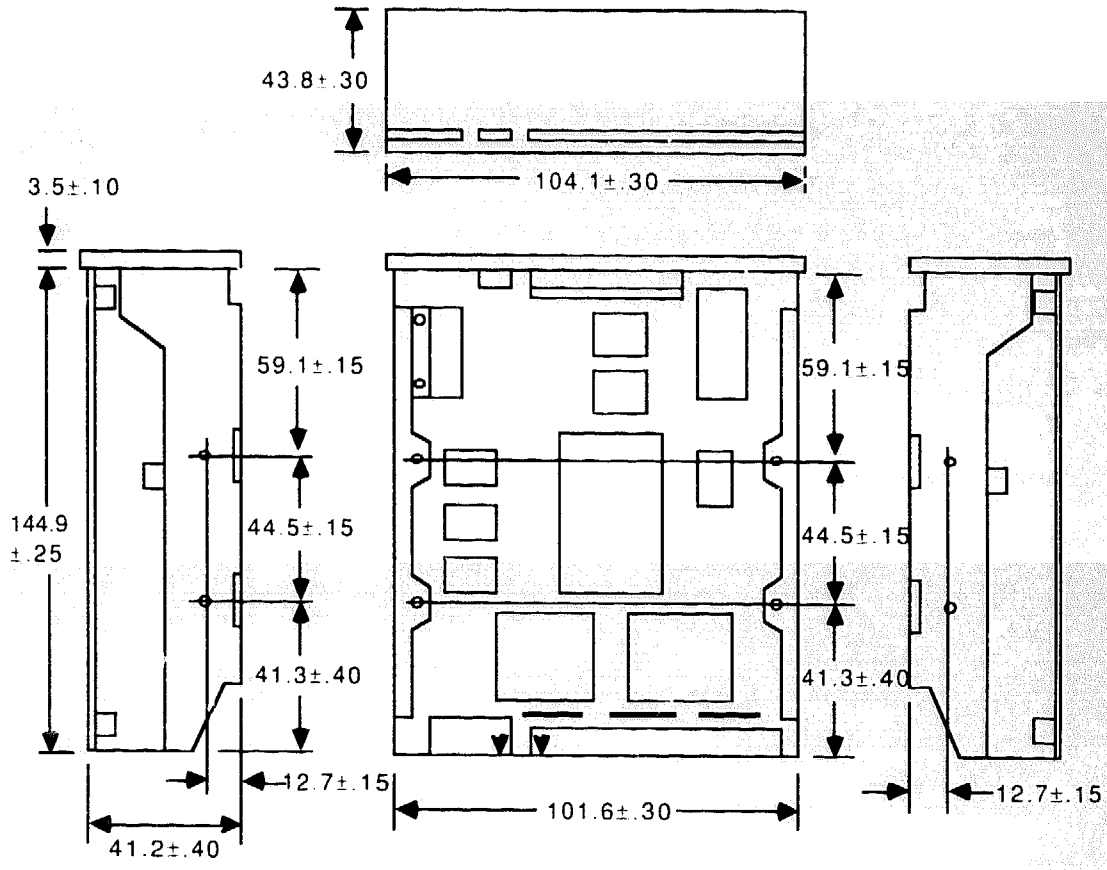
A. Shipping Container (8-pack)
B. Internal Padding
C. ***ProDrive*** Disk Drive
D. Package inserts

NOTES: After unpacking the disk drive(s), store the packing materials for possible future use.

The ESD bag is used to prevent electronic component damage during handling and shipment. You should ensure that your handling and shipping procedures will also preclude damage due to electrostatic discharge.

2.1.3 MOUNTING

The ***ProDrive*** may be mounted in any orientation. The mounting bracket with integral shock mounts is designed for this purpose. Figure 2-3 shows the location of the mounting bracket and the four mounting holes on each side of the bracket.



All dimensions in millimeters

FIGURE 2-3 ProDrive Mounting Dimensions

CAUTION:

The base casting is very close to the drive mounting bracket. Mounting screw lengths must be chosen so that no more than the specified length of screw thread protrudes through the mounting bracket holes. See Figure 2-4. This length will allow full use of the mounting hole threads and avoid damaging or placing unwanted stress on the base casting. To avoid stripping the mounting hole threads, the maximum torque applied to the mounting screws must not exceed 8 inch-pounds.

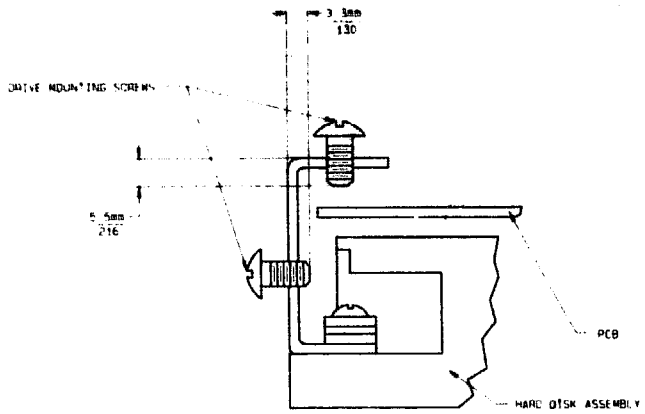


FIGURE 2-4 ProDrive Mounting Screw Clearance

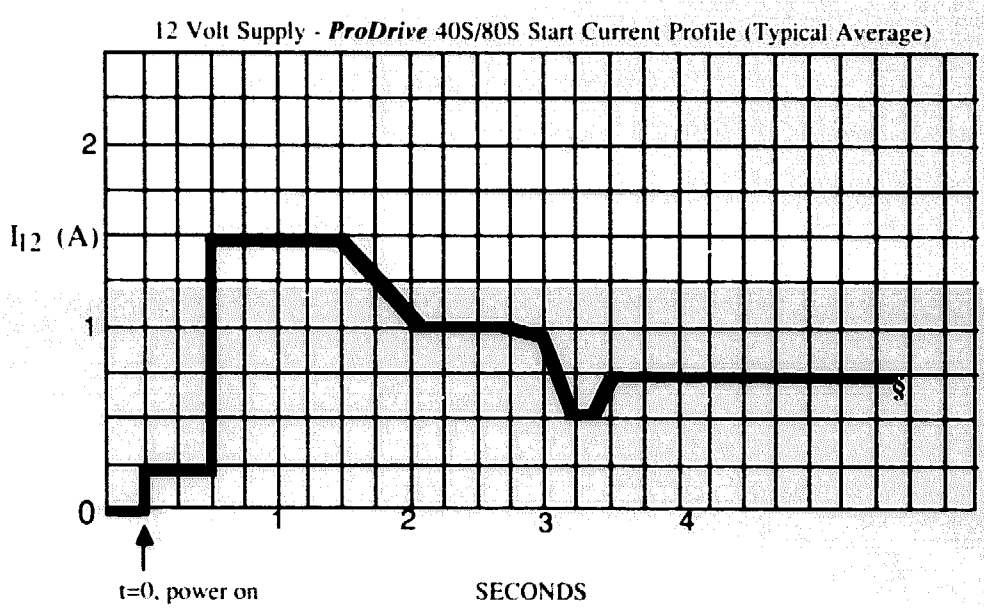
2.1.4 POWER REQUIREMENTS

DC Power

The voltages and current requirements of the DC Power supplied to the drive are listed below. No power sequencing either OFF or ON is required by the ***ProDrive***. Power requirements include SCSI terminator power.

Voltage	Nominal	+12V	+5V
	Tolerance	±10%	±5%
Current	Typical (Idle)	0.50A	0.50A
	Typical (Seeking)	0.80A	0.60A
	Maximum (Power Up)	1.60A	0.65A
Ripple and Noise	Maximum	100 mV P-P	50 mV P-P

Drive Startup Current Profile



Power Sequencing

No damage or loss of data will occur if power is applied or removed during drive operation, except that data may be lost in the sector being written at the time of power loss. In particular, the drive can sustain transient voltages +10% to -100% from nominal while powering up or down, as well as the shorting out or opening up of either voltage or return line.

Power Reset Limits

+5 Volts: 4.6 to 4.5 Volts
+12 Volts: 10.2 to 9.6 Volts

When powering up, the drive will remain reset (inactive) until both reset limits are exceeded. When powering down, the drive will become reset when either supply voltage drops below the lower threshold; hysteresis is 50 mV minimum.

2.2 VENTILATION

The ***ProDrive*** operates without a cooling fan provided the ambient air temperature does not exceed 122°F (50°C). Any user-designed cabinet should provide adequate air circulation so that this maximum air temperature is not exceeded.

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2.3 INTERCONNECTING CABLE CONNECTORS

2.3.1 DC POWER CONNECTOR

The DC power connector (J2) is a 4 pin DuPont Connector (SK 20055-000) mounted on the back edge of the PCB near the SCSI connector. See Figure 2-5. The recommended mating connector (P2) (AMP P/N 1-480424-0) utilizes AMP pins [P/N 350078-4 (strip) or P/N 61173-4 (loose piece)]. J2 pins are labeled on the J2 connector.

Pin 1 +12 volts DC
Pin 2 +12 volt return (ground)
Pin 3 +5 volt return (ground)
Pin 4 +5 volts DC

NOTE: Pins 2 and 3 are connected on the drive.



FIGURE 2-5 DC Power Connector (J2)

2.3.2 SCSI CONNECTOR

One SCSI cable connector (J1) is required for the ***ProDrive***. Details of the signals required can be found in Section 4 - SCSI Interface.

Connection to J1 is through a 50-pin Universal Header connector. A connector sketch is shown in Figure 2-6. A key slot is provided to prevent incorrect installation of the mating connector. The recommended mating connector for J1 is AMP receptacle P/N 1-499508-2 (with strain relief) or P/N 1-746195-2 (without strain relief), or equivalent.

NOTE: Unkeyed mating connectors should not be used due to the possibility of plugging the connector in backwards.

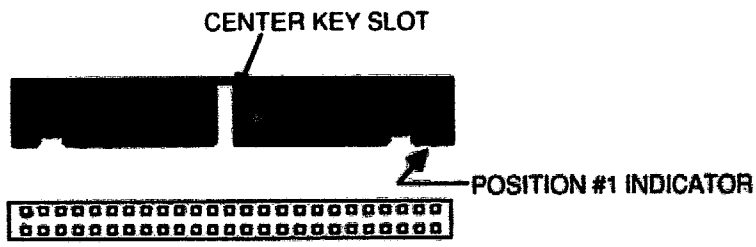


FIGURE 2-6 SCSI Connector (J1)

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2.4 OPERATION

2.4.1 GENERAL PROCEDURES

Configuration of a ***ProDrive*** disk drive varies depending on the system in which it is to be installed. This section describes the user-selectable hardware options that should be set prior to installation. Figure 2-7 identifies the location of shorting plugs and terminators on the Printed Circuit Board which control these options. In addition to the optional hardware configurations described below. ***ProDrive*** operation can also be affected by many optional features controlled by individual SCSI commands. See Section 5 for information about the SCSI commands.

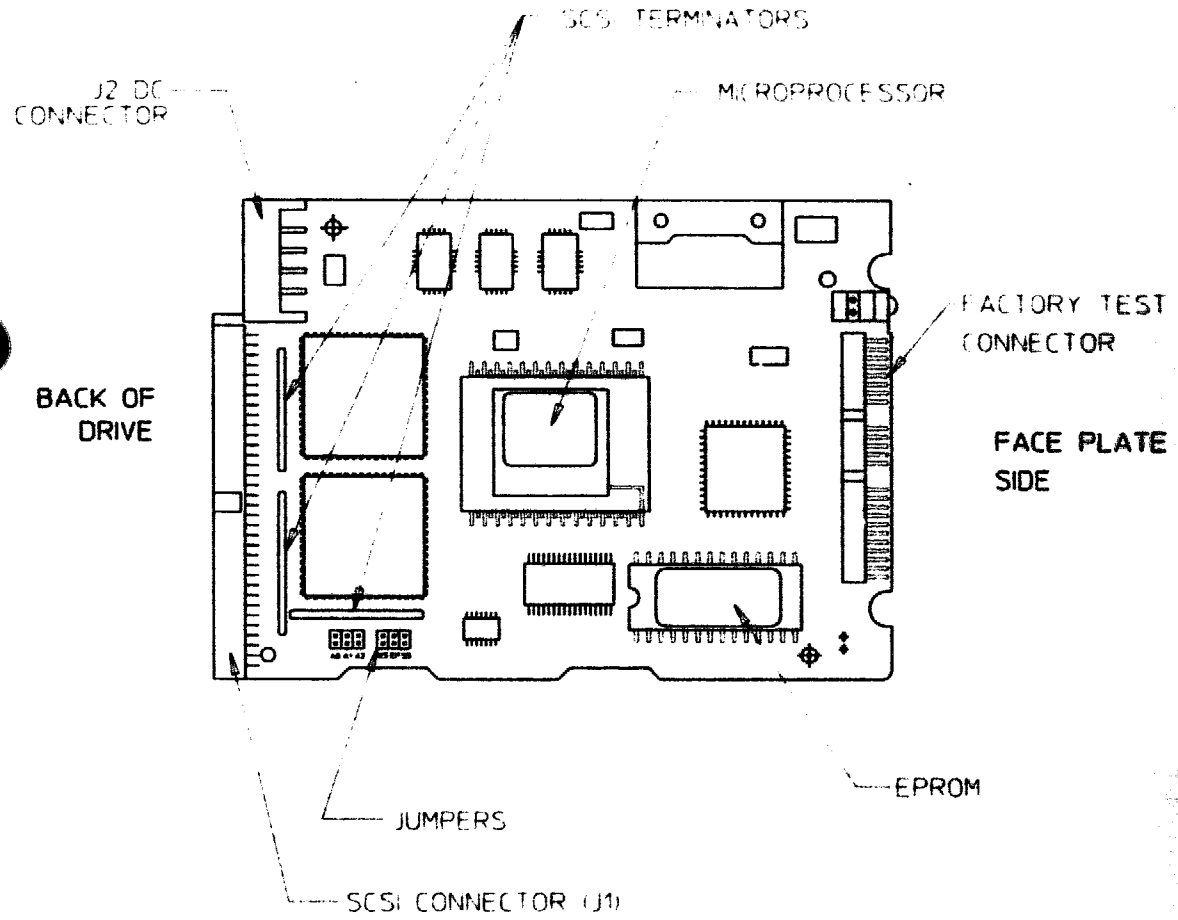


FIGURE 2-7 Shorting Plug/Terminator Locations on the PCB

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2.4.2 SELF SEEK TEST OPTION

The self seek test continuously exercises the actuator of the drive. When shorting plug option SS is installed, the drive will perform random seek patterns, verifying target IDs after every seek. The pattern will repeat as long as power is applied to the drive or until an error has occurred.

The ***ProDrive*** is sent from the factory with shorting plug SS not installed (Self Seek Test disabled).

2.4.3 ENABLE PARITY OPTION

Shorting plug EP controls the checking of parity across the SCSI bus. When this plug is installed, parity checking of data across the SCSI bus is enabled. With EP removed, parity checking is not performed, although parity is still generated.

The ***ProDrive*** is sent from the factory with shorting plug EP installed (Parity enabled).

2.4.4 WAIT SPIN OPTION

The WS shorting plug controls the Wait/Spin option. When this plug is installed, the motor will not spin upon power-up or reset until the host sends the START/STOP command across the SCSI bus. This permits power sequencing so that the system power supply will not be overloaded by many devices demanding peak start current at the same time. Once the START/STOP command is received, the drive will be ready within 15 seconds. When the WS shorting plug is not installed, the motor will automatically start spinning upon power-up or reset and be ready within 15 seconds.

The ***ProDrive*** is sent from the factory with the WS plug not installed (Wait/Spin option disabled).

2.4.5 SCSI BUS DEVICE IDENTIFICATION

The SCSI bus can support up to eight devices including the host system. The identity number determines the priority level of each device, so careful consideration must be taken in choosing the identity number of the ***ProDrive*** prior to installation.

Three shorting plugs (A2, A1 and A0) shown in Figure 2-7, are used for device identification. These plugs comprise a 3-bit binary number in which A2 is the most significant bit and A0 is the least significant. Installation represents a 1, meaning that with all shorting plugs installed the device identity is 7. With no shorting plugs installed, the device identity is 0.

The ***ProDrive*** is sent from the factory with plugs A2 and A1 installed (device 6).

2.4.6 FACEPLATE LED OPERATION

The green LED located on the ***ProDrive's*** faceplate illuminates when the drive is executing a command. It lights at the beginning of a command and does not go off until the command is completed or aborted. The LED remains on even when the drive is disconnected from the initiator during a command.

2.4.7 DRIVER TERMINATORS

The ***ProDrive*** contains three resistor networks, in sockets, to terminate the SCSI bus. The location of these terminators is shown in Figure 2-7. Section 3.2.2 of the manual describes the function of these terminators. It is important to note that only the first device (usually the host) and the last device on the SCSI bus should contain the terminators. When a ***ProDrive*** is used in a position on the bus other than the first or last, all three of the terminators must be removed.

The ***ProDrive*** is sent from the factory with the terminators installed.

3.1 *ProDrive* 40S/80S DRIVE MECHANISM

The drive mechanism consists of the mechanical subassemblies which are sealed under a metal cover. **These subassemblies are not adjustable nor are they field repairable**. Please refer to Figure 3-1.

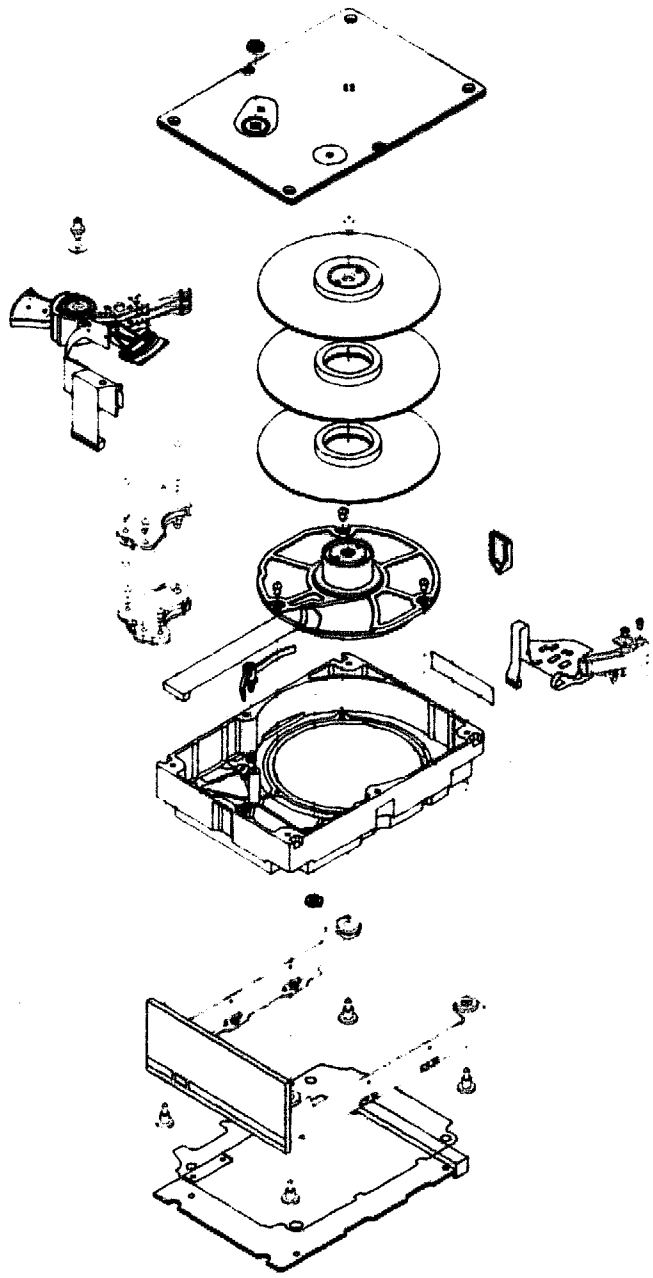


FIGURE 3-1 ProDrive Exploded View

3.1.1 BASE CASTING ASSEMBLY

The base casting is a single-piece cast aluminum alloy which provides a mounting surface for the rest of the drive mechanism. It has two machined holes for mounting the motor/spindle assembly and the positioner assembly. A gasket is mounted on the outside top edge to ensure a seal with the metal cover. Surfaces are provided for mounting the magnet plate assemblies for the rotary positioner assembly, and a read/write preamplifier. Mounting holes are provided outside the cover area, for the PCB and shock mount bracket assembly.

3.1.2 DISK STACK ASSEMBLY

The disk stack assembly is secured to the DC spindle motor which is bolted to the base casting. It consists of disks, disk spacers and a disk clamp. The DC motor assembly consists of a DC motor, spindle bearing assembly, disk mounting hub, and ferro-fluid magnetic seal. This seal prevents outside air from entering the drive through the bearing bore or along the bearing shaft. In the ***ProDrive*** 80S, three disks and two spacers are placed on the hub and clamped in place; the ***ProDrive*** 40S uses two disks and one spacer. The disks are an aluminum alloy with a thin film magnetic metal coating which is lubricated using a carbon overcoat. This overcoat prevents head and media wear when the heads are in contact with the disk surface, which only occurs outside the data area.

3.1.3 ROTARY POSITIONER ASSEMBLY (ACTUATOR)

The positioner used on the ***ProDrive*** is a Quantum proprietary design. It consists of the upper and lower magnet plates, a rotary single phase coil, a headstack mounting hub, and a bearing shaft. The magnets are composed of two alternating poles bonded to the magnet plates which in turn, are bolted to the base casting. The rotor and hub are molded together. The shaft is pressed into the base casting. Crash stops mounted to the magnet plate assembly prevent the heads from being driven into the spindle or off the disk surface.

3.1.4 HEADSTACK ASSEMBLY

The headstack assembly consists of the read/write heads, head arms, spacers, flex circuit, an optical scale, and the rotary positioner assembly. It is designed such that the mass center of the entire stack is at the center of the mounting hub. This is accomplished without the need for external counterbalances through a design in which the head arms, optical scale, and rotary positioner coil assembly balance each other. The heads are mini-composite slider type heads. They are mounted to Whitney-style spring steel flexures which are screwed to the head arms. The head conductors are flex cables routed through one flex circuit. A read preamplifier/write driver is mounted to this flex circuit.

3.1.5 OPTICAL ENCODER

The optical encoder assembly consists of a housing, an infared light-emitting diode (LED), a mirror, an optical reticle, a multi-cell photo diode matrix, and a flex circuit.

The infrared LED and the mirror are mounted in the upper portion of the housing. This allows the optical scale mounted with the headstack to move between the mirror-reflected light from the infared LED and the lower portion of the housing which contains the reticle and photo cells. The reticle masks the photo cells so that each cell only receives light through a specific portion of the movable scale. Both the clearance and angular position of the reticle and scale are precision adjustments made when the drive is manufactured.

3.1.6 AUTOMATIC ACTUATOR LOCK

The ***ProDrive*** uses a dedicated landing zone to ensure data integrity and prevent damage during shipment. It also uses AIRLOCK®, Quantum's patented means of locking the headstack in the landing zone. The AIRLOCK consists of an airvane mounted close to the edge of the disk stack with an arm that intersects the actuator to hold the headstack in the landing zone whenever the disk is not rotating. As DC power is applied to the motor and the disk stack starts rotating, an airflow is generated around the disk. As airflow increases with disk rotation, the airvane and its arm rotate, enabling the headstack to move freely out of the landing zone. When DC power is removed from the motor, an electronic return mechanism automatically pulls the actuator into the landing zone so the AIRLOCK can hold it in place.

3.1.7 AIR FILTRATION

The ***ProDrive*** Series drives are Winchester type drives and, as such, the heads fly very close to the media surface. The nominal flying height is 8 microinches - more than 2500 times smaller than the period at the end of this sentence.

It is absolutely essential that the air circulating within the drive be kept free of particles. To this end, the drive is assembled in a Class 100 purified air environment, then sealed with a metal cover. During the life of the drive, the rotating disks act as an air pump to force the air through an internal filter. Figure 3-2 shows the air flow in the enclosed area of the drive.

The lowest pressure area within the drive is at the top in the center of the spindle. A 0.3 micron breather filter is bonded in this area of the cover. This filter allows outside air into the sealed area of the drive to equalize internal and external pressures. The highest pressure area within the drive is located at the outer edge of the disk. Another 0.3 micron filter called the circulation filter is mounted to the base casting at this location. Air is pumped continuously into the side of the filter facing the rotating direction of the disks, is filtered, and exits from the side of the filter facing away from the rotating direction of the disks. Since this area of the drive is at a lower pressure than at the edge of the disks, air will circulate through the filter. This setup ensures a continuous flow of filtered air as soon as the disks start to rotate. Due to the stringent cleanliness required, the cover and seals should not be tampered with.

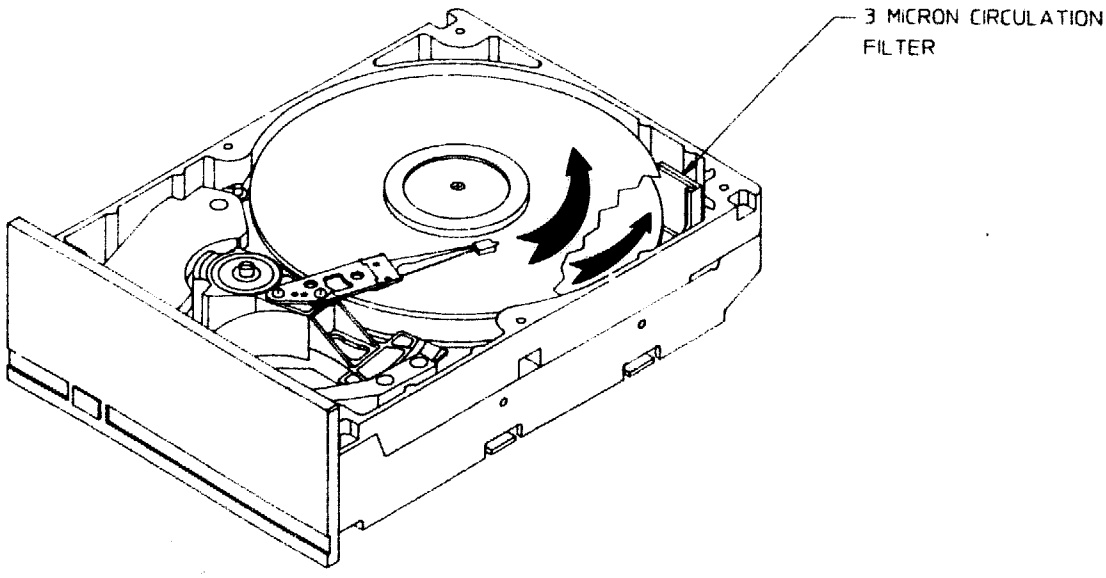
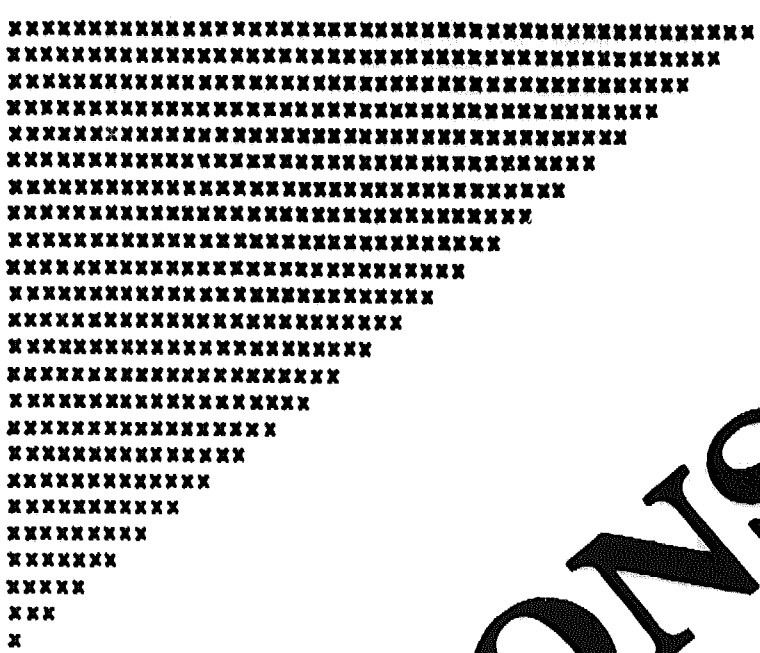
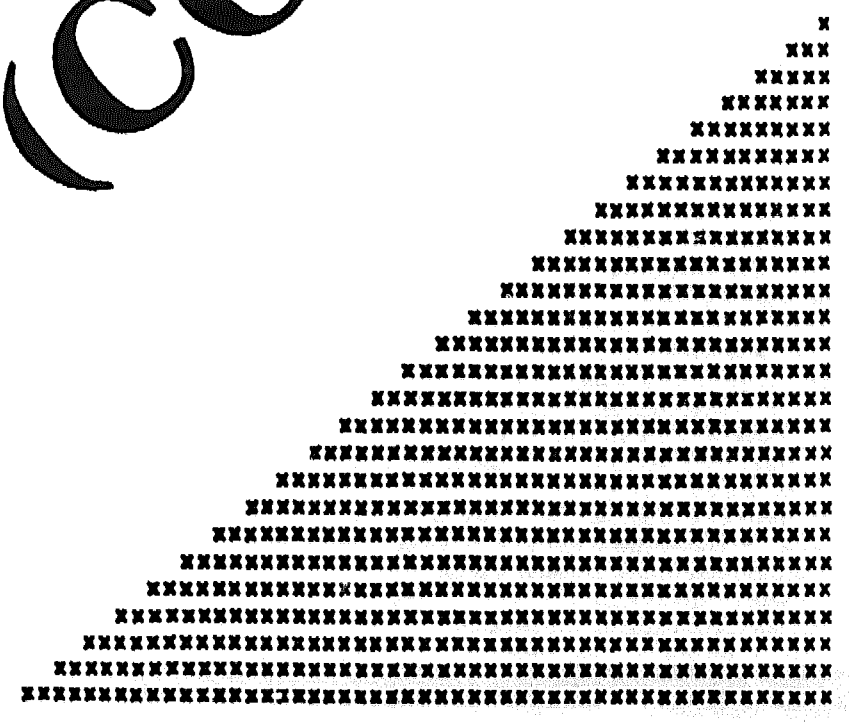


FIGURE 3-2 Air Filtration

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OPTIONS (CONT'D)



3.2 *ProDrive* 40S/80S DRIVE ELECTRONICS

3.2.1 GENERAL DESCRIPTION

All drive electronics, including SCSI controller functions, are contained on one Printed Circuit Board Assembly (PCBA). This is accomplished through advanced circuit design and the use of miniature surface-mounted devices and proprietary VLSI components. The only electrical components not contained on the PCBA are the preamplifier chip for the read/write circuitry, and the electronic circuitry for the optical encoder photocells and infared LED; these are located under the drive cover. The preamplifier is mounted as close to the read/write heads as possible to improve the signal-to-noise ratio. The following paragraphs provide operation details for major functional circuits within the drive.

3.2.2 HEAD POSITIONING SYSTEM

At power-on and at other predetermined times, wedge data on the inside and outside tracks is read by the read channel for each disk surface. This analog data is converted to a digital value by an on-chip A/D converter on the microcontroller. The controller uses these values to calculate the slope of the expected track position error line from outside to inside of each surface. These values are stored along with the current HDA internal temperature and a time mark. New values are read and the slope is recalculated whenever the temperature and/or time exceeds a predetermined value. When seeking, signals P1 and P2 from the optical encoder are used to determine track crossings. Once the actuator has positioned the head close to the desired track, the position error for that track is applied, and the head settles to the center of the proper track. Signals P1 and P2 are monitored and compared with a reference position to hold the head on track. Differences between the reference position and the position indicated by P1 and P2 will result in an output from the pulse width modulator. This signal is converted to an analog form and applied to the actuator driver, causing the actuator to move the head back onto the desired track centerline.

Figure 3-3 provides a block diagram of the head positioning electronics.

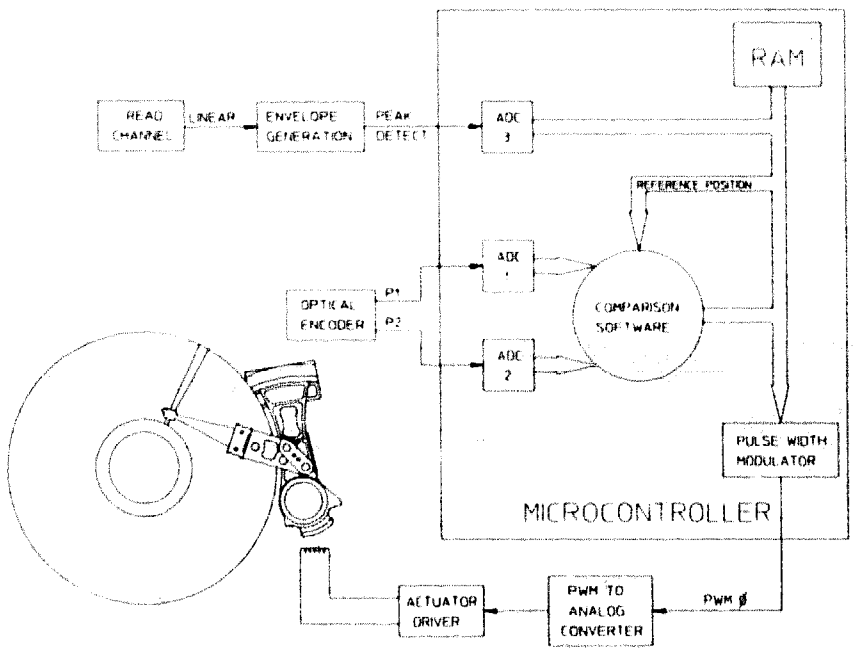


FIGURE 3-3 Head Positioning Electronics

3.2.3 READ/WRITE SYSTEM

The read channel path on the ***ProDrive*** begins at the heads as the magnetic flux transitions recorded on the disk pass under the heads causing a low amplitude output differential voltage. These signals pass from the head onto a flex circuit where a preamplifier/write driver IC is mounted to amplify the signal. Preamplification is done on the flex circuit at the point closest to the head to improve the signal to noise performance.

The flex circuit leaves the enclosed drive through a gap between the base casting and the cover, and connects with a mating header on the PCB. This gap is sealed by the cover gasket. Here the read signal is amplified further, filtered, and differentiated by the read data processor IC which outputs the signal READ DATA. This signal is fed to the data synchronizer/ENDEC IC which decodes the data into an NRZ data stream (NRZ), and a byte clock (BCLK). The IC also provides the signal address mark detected (AMD) if the data pattern read is the address mark pattern. These signals are fed to the data sequencer/DMA controller IC called SOLO. Once SOLO has identified the incoming data as belonging to the target sector(s) the data sequencer portion converts the NRZ serial bit stream into an 8 bit word. The DMA portion of SOLO then feeds this word to the cache/buffer RAM. The interface IC then outputs the data to the host with DMA control from SOLO.

Writing data is the reverse of reading in that data is presented at the interface IC and passed to SOLO as an 8-bit word. Data presented at a rate faster than can be written are temporarily stored in the cache/buffer RAM. In this way, data can be passed to the drive at a rate independent of the rate at which data can be written to the disk.

The data synchronizer/ENDEC IC provides SOLO with the signal address mark detect (AMD) and data to identify the target sector. Once SOLO detects the correct sector, it converts the data from an 8-bit word into a serial bit stream and passes this data and a clock to the data synchronizer/ENDEC IC. The data is then encoded into an RLL 2,7 bit stream and passed to the preamplifier/write driver IC via the write data line. The preamplifier/write driver IC receives the signal write gate from SOLO and writes the data to the disk.

Figure 3-4 provides a block diagram of the read/write electronics.

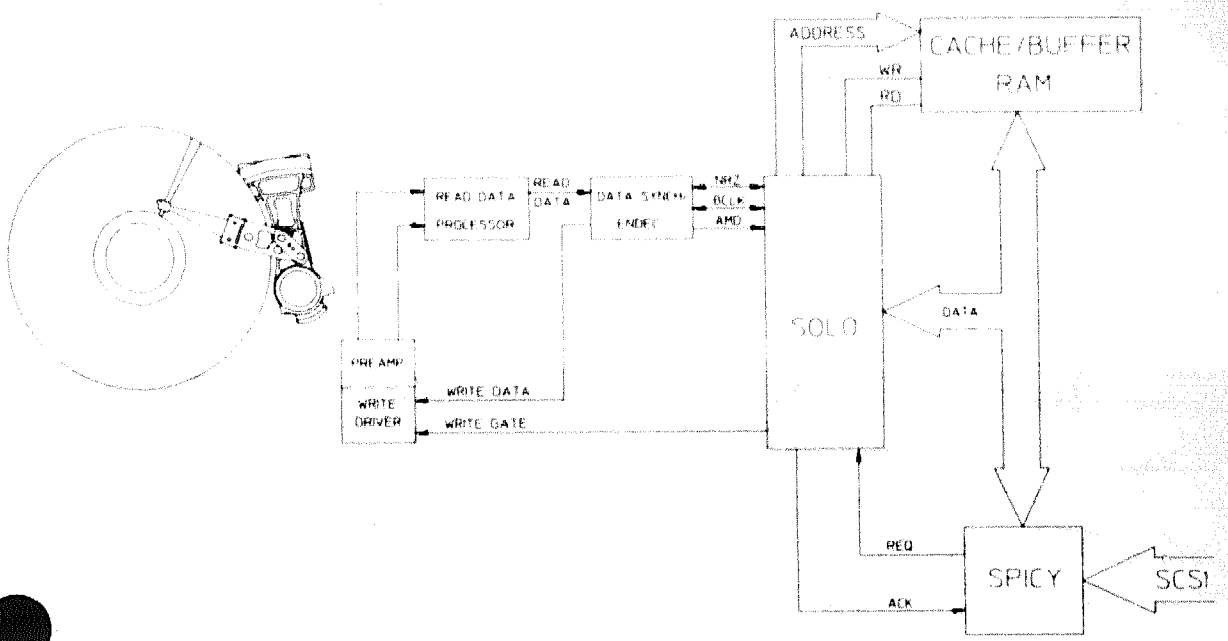


Figure 3-4 Read/Write Block Diagram

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3.2.4 Interface Control

The Small Computer System Interface (SCSI) logic is implemented using an SCSI controller chip called SPICY. This chip interfaces to the host system through the 50-pin SCSI connector (J1); and to drive electronics including the microprocessor's control lines and address/data bus, and the DMA controller/data sequencer (SOLO).

The controller chip is configured to operate under control of the microprocessor, which can send and receive information through the multiplexed address/data bus. An address is strobed into the SCSI controller chip on the falling edge of ALE (Address Latch Enable). Data is then strobed from or onto the bus by -RD (read status from the controller chip) or -WR (write to the controller chip) if the address selects the chip.

The microprocessor can also command SPICY to perform data transfer operations between the SCSI bus and the buffer RAM in synchronous or asynchronous mode. SPICY reads or writes data from/to the buffer RAM over nine lines (eight data lines and one parity line). The transfer is controlled by the DMA controller/data sequencer IC (SOLO) which handles addressing of the buffer RAM for SPICY. Data can be transferred between the buffer RAM and SPICY at up to 8.0 MBytes/second in SOLO page mode operations. This high DMA transfer rate allows SPICY to communicate over the SCSI bus at a synchronous data rate of 4.0 MBytes/second, while SOLO simultaneously controls disk-to-RAM transfers and RAM refresh operations.

4.1 INTRODUCTION

The ***ProDrive*** 40S and ***ProDrive*** 80S disk drives are "intelligent" disk drives in that they feature an integrated Small Computer System Interface (SCSI) controller. This section defines the functional requirements for interfacing with the ***ProDrive*** 40S/80S via the SCSI bus, including the command set, bus timing, and other parameters. The paragraphs below are intended to provide a brief description of this interface. Refer to Section 5 for more detailed information on the ***ProDrive*** 40S/80S programming requirements.

4.2 ANSI CONFORMANCE

4.2.1 Conformance Level and Alternatives

The ***ProDrive*** 40S and 80S conform to ANSI X3T9.2/82-2 Revision 17B at conformance level 2 with the following alternatives supported: single-ended drivers, terminator power, parity, hard reset, and reservation queuing. In addition, the synchronous data transfer option is implemented with a minimum transfer period of 250 nanoseconds and a maximum REQ/ACK offset of 8.

4.2.2 Hardware Implementation Choices

In many cases, the ANSI specification allows more than one option. When more than one option is allowed, and only one option was implemented, the decision as to which option to implement was based on the following:

- All SCSI bus drivers are OR-tied type drivers and do not actively drive any signals to the false state.
- During arbitration, if the ***ProDrive*** loses arbitration due to a higher priority SCSI ID bit being driven on the SCSI data bus, it will release its signals without waiting for SEL to become true.
- During arbitration phase, DB(P) will be undriven.

4.3 SCSI INTERFACE CHARACTERISTICS

4.3.1 GENERAL DESCRIPTION

The SCSI bus can support up to eight SCSI devices in any combination of initiators and targets. The ***ProDrive*** always assume a fixed role as a target.

Certain SCSI bus functions are assigned to the initiator or the target:

- The initiator may arbitrate for the SCSI bus and select a particular target.
- The target may request the transfer of COMMAND, DATA, STATUS, or other information on the DATA BUS, and in some cases it may arbitrate for the SCSI bus and reselect an initiator for the purpose of continuing an operation.

Communication with the ***ProDrive*** takes place on the SCSI DATA BUS in asynchronous or synchronous mode, using a defined REQ/ACK handshake protocol.

4.3.2 SCSI ELECTRICAL CHARACTERISTICS

All signals are low true and use open collector drivers terminated with 220 ohms to +5 volts (nominal) and 330 ohms to ground at each end of the cable. Resistor networks in sockets are provided on the ***ProDrive*** to terminate the lines.

NOTE: If multiple devices will be connected to the SCSI bus, terminators should be removed in all but the two devices at the cable ends. See Section 2.4 of this manual for the location of terminators on the drive.

Each signal driven by the ***ProDrive*** has the following output characteristics:

- True (Signal Assertion) = 0.0 to 0.5 Vdc at 48 mA (max)
- False (Signal Non-Assertion) = 2.5 to 5.25 Vdc

Each signal from the host to the ***ProDrive*** must have the following characteristics (measured at the drive):

- True (Signal Assertion) = 0.0 to 0.8 Vdc
- False (Signal Non-Assertion) = 2.5 to 5.25 Vdc

A 50-pin connector is provided at position J1 for connecting to the standard SCSI bus. The standard SCSI single-ended non-shielded connection is used. All signals are asserted at the low level. All odd pins are grounded. (An exception is Pin 25 which is not connected.) A maximum cable length of 20 ft. (6 meters) is allowed. Figure 4-1 shows the SCSI connection pins.

SCSI Pins

Ground	Signal	
1	2	Data Bit 0 (DB0)
3	4	Data Bit 1
5	6	Data Bit 2
7	8	Data Bit 3
9	10	Data Bit 4
11	12	Data Bit 5
13	14	Data Bit 6
15	16	Data Bit 7 (DB7)
17	18	Data Bit P (DBP)
19	20	Ground
21	22	Ground
23	24	Ground
25		Open
	26	Terminator Power
27	28	Ground
29	30	Ground
31	32	ATN
33	34	Ground
35	36	BSY
37	38	ACK
39	40	RST
41	42	MSG
43	44	SEL
45	46	C/D
47	48	REQ
49	50	I/O

FIGURE 4-1 SCSI Bus Pin Assignments

4.3.2.1 Terminator Power

ProDrive supplies terminator power through a schottky diode and a 1-Amp fuse with the following characteristics:

V_{TERM} = 4.25 VDC to 5.25 VDC
800 milliamps minimum source drive capability when supplying both sets of terminators
1.0 milliamp maximum sink capability, except for the purposes of providing power to an internal terminator
1.0 Amp current limiting (fuse)

4.3.3 BUS SIGNALS

There are a total of 18 SCSI bus signals. Nine are control signals and nine are used for data. (The parity signal option is included as a data signal.) Definitions of these signals are given below:

Control Signals:

BSY (BUSY) - An "OR-tied" signal that indicates that the bus is being used.

SEL (SELECT) - A signal used by an initiator to select a target or by a target to reselect an initiator.

C/D (CONTROL/DATA) - A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.

I/O (INPUT/OUTPUT) - A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.

MSG (MESSAGE) - A signal driven by a target during the MESSAGE phase.

REQ (REQUEST) - A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.

ACK (ACKNOWLEDGE) - A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.

ATN (ATTENTION) - A signal driven by an initiator to indicate the ATTENTION condition.

RST (RESET) - An "OR-tied" signal that indicates the RESET condition.

Data Signals:

DB(7-0,P) (DATA BUS) - Eight data-bit signals, plus a parity-bit signal that form a DATA BUS. DB(7) is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to DB(0). A data bit is defined as one when the signal value is true and zero when the signal value is false.

DB(P) is set to either zero or one so that data parity is odd. The use of parity is a system option, but parity generation and checking must be consistent for all SCSI devices on the bus: either all SCSI devices on the bus must generate and check parity, or all SCSI devices on the bus must not check parity. Parity is not valid during the ARBITRATION phase.

4.3.3.1 Signal Values

Signals may assume true or false values. If any driver is asserted, the signal is true. Whenever the term negated is used in this manual, it means that the signal is actively driven false.

4.3.3.2 OR-Tied Signals

The BSY and RST signals are OR-tied only. During ordinary operation of the bus, these signals are simultaneously driven true by several drivers. No signals other than BSY, RST, and DB(P) are simultaneously driven by two or more drivers, and any signal other than BSY and RST may employ OR-tied or non-OR-tied drivers. DB(P) shall not be driven false during the ARBITRATION phase. There is no operational problem in mixing OR-tied and non-OR-tied drivers on signals other than BSY and RST.

4.3.3.3 Signal Sources

Table 4-1 indicates which type of SCSI device may source each signal. No attempt is made to show if the source is driving asserted, driving negated, or is passive. All SCSI device drivers that are not active sources must be in the passive state. Note that the RST signal may be sourced by any SCSI device at any time.

TABLE 4-1 SIGNAL SOURCES

	Signal		C/D I/O MSG	ACK	
Bus Phase	**BSY**	**SEL**	**REQ**	**ATN**	**DB(7-0,P)**
BUS FREE	None	None	None	None	None
ARBITRATION	All	Winner	None	None	SCSI ID
SELECTION	I&T	Initiator	None	Initiator	Initiator
RESELECTION	I&T	Target	Target	Initiator	Target
COMMAND	Target	None	Target	Initiator	Initiator
DATA IN	Target	None	Target	Initiator	Target
DATA OUT	Target	None	Target	Initiator	Initiator
STATUS	Target	None	Target	Initiator	Target
MESSAGE IN	Target	None	Target	Initiator	Target
MESSAGE OUT	Target	None	Target	Initiator	Initiator

Notes for Table 4-1:

All: The signal is driven by all SCSI devices that are actively arbitrating.

SCSI ID: A unique data bit (the SCSI ID) is driven by any SCSI device that is actively arbitrating; the other seven data bits are released (not driven) by this SCSI device. The parity bit (DP(P)) may be undriven or driven to the true state, but must never be driven to the false state during the arbitration phase.

I&T: The signal is driven by the initiator, target, or both, as specified in the SELECTION phase and RESELECTION phase.

Initiator: If this signal is driven, it is driven only by the active initiator.

None: The signal must be released, i.e., not be driven by any SCSI device. The bias circuitry of the bus terminators pulls the signal to the false state.

Winner: The signal is driven by the SCSI device that wins arbitration.

Target: If the signal is driven, it is driven only by the active target.

4.3.4 SCSI BUS TIMING

Unless otherwise indicated, the delay-time measurements are at the drive's own SCSI bus connection. Thus, these measurements, except cable skew delay, can be made without considering delays in the cable.

ARBITRATION DELAY (2.4 microseconds) - The minimum time an SCSI device must wait from asserting **BSY** for arbitration until the DATA BUS can be examined to see if arbitration has been won. There is no maximum time.

ASSERTION PERIOD (90 nanoseconds) - The minimum time ***ProDrive*** will assert **REQ** during synchronous data transfers. Also, the minimum time an initiator will assert **ACK** during synchronous transfers.

BUS CLEAR DELAY (800 nanoseconds) - The maximum time for an SCSI device to stop driving all bus signals after:

1) The BUS FREE phase is detected (**BSY** and **SEL** both false for a *bus settle delay*)

2) **SEL** is received from another SCSI device during the ARBITRATION phase

3) The transition of **RST** to true.

NOTE For the first condition above, the maximum time for an SCSI device to clear the bus is 1200 nanoseconds from both **BSY** and **SEL** first becoming false. If an SCSI device requires more than a *bus settle delay* to detect BUS FREE phase, it must clear the bus within a *bus clear delay* minus the excess time.

BUS FREE DELAY (800 nanoseconds) - The minimum time that an SCSI device must wait from its detection of the BUS FREE phase (**BSY** and **SEL** both false for a *bus settle delay*) until its assertion of **BSY** when going to the ARBITRATION delay.

BUS SET DELAY (1.8 microseconds) - The maximum time before an SCSI device must assert **BSY** and its SCSI ID bit on the DATA BUS after it detects BUS FREE phase (**BSY** and **SEL** both false for a *bus settle delay*) for the purpose of entering the ARBITRATION phase.

BUS SETTLE DELAY (400 nanoseconds) - The time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

CABLE SKEW DELAY (10 nanoseconds) - The maximum difference in propagation time allowed between any two SCSI bus signals when measured between any two SCSI devices.

DATA RELEASE DELAY (400 nanoseconds) - The maximum time before an initiator must release the DATA BUS signals following the transition of the **I/O** signal from false to true.

DESKEW DELAY (45 nanoseconds) - The minimum time required for deskew of certain signals.

HOLD TIME (45 nanoseconds) - During synchronous data transfers, the minimum time added between the assertion of **REQ** or **ACK** and the changing of the data lines to provide hold time in the initiator or target, respectively.

NEGATION PERIOD (90 nanoseconds) - During synchronous data transfers, the minimum time the ***ProDrive*** will negate **REQ**, and the minimum time an initiator will negate **ACK**.

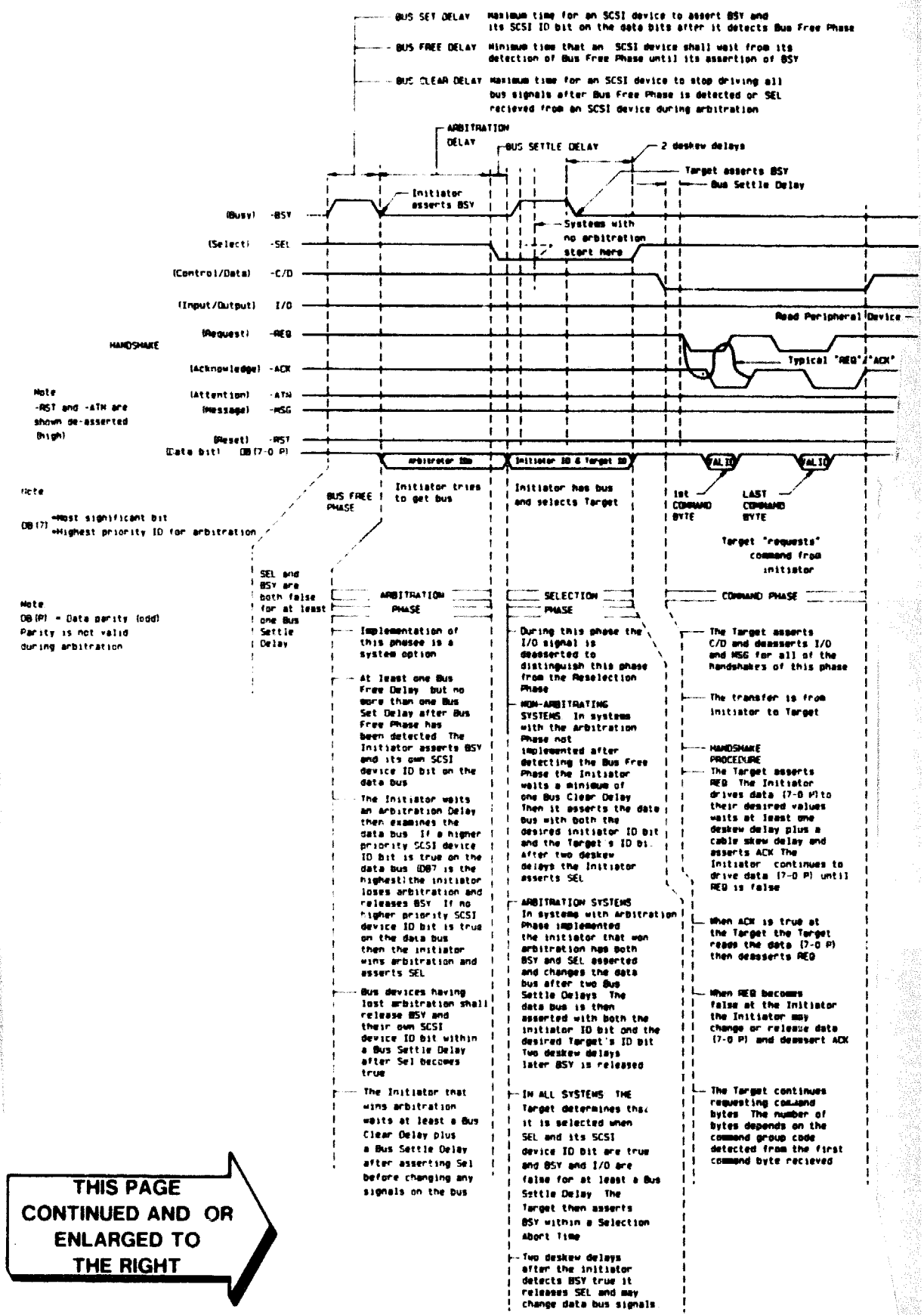
RESET HOLD TIME (25 microseconds) - The minimum time for which **RST** is asserted. There is no maximum time.

SELECTION ABORT TIME (200 microseconds) - The maximum time a target (or initiator) may take from its most recent detection of being selected (or reselected) until asserting a **BSY** response. This timeout is required to ensure that a target (or initiator) does not assert **BSY** after a SELECTION (or RESELECTION) phase has been aborted. This is not the selection timeout period.

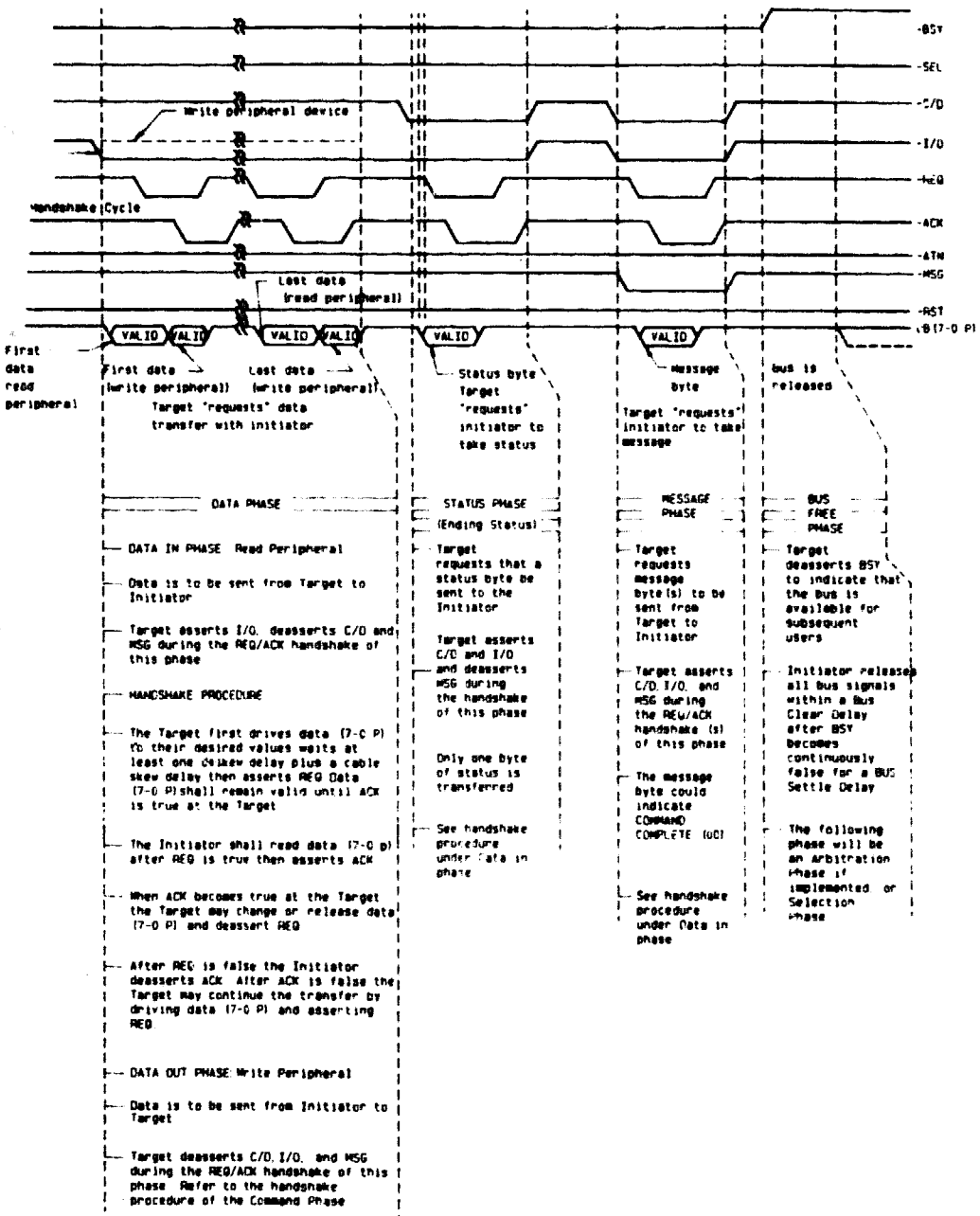
SELECTION TIMEOUT DELAY (250 milliseconds) - The minimum time that an initiator (or target) should wait for a **BSY** response during the SELECTION (or RESELECTION) phase before starting the timeout procedure.

Figure 4-2 provides an SCSI bus timing diagram.

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-BSY
-SEL
-C/D
-I/O
-REQ
-ACK
-ATN
-MSG
-RST
-DB(7-0 P)
Write peripheral device
Handshake Cycle
Last data (read peripheral)
VALID
VALID
VALID
VALID
VALID
VALID
First data read peripheral
First data → (write peripheral)
Last data → (write peripheral)
Target "requests" data transfer with initiator
Status byte Target "requests" initiator to take status
Message byte
Target "requests" initiator to take message
Bus is released
DATA PHASE
DATA IN PHASE Read Peripheral
Data is to be sent from Target to Initiator
Target deasserts I/O, deasserts C/D and MSG during the REQ/ACK handshake of this phase
HANDSHAKE PROCEDURE
The Target first drives data (7-0 P) to their desired values waits at least one deskew delay plus a cable skew delay then asserts REQ Data (7-0 P) shall remain valid until ACK is true at the Target
The Initiator shall read data (7-0 p) after REQ is true then asserts ACK
When ACK becomes true at the Target the Target may change or release data (7-0 P) and deassert REQ
After REQ is false the Initiator deasserts ACK After ACK is false the Target may continue the transfer by driving data (7-0 P) and asserting REQ
DATA OUT PHASE Write Peripheral
Data is to be sent from Initiator to Target
Target deasserts C/D, I/O, and MSG during the REQ/ACK handshake of this phase Refer to the handshake procedure of the Command Phase
STATUS PHASE (Ending Status)
Target requests that a status byte be sent to the Initiator
Target asserts C/D and I/O and deasserts MSG during the handshake of this phase
Only one byte of status is transferred
See handshake procedure under Data in phase
MESSAGE PHASE
Target requests message byte(s) to be sent from Target to Initiator
Target asserts C/D, I/O, and MSG during the REQ/ACK handshake (s) of this phase
The message byte could indicate COMMAND COMPLETE (00)
See handshake procedure under Data in phase
BUS FREE PHASE
Target deasserts BSY to indicate that the bus is available for subsequent users
Initiator releases all bus signals within a Bus Clear Delay after BSY becomes continuously false for a BUS Settle Delay
The following phase will be an Arbitration Phase if implemented or Selection Phase

4-7 (cont'd)

SECTION 5
SCSI PROGRAMMING GUIDELINES

5.1 GENERAL DESCRIPTION

This section explains the functional operation of the SCSI commands implemented on the ***ProDrive*** 40S and 80S disk drives. Details on ***DisCache***, track format, and defect management can be found at the end of this manual in Appendices A, B, and C, respectively.

5.2 SCSI BUS PHASES

The SCSI architecture includes eight distinct phases:

BUS FREE phase
ARBITRATION phase
SELECTION phase
RESELECTION phase
COMMAND phase \
DATA phase \ These phases are collectively termed the
STATUS phase / information transfer phases
MESSAGE phase /

The SCSI bus can never be in more than one phase at any given time. Unless otherwise noted in the following descriptions, signals that are not mentioned are not asserted.

5.2.1 BUS FREE PHASE

The BUS FREE phase is used to indicate that no SCSI device is actively using the SCSI bus and that it is available for subsequent users. SCSI devices must detect the BUS FREE phase after **SEL** and **BSY** are both false for at least a *bus settle delay*. All SCSI bus signals must be released by SCSI devices within a *bus clear delay* after **BSY** and **SEL** become continuously false for a *bus settle delay*. If a device requires more than a *bus settle delay* to detect the BUS FREE phase, it must release all SCSI bus signals within a *bus clear delay* minus the excess time to detect the BUS FREE phase. The total time to clear the SCSI bus must not exceed a *bus settle delay* plus a *bus clear delay*.

5.2.2 ARBITRATION PHASE

The ARBITRATION phase allows one SCSI device to gain control of the SCSI bus so it can assume the role of an initiator or target.

NOTE. Implementation of the ARBITRATION phase is a system option. Systems that do not implement this option can have only one initiator. The ARBITRATION phase is required for systems that use the RESELECTION phase.

The procedure the ***ProDrive*** uses to obtain control of the SCSI bus is as follows:

1) The ***ProDrive*** will first wait for the BUS FREE phase to occur. This phase is detected whenever both **BSY** and **SEL** are simultaneously and continuously false for a minimum of a *bus settle delay*.

2) It will then wait at least a *bus free delay* after detecting the BUS FREE phase (i.e., after **BSY** and **SEL** are both false for a *bus settle delay*) before driving any signal.

3) Following the *bus free delay* in Step 2, the ***ProDrive*** will arbitrate for the SCSI bus by asserting both **BSY** and its own **SCSI ID**; however, it will not start to arbitrate (i.e., assert **BSY** and its **SCSI ID**) if more than a *bus set delay* has passed since the BUS FREE phase was last observed.

4) After waiting at least an *arbitration delay* (measured from its assertion of **BSY**) the ***ProDrive*** will examine the DATA BUS. If a higher priority **SCSI ID** bit is true on the DATA BUS (DB(7) is the highest), the ***ProDrive*** has lost the arbitration and will release its signals and return to Step 1. If no higher priority **SCSI ID** bit is true on the DATA BUS, the ***ProDrive*** has won the arbitration and will assert **SEL**.

5) If the ***ProDrive*** wins arbitration, it will wait at least a *bus clear delay* plus a *bus settle delay* after asserting **SEL** before changing any signals.

NOTE The **SCSI ID** bit is a single bit on the DATA BUS that corresponds to the SCSI device's unique SCSI address. The other seven DATA BUS bits will be released by the ***ProDrive***. Parity is not valid during the ARBITRATION phase. During the ARBITRATION phase, DB(P) is undriven by the ***ProDrive***.

5.2.3 SELECTION PHASE

The SELECTION phase allows an initiator to select a target (***ProDrive***) for the purpose of initiating a target function such as a READ or WRITE command.

NOTE The **I/O** signal is undriven to distinguish this phase from the RESELECTION phase.

5.2.3.1 Non Arbitrating Systems

If the ARBITRATION phase is not implemented, the initiator must first detect the BUS FREE phase, then wait a minimum of a *bus clear delay*. Then, except in certain single initiator environments with initiators employing the single initiator option, the initiator must assert the desired target's **SCSI ID** and its own initiator **SCSI ID** (and the parity bit if parity checking is implemented) on the DATA BUS. After two *deskew delays*, the initiator must assert **SEL**. See Section 5.2.3.4 for a description of the single initiator option.

5.2.3.2 Arbitrating Systems

If the ARBITRATION phase is implemented, the device that won the arbitration has both **BSY** and **SEL** asserted and has delayed at least a *bus clear delay* plus a *bus settle delay* before ending the ARBITRATION phase. This device becomes an initiator by not asserting **I/O**. Except in certain single initiator environments with initiators employing the single initiator option, the initiator must assert the desired target's **SCSI ID** and its own initiator **SCSI ID** (and the parity bit if parity is implemented) on the DATA BUS. The initiator must then wait at least two *deskew delays* and release **BSY**, then wait at least a *bus settle delay* before looking for a response from the target.

5.2.3.3 All Systems

In all systems, the ***ProDrive*** will determine that it is selected when **SEL** and its **SCSI ID** bit are true and **BSY** and **I/O** are false for at least a *bus settle delay*. The ***ProDrive*** will examine the DATA BUS in order to determine the **SCSI ID** of the selecting initiator unless the initiator employed the single initiator option (5.2.3.4). The ***ProDrive*** will then assert **BSY** within a *selection abort time* of its most recent detection of being selected; this is required for correct operation of the timeout procedure. If parity is implemented, the ***ProDrive*** will not respond to a selection if bad parity is detected. Also, if more than two **SCSI ID** bits are on the DATA BUS, the ***ProDrive*** will not respond to selection.

At least two *deskew delays* after the initiator detects **BSY** is true, it must release **SEL** and may change the DATA BUS. The ***ProDrive*** will wait for the initiator to release **SEL** before setting an information phase.

5.2.3.4 Single Initiator Option

Initiators that do not implement the RESELECTION phase and do not operate in the multiple initiator environment may set only the target's **SCSI ID** bit and not their own **SCSI ID** bit during the SELECTION phase. This makes it impossible for the target to determine the initiator's **SCSI ID.**

5.2.3.5 Selection Timeout Procedure

Two selection timeout procedures are specified for clearing the SCSI bus if the initiator waits a minimum of a *selection timeout delay* and there has been no **BSY** response from the ***ProDrive***:

1) Optionally, the initiator may assert the **RST** signal. (See Section 5.3.2.)

2) Optionally, the initiator may continue asserting **SEL** and release the DATA BUS. If the initiator has not detected **BSY** to be true after at least a *selection abort time* plus two *deskew delays*, the initiator shall release **SEL**, allowing the SCSI bus to go to the BUS FREE phase. The ***ProDrive*** will only respond to a selection if the selection was still valid within a *selection time* of its assertion of **BSY**. This ensures that an improper selection does not result (two targets connected to the same initiator, wrong target connected to an initiator, or a target connected to no initiator).

5.2.4 RESELECTION PHASE

The RESELECTION phase allows a target to reconnect to an initiator to continue some operation that was previously started by the initiator but was suspended by the target (i.e., the target disconnected by allowing a BUS FREE phase to occur before the operation was complete).

5.2.4.1 Reselection

RESELECTION can only be used in systems that implement the ARBITRATION phase.

Following the ARBITRATION phase, the winning SCSI device has both **BSY** and **SEL** asserted and has delayed at least a *bus clear delay* plus a *bus settle delay*. The ***ProDrive*** becomes a target by asserting the **I/O** signal. It will also set the DATA BUS to a value that is the OR of its **SCSI ID** bit and the initiator's **SCSI ID** bit. The ***ProDrive*** will wait at least two *deskew delays* and release **BSY**, then will wait at least a *bus settle delay* before looking for a response from the initiator.

The initiator will determine that it is reselected when **SEL**, **I/O**, and its **SCSI ID** bit are true and **BSY** is false for at least a *bus settle delay*. The reselected initiator may examine the DATA BUS to determine the **SCSI ID** of the reselecting target. It must then assert **BSY** within a *selection abort time* of its most recent detection of being reselected; this is required for correct operation of the timeout procedure. If parity is implemented, the initiator must not respond to a RESELECTION if bad parity is detected. Also, it should not respond to a RESELECTION if more than two **SCSI ID** bits are on the DATA BUS.
After the ***ProDrive*** detects **BSY**, it will also assert **BSY** and wait at least two *deskew delays*, then release **SEL**. It may then change the **I/O** signal and the DATA BUS. After the reselected initiator detects **SEL** false, it must release **BSY**. The ***ProDrive*** will continue asserting **BSY** until it is ready to relinquish the SCSI bus.

5.2.4.2 Reselection Timeout Procedure

A RESELECTION timeout procedure is specified for clearing the SCSI bus during a RESELECTION phase if the target waits for a minimum of a *selection timeout* period and there has been no **BSY** response from the initiator:

The ***ProDrive*** will continue asserting **SEL** and **I/O** and will release all DATA BUS signals. If it does not detect **BSY** to be true after at least a *selection abort time* plus two *deskew delays*, it will release **SEL** and **I/O**, allowing the SCSI bus to go to the BUS FREE phase. When responding to RESELECTION, the

ProDrive will ensure that the RESELECTION was still valid within a *selection abort time* of its assertion of **BSY**. Otherwise, an improper reselection could result (two initiators connected to the same target or the wrong initiator connected to a target).

5.2.5 INFORMATION TRANSFER PHASES

The COMMAND, DATA, STATUS, and MESSAGE phases are grouped together as the information transfer phases because they are all used to transfer data or control information via the DATA BUS.

The **C/D**, **I/O**, and **MSG** signals are used to distinguish between the different information transfer phases. (See Table 5-1.) The target drives these three signals and, therefore, controls all changes from one phase to another. The initiator can request a MESSAGE OUT phase by asserting **ATN**, while the ***ProDrive*** can cause the BUS FREE phase by releasing **MSG**, **C/D**, **I/O**, and **BSY**.

TABLE 5-1 Information Transfer Phases

Signal					
MSG	**C/D**	**I/O**	**Phase Name**	**Direction of Transfer**	**Comment**
0	0	0	DATA OUT	Initiator to target	Data phase
0	0	1	DATA IN	Initiator from target	Data phase
0	1	0	COMMAND	Initiator to target	
0	1	1	STATUS	Initiator from target	
1	0	0	*		
1	0	1	*		
1	1	0	MESSAGE OUT	Initiator to target	Message phase
1	1	1	MESSAGE IN	Initiator from target	Message phase

Key: 0 = False, 1 = True, * = Reserved for future standardization

The information transfer phases use one or more **REQ**/**ACK** handshakes to control the information transfer. Each **REQ**/**ACK** handshake allows the transfer of one byte of information. During the information transfer phases, **BSY** must remain true and **SEL** must remain false. Additionally, during the information transfer phases, the ***ProDrive*** will continuously envelope the **REQ**/**ACK** handshake(s) with **C/D**, **I/O**, and **MSG** in such a manner that these control signals are valid for a *bus settle delay* before the assertion of **REQ** of the first handshake and remain valid until the negation of **ACK** at the end of the last handshake.

5.2.5.1 ASYNCHRONOUS TRANSFER

The ***ProDrive*** controls the direction of information transfer by means of the **I/O** signal. When **I/O** is true, information will be transferred from the ***ProDrive*** to the initiator. When **I/O** is false, information is transferred from the initiator to the ***ProDrive***.

If **I/O** is true (transfer to the initiator), the ***ProDrive*** will drive DB(7-0,P) to their desired values, delay at least one *deskew delay* plus a *cable skew delay*, then assert **REQ**. DB(7-0,P) will remain valid until **ACK** is true at the drive. The initiator should read DB(7-0,P) after **REQ** is true, then signal its acceptance of the data by asserting **ACK**. When **ACK** becomes true at the ***ProDrive***, the drive may change or release DB(7-0,P) and will release **REQ**. After **REQ** is false, the initiator should negate **ACK**. Once **ACK** is false, the ***ProDrive*** may continue the transfer by driving DB(7-0,P) and asserting **REQ**, as described above.

If **I/O** is false (transfer to the target) the ***ProDrive*** will request information by asserting **REQ**. The initiator should drive DB(7-0,P) to their desired values, delay at least one *deskew delay* plus a *cable skew delay*, then assert **ACK**. When **ACK** becomes true at the ***ProDrive***, the drive will read DB(7-0,P), then release **REQ**. When **REQ** becomes false at the initiator, the initiator may change or release DB(7-0,P) and must negate **ACK**. The target may continue the transfer by asserting **REQ**, as described above.

5.2.5.2 SYNCHRONOUS TRANSFER

Synchronous data transfer may be used in the data phase only if it was previously agreed to by the initiator and target via the message system. The messages determine the use of synchronous mode by the two SCSI devices, establishing a REQ/ACK offset and transfer period. See the Synchronous Data Transfer Request message (Section 5.6.2).

The REQ/ACK offset specifies the maximum number of **REQ** pulses that can be sent by the target before corresponding **ACK** pulses are received from the initiator. This establishes a pacing mechanism. If the number of **REQ** pulses sent exceeds the number of **ACK** pulses received by the **REQ/ACK** offset, the ***ProDrive*** will not assert **REQ** again until it receives the next **ACK** pulse. The number of **ACK** and **REQ** pulses must be equal for the data phase to be successfully completed.

The ***ProDrive*** will assert **REQ** for at least an assertion period. Before asserting **REQ**, it will wait at least a transfer period from the last transition of **REQ** to true, and a minimum of a negation period from the last transition of **REQ** to false.

The initiator must send one pulse on the **ACK** signal for each **REQ** signal received. The **ACK** signal must be asserted for at least an assertion period. Before asserting the **ACK** signal, the initiator must wait at least a transfer period from the last transition of **ACK** to true and a negation period from the last transition of **ACK** to false.

If **I/O** is true, (transfer to the initiator), the ***ProDrive*** will first drive DB(7-0,P) to the appropriate values, wait at least one deskew delay plus a cable skew delay, then assert **REQ**. DB(7-0,P) will be held valid for at least one deskew delay plus one cable skew delay, plus one hold time after the assertion of **REQ**. The ***ProDrive*** will assert **REQ** for at least an assertion period. It may then release **REQ** and change or release DB(7-0,P). The initiator must read the value on DB(7-0,P) within one hold time of the transition of **REQ** to true. It must then respond with an **ACK** pulse.

If **I/O** is false, (transfer to the ***ProDrive***), the initiator must transfer one byte for each **REQ** pulse received. After receiving a **REQ** pulse, the initiator must first drive DB(7-0,P) to the appropriate values, delay at least one deskew delay plus one cable skew delay, then assert **ACK**. DB(7-0,P) must be valid for at least one deskew delay plus one cable skew delay plus one hold time after the assertion of **ACK**. **ACK** must be asserted for a minimum of an assertion period. At that point, the initiator may negate **ACK** and may change or release DB(7-0,P). The ***ProDrive*** will read the value of DB(7-0,P) within one hold time of the transition of **ACK** to true.

5.2.6 COMMAND PHASE

The COMMAND phase allows the target to request command information from the initiator. The ***ProDrive*** will assert the **C/D** signal and negate **I/O** and **MSG** during the **REQ/ACK** handshake(s) of this phase.

5.2.7 DATA PHASE

The data phase encompasses both the DATA IN and the DATA OUT phases.

5.2.7.1 DATA IN PHASE

The DATA IN phase allows the target to request that data be sent to the initiator from the target. The ***ProDrive*** will assert the **I/O** signal and negate **C/D** and **MSG** during the **REQ/ACK** handshake(s) of this phase.

5.2.7.2 DATA OUT PHASE

The DATA OUT phase allows the target to request that data be sent from the initiator to the target. The ***ProDrive*** will negate the **C/D**, **I/O**, and **MSG** signals during the **REQ/ACK** handshake(s) of this phase.

5.2.8 STATUS PHASE

The STATUS phase allows the target to request that status information be sent from the target to the initiator. The ***ProDrive*** will assert **C/D** and **I/O** and negate the **MSG** signal during the **REQ/ACK** handshake of this phase.

5.2.9 MESSAGE PHASE

The message phase refers to both the MESSAGE IN and MESSAGE OUT phases. The first byte transferred in either of these phases must be a single-byte message or the first byte of a multiple-byte message. Multiple-byte messages must be wholly contained within a single message phase.

5.2.9.1 MESSAGE IN Phase

The MESSAGE IN phase allows the target to request that messages be sent to the initiator from the target. The ***ProDrive*** will assert **C/D**, **I/O**, and **MSG** during the **REQ/ACK** handshake(s) of this phase.

5.2.9.2 MESSAGE OUT Phase

The MESSAGE OUT phase allows the target to request that a message be sent from the initiator to the target. The ***ProDrive*** will invoke this phase at its convenience in response to the ATTENTION condition created by the initiator. (See Section 5.3.1 for a description of the ATTENTION condition.)

The ***ProDrive*** will assert **C/D** and **MSG** and negate **I/O** during the **REQ/ACK** handshake(s) of this phase. It will handshake byte(s) in this phase until **ATN** goes false.

If the ***ProDrive*** receives all the message byte(s) successfully (i.e., no parity errors), it will change to any information transfer phase other than the MESSAGE OUT phase and transfer at least one byte. The ***ProDrive*** may also indicate that it has successfully received the message byte(s) by changing to the BUS FREE phase (e.g., ABORT or BUS DEVICE RESET messages).

5.2.10 SIGNAL RESTRICTIONS BETWEEN PHASES

When the SCSI bus is between two information transfer phases, the following restrictions apply to the SCSI bus signals:

1) The **BSY**, **SEL**, **REQ**, and **ACK** signals must not change.

2) The **C/D**, **I/O**, **MSG**, and **DATA BUS** signals may change. When switching the **DATA BUS** direction from out to in (target to initiator), the ***ProDrive*** will delay driving the **DATA BUS** by at least a *data release delay* plus a *bus settle delay* after asserting the **I/O** signal, and the initiator must release the **DATA BUS** no later than a *data release delay* after the transition of the **I/O** signal to true. When switching the **DATA BUS** direction from in to out (initiator to target), the ***ProDrive*** will release the **DATA BUS** no later than a *deskew delay* after negating **I/O**.

3) The **ATN** and **RST** signals may change as defined under the descriptions for the ATTENTION condition (5.3.1) and RESET condition (5.3.2).

5.3 SCSI BUS CONDITIONS

The SCSI bus has two asychronous conditions: the ATTENTION condition and the RESET condition. These conditions cause a SCSI device to perform certain actions and can alter the phase sequence.

5.3.1 ATTENTION CONDITION

The ATTENTION condition allows an initiator to inform a target that the initiator has a message ready. The target may get this message at its convenience by performing a MESSAGE OUT phase.

- The initiator creates the ATTENTION condition by asserting **ATN** at any time except during the ARBITRATION or BUS FREE phases.
- The ***ProDrive*** may respond with the MESSAGE OUT phase.

The initiator must keep **ATN** asserted if more than one byte is to be transferred. The initiator may negate the **ATN** signal at any time except while the **ACK** signal is asserted during a MESSAGE OUT phase. Normally, the initiator negates **ATN** while **REQ** is true and **ACK** is false during the last **REQ/ACK** handshake of the MESSAGE OUT phase.

5.3.2 RESET CONDITION

The RESET condition is used to immediately clear all SCSI devices from the bus. This condition takes precedence over all other phases and conditions. SCSI devices create the RESET condition by asserting **REQ** for a minimum of a reset hold time. During the RESET condition, the state of all SCSI bus signals other than **RST** is not defined.

NOTE The ***ProDrive*** will never assert **RST**, but it will respond to a **RST** asserted by another SCSI device.

When RST is asserted, the ***ProDrive*** will release all SCSI bus signals (except **RST**) within a bus clear delay of the transition of **RST** to true. The BUS FREE phase always follows the RESET condition.

5.4 SCSI BUS PHASE SEQUENCES

Phases are used on the SCSI bus in a prescribed sequence. In all systems, the RESET condition can abort any phase and is always followed by the BUS FREE phase. Also, any other phase can be followed by the BUS FREE phase.

5.4.1 NON-ARBITRATING SYSTEMS

In systems which do not use the ARBITRATION phase, the BUS FREE phase is followed by the SELECTION phase, then one or more of the information transfer phases (COMMAND, DATA, STATUS, or MESSAGE). See Figure 5-1.

5.4.2 ARBITRATING SYSTEMS

In systems which use the ARBITRATION phase, the BUS FREE phase is followed by ARBITRATION, then SELECTION or RESELECTION, then one or more of the information transfer phases (COMMAND, DATA, STATUS, or MESSAGE). See Figure 5-2.

5.4.3 ALL SYSTEMS

There are no restrictions on the sequences of information transfer phases. A phase type may even be followed by the same phase type: for example, a data phase may be followed by another data phase.

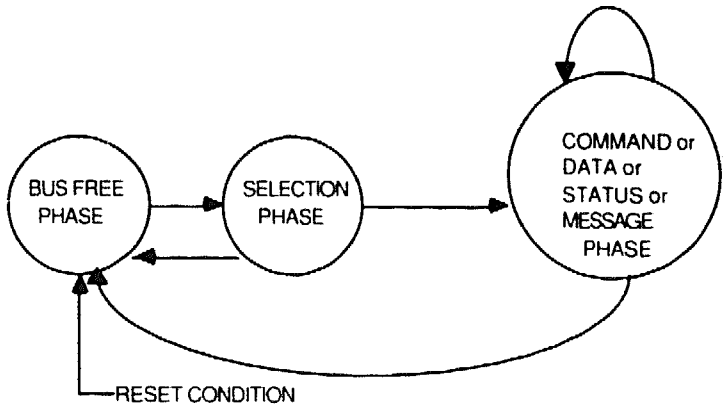


FIGURE 5-1 Phase Sequences without Arbitration

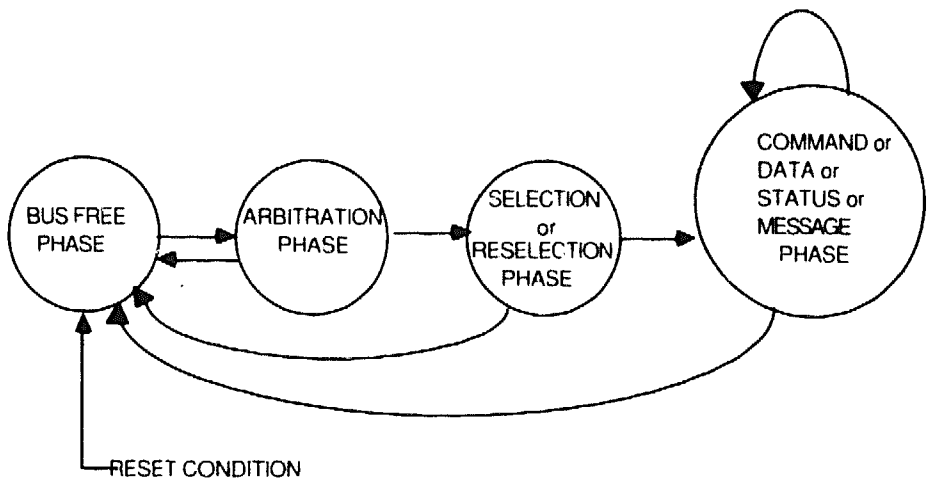


Figure 5-2 Phase Sequences With Arbitration

5.5 SCSI POINTERS

Consider the system shown in Figure 5-3 in which an initiator and target communicate on the SCSI bus to execute a command.

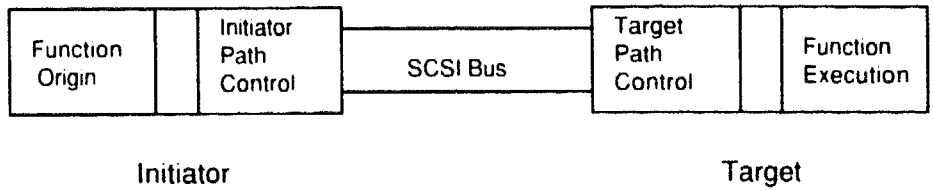


FIGURE 5-3 Simplified SCSI System

The SCSI architecture provides for two sets of three pointers within each initiator. The pointers reside in the initiator path control. The first set of pointers are the current (or active) pointers. These pointers are used to represent the state of the interface and point to the next command, data, or status byte to be transferred between the initiator's memory and the target. There is only one set of current pointers in each initiator. The current pointers are used by the target currently connected to the initiator.

The second set of pointers are the saved pointers. There is one set of saved pointers for each command that is currently active (whether or not it is currently connected). The saved command pointer always points to the start of the command descriptor block for the current command. (See Section 5.7.1.) The saved status pointer always points to the start of the status area for the current command. At the beginning of each command, the saved data pointer points to the start of the data area. It remains at this value until the target sends a SAVE DATA POINTER message (5.6.2) to the initiator. In response to this message, the initiator stores the value of the current data pointer into the saved data pointer. The target may restore the current pointers to their saved values by sending a RESTORE POINTERS message (5.6.2) to the initiator. The initiator moves the saved value of each pointer into the corresponding current pointer. Whenever a device disconnects from the SCSI bus, only the saved pointer values are retained. The current pointer values are restored from the saved values upon the next reconnection.

NOTE On a READ, if the ***ProDrive*** disconnects before any data is transferred, the SAVE DATA POINTER message is not issued. Similarly, on a WRITE, if the drive disconnects after all data have been transferred, the SAVE DATA POINTER message is not issued.

5.6 MESSAGE SYSTEM SPECIFICATION

The message system allows communication between an initiator and target for the purpose of physical data path management.

5.6.1 MESSAGE PROTOCOL

The ***ProDrive*** requires any SCSI device it communicates with to be able to receive and understand the COMMAND COMPLETE message. This is the only message an initiator communicating with the ***ProDrive*** is required to implement. To maximize flexibility, the ***ProDrive*** also supports all single byte (non-extended) messages defined in the ANSI SCSI Specification. The ***ProDrive*** will not send any message other than COMMAND COMPLETE until it is informed by the initiator that it can support other messages. The initiator does this in the SELECTION phase by asserting **ATN** prior to the SCSI bus condition of **SEL** true and **BSY** false. This informs the ***ProDrive*** that the initiator can at least generate a MESSAGE REJECT message if it does not understand a message from the ***ProDrive***.

If the ***ProDrive*** detects the **ATN** signal asserted during SELECTION phase, it will enter MESSAGE OUT phase and take a message byte from the initiator. The ***ProDrive*** expects an IDENTIFY message at

this time. The NO OPERATION, BUS DEVICE RESET and ABORT messages will also function properly here. All other messages will be rejected with a MESSAGE REJECT message.

The IDENTIFY message the initiator sends to the ***ProDrive*** should specify LUN=0. If the initiator supports disconnect/reconnect, it should set bit 6 in the IDENTIFY message. (See Section 5.6.2.) Unless bit 6 is set, the ***ProDrive*** will not attempt to disconnect at any point during a command. Bit 6 should not be set unless the initiator can support receiving the SAVE DATA POINTER, and DISCONNECT messages. Upon receipt of a legitimate IDENTIFY message, the ***ProDrive*** will enter COMMAND phase and begin requesting command bytes from the initiator.

The ***ProDrive*** supports the messages shown in Table 5-2:

TABLE 5-2 Message Codes Supported By ProDrive

Code	Description	Direction	Supported
00_H	COMMAND COMPLETE	In	
01_H	EXTEN'DED MESSAGE - SYNCHRONOUS DATA TRANSFER REQUEST	In	Out
02_H	SAVE DATA POINTER	In	
03_H	RESTORE POINTERS	In	
04_H	DISCONNECT	In	
05_H	INITIATOR DETECTED ERROR		Out
06_H	ABORT		Out
07_H	MESSAGE REJECT	In	Out
08_H	NO OPERATION		Out
09_H	MESSAGE PARITY ERROR		Out
$0A_H$	LINKED COMMAND COMPLETE	In	
$0B_H$	LINKED COMMAND COMPLETE (WITH FLAG)	In	
$0C_H$	BUS DEVICE RESET		Out
80_H - FF_H	IDENTIFY	In	Out

KEY:	In =	***ProDrive*** will originate message and send to Initiator
	Out =	***ProDrive*** will support receiving message from Initiator

5.6.2 MESSAGES

The single byte messages supported by the ***ProDrive*** (Table 5-2) are listed below along with their code values and definitions.

COMMAND COMPLETE 00_H - This message is sent from the ***ProDrive*** to an initiator to indicate that the execution of a command (or series of linked commands) has terminated and that valid status has been sent to the initiator. After successfully sending this message, the ***ProDrive*** will go into the BUS FREE phase by releasing **BSY**. This message must be supported by any initiator selecting the ***ProDrive***.

NOTE: The completion status of the command is indicated in the status byte.

EXTENDED MESSAGE 01_H - This message is sent to establish synchronous data transfer. The message and responses establish the transfer period and the **REQ/ACK** offset.

SYNCHRONOUS DATA TRANSFER REQUEST:

Byte	Value	Description
0	01h	Extended Message
1	03h	Extended Message Length
2	01h	SYNCHRONOUS DATA TRANSFER REQUEST code
3	m	Transfer Period (m times 4 nanoseconds)
4	x	REQ/ACK Offset

The transfer period is the clock rate for the transfer. The minimum transfer period for the ***ProDrive*** is 250 ns or 62 ($3E_H$). This value is equivalent to a maximum transfer rate of 4.0 MBytes/second. Table 5-3 shows the transfer rates supported and the transfer period values for the ***ProDrive***.

The REQ/ACK offset is the maximum number of **REQ** pulses that may be sent before a corresponding **ACK** pulse is received at the ***ProDrive***. A REQ/ACK offset value of zero indicates asynchronous mode. For the ***ProDrive***, the maximum value of REQ/ACK offset is 8.

If the initiator recognizes that negotiation is required, it asserts **ATN**, sends a SYNCHRONOUS DATA TRANSFER REQUEST message indicating a REQ/ACK offset and minimum transfer period. The REQ/ACK offset is chosen to prevent initiator buffer overflows, while the minimum transfer period is chosen to meet the initiator's data handling requirements. The ***ProDrive*** responds in one of the following ways:

ProDrive Response	Implied Agreement
1) REQ/ACK offset less than or equal to the requested value; minimum transfer period equal to or greater than requested period.	REQ/ACK offset equal to ***ProDrive*** value; minimum transfer period equal to the ***ProDrive*** value.
2) REQ/ACK offset equal to zero.	Asynchronous transfer.
3) MESSAGE REJECT.	Asynchronous transfer.

TABLE 5-3 Transfer Rates Supported/Transfer Period Values

TRANSFER PERIOD VALUE DEC	HEX	TRANSFER RATE IN MHZ
0 - 62	00 - $3E_H$	4.00
63 - 93	$3F_H$ - $5D_H$	2.67
94 - 125	$5E_H$ - $7D_H$	2.00
126 - 156	$7E_H$ - $9C_H$	1.60
157 - 187	$9D_H$ - BB_H	1.33
188 - 218	BC_H - DA_H	1.14
219 - 250	DB_H - FA_H	1.00
251 - 255	FB_H - FF_H	0.89

If the ***ProDrive*** recognizes that negotiation is required, it sends a SYNCHRONOUS DATA TRANSFER REQUEST message to the initiator. The REQ/ACK offset is selected to prevent buffer and offset counter overflows, while the minimum transfer period is chosen to meet the ***ProDrive's*** data handling requirements.

The implied agreement will remain in effect until a BUS DEVICE RESET message is received, until a "hard" RESET condition occurs, or until one of the two devices elects to modify the agreement. Renegotiation at every selection is not recommended, since a significant performance impact is likely.

The default mode of data transfer is asynchronous. This mode is entered at power on, after a BUS DEVICE RESET message, or after a "hard" RESET condition. The SYNCHRONOUS DATA TRANSFER REQUEST message exchange can only take place following a SELECTION phase that includes the SCSI IDs for both the initiator and ***ProDrive***. Violation of this rule may make data transfer impossible owing to disagreements among devices about the data transfer mode.

SAVE DATA POINTER 02_H - This message is sent from the ***ProDrive*** to direct the initiator to save a copy of the present active data pointer for the drive. (See Section 5.4 for a definition of pointers.) This message is usually sent just prior to the DISCONNECT message when disconnecting in the DATA phase.

DISCONNECT 04_H - This message is sent from the ***ProDrive*** to inform an initiator that the present physical data path is going to be broken (the ***ProDrive*** plans to disconnect by releasing **BSY**), but that a later reconnect will be required to complete the current operation. If the initiator detects the BUS FREE phase (other than as a result of an ABORT or BUS DEVICE RESET message or a RESET condition) without first receiving a DISCONNECT or COMMAND COMPLETE message, it should consider it a catastrophic error condition. The initiator should not save the data pointer as a result of this message.

INITIATOR DETECTED ERROR 05_H - This message is sent from an initiator to inform the ***ProDrive*** that an error (e.g., parity error on the SCSI bus) has occurred that does not preclude a retry of the operation. The ***ProDrive*** will terminate the command with a CHECK CONDITION status. The sense key will be set to ABORTED COMMAND with a sense code of Initiator Detected Error.

ABORT 06_H - This message is sent from the initiator to the ***ProDrive*** to clear the present operation. All pending data and status for the issuing initiator will be cleared, and the ***ProDrive*** will go to the BUS FREE phase. Pending data and status for other initiators will not be cleared. No status or ending message will be sent for the operation.

MESSAGE REJECT 07_H - This message will be sent by the ***ProDrive*** to an initiator if the last message received from that initiator was inappropriate or has not been implemented. This message will be interpreted in the same way if it is received from an initiator.

To indicate its intentions of sending this message, the initiator must assert the **ATN** signal prior to its release of **ACK** for the REQ/ACK handshake of the message that is to be rejected. When the ***ProDrive*** sends this message, it will change to MESSAGE IN phase and send the message prior to requesting additional message bytes from the initiator. This provides an interlock so that the initiator can determine which message is rejected. The initiator must support this message if it asserts **ATN** during the initial SELECTION phase of the command.

NO OPERATION 08_H - This message is sent from an initiator in response to the ***ProDrive 's*** request for a message, when the initiator currently has no other valid message to send. No action will be taken by the ***ProDrive*** upon receipt of this message.

MESSAGE PARITY ERROR 09_H - This message is sent from the initiator to the ***ProDrive*** to indicate that one or more bytes in the last message it received had a parity error.

To indicate its intent to send this message, the initiator must assert **ATN** prior to releasing **ACK** for the REQ/ACK handshake of the message that has the parity error. This provides an interlock so the ***ProDrive*** can determine which message has the parity error.

LINKED COMMAND COMPLETE $0A_H$ - This message is sent from the ***ProDrive*** to an initiator to indicate that the execution of a linked command has been completed and status has been sent. The initiator must then set the pointers to the initial state for the next linked command. Refer also to Sections 5.7.1.8 and 5.7.1.9.

LINKED COMMAND COMPLETE (WITH FLAG) $0B_H$ - This version of the LINKED COMMAND COMPLETE message is used when the flag bit of the command is set to one. Refer also to Sections 5.7.1.8 and 5.7.1.9.

BUS DEVICE RESET $0C_H$ - This message is sent from an initiator to direct the ***ProDrive*** to clear all current commands. This message forces the drive to an initial state with no operations pending for any initiator. Upon recognizing this message, the ***ProDrive*** will go to the BUS FREE phase. This message does not affect MODE SELECT command parameters.

IDENTIFY 80_H - FF_H - These messages may be either sent from or received by the ***ProDrive*** to establish the physical path connection between an initiator and the drive.

Bit 7 - This bit is always set to one to distinguish an IDENTIFY message from the other messages.

Bit 6 - This bit is set to one only by the initiator. When set to one, it indicates that the initiator has the ability to accommodate disconnection and reconnection. It also indicates that the SAVE DATA POINTER, RESTORE POINTERS and DISCONNECT messages are supported by the initiator.

Bits 5-3 - Reserved; must be set to zero.

Bits 2-0 - These bits specify a logical unit number (LUN) in a target. For the ***ProDrive***, the only valid LUN is zero.

When an IDENTIFY message is sent from the ***ProDrive*** to an initiator during reconnection, an implied RESTORE POINTERS message must be performed by the initiator prior to completion of this message.

5.6.3 MESSAGE ERROR RECOVERY STRATEGY

5.6.3.1 Parity Errors During Message Phase

Parity is an SCSI option. This section is relevant only if the parity option is enabled.

If the initiator detects a parity violation as the ***ProDrive*** transfers a message byte to it, it should ignore that message and immediately assert **ATN** (before releasing **ACK** on the offending byte). The initiator should continue receiving and ignoring bytes until the ***ProDrive*** requests a MESSAGE OUT byte. At that point, the initiator should send a MESSAGE PARITY ERROR message; the ***ProDrive*** will abort the command and release the bus. The sense key will be set to ABORTED COMMAND ($0B_H$) and the sense code set to Parity error on the SCSI bus (47_H).

If the ***ProDrive*** detects a parity error during a MESSAGE OUT phase, it will continue to request MESSAGE OUT bytes until the initiator deasserts **ATN**. This procedure should guarantee that the initiator transfers the entire message containing the parity error. The current command will be terminated,

the status set to CHECK CONDITION, the sense key set to ABORTED COMMAND ($0B_H$), and the sense code set to Parity error on the SCSI bus (47_H).

5.6.3.2 Rejected Messages

The ***ProDrive*** will send MESSAGE REJECT to the initiator any time it receives a message it does not support (e.g., extended messages) or a message that does not make sense at that time (e.g., the initiator sending COMMAND COMPLETE).

When the ***ProDrive*** receives MESSAGE REJECT from the initiator, it takes action based on which command was rejected.

COMMAND COMPLETE - The ***ProDrive*** goes to BUS FREE. This is not considered an error.

DISCONNECT - The ***ProDrive*** will stop trying to disconnect at this time. It may attempt to disconnect again at a later time.

IDENTIFY - The ***ProDrive*** only sends this when it is attempting to reconnect. If this message is rejected during reconnection, the present command will be terminated. The drive will post a CHECK CONDITION status, set the sense key to ABORTED COMMAND ($0B_H$), and set the sense code to Message reject error (43_H). The ***ProDrive*** will then go immediately to BUS FREE.

LINKED COMMAND COMPLETE - The ***ProDrive*** will go immediately to BUS FREE. The sense key will be set to ABORTED COMMAND ($0B_H$) and the sense code set to Message reject error (43_H).

LINKED COMMAND COMPLETE WITH FLAG - Same procedure as for LINKED COMMAND COMPLETE.

MESSAGE REJECT - The ***ProDrive*** will immediately terminate the current command with a CHECK CONDITION status. The sense key will be set to ABORTED COMMAND ($0B_H$) and the sense code set to Message reject error (43_H).

SAVE DATA POINTERS - Same procedure as for DISCONNECT message.

5.7 COMMAND IMPLEMENTATION

This section defines the SCSI commands supported by the ***ProDrive*** 40S/80S intelligent Disk Drives. Each command consists of a group of command bytes and an optional associated group of data bytes. After ARBITRATION, SELECTION, and any optional initial messages, the ***ProDrive*** will enter the COMMAND phase and request the command bytes. The opcode of the command determines how many bytes the ***ProDrive*** will request. After receipt of the command bytes, the ***ProDrive*** will enter DATA phase if a data structure is defined for the command. The data structure in a single command may transfer one or more logical blocks of data. The ***ProDrive*** may disconnect from the SCSI bus to allow activity by other SCSI devices while it is preparing to transfer data.

Upon completion of a command (successful or unsuccessful), the ***ProDrive*** will return a status byte to the initiator. Since most error and exception conditions cannot adequately be described with a single status byte, the CHECK CONDITION status code indicates that additional information is available. The initiator may issue a REQUEST SENSE command to retrieve this additional information.

The following subsections on each command describe the sequence of bytes an initiator must transfer to the ***ProDrive*** during the COMMAND phase to request a desired action from the drive. For those commands for which it is relevant, these sections also further describe the format of data bytes that may be transferred to or from the initiator following the COMMAND phase.

5.7.1 COMMAND DESCRIPTOR BLOCK (CDB)

A request is made to a device by transferring a Command Descriptor Block (CDB) to that device. The ***ProDrive*** supports two basic command formats: six-byte commands and ten-byte commands. The command format is recognizable from the opcode of the command. Six-byte commands have opcodes between 00_H and $1F_H$; ten-byte commands have opcodes from 20_H to $3F_H$ or $E0_H$ to FF_H. This section defines the CDB fields. The uses of the CDB fields in particular commands are fully described in Section 5.11.

5.7.1.1 Opcode

The opcodes (operation codes) for Groups 0 and 1 are listed in Table 5-4.

TABLE 5-4 Commands Supported By ProDrive

OPCODE	COMMAND	SECTION
00_H	TEST UNIT READY	5.11.1
01_H	REZERO UNIT	5.11.2
03_H	REQUEST SENSE	5.11.3
04_H	FORMAT UNIT	5.11.4
07_H	REASSIGN BLOCKS	5.11.5
08_H	READ	5.11.6
$0A_H$	WRITE	5.11.7
$0B_H$	SEEK	5.11.8
12_H	INQUIRY	5.11.9
15_H	MODE SELECT	5.11.10
16_H	RESERVE	5.11.11
17_H	RELEASE	5.11.12
$1A_H$	MODE SENSE	5.11.13
$1B_H$	START/STOP UNIT	5.11.14
$1D_H$	SEND DIAGNOSTIC	5.11.15
25_H	READ CAPACITY	5.11.16
28_H	READ EXTENDED	5.11.17
$2A_H$	WRITE EXTENDED	5.11.18
$2B_H$	SEEK EXTENDED	5.11.19
$2E_H$	WRITE AND VERIFY	5.11.20
$2F_H$	VERIFY	5.11.21
37_H	READ DEFECT DATA	5.11.22
$3B_H$	WRITE BUFFER	5.11.23
$3C_H$	READ BUFFER	5.11.24
$E8_H$	READ LONG	5.11.25
EA_H	WRITE LONG	5.11.26

5.7.1.2 Logical Unit Number (LUN)

The Logical Unit Number for the ***ProDrive*** is zero. The LUN is found in two places: bits 5-7 of byte 1 of the Command Descriptor Block and bits 0-2 of the IDENTIFY message field. (See Section 5.6.2.) The LUN field in both the CDB and IDENTIFY message field must be zero. If a LUN other than zero is specified in any command except INQUIRY and REQUEST SENSE, the command will be rejected with a CHECK CONDITION status and the sense key set to ILLEGAL REQUEST - Invalid LUN.

5.7.1.3 Logical Block Address (LBA)

The 21-bit (or 32-bit) Logical Block Address signifies the first or starting block of an operation. A Logical Block can be 512, 1024, or 2048 bytes in length. The MODE SELECT command is used to configure the Block Length. Each ***ProDrive*** is configured with a Logical Block Length of 512 bytes.

5.7.1.4 Transfer or Allocation Length

The transfer length in blocks, or the allocation length in bytes, is the number of blocks or bytes or data to be transferred for a single command.

- For six-byte commands, acceptable values are $00\text{-}FF_H$. For block lengths, a value of $(0)_H$ transfers 256 blocks. See allocation byte lengths under specific commands.
- For 10-byte commands, acceptable values are $0000\text{-}FFFF_H$. A value of $(0000)_H$ transfers no blocks.

5.7.1.5 Vendor Unique (VU)

Vendor unique bits allow for slight command modifications or special conditions to be selected. Vendor unique bits are to be filled with zeros.

5.7.1.6 Reserved (R)

These bits are reserved and must be set to zero by the initiator.

5.7.1.7 Flag (F)

If the link bit (5.7.1.8) is zero, the flag bit must be zero. Suppose the link bit is one. If the flag bit is zero, the target sends the LINKED COMMAND COMPLETE message when the command terminates; if the flag bit is one, it sends the LINKED COMMAND COMPLETE (WITH FLAG) message.

5.7.1.8 Link (L)

If the link bit is one, when the command terminates, the ***ProDrive*** sends one of the two messages defined by the flag bit (above). In addition, the ***ProDrive*** does not go to Bus Free, but immediately goes to the Command Out phase. If the link bit is zero, the ***ProDrive*** sends the normal COMMAND COMPLETE message.

5.7.1.9 Relative Address (RELADR)

This bit is found only in 10-byte commands (opcodes 20_H - $3F_H$) and is not supported by the ***ProDrive*** 40S/80S.

NOTE: If the reserved bits of the IDENTIFY message or the vendor unique, reserved or relative address bits of the CDB are non-zero, a CHECK CONDITION status is returned with the sense key set to ILLEGAL REQUEST and sense code set to Illegal use of bit or byte in CDB or IDENTIFY message.

5.8 COMPLETION STATUS BYTE

A status byte will be sent from the ***ProDrive*** to the initiator during the STATUS phase at the termination of each command as specified in Tables 5-6 and 5-7, unless the command is cleared by an ABORT or BUS DEVICE RESET message, or by a "hard" RESET condition. Table 5-5 presents the status bytes; Table 5-7 defines the status codes as implemented on the ***ProDrive***.

TABLE 5-5 Status Byte

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED	VENDOR UNIQUE		STATUS BYTE CODE				VENDOR UNIQUE

TABLE 5-6 ProDrive Status Byte Code Bit Values

Bits of Status Byte								
7	6	5	4	3	2	1	0	Status(es) Represented
R	V	V	0	0	0	0	V	GOOD
R	V	V	0	0	0	1	V	CHECK CONDITION
R	V	V	0	1	0	0	V	BUSY
R	V	V	1	0	0	0	V	INTERMEDIATE/GOOD
R	V	V	1	1	0	0	V	RESERVATION CONFLICT

KEY: R = Reserved Bit (zero)
V = Vendor Unique Bit (zero)

TABLE 5-7 ProDrive Status Codes

STATUS BYTE CODE	MEANING
GOOD (00_H)	COMMAND HAS COMPLETED WITH NO ERROR CONDITIONS.
INTERMEDIATE/ GOOD (10_H)	LINKED COMMAND HAS COMPLETED WITH NO ERROR CONDITIONS. This code is issued for every command in a series of linked commands (except the last, for which the link bit is zero) unless CHECK CONDITION or RESERVATION CONFLICT is appropriate. If this code is not returned, the chain of linked commands is broken.
CHECK CONDITION (02_H)	AN ABNORMAL CONDITION HAS OCCURRED. This code is issued whenever an error, exception or abnormal condition occurred during the execution of a command (the command may or may not have completed successfully). A REQUEST SENSE command should be issued following a CHECK CONDITION status to determine the nature of the condition.
BUSY (08_H)	TARGET IS BUSY. This code is issued if the target is busy executing a previous command, after a disconnection has occurred, or if the target is otherwise unable to accept a command. The command that received the BUSY status is discarded and no action is taken; it may be reissued as if it were issued for the first time.
RESERVATION CONFLICT (18_H)	ATTEMPTED ACCESS OF A RESERVED BLOCK, OR DEVICE. This code is issued when a device attempts to access a reserved area, in which case the command will be rejected. See RESERVE command.

5.9 READING AND WRITING

5.9.1 LOGICAL BLOCKS

The basic functions of a disk drive are to store and retrieve information. Information is stored on the ***ProDrive*** and retrieved as groups of 8-bit bytes. These groups of bytes have a standard size and are referred to as logical blocks. The size of a logical block (the number of bytes contained in each block) is set via the MODE SELECT command. The ***ProDrive*** will support three logical block sizes: 512, 1024, and 2048 bytes per block. The drive is initially configured as 512 bytes per logical block. A unique feature of the ***ProDrive*** is that when the default tracks/zone (0) is set, changing the block size will not destroy data on the drive; it simply changes the grouping of the information (e.g., 1024-byte blocks would be reconfigured as two 512-byte blocks). If a tracks/zone setting other than the default is used, changing block size could cause some data to become inaccessible.

To the user, the ***ProDrive*** appears as a series of logical blocks, each with its own unique address called the Logical Block Address (LBA). The first logical block on the drive is address 0. The address of the last logical block on the drive varies depending on the capacity of the drive and the size of the logical block.

5.9.2 LOGICAL BLOCK ADDRESS RANGES

	Block Size	Valid Logical Block Address Range Decimal	Hex
ProDrive 40S	512 or 200_H	0 - 82,028	0 - $1406C_H$
	1024 or 400_H	0 - 41,013	0 - $A035_H$
	2048 or 800_H	0 - 20,505	0 - 5019_H
ProDrive 80S	512 or 200_H	0 - 164,057	0 - $280D9_H$
	1024 or 400_H	0 - 82,028	0 - $1406C_H$
	2048 or 800_H	0 - 41,013	0 - $A035_H$

NOTE The number of available logical blocks may vary depending on the value set for tracks per zone (MODE SELECT command page 3) selected by the user.

If an initiator attempts to access a logical block at an address outside the valid address range, the command will not be executed. The drive will return a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST - Invalid Logical Block Address was specified.

5.9.3 TRANSFERRING DATA

The actual storing away and retrieving of logical blocks is done with the WRITE and READ commands. WRITE will place data on the disk and READ will retrieve data from the disk. In both the READ and WRITE commands, the user (initiator) must specify the logical block address of the first logical block to be transferred and the total number of blocks to be transferred. The interpretation of a value of zero in the number of blocks to be transferred depends on which form of the READ or WRITE command is used.

- If the extended form of the commands is used (opcodes 28_H and $2A_H$), a transfer length of zero implies transfer no data.
- The non-extended form of the comand has only one byte to specify transfer length. If this shorter command format is used (opcodes 08_H and $0A_H$), a transfer length of zero means transfer 256 blocks during the command.

The number of bytes transferred during the DATA phase following the command bytes is determined by the transfer length specified in the command and the logical block size:

- Number of Data Bytes = Logical BLock Size (in bytes) x Transfer Length (in blocks)

Note that in case of errors, a fewer number of bytes will sometimes be transferred.

The rate at which data is transferred to or from the disk depends solely on how densely the data is written on the disk and how fast the disk is rotating. Neither of these quantities can be easily modified, so the disk transfer rate should be regarded as a constant. The ***ProDrive*** has two data zones, an inner zone and an outer zone, with two different data rates:

- The transfer rate when the head is over data in the outer zone is 10 Mbit/sec (1.25 Mbyte/sec).
- When the head is over data in the inner zone, the transfer rate is 8 Mbit/sec (1 Mbyte/sec).

If the transfer rate across the SCSI bus is slower than this sustained disk transfer rate, the drive will run out of data if the transfer is a WRITE, or begin to have data collect in its buffer if the transfer is a READ. Other disk drive subsystems might require the user to interleave sectors on the disk to match the sustained disk transfer rate with the SCSI bus transfer rate. This is not necessary with the ***ProDrive*** since it includes a large on-board cache (64K bytes). All READ and WRITE transfers are channeled through this buffer, enabling the drive to maintain steady transfer when the transfer rate is less than 1.25 Mbyte/second.

This buffer also serves as an on-board cache (***DisCache***). The caching function can be enabled/disabled, and various cache parameters can be configured to best fit the application via the MODE SELECT command. Refer to the section on the MODE SELECT command (5.11.10) and Appendix A for a more detailed discussion of the ***DisCache*** feature.

5.10 CONFIGURING THE *PRODRIVE*

5.10.1 *PRODRIVE* OPERATING MODES

The manner in which the ***ProDrive*** operates can be changed to more precisely match its features with user requirements. This is referred to as changing the Operating Mode of the drive and is done through the use of the MODE SELECT and MODE SENSE commands. The MODE SELECT command is used to set the Operating Mode of the ***ProDrive*** to achieve the desired behavior. The MODE SENSE command may be used to determine the current Operating Mode of the drive, or to gather other information that would be useful in setting the Operating Mode.

An example of a common user-adjusted Operating Mode parameter is the number of retries the drive should attempt when it detects a read error. If an initiator wished to retry only once when the drive detected incorrect data, the initiator's software could first issue a MODE SENSE command to the ***ProDrive*** to determine its current configuration. The data returned to the initiator during the DATA phase of the MODE SENSE command would contain the current Mode Parameters, including how many retries the drive will attempt when it detects a read error. If the number of retries is not set to the desired number, the initiator could then send a MODE SELECT command with the data byte corresponding to the Retry Count Parameter set to one. From then on, the ***ProDrive*** would only retry once on READ commands.

5.10.2 OPERATING MODE TABLES

The ***ProDrive*** Operating Mode is determined by the contents of the Current Mode Table. Because of the need for frequent and fast access to its parameters, the Current Mode Table is stored in RAM. This table is referenced whenever there is more than one possible way for the drive to behave. In the previous example, the initiator will have set the Retry Count in the Current Mode Table to one. Each time a READ command is executed, the firmware checks the Current Mode Table and looks up the Retry Count Parameter. It then uses this number to determine how many times it should attempt to re-read a block if the data is detected to be incorrect.

Storing the Current Mode Table in RAM means that the drive's Operating Mode is lost when power is removed or the drive is reset. For this reason, a copy of the Current Mode Table can be saved on the disk itself. This saved copy is called the Saved Mode Table. The Saved Mode Table is stored on a hidden area of the disk that is not accessible by the user. This way, no user data storage area is sacrificed, nor can a user inadvertently erase the table. The Saved Mode Table is used to load the Current Mode Table at power-up or whenever the drive is reset. The contents of the Current Mode Table can be copied into the Saved Mode Table via the MODE SELECT command. If the Save Parameters bit is set to one in the MODE SELECT command (bit 0 of byte 1), the entire contents of the Current Mode Table will be transferred to the Saved Mode Table when the command is completed.

NOTE: If the MODE SELECT command makes changes to the Current Mode Table, these changes will be implemented first and then incorporated in the Saved Mode Table. In other words, if a MODE SELECT command contains new mode information and the Save Parameters bit is set, the new mode information will appear in the Saved Mode Table as well as in the Current Mode Table.

The Saved Mode Table is a very powerful tool for the user. Using the Save Parameters bit allows the drive to be permanently configured to the user's requirements with the execution of a single MODE SELECT command. This means that a once-in-a-lifetime configuration can be done (e.g., at the user's factory), eliminating the burden from the device driver of sending vendor specific MODE SELECT commands after every reset.

There are two other Mode Tables supported by the ***ProDrive*** that are of interest to the user. These are the Changeable Parameters Table and the Default Mode Table. Both of these tables are contained in the firmware ROM and are for reference only. They cannot be modified by the user. These two tables can be referenced only by the MODE SENSE command.

- The Changeable Parameters Table allows an initiator to determine which Operating Mode parameters the ***ProDrive*** will allow to be changed via a MODE SELECT command. If a parameter in the Current Mode Table is changeable, the corresponding entry will have all bits set to one. Before trying to change any Operating Mode parameter with a MODE SELECT command, the software driver should first check to make sure that the device will support changing that parameter.

- The Default Mode Table allows the user to restore the drive to a known or reference condition. If for any reason the Current and Saved mode tables are inaccessible, the ***ProDrive*** will use the default mode table.

5.11 COMMAND DESCRIPTIONS

Following are descriptions of the individual commands listed in Table 5-4. Refer to the REQUEST SENSE command (Section 5.11.3) for a description of error codes and sense keys. Refer to the Command Descriptor Block section (5.7.1) for definitions of the CDB fields.

5.11.1 TEST UNIT READY COMMAND: OPCODE = 00(hex)

The TEST UNIT READY command (Table 5-8) provides a means to check if the drive is up to speed and ready to accept commands requiring disk access.

TABLE 5-8 TEST UNIT READY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 00_H							
1	LUN = 0			RESERVED = 0				
2-4	RESERVED = 0							
5	VU = 0		RESERVED = 0				F	L

When the ***ProDrive*** is ready, the completion status byte will indicate GOOD (00_H). If the drive is not ready, the completion status byte will indicate CHECK CONDITION (02_H), with the sense key set to NOT READY (02_H).

The commands which do not require disk access are:

REQUEST SENSE — INQUIRY *
RESERVE — SEND DIAGNOSTICS
RELEASE — START/STOP UNIT
READ BUFFER — WRITE BUFFER
MODE SELECT (if Save Parameters bit is not set)
MODE SENSE (if Save Parameters are not requested)

* If the ***ProDrive*** is not ready when the INQUIRY command is received, the disk is not accessed and the default inquiry data is returned (see 5.11.9).

The ***ProDrive*** will execute any of the above commands after a delay of one second, maximum, following application of power to the drive. They will not return CHECK CONDITION status with the NOT READY sense key even if the drive is not ready. All other commands could require disk access. (Refer to START/STOP UNIT command, Section 5.11.14 below.)

5.11.2 REZERO UNIT COMMAND: OPCODE = 01(hex)

The REZERO UNIT command (Table 5-9) requests that the drive actuator be repositioned to cylinder zero and head zero.

TABLE 5-9 REZERO UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 01_H							
1	LUN = 0			RESERVED = 0				
2-4	RESERVED = 0							
5	VU = 0		RESERVED = 0				F	L

5.11.3 REQUEST SENSE COMMAND: OPCODE = 03(hex)

5.11.3.1 Command Structure

The REQUEST SENSE command (Table 5-10) requests that the sense data be sent to the initiator.

The sense data applies to the previous command from the same initiator. Sense data is saved for an initiator until it is retrieved by that initiator or until another command is received from that initiator. Commands from any initiator will not alter the sense data saved for other initiators.

TABLE 5-10 REQUEST SENSE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 03_H							
1	LUN = 0			RESERVED = 0				
2-3	RESERVED = 0							
4	ALLOCATION LENGTH (BYTES)							
5	VU = 0		RESERVED = 0				F	L

ALLOCATION LENGTH - specifies the maximum number of bytes allocated by the initiator for returned sense data. Acceptable values are 00-FF_H. (A value of 00 indicates that four bytes of data will be returned.) The ***ProDrive*** will terminate the DATA IN phase when the allocated number of bytes have been transferred or when all available sense data have been transferred to the initiator, whichever is less. For the ***ProDrive***, an allocation length of 18 (12_H) is recommended.

If the allocation length prevents all available sense data from being sent to the initiator, the initiator may not use a subsequent REQUEST SENSE command to recover the remaining portion.

The ***ProDrive*** uses the extended format for sense data. (See Table 5-11.)

5.11.3.2 Extended Sense Format

TABLE 5-11 Extended Sense Format

Bit / Byte	7	6	5	4	3	2	1	0
0	VALID	ERROR CLASS AND CODE = 70_H						
1	SEGMENT NUMBER = 0							
2	FM=0	EOM=1	ILI=0	R=0	SENSE KEY			
3 - 6	(MSB)	INFORMATION BYTE						(LSB)
7	ADDITIONAL SENSE LENGTH (BYTES) = $0A_H$							
8-11	RESERVED = 0							
12	ADDITIONAL SENSE CODE							
13	RESERVED = 0							
14	FRU FAILED = 0							
15	FPV	C/D	VU	VU	BPV	BIT POINTER = 0		
16-17	(MSB)	FIELD POINTER						(LSB)

VALID - INFORMATION VALID (Byte 0, Bit 7) - Set to 1 if the information bytes contain valid data.

ERROR CLASS AND CODE (Byte 0, Bits 6-0) - Set to 70_H to indicate extended status.

SEGMENT NUMBER (Byte 1) - Set to zero for the ***ProDrive***.

FM - FILE MARK (Bit 7, Byte 2) - Indicates that a filemark has been read; set to zero for the ***ProDrive***.

EOM - END-OF-MEDIUM (Byte 2, Bit 6) - Indicates that an end-of-medium condition exists; set to zero for the ***ProDrive***.

ILI - INCORRECT LENGTH INDICATOR (Byte 2, Bit 5) - Indicates that the requested logical block length does not match the block length on the medium. This bit is normally set to zero for the ***ProDrive***; an exception is in response to the READ BUFFER command, when the requested transfer length is greater than the buffer size.

R - RESERVED (Byte 2, Bit 4) - Must be zero for the ***ProDrive***.

SENSE KEY (Byte 2, Bits 3-0) - Values for sense key data are shown in Table 5-12.

INFORMATION BYTES (Bytes 3-6) - If the VALID bit is 1, the information bytes are valid and are defined as he logical block address associated with the sense key.

ADDITIONAL SENSE LENGTH (Byte 7) - The number of additional bytes to follow. This value will not be truncated if the allocation length in the command descriptor block is too small to transfer all of the additional sense bytes. The ***ProDrive*** uses a value of 0A H in byte 7.

ADDITIONAL SENSE CODE (Byte 12) - Refer to Table 5-12.

FRU - FIELD REPLACEABLE UNIT FAILED (Byte 14) - The format of this byte is vendor unique. A value of zero means that no FRU is to be reported.

FPV - FIELD POINTER VALID (Byte 15, Bit 7) - Set to zero indicates that the C/D bit and BPV bit, and bytes 16 and 17 are not valid. An FPV bit set to one indicates that the field pointer bytes 16 and 17, the C/D bit and BPV bit, are significant.

C/D - CONTROL/DATA BIT (Byte 15, Bit 6) - Set to one indicates that the value reported in the field pointer is the Command Descriptor Block (CDB) byte number for which an ILLEGAL REQUEST sense key was issued. A C/D bit of zero indicates that the value reported in the field pointer is the byte number of the DATA phase for which an ILLEGAL REQUEST sense key was issued.

VENDOR UNIQUE (Byte 15, Bits 5-4) - Bits 5 and 4 of byte 15 are vendor unique.

BPV - BIT POINTER VALID (Byte 15, Bit 3) - Set to zero indicates that the bit pointer field is not valid. A BPV bit set to one indicates that the bit pointer field (Bits 0 - 2) is valid.

BIT POINTER (Byte 15, Bits 2-0) - If **BPV** is set, this field points to the bit within the byte that is in error.

FIELD POINTER (Bytes 16-17) - These bytes represent an index into the Command Descriptor Block fields or the DATA phase fields for which an ILLEGAL REQUEST sense key was issued. In the case of multiple byte fields, the field pointer bytes index the most significant byte of the field for which an illegal request sense key was issued. These bytes are only valid if the Field Pointer Valid (FPV) bit is set to one.

TABLE 5-12 Sense Error Codes

Sense Key (hex)	Additional Sense Code (hex)	Description
0		NO SENSE. No specific sense key information to be reported. This would be the case for a successful command or a command that received a CHECK CONDITION status because one of the filemark, EOM, or ILI bits is set to one.
	00	No additional information
1		RECOVERED ERROR. The last command was completed successfully with some recovery action performed by the ***ProDrive***. Details may be determined by examining the additional sense bytes and the information bytes.
	00	No additional information
	02	Recovered seek timeout
	10	Recovered ID CRC error
	11	Recovered data ECC on last retry

Table 5-12 Sense Error Codes (cont.)

Sense Key (hex)	Additional Sense Code (hex)	Description
	13	Recovered data sync timeout
	14	Recovered no record found
	15	Recovered seek error
	16	Recovered data marker not found
	17	Recovered data ECC with retries
	18	Recovered data ECC error
	86	Recovered unexpected sequencer error
	95	Recovered SOLO timeout
	96	Recovered bump
	97	Recovered underrun/overrun error
	98	Recovered timeout in settling
	A8	Spurious nmi interrupt
	AB	Requested format not available
2		NOT READY. Target cannot be accessed. Operator intervention may be required to correct this condition.
	00	No additional information
	B0	Drive recalibrating
	B1	Drive not up to speed
	B2	Drive waiting for command to start
3		MEDIUM ERROR. The command terminated with a non-recovered error condition that was probably caused by a flaw in the medium or an error in the recorded data.
	00	No additional information
	10	All IDs have CRC errors
	11	Uncorrectable data error
	13	Data sync timeout
	14	No record found
	16	Data marker not found
	19	Bad defect list
	1C	No primary defect list found
	31	Format failed or not formatted
	32	No more spares available
	80	Can't write system sector
	81	Can't read system sector
	95	SOLO timeout
	97	Underrun/overrun error
	A3	Reassign Blocks READ failure
	AA	Reallocated uncorrectable data read

Table 5-12 Sense Error Codes (cont.)

Sense Key (hex)	Additional Sense Code (hex)	Description
4		HARDWARE ERROR. The target detected a non-recoverable hardware failure while performing the command.
	00	No additional information
	01	No index signal
	02	Seek timeout
	03	Write fault
	06	Recalibrate failure
	09	Servoing error
	15	Seek error
	1B	Synchronous request error
	32	Defect list is full
	40	Buffer RAM failure
	41	ECC failure
	42	Power-on failure
	43	Message reject
	44	Firmware error
	45	Reselect timeout
	82	No digital P1 or P2 signal
	83	Analog P1 or P2 are bad
	84	Failure writing to format parameter RAM
	85	Rejected message was not sent
	86	Unexpected sequencer error
	87	A and B servos not equal
	88	Airlock stuck closed
	89	Bad head amplifier
	8A	Bad head select
	90	Synchronous acknowledge error
	91	FIFO unload error
	92	FIFO load error
	93	FIFO predicted full error
	94	Undocumented SPICY error
	96	Bump timeout
	98	Timeout in settling
	99	Bump retry counter expired
	9D	Motor never gets up to speed
	9E	Motor drops out of legal speed range
	9F	Internal ROM checksum error
	A0	External PROM checksum error
	A1	Sequencer rollover register failure
	A2	External RAM failure
	A4	Bad thermistor
	A6	A and B servos not detected

Table 5-12 Sense Error Codes (cont.)

Sense Key (hex)	Additional Sense Code (hex)	Description
	A7	Offtrack timeout
	A9	SOLO DMA pointer error
	AC	Airlock stuck open
	AD	No servo interrupt
5		ILLEGAL REQUEST. There was an illegal parameter in the command descriptor block or in the additional parameters supplied as data for a command. If the ***ProDrive*** detects an invalid parameter in the command descriptor block, it will terminate the command without altering the medium; if the invalid parameter is in the additional parameters supplied as data, it may have already altered the medium.
	00	No additional information
	19	Entered defect list in error
	1A	Parameter overrun
	20	Invalid command
	21	Invalid LBA
	22	Illegal function for device type
	24	Illegal field in CDB
	25	Invalid LUN
	26	Illegal field in parameter list
	8A	Invalid head
	8B	Invalid cylinder
	8C	Select from same initiator while active
	8D	Bad BPB/BPS
	8F	Invalid sector
	9B	Invalid period or offset in sync message
	9C	Active initiator attempted another select
	A5	Defect list out of order
	AE	Bad parameter(s) in mode page
6		UNIT ATTENTION. MODE SELECT parameters have been changed by another initiator, or the ***ProDrive*** has been reset by a bus device reset message, a "hard" reset condition (RST asserted) or a power-on reset. The UNIT ATTENTION condition will persist until receipt of a command other than INQUIRY or REQUEST SENSE. The command issued will not be performed; the CHECK CONDITION status will be reported, allowing the initiator to discover and clear the UNIT ATTENTION condition by issuing a REQUEST SENSE command. An INQUIRY command will be performed with no effect to the UNIT ATTENTION condition. If a REQUEST SENSE command is received before the ***ProDrive*** reports CHECK CONDITION for the UNIT ATTENTION condition, the condition will be reported and cleared.
	00	No additional information
	29	Drive reset
	2A	Mode select parameter changed
	8E	Unexpected SCSI interrupt occurred
	9A	Target attempted to reselect ***ProDrive***

Table 5-12 Sense Error Codes (cont.)

Sense Key (hex)	Additional Sense Code (hex)	Description
B		ABORTED COMMAND. The ***ProDrive*** aborted the command. The initiator may be able to recover by trying the command again.
	00	No additional information
	40	Buffer RAM parity error
	47	Parity error on SCSI bus
	48	Initiator detected error
	49	Inappropriate/illegal message
E		MISCOMPARE. The source data dit not match the data read from the medium.
	00	No additional information
	AF	Buffer corrupted

5.11.4 FORMAT UNIT COMMAND: OPCODE = 04(hex)

The FORMAT UNIT command (Table 5-13) assigns logical blocks to physical sectors for optimum sequential access (within the limitations of available spare blocks), skipping known defective areas. An option causes a repetitive (one byte) data pattern to be written in every block. The ***ProDrive*** is formatted when shipped from the factory, with data being undefined.

NOTE: Issuing this command typically causes loss of data, even when the repetitive data pattern option is not used. All data should be backed up prior to formatting.

5.11.4.1 Command Structure

TABLE 5-13 FORMAT UNIT Command

Byte \ Bit	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			FMTDAT	CMPLST	DEFECT LIST FORMAT		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

FMTDAT - FORMAT DATA (Byte 1, Bit 4) - Set to one indicates that defective block data is supplied during the DATA OUT phase. The defect list included with this data specifies the defects that will be entered onto the defect map. The defect list refers to the current block length and current logical block addresses (not physical addresses). The format of the defect list is shown in Table 5-15. A FMTDAT bit of zero indicates that the DATA OUT phase will not occur, i.e., no defect list header and no defect data shall be supplied by the initiator. See Table 5-15.

CMPLST - COMPLETE LIST (Byte 1, Bit 3) - Set to one indicates the data supplied is the complete list of known initiator-specified or field replacement defects. Any previous initiator-specified defect map or defect data is erased. This purges any previous initiator-specified defect list and builds a new defect list, which includes the initiator-specified list and the factory defects. A CMPLST bit of zero indicates that the data supplied is in addition to existing defect data using the current format.

DEFECT LIST FORMAT (Byte 1, Bits 2-0) - Specifies additional information related to the defect list. See Table 5-14 for further information.

DATA PATTERN (Byte 2) - User data pattern to be written repetitively into each sector during FORMAT UNIT command (if this option is enabled by the Fill Data Pattern bit in Page 39_H of the MODE SELECT command).

INTERLEAVE FIELD (Bytes 3-4) - Specifies the interleave factor. Any value specified in this field by the initiator will be ignored by the ***ProDrive***. The ***ProDrive*** uses a 1:1 interleave.

TABLE 5-14 FORMAT UNIT Command Variations

Bit Reference (CDB byte 1)					Defect List Byte 1		Defect List Length	Option (See 5.11.4.2)
4	3	2	1	0	7	6		
FMTDAT	CMPLST		DEFECT LIST FORMAT		FOV	DPRY		
1	1	0	X	X	1	1	0	1
1	1	0	X	X	0	0	0	2
1	0	0	X	X	1	1	0	3
0	X	X	X	X	NO DEFECT LIST*			4
1	1	0	X	X	1	1		5
1	1	0	X	X	0	0		6
1	0	0	X	X	1	1		7
1	0	0	X	X	0	0		8
					COMMENTS			
1	X	1	0	X	Not Supported			
1	X	1	1	0	Vendor Unique (Not Used)			
1	X	1	1	1	Reserved			

Key: X = 1 or 0 (ignored by ***ProDrive***)

*Since the DATA OUT phase does not occur, there is no defect list header.

The defect list shown in Table 5-15 contains a four-byte header which may be folowed by defect descriptors. The defect list length is equal to four times the number of defect descriptors; it specifies the total length in bytes of the defect descriptors that follow. Each defect descriptor for the logical block format specifies a four-byte defect logical block address that contains the defect. The defect addresses must be in ascending order. The defect list length may be zero.

TABLE 5-15 Defect List - Logical Block Format

Bit / Byte	7	6	5	4	3	2	1	0
	DEFECT LIST HEADER							
0	RESERVED = 0							
1	FOV	DPRY	DCRT	STPF	RESERVED = 0			
2-3	(MSB)	DEFECT LIST LENGTH						(LSB)
	Defect Descriptor(s):							
0-4	(MSB)	DEFECT LOGICAL BLOCK ADDRESS						(LSB)

FOV - FORMAT OPTIONS VALID (Byte 1, Bit 7) - Set to one authorizes the setting of bits 4 through 6 (STPF, DCRT, and DPRY). A FOV bit of zero indicates that the initiator requests the ***ProDrive*** default format scheme to be implemented for the functions defined by bits 4 through 6.

DPRY - DISABLE PRIMARY (Byte 2, Bit 6) - Set to one indicate that the ***ProDrive*** will exclude the factory defect map (primary list or P list) from its list of flaws to manage while formatting. A DPRY bit set to zero indicates that the ***ProDrive*** will include the factory defect map in its list of flaws to manage while formatting. Note that the inclusion of the factory defect map is the default condition of the ***ProDrive***.

DCRT - DISABLE CERTIFICATION (Byte 1, Bit 5) - Not supported by the ***ProDrive***. Must be set to zero by the initiator.

STPF - STOP FORMAT (Byte 1, Bit 4) - Not supported by the ***ProDrive***. Must be set to zero by the initiator.

5.11.4.2 Application of FORMAT UNIT Command

The ***ProDrive*** offers eight formatting options as follows:

1) Format with absolutely no defects
2) Format with original factory defects only
3) Format with grown defects only (discarding factory defects)
4) Format with existing defects (factory and grown defects)
5) Format with provided defects only (discarding factory and existing grown defects)
6) Format with provided defects in addition to factory defects (discarding existing grown defects)
7) Format with provided defects in addition to existing grown defects (discarding factory defects)
8) Format with provided defects in addition to existing defects

NOTE With any of the above options, the list of grown defects is always updated to reflect the latest condition; meanwhile, the original factory defects are always preserved.

The following tables illustrate the setting of the FORMAT UNIT CDB and defect list header required to implement each of the listed options.

(1) Format with absolutely no defects.

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	1	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	1	1	0	0	RESERVED = 0			
2-3	(MSB)	DEFECT LENGTH = 0						(LSB)

NOTE: The list of grown defects will be erased.

(2) Format with original factory defects only.

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	1	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	0	0	0	0	RESERVED = 0			
2-3	(MSB)	DEFECT LENGTH = 0						(LSB)

NOTE: The list of grown defects will be erased.

(3) Format with grown defects only; discard factory defects.

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	0	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	1	1	0	0	RESERVED = 0			
2-3	(MSB)	DEFECT LENGTH = 0						(LSB)

NOTE The list of grown defects will be erased.

(4) Format with existing defects (factory and grown defects). The data out phase is not used.

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			0	0	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

NOTE No defect list header or defect descriptor blocks follow the command.

(5) Format with provided defects only; discard factory and existing grown defects.

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	1	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	1	1	0	0	RESERVED = 0			
2-3	(MSB)	DEFECT LENGTH						(LSB)

NOTE The defect descriptor blocks follow the defect list header.

(6) Format with provided defects in addition to factory defects; discard existing grown defects)

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	1	0		
2	DATA PATTERN							
3-4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	L

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	0	0	0	0	RESERVED = 0			
2-3	(MSB)	DEFECT LENGTH						(LSB)

NOTE The defect descriptor blocks folow the defect list header. The provided defects will replace the existing grown defects.

(7) Format with provided defects in addition to existing grown defects; discard factory defects)

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	0	0		
2	DATA PATTERN							
3,4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				F	1

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	1	1	0	0	RESERVED = 0			
2,3	(MSB)	DEFECT LENGTH = 0						(LSB)

NOTE The defect descriptor blocks follow the defect list header. The existing list of grown defects will be added with the provided defects, becoming the updated grown defects.

(8) Format with provided defects in addition to existing defects

FORMAT UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 04_H							
1	LUN = 0			1	0	0		
2	DATA PATTERN							
3,4	(MSB)	INTERLEAVE = XX						(LSB)
5	VU = 0		RESERVED = 0				1	1

Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	0	0	0	0	RESERVED = 0			
2,3	(MSB)	DEFECT LENGTH = 0						(LSB)

NOTE The defect descriptor blocks follow the defect list header. The existing list of grown defects will be added with the provided defects, becoming the updated grown defects.

5.11.5 REASSIGN BLOCKS COMMAND: OPCODE = 07(hex)

The REASSIGN BLOCKS command (Table 5-16) requests the ***ProDrive*** to reassign the defective logical blocks to areas on the drive reserved for this purpose.

The initiator transfers a defect list during the DATA OUT phase following the command bytes; the defect list contains the logical block addresses to be reassigned by the ***ProDrive***. The drive will reassign the physical medium used for each logical block address in the list. The data contained in the logical blocks specified in the defect list will be preserved if recoverable within the limits prescribed by MODE SELECT error recovery parameters; the data in all other logical blocks on the medium will be preserved. If a logical block that has previously been reassigned is specified to be reassigned, the block will be reassigned again. The defective block address will be added to the drive's field replacement defect map.

NOTES The REASSIGN BLOCKS command should not be used to redundantly reassign defective logical blocks which have already been so reassigned with the automatic reallocation feature of MODE SELECT.

Block reassignment can degrade performance by requiring spare locations to be accessed. This can be remedied by moving a file to a more appropriate area (as determined using the READ CAPACITY command) or possibly by reassigning all logical block addresses with the FORMAT UNIT command.

TABLE 5-16 REASSIGN BLOCKS Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 07_H							
1	LUN = 0			RESERVED = 0				
2-4	RESERVED = 0							
5	VU = 0		RESERVED = 0				F	L

The REASSIGN BLOCKS defect list (Table 5-17) contains a four byte header followed by one or more defect descriptors. The length of each defect descriptor is four bytes. The defect list length field specifies the total length in bytes of the defect descriptors that follow. The defect list length is, therefore, equal to four times the number of defect descriptors.

TABLE 5-17 REASSIGN BLOCKS Defect List

Byte \ Bit	7	6	5	4	3	2	1	0
Defect List Header:								
0-1	RESERVED = 0							
2-3	(MSB)	DEFECT LIST LENGTH						(LSB)
Defect Descriptor(s):								
0-4	(MSB)	DEFECT LOGICAL BLOCK ADDRESS						(LSB)

The defect descriptor specifies a four-byte defect logical block address that contains the defect. The defect addresses must be in ascending order. All of the 512-byte sectors associated with a logical block (1, 2, or 4 sectors) will be reassigned.

If the drive has insufficient capacity to reassign all of the defective logical blocks, the command will terminate with a CHECK CONDITION status and the sense key will be set to MEDIUM ERROR. The logical block address of the first logical block not reassigned will be returned in the information bytes of the sense data.

5.11.6 READ COMMAND: OPCODE = 08(hex)

The READ command (Table 5-18) requests that the target transfer data to the initiator.

5.11.6.1 Command Structure

TABLE 5-18 READ Command

Byte \ Bit	7	6	5	4	3	2	1	0
0	OPCODE = 08_H							
1	LUN = 0			(MSB)	LOGICAL BLOCK ADDRESS			
2-3	LOGICAL BLOCK ADDRESS							(LSB)
4	TRANSFER LENGTH							
5	VU = 0		RESERVED = 0				F	L

LOGICAL BLOCK ADDRESS (Byte 1, Bits 4-0; Bytes 2-3) - Specifies the logical block at which the READ operation will begin.

TRANSFER LENGTH (Byte 4) - Specifies the number of contiguous logical blocks of data to be transferred. A transfer length of zero indicates that 256 blocks shall be transferred. Acceptable values are 00-FF_H.

5.11.6.2 READ Command Operation

Read operations on the ***ProDrive*** are buffered using a 64K byte buffer. When data is read from the drive, it is first stored in the buffer. After a logical block has been read successfully into the buffer, those data bytes are transferred from the buffer to the SCSI bus.

The two operations involved in reading, transferring data from the disk to the buffer and transferring data from the buffer to the SCSI bus, are essentially independent processes. The first operation, transferring data from the disk to the buffer, will continue as long as the transfer length indicates that there is more data to be read from the disk and there is room in the buffer. The second operation, transferring data from the buffer to the SCSI bus, will start whenever the buffer contains at least one logical block. If the buffer fills completely because the second operation (buffer to SCSI bus) is slower than the first (disk to buffer), transfer to the buffer will be temporarily halted to allow the transfer from the buffer to the SCSI bus to free-up room in the buffer. Transfer from disk to buffer continues until the transfer length is exhausted. Transfer from the buffer to the SCSI bus continues until the first operation is completed and the buffer is totally emptied.

The disconnect/reconnect strategy is tied to the dual processes of filling and emptying the buffer. The ***ProDrive*** will not disconnect unless the initiator sends an IDENTIFY message with the "I Support Disconnect" bit (bit 6) set. If disconnect is supported by the initiator, the drive will disconnect whenever the buffer is empty and the transfer count is not exhausted. The point at which reconnect occurs is controlled by the Buffer Full Ratio (MODE SELECT Page 2 byte 2). When the buffer fills to the level specified by the Buffer Full Ratio, the ***ProDrive*** will initiate a reconnection. When reconnection to the bus is established, the buffer to SCSI bus transfer operation will resume. If there is a delay in establishing the reconnection (e.g., the bus is busy), the disk to buffer operation will continue until the buffer is full, or the number of blocks requested has been reached.

5.11.7 WRITE COMMAND: OPCODE = 0A(hex)

The WRITE command (Table 5-19) requests that the data transferred to the target be written in the area specified by the logical block address.

5.11.7.1 Command Structure

TABLE 5-19 WRITE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $0A_H$							
1	LUN = 0			(MSB) LOGICAL BLOCK ADDRESS				
2-3	LOGICAL BLOCK ADDRESS							(LSB)
4	TRANSFER LENGTH							
5	VU = 0		RESERVED = 0				F	L

LOGICAL BLOCK ADDRESS (Byte 1, Bits 4-0; Bytes 2-3) - Specifies the logical block at which the WRITE operation will begin.

TRANSFER LENGTH (Byte 4) - Specifies the number of contiguous logical blocks to be transferred. A transfer length of zero indicates that 256 blocks will be transferred. Acceptable values are 00-FF_H.

5.11.7.2 WRITE Command Operation

WRITE commands on the ***ProDrive*** are buffered using a 64K byte buffer. Data to be stored on the disk, is first stored in the buffer. When the head is correctly positioned on the track over the appropriate data area, data will be written from the buffer to the disk.

The two operations involved in writing, transferring data from the SCSI bus to the buffer and transferring data from the buffer onto the disk, are essentially independent processes. The first operation, transferring data from the SCSI bus into the buffer, will continue as long as the transfer length indicates that there is more data to be transferred across the SCSI bus from the initiator and there is room in the buffer. If the buffer fills completely, the transfer of data across the SCSI bus will temporarily halt. The second operation, transferring data from the buffer onto the disk, will occur as long as the buffer is not empty and the head is correctly positioned over the appropriate data area. The only interaction between these two operations involves the buffer level. The buffer-to-disk operation will stop if the SCSI bus-to-buffer transfer process cannot keep up and the buffer empties. In turn, the SCSI-to-buffer transfer will temporarily halt if the buffer-to-disk transfer process falls behind and the buffer fills completely.

The disconnect/reconnect strategy is tied to the dual processes of filling and emptying the buffer. The ***ProDrive*** will not disconnect unless the initiator sends an IDENTIFY message with the "I Support Disconnect" bit (bit 6) set. If disconnect is supported by the initiator, the drive will disconnect whenever it can no longer transfer data from the SCSI bus to the buffer because the buffer is full (or the transfer count is exhausted). The point at which reconnection occurs is controlled by the Buffer Empty Ratio (MODE SELECT Page 2 byte 3). This ratio determines how low the buffer level must get via data transfer to disk before reconnection is attempted. After a successful reconnection, the SCSI bus-to-buffer transfer operation will resume.

5.11.8 SEEK COMMAND: OPCODE = 0B(hex)

The SEEK command (Table 5-20) requests that the drive seek to the specified logical block address.

TABLE 5-20 SEEK Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $0B_H$							
1	LUN = 0		(MSB) LOGICAL BLOCK ADDRESS					
2-3	LOGICAL BLOCK ADDRESS (LSB)							
4	RESERVED = 0							
5	VU = 0		RESERVED = 0				F	L

LOGICAL BLOCK ADDRESS (Byte 1, Bits 5-0; Bits 2-3) - Specifies the logical block to which the actuator will be repositioned after the SEEK operation is complete.

5.11.9 INQUIRY COMMAND: OPCODE = 12(hex)

The INQUIRY command (Table 5-21) requests that information regarding identification of the target be sent to the initiator.

5.11.9.1 Command Structure

TABLE 5-21 INQUIRY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 12_H							
1	LUN = 0			RESERVED = 0				
2-3	RESERVED = 0							
4	ALLOCATION LENGTH (BYTES)							
5	VU = 0		RESERVED = 0				F	L

ALLOCATION LENGTH - Specifies the maximum number of bytes that the initiator has allocated for returned INQUIRY data. A value of 00 indicates that no data will be returned. Acceptable values are 00-FF_H. The ***ProDrive*** will terminate the DATA IN phase when the allocation length bytes have been transferred or when all available INQUIRY data have been transferred to the initiator, whichever is less. (For the ***ProDrive***, an allocation length of 130 (82_H) is recommended.)

5.11.9.2 INQUIRY DATA Format

TABLE 5-22 INQUIRY DATA Format

Bit / Byte	7	6	5	4	3	2	1	0
0	PERIPHERAL DEVICE TYPE = 0							
1	RMB = 0	DEVICE TYPE QUALIFIER = 0						
2	RESERVED = 0		ECMA VERSION = 0			ANSI VERSION = 1		
3	RESERVED = 0				RESPONSE DATA FORMAT = 1			
4	ADDITIONAL LIST LENGTH							

PERIPHERAL DEVICE TYPE (Byte 0) - Set to a value of zero for the ***ProDrive*** (Direct Access Device), unless the LUN specified in the Command Descriptor Block is invalid. If the LUN is invalid, the peripheral device type is set to $7F_H$. The reset of the data bytes is not affected and are returned as if the LUN was set to a value of zero.

RMB - REMOVABLE MEDIUM BIT (Byte 1, Bit 7) - Always set to zero for the ***ProDrive*** to indicate non-removable media.

DEVICE TYPE QUALIFIER (Byte 1, Bits 6-0) - Not supported by ***ProDrive***; it is set to a value of zero.

ECMA VERSION (Byte 2, Bits 5-3) - Set to zero to indicate that the ***ProDrive*** does not claim compliance to the European Computer Manufacturers Association version of SCSI.

ANSI VERSION (Byte 2, Bits 2-0) - Set to one to indicate compliance with the ANSI specification for SCSI.

RESPONSE DATA FORMAT (Byte 3, Bits 3-0) - Set to one to indicate compliance with the Common Command Set proposed by an ANSC X3T9.2 working group.

ADDITIONAL LIST LENGTH (Byte 4) - Specifies the length in bytes of the list of drive identification information. The ***ProDrive*** identification information is shown on the following chart. If the allocation length of the command descriptor block is too small to transfer all of the vendor unique parameters, the additional length value will not be adjusted to reflect the truncation.

ProDrive DRIVE IDENTIFICATION INFORMATION

BYTE	Information
5	Vendor Unique = 0
6 - 7	Reserved = 0
8 - 15	Vendor Identification = 'QUANTUM'
16 - 20	Product Identification (Model) = P40S (P80S)
21 - 31	Product Identification (Part Number) = 940-40-94XX (980-80-94XX) XX is replaced by the appropriate digits
32 - 35	Microcode Revision Level (Variation Code) = 'VV' VV is replaced by the appropriate variation code
36 - 43	Microcode Date = 'MM/DD/YY' MM = month DD = day YY = year
44 - 55	Drive Serial Number = 'ccymmdd-ssss' cc = capacity (40 or 80) y = last digit of year drive built mm = month dd = day ssss = drive sequence number
56 - 97	Reserved = 0
98 - 119	Vendor Unique

NOTE: Bytes 8 through 55 are ASCII values. If the drive is not ready when the INQUIRY command is received, it will be unable to return the correct data for bytes 16-31 and 44-55. In this case, the data returned will be the default data as shown in the following table.

BYTES	DATA
16 - 31	"P30S 940-40-94XX "
44 - 55	"DRV SER NUM "

5.11.10 MODE SELECT COMMAND: OPCODE = 15(hex)

The MODE SELECT command (Table 5-23) provides a means for the initiator to specify device parameters to the drive. A MODE SELECT command will override any previous selection of device parameters, even from another initiator. Execution of the command will create a UNIT ATTENTION condition for other initiators, provided that at least one parameter is changed.

5.11.10.1 Command Structure

TABLE 5-23 MODE SELECT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 15_H							
1	LUN = 0			RESERVED = 0				SP
2	RESERVED = 0							
3	RESERVED = 0							
4	PARAMETER LIST LENGTH (BYTES)							
5	VU = 0		RESERVED = 0				F	L

When the ***ProDrive*** is powered on and the motor spins up, the most recent set of device parameters is read from an unaddressable area on the drive, and a UNIT ATTENTION condition is set for all initiators. (See the Saved Mode Table, Section 5.10.)

- If the parameter values cannot be successfully read from the Saved Mode Table, they will revert to their default values as shipped from the factory and the additional sense code will be set to $2A_H$ as if another initiator altered the parameters.
- If the parameter values are read successfully, the additional sense code will be set to 29_H to indicate a reset.

NOTE: If bit 1, Byte 2 of MODE SELECT, Page 39_H is set to a value of one, the UNIT ATTENTION condition will not occur, see Section 5.11.10.5.

SP - SAVE PARAMETERS (Byte 1, Bit 0) - If set to one, only the saveable pages of the Current Mode Table will be copied to the Saved Mode Table. See Section 5.10 for a description of the Saved Mode Table.

PARAMETER LIST LENGTH (Byte 4) - Specifies the length in bytes of the MODE SELECT parameter list that will be transferred during the DATA OUT phase. A parameter list length of zero indicates that no data will be transferred. This condition should not be considered an error.

5.11.10.2 MODE SELECT Parameter List

The MODE SELECT parameter list (Table 5-24) contains a four byte header, followed by zero or one block descriptor, then zero or more "pages".

TABLE 5-24 MODE SELECT Parameter List

Bit / Byte	7	6	5	4	3	2	1	0
Mode Select Header:								
0	RESERVED = 0							
1	MEDIUM TYPE = 0							
2	RESERVED = 0							
3	BLOCK DESCRIPTOR LENGTH (BYTES)							
Block Descriptors								
0	DENSITY CODE = 0							
1-3	(MSB) NUMBER OF BLOCKS = 0 (LSB)							
4	RESERVED = 0							
5-7	(MSB) BLOCK LENGTH (LSB)							
Page Descriptor(s):								
0	RESERVED = 0			PAGE CODE				
1	PAGE LENGTH							
2 to n	REFER TO PAGE DESCRIPTION							

MEDIUM TYPE (Byte 1) - Set to zero for default (currently mounted medium type) since the ***ProDrive*** has non-removable media.

BLOCK DESCRIPTOR LENGTH (Byte 3) - Specifies the length in bytes of all the block descriptors. It is equal to the number of block descriptors times eight; it does not include the pages, if any. A block descriptor length of zero indicates that no block descriptors will be included in the parameter list. A single block descriptor is used for the ***ProDrive***.

BLOCK DESCRIPTORS: The block descriptors specify the logical block length for the drive including a density code, number of blocks, and block length.

DENSITY CODE (Byte 0) - Set to zero, indicating the default density of the medium, since the ***ProDrive*** uses only one density.

NUMBER OF BLOCKS (Bytes 1-3) - Specifies the number of logical blocks on the medium that meet the density code and block length in the block descriptor. A value of zero indicates that all remaining logical blocks of the drive have the medium characteristics specified by the block descriptor. Any non-zero value within the capacity of the ***ProDrive*** can be used to limit access of the drive to a certain number of blocks.

BLOCK LENGTH (Bytes 5-7) - The block length specifies the length in bytes of each logical block described by the block descriptor. For the ***ProDrive*** , allowable values are 512 (200_H), 1024 (400_H), or 2048 (800_H). The default block length is 512 (200_H).

NOTE: The block length may be altered without reformatting the drive or affecting stored data.

PAGE DESCRIPTOR(S):

PAGE CODE (Byte 0, Bits 5-0) - Pages are optional; they may be included in any order, immediately following the block descriptor. The mode parameters are divided into pages to avoid having to specify all Mode Parameters each time a MODE SELECT command is issued. A page is the minimum unit that can be specified in a MODE SELECT or MODE SENSE command. Each time a page is referenced, all parameters on that page must be specified. Changeable parameters may be set to any acceptable values; non-changeable parameters must be set to zero.

The pages are numbered for reference. Each page contains parameters grouped by functionality. For example, Page 1 contains the Read/Write Error Recovery Parameters. These are the parameters which determine drive behavior during a data handling error. The Retry Count Parameter is located on this page, as are the bits which turn on/off error detection, and determine if soft errors are reported.

The ***ProDrive*** supports the following pages:

Page	Description
01_H	Read/Write Error Recovery Parameters
02_H	Disconnect/Reconnect Control Parameters
03_H	Direct Access Device Format Parameters
04_H	Rigid Disk Drive Geometry Parameters*
37_H	Quantum Unique Control Parameters
39_H	Quantum Unique Drive Control Parameters

* Read-only. Can only be referenced via the MODE SENSE command.

PAGE LENGTH (Byte 1) - Indicates the number of bytes of the page that will follow, beginning with the first byte of flags or values and continuing consecutively. The page length must be set to the value returned by the ***ProDrive*** in the MODE SENSE Page Length byte. Otherwise, a CHECK CONDITION status with a sense key of ILLEGAL REQUEST will result.

5.11.10.3 Error Recovery Parameters, Page Code 1_H

Byte \ Bit	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 1_H					
1	PAGE LENGTH = 0_H							
2	AWRE	ARRE	TB	RC	EEC	PER	DTE	DCR
3	RETRY COUNT							
4	CORRECTION SPAN							
5	HEAD OFFSET COUNT = 0							
6	DATA STROBE OFFSET COUNT = 0							
7	RECOVERY TIME LIMIT = 0							

DCR - DISABLE CORRECTION (Byte 2, Bit 0) - Set to one indicates that the data will be transferred without correction, whether or not it is possible to correct it. A DCR bit of zero indicates that the data will be corrected if possible; uncorrectable data will be transferred with no attempt at correction, although retries will still be attempted. If RC (bit 4 of byte 2) is set to one, this bit is ignored. The default is zero.

DTE - DISABLE TRANSFER ON ERROR (Byte 2, Bit 1) - Set to one indicates that the ***ProDrive*** will create the CHECK CONDITION status immediately upon detection of an error, if PER (bit 2 of byte 2) is also set to one. Data transfer to the initiator will be terminated; the block in error may or may not be transferred to the initiator dependingon the setting of the TB bit. A DTE bit set to zero enables data transfer for any data which can be recovered within the limits of the Error Recovery Flags. Any errors that would be posted are not posted until the transfer length is exhausted. If PER is zero, or RC is one, this bit is ignored. The default is zero.

PER - POST ERROR (Byte 2, Bit 2) - Set to zero indicates that the ***ProDrive*** will not create the CHECK CONDITION status for errors recovered within the limits established by the other Error Recovery Flags. Recovery procedures exceeding the limits established by the other Error Recovery Flags will be posted. The transfer may terminate prior to exhausting the transfer length depending on the error and state of the other Error Recovery Flags. A PER bit (bit 2 of byte 2) set to one will enable reporting of the CHECK CONDITION status for detected errors, with the appropriate sense key. If multiple errors occur, the sense data will report the block address of the unrecoverable error;if no unrecoverable error occurred, it will report the last block with recovered error. The default is zero.

EEC - ENABLE EARLY CORRECTION (Byte 2, Bit 3) - Set to one indicates that the ***ProDrive*** will use its ECC algorithm if two consecutive equal error syndromes (non-zero syndromes) are detected. It will not perform read retries before applying correction unless it determines the error to be uncorrectable. Seek or positioning retries and the recovery procedure retries of the message system are not affected by the value of this bit. An EEC bit set to zero indicates that the ***ProDrive*** will use its normal recovery procedures when an error occurs. (See Appendix A for information on ECC.) If the RC bit is one, this bit is ignored. The default is zero.

RC - READ CONTINUOUS (Byte 2, Bit 4) - Set to one instructs the ***ProDrive*** to transfer the requested length without adding delays which would increase data integrity, i.e., delays caused by the ***ProDrive's*** error recovery schemes. Thus, to maintain a continuous flow of data and avoid delays, the ***ProDrive*** will send data which may be erroneous; ignored errors will not create the CHECK CONDITION status. An RC bit set to zero indicates that time-consuming operations for error recovery are acceptable during data transfer. The default is zero.

TB - TRANSFER BLOCK (Byte 2, Bit 5) - Set to one, if DTE bit (bit 1 of byte 2) is also set to one, indicates that the failing block data (recovered or unrecoverable) will be transferred to the initiator. A TB bit of zero, when DTE bit is set to one, indicates that the failing block will not be transferred to the initiator. If DTE is zero, or RC is one, this bit is ignored. On unrecoverable errors, TB is checked regardless of the state of DTE. The default is zero.

ARRE - AUTOMATIC READ REALLOCATION ENABLED (Byte 2, Bit 6) - Set to one indicates that the ***ProDrive*** will enable automatic reallocation of bad blocks. The execution of the automatic reallocation is similar to the function of the REASSIGN BLOCKS command, but is initiated by the ***ProDrive*** when a hard error is encountered, i.e., same non-zero ECC syndrome on two consecutive retries. (See Appendix A.) An ARRE bit set to zero indicates that the ***ProDrive*** will not perform automatic reallocation of bad blocks. If RC is one, this bit is ignored. The default is zero.

AWRE - AUTOMATIC WRITE REALLOCATION ENABLED (Byte 2, Bit 7) - Not supported by ***ProDrive***. Must be set to zero by the initiator.

RETRY COUNT (Byte 2) - The number of times the ***ProDrive*** will attempt to recover from data errors by rereading before applying correction. The default is 8.

CORRECTION SPAN (Byte 4) - Specifies the size in bits of the largest read data error on which correction may be attempted. It can be set to values from 0-11; the default is 11.

NOTE The Head Offset Count, Data Strobe Offset, and Recovery Time Limit (Bytes 5 - 7) are not supported by ***ProDrive***.

The following table summarizes the valid modes of operation on the ***ProDrive***.

EEC	PER	DTE	DCR	Description
0	0	0	0	Normal error recovery procedure. Read retries are attempted until good data is read, a stable syndrome is obtained, or the retry count is exhausted. ECC is invoked if needed when correction is possible. Complete data transfer occurs unless an uncorrectable error is encountered. Only uncorrectable errors are reported.
0	0	0	1	Same as (0,0,0,0) except no ECC correction is attempted. If read retries are not successful, data transfer is stopped and an unrecoverable error is reported.
0	0	1	0	Invalid Request
0	0	1	1	Invalid Request
0	1	0	0	Same as (0,0,0,0) except all data errors (recoverable and unrecoverable) are reported. A recoverable error is reported after the data transfer is completed.
0	1	0	1	Same as (0,0,0,0) except all data errors are reported. A data error recovered via read retries is reported after the data transfer is completed.
0	1	1	0	Read retries are attempted until good data is read, stable syndrome is obtained, or the retry count is exhausted. If needed, ECC is invoked if correction is possible. Data transfer is stopped upon error detection and all data errors are reported.
0	1	1	1	Same as (0,1,1,0) except no ECC correction is attempted. If read retries are not successful, the error is reported as unrecoverable.
1	0	0	0	ECC is invoked immediately if correction is possible. If error is uncorrectable, read retries are attempted until good data is read, a stable syndrome is obtained, or the retry count is exhausted. Complete data transfer occurs unless an unrecoverable error is encountered. Only unrecoverable errors are reported.
1	0	0	1	Invalid Request
1	0	1	0	Invalid Request
1	0	1	1	Invalid Request
1	1	0	0	Same as (1,0,0,0) except all data errors are reported. A recoverable error is reported after the data transfer is completed.
1	1	0	1	Invalid Request
1	1	1	0	Same as (1,0,0,0) except data transfer is stopped upon error detection (recoverable and unrecoverable) and all data errors are reported.
1	1	1	1	Invalid Request

5.11.10.4 Disconnect/Reconnect Control Parameters, Page Code 2_H

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 2_H					
1	PAGE LENGTH = A_H							
2	BUFFER FULL RATIO							
3	BUFFER EMPTY RATIO							
4-5	(MSB)	BUS INACTIVITY LIMIT = 0						(LSB)
6-7	(MSB)	DISCONNECT TIME LIMIT = 0						(LSB)
8-9	(MSB)	CONNECT TIME LIMIT = 0						(LSB)
10-11	RESERVED							

Buffer Full Ratio (Byte 2) - Indicates to the ***ProDrive*** how full the buffer must be prior to reconnecting, for commands requiring data transfer to the initiator (unless the buffer contains all the required data). The ***ProDrive*** disconnects on a read when there is no data in the buffer (buffer is empty). The buffer full ratio value represents the percentage of the buffer that will fill prior to reconnection, i.e., 255 (FF_H) represents 100% full, 128 (80_H) represents 50% full, and so on. Each bit is equal to 1/256th of the maximum buffer size. The default value is 0 (00_H); at least 512 bytes must be transferred to the buffer before reconnection.

Buffer Empty Ratio (Byte 3) - Indicates to the ***ProDrive*** how empty the buffer must be prior to reconnecting to fetch more data, for commands requiring data transfer from the initiator (unless the buffer can hold all the required data). This value represents the percentage of the buffer that will empty, i.e., 255 (FF_H) represents 100% empty, 128 (80_H) represents 50% empty, and so on. Each bit represents 1/256th of the maximum buffer size. The default value is 255 (FF_H); the buffer must be completely empty before reconnection.

NOTES Both the Buffer Full Ratio and the Buffer Empty Ratio are rounded (down or up, respectively) by the ***ProDrive*** to the nearest multiple of 512 bytes for commands requiring logical block transfer.

None of the remaining bytes (4 through 11) is implemented on the ***ProDrive***.

5.11.10.5 Direct-Access Device Format Parameters, Page Code 3_H

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 3_H					
1	PAGE LENGTH = 16_H							
Handling of Defects Fields								
2-3	(MSB)	TRACKS PER ZONE						(LSB)
4	(MSB)	ALTERNATE SECTORS PER ZONE = 0						
5		ALTERNATE SECTORS PER ZONE = 1_H						(LSB)
6	(MSB)	ALTERNATE TRACKS PER ZONE = 0						
7		ALTERNATE TRACKS PER ZONE = 0						(LSB)
8	(MSB)	ALTERNATE TRACKS PER VOLUME = 0						
9		ALTERNATE TRACKS PER VOLUME = 0						(LSB)
Track Format Field								
10	(MSB)	SECTORS PER TRACK = 0						
11		SECTORS PER TRACK = 0						(LSB)
Sector Format Fields								
12	(MSB)	DATA BYTES PER PHYSICAL SECTOR = 02_H						
13		DATA BYTES PER PHYSICAL SECTOR = 0						(LSB)
14	(MSB)	INTERLEAVE = 0						
15		INTERLEAVE = 1_H						(LSB)
16	(MSB)	TRACK SKEW FACTOR = 0						
17		TRACK SKEW FACTOR = 07_H						(LSB)
18	(MSB)	CYLINDER SKEW FACTOR = 0						
19		CYLINDER SKEW FACTOR = $0F_H$						(LSB)
Drive Type Field								
20	SSEC=1	HSEC=0	RMB=0	SURF=0	INS=0	RESERVED=0		
21-23	RESERVED = 0							

HANDLING OF DEFECTS FIELDS:

TRACKS PER ZONE (Byte 2-3) - Indicates the number of tracks per defect zone on the ***ProDrive***. The default value is six. This value is the only changeable field in page 3_H. A change in zone size will be effective after the FORMAT UNIT command is executed.

ALTERNATE SECTORS PER ZONE (Bytes 4-5) - Indicates that the ***ProDrive*** will deallocate one sector per zone from the initiator addressable blocks during the FORMAT UNIT command. These sectors will be available as replaceable sectors for defective sectors.

ALTERNATE TRACKS PER ZONE (Bytes 6-7) - Set to zero; the ***ProDrive*** does not allocate alternate tracks.

ALTERNATE TRACKS PER VOLUME (Bytes 8-9) - Set to zero; the ***ProDrive*** does not allocate alternate tracks.

TRACK FORMAT FIELD:

SECTORS PER TRACK (Bytes 10-11) - Indicates the number of physical sectors the ***ProDrive*** allocates per disk track. The value of zero indicates that the ***ProDrive*** has a variable number of sectors per track (28 or 35).

SECTOR FORMAT FIELDS:

DATA BYTES PER PHYSICAL SECTOR (Bytes 12-13) - Indicates the number of data bytes the ***ProDrive*** will allocate per physical sector. This value may be different than the logical block size in the block descriptor section of the MODE SELECT data. This implies that the ***ProDrive*** set an equal number of sectors per track accordingly. The ***ProDrive*** has 512 data bytes per physical sector.

INTERLEAVE (Bytes 14-15) - The ***ProDrive*** has an interleave factor of one.

TRACK SKEW FACTOR (Bytes 16-17) - Indicates the number of physical sectors between the last logical block of one track and the first logical block on the next sequential track of the same cylinder. This field is set to 7 for the ***ProDrive***.

CYLINDER SKEW FACTOR (Bytes 18-19) -Indicates the number of physical sectors between the last logical block of one cylinder and the first logical block on the next sequential cylinder. This field is set to15 for the ***ProDrive***.

SSEC - SOFT SECTOR (Byte 20, Bit 7) - Always set to one for the ***ProDrive***, indicating that it uses soft-sector formatting.

HSEC - HARD SECTOR (Byte 20, Bit 6) - Always set to zero, indicating that the ***ProDrive*** does not use hard sector formatting. The HSEC and SSEC bits are mutually exclusive.

RMB - REMOVABLE (Byte 20, Bit 5) - Set to zero for the ***ProDrive***, indicating that the logical unit is not removable.

SURF - SURFACE (Byte 20, Bit 4) - Set to zero to indicate that the ***ProDrive*** will allocate progressive addresses to all sectors within a cylinder prior to allocating sector addresses to the next cylinder.

INHIBIT SAVE (INS) (Byte 20, Bit 3) - Set to zero to indicate that the ***ProDrive*** will save the parameters of the page defined by Page Code 4_H as a read only page.

5.11.10.6 Quantum Unique Control Parameters, Page Code 37_H

Byte \ Bit	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 37_H					
1	PAGE LENGTH = $0E_H$							
2	RESERVED = 0		PSM	SSM	WIE	PO	PE	CE
3	NUMBER OF CACHE SEGMENTS							
4	MINIMUM PREFETCH							
5	MAXIMUM PREFETCH							
6-15	RESERVED = 0							

PSM - PRESERVE SYNCHRONOUS MODE (Byte 2, Bit 5) - Set to one indicates the ***ProDrive*** will not clear the table of synchronous mode parameters for all initiators when the drive is reset. A PSM bit set to zero will cause all these parameters to be cleared when the drive is reset. The default is zero.

SSM - SEND SYNCHRONOUS MESSAGE (Byte 2, Bit 4) - Set to one indicates that the ***ProDrive*** will initiate sending the Extended Message (01) Synchronous Data Transfer Request to the initiator. A SSM bit set to zero indicates that the initiator must initiate sending the Synchronous Data Transfer Request message. The default is zero.

NOTE - The following parameters control the operation of Quantum's unique ***DisCache*** feature. See Appendix A for a description of ***DisCache***, and more information on these options.

WIE - WRITE INDEX ENABLE (Byte 2, Bit 3) - All data from WRITES create a cache segment stored in the cache and indexed by the cache table. A WIE bit set to zero indicates that the ***ProDrive*** will overwrite this segment in the cache on the next READ or WRITE. A WIE bit set to one indicates that the ***ProDrive*** will treat this segment as if it had been generated by a READ. Setting WIE to zero preserves more data in the cache from READs, increasing the likelihood that the data for subsequent READ requests will be in the cache; the magnitude of this increase depends on the size and frequency of WRITE requests. The default is zero.

PO - PREFETCH ONLY (Byte 2, Bit 2) - Set to one indicates that the ***ProDrive*** will only retain prefetch data in the cache; the originally requested read data will be overwritten with prefetch data. A PO bit set to zero indicates that both original read data and prefetched data will be retained in the segment. The default is zero.

PE - PREFETCH ENABLE (Byte 2, Bit 1) - Set to one indicates that the ***ProDrive*** will perform prefetching. A PE bit set to a value of zero indicates that no prefetching will occur. The CE bit must be set to one to enable use of the PE bit. The default is one.

CE - CACHE ENABLE (Byte 2 Bit 0) - Set to one indicates that the ***ProDrive*** will activate caching on all READS. A CE bit set to zero indicates that the ***ProDrive*** will disable caching and use the 64K RAM as a transfer buffer only. The default is one.

NUMBER OF CACHE SEGMENTS (Byte 3) - Indicates to the ***ProDrive*** the number of segments to index in the cache, i.e., the number of entries in the cache table. Valid entries are 1, 2, 4, 8, 16. Any other entry will result in a CHECK CONDITION status with a sense key of ILLEGAL REQUEST. The default is four.

MINIMUM PREFETCH (Byte 4) - Indicates to the ***ProDrive*** the minimum number of logical blocks to prefetch on a cache miss for a READ command. The valid range is 0 to 128; any value outside this range will result in a CHECK CONDITION status with a sense key of ILLEGAL REQUEST. The default value is one.

MAXIMUM PREFETCH (Byte 5) - Indicates to the ***ProDrive*** the maximum number of logical blocks to prefetch on a cache miss for a READ command. The valid range is 0 to 128; any value outside this range will result in a CHECK CONDITION status with a sense key of ILLEGAL REQUEST. The default is 16.

5.11.10.7 Quantum Unique Drive Control Parameters, Page Code 39_H

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 39_H					
1	PAGE LENGTH = 6_H							
2	DIO	DII	FDB	RUEE	FDPE	R=0	DUA	DRT
3	DDIS	DELDIS	RESERVED = 0		SSID	SCSIADR		
4-7	RESERVED = 0							

DIO - DISABLE IDENTIFY OUT (Byte 2, Bit 7) - Set to one indicates that the ***ProDrive*** will not require an IDENTIFY message from the initiator to be able to disconnect and reconnect. A DIO bit set to zero indicates that the ***ProDrive*** will require the initiator to send the IDENTIFY message to be able to disconnect. The default is zero.

DII - DISABLE IDENTIFY IN (Byte 2, Bit 6) - Set to one indicates that the ***ProDrive*** will not send an IDENTIFY message after reconnecting to an initiator. A DII bit set to zero indicates that the ***ProDrive*** will send the IDENTIFY message after reconnecting. The default is zero.

FDB - FAST DEASSERTION OF BUSY (Byte 2, Bit 5) - Not used nor required by applications using the ***ProDrive***. It is included to maintain software compatibility with Quantum's Q200 Series™ disk drives.

RUEE - REALLOCATE UNCORRECTABLE ERROR ENABLED (Byte 2, Bit 4) - Set to one indicates that the ***ProDrive*** will automatically reallocate uncorrectable hard errors if the ARRE bit in Page 1 of the Error Recovery Parameters is set. The uncorrectable (bad) data is written to a new block and a new ECC (one that is correct for this data) is appended. Reading the new block will result in a MEDIUM (re-allocated uncorrectable data read) error with Sense key set to 3, and sense code set to AA_H. Any write to the new block will clear this condition. A RUEE bit set to zero indicates that the ***ProDrive*** will not attempt automatic reallocation if the hard error encountered is determined to be uncorrectable. In this case, a CHECK CONDITION with a sense key of MEDIUM ERROR - Uncorrectable Data Error will result. The default is zero.

FDPE - FILL DATA PATTERN ENABLED (Byte 2, Bit 3) - Set to one indicates that the ***ProDrive*** will write the data pattern specified in Byte 2 of the FORMAT UNIT command into every user-accessible sector of the drive when a FORMAT UNIT command is executed. A FDPE bit set to zero indicates that the ***ProDrive*** will ignore the information in Byte 2 of the FORMAT UNIT command. Issuing a FORMAT UNIT command will typically cause loss of data, even if FDPE is set to zero; users should back up data prior to formatting. The default is zero.

NOTE: Bit 3 of byte 2 is reserved; it must be set to zero.

DUA - DISABLE UNIT ATTENTION (Byte 2, Bit 1) - Set to one indicates that the ***ProDrive*** will not issue a CHECK CONDITION status with the UNIT ATTENTION sense key on the first command after a reset. The first command issued after the reset condition will be executed as usual. A DUA bit set to zero indicates that the unit attention condition will exist after the ***ProDrive*** has been powered-on or reset (by a BUS DEVICE RESET message or a "hard" RESET condition). The default is zero.

DRT - DISABLE RESELECTION TIMEOUT (Byte 2, Bit 0) - Set to one indicates that the ***ProDrive*** will not timeout during a reselection request. A DRT bit set to zero indicates that the ***ProDrive*** will clear the bus if there is no BSY response from the initiator after a selection time out period (250 msec). The default is zero.

DDIS - DISABLE DISCONNECTION (Byte 3, Bit 7) - Set to one prevents disconnection and reconnection during a data transfer (READ and WRITE). The initial disconnection due to the implied seek of a READ command is *not* prevented, but no other disconnects will occur. For a WRITE command, the ***ProDrive*** will disconnect after all data has been transferred into the buffer. A DDIS bit set to zero indicates no suppression of disconnection. The default value is zero.

DELDIS - DELAY OF DISCONNECTION (Byte 3, Bit 6) - Not used nor required by applications using the ***ProDrive***. It is included to maintain software compatibility with Quantum's Q200 Series disk drives.

SSID - SOFTWARE SELECTABLE ID (Byte 3, Bit 3) - Set to zero indicates that the drive SCSI ID will be determined by the value set by the jumpers on the drive PCB at all times. An SSID bit set to one indicates that the drive SCSI ID will be determined by the value of the SCSIADR bits (bits 0-2 of byte 3); the value set by the jumpers will be ignored. When the SSID bit is set to one, the SCSI ID will not be altered until the next RESET or power up of the drive. If upon initial power-up, the SSID bit is set to one (i.e., it was previously set and saved to the disk), the SCSIADR bits will determine the SCSI ID; otherwise, the SCSI ID will be determined by the jumpers on the PCB. The default value of SSID is zero.

SCSIADR - SCSI Address (Byte 3, Bits 2-0) - Determines the SCSI ID, if SSID (bit 3 of byte 3) is set to one. If SSID is set to zero, the SCSI ID is determined by jumpers on the PCB. See the description of SSID, above. The default is zero.

5.11.11 RESERVE COMMAND: OPCODE = 16(hex)

The RESERVE command (Table 5-25) is used to reserve a logical unit for the use of the initiator or another specified (third party) SCSI device. This command requests that the drive be reserved for the exclusive use of the initiator (or third party) until the reservation is superseded by another valid RESERVE command from the same initiator or is released by a RELEASE command from the same initiator, a BUS DEVICE RESET message from any initiator, or a "hard" RESET condition. A logical unit reservation will not be granted if the drive is reserved by another initiator. It is permissible for an initiator to reserve the drive when it is currently reserved for that initiator; in that case, the reservation identification and the extent list length will be ignored.

If the drive is reserved for another initiator, it will respond by either returning a RESERVATION CONFLICT status or, if disconnection is allowed, by queing the reserve request and disconnecting.

If, after honoring the reservation, any other initiator then subsequently attempts to perform any command on the reserved drive (other than a RELEASE command which will be ignored, or a reserve command which may be queued), the command will be rejected with RESERVATION CONFLICT status.

TABLE 5-25 RESERVE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 16_H							
1	LUN = 0			3RDPTY	3RD PARTY DEVICE ID			EXTENT
2	RESERVATION IDENTIFICATION = XX							
3-4	(MSB)	EXTENT LIST LENGTH = XX						(LSB)
5	VU=0		RESERVED = 0				F	L

EXTENT - EXTENT RESERVATION (Byte 1, Bit 0) - Must be set to zero. If this bit is set to one, the ***ProDrive*** will reject the RESERVE command with CHECK CONDITION status with the ILLEGAL REQUEST sense key.

3RDPTY - THIRD-PARTY RESERVATION (Byte 1, Bit 4) - This is an option for the RESERVE command that allows an initiator to reserve a logical unit for another SCSI device. It is intended for use in multiple-initiator systems that use the COPY command.

5.11.12 RELEASE COMMAND: OPCODE = 17(hex)

The RELEASE command (Table 5-26) is used to release a previously reserved logical unit. It is not an error for an initiator to attempt to release a reservation that is not currently active.

TABLE 5-26 RELEASE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 17_H							
1	LUN = 0			3RDPTY	3RD PARTY DEVICE ID			EXTENT
2	RESERVATION IDENTIFICATION							
3-4	RESERVED = 0							
5	VU=0		RESERVED = 0				F	L

EXTENT - EXTENT RESERVATION (Byte 1, Bit 0) - Must be set to zero. If this bit is set to one, the ***ProDrive*** will reject the RELEASE command with CHECK CONDITION status with the ILLEGAL REQUEST sense key.

3RDPTY - THIRD-PARTY RESERVATION (Byte 1, Bit 4) - An option for the RESERVE command that allows an initiator to release a logical unit that was previously reserved via the third-party reservation option. It is intended for use in multiple-initiator systems that use the COPY command. If the third-party bit is zero, the third-party release option is not requested. If it is set to one, the ***ProDrive*** will release the specified logical unit, but only if the reservation was made using the third-party reservation option by the same initiator for the same SCSI device specified in the third-party device ID field.

5.11.13 MODE SENSE COMMAND: OPCODE = 1A(hex)

The MODE SENSE command (Table 5-27) provides a means for the target to report its peripheral device parameters to the initiator. This command complements the MODE SELECT command.

5.11.13.1 MODE SENSE Command Structure

TABLE 5-27 MODE SENSE Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 1A$_H$							
1	LUN = 0			RESERVED = 0				
2	PCF		PAGE CODE					
3	RESERVED = 0							
4	ALLOCATION LENGTH							
5	VU=0		RESERVED = 0				F	L

PCF - PAGE CONTROL FIELD (Byte 2, Bits 7,6) - Defines the type of page parameter values to be returned. There are four options:

Report Current Values (PCF = 00)
The page defined by the page code is returned to the initiator with fields and bits set to current values. The current values are either:

- as set in the last successfully completed MODE SELECT command
- identical to the saved values if no MODE SELECT commands were issued since the last power-up or reset.

Fields and bits not supported by the ***ProDrive*** are set to zero.

Report Changeable Values (PCF = 01)
The page defined by the page code is returned to the initiator with all fields and bits changeable by the initiator set to ones. Fields and bits not allowed to be changed by the initiator are set to zero.

Report Default Values (PCF = 10)
The page defined by the page code is returned to the initiator with fields and bits set to the ***ProDrive's*** default values (i.e. as shipped from the factory). Fields and bits not supported by the ***ProDrive*** are set to zero. If there is confusion over whether a returned value of zero indicates a default parameter or a nonsupported parameter, the initiator can examine the changeable values.

Report Saved Values (PCF = 11)
The page defined by the page code is returned to the initiator with fields and bits set to saved values. The saved values are either:

- as set in the last successfully completed MODE SELECT command with the SP (Save Parameters) bit 0, byte 1 of the CDB set to one.
- identical to the Default values if no MODE SELECT commands with the SP bit set were ever issued (and completed successfully).

Fields and bits not supported by the ***ProDrive*** are set to zero.

PAGE CODE (Byte 2, Bits 5-0) - For all the above options, the Page Length byte value returned indicates the number of bytes the ***ProDrive*** supports within each page. This value must be specified in the Page Length field (Byte 1 of each Page Descriptor) when issuing the MODE SELECT command. The page code specifies the particular page information to be returned to the initiator in the MODE SENSE data. The ***ProDrive*** supports the following pages:

Page	Description
01_H	Read/Write Error Recovery Parameters
02_H	Disconnect/Reconnect Control Parameters
03_H	Direct-Access Device Format Parameters
04_H	Rigid Disk Drive Geometry Parameters (valid for MODE SENSE command only)
37_H	Quantum Unique Control Parameters
38_H	Read-only; included for compatibility with Q200 Series drives
39_H	Quantum Unique Drive Control Parameters
$3F_H$	Return all pages to the initiator (valid for MODE SENSE command only)

The MODE SENSE data provides information to the initiator on the configuration of the ***ProDrive's*** Format Parameters and Drive Geometry Parameters, if Pages 03_H and 04_H, respectively, are specified. If Page $3F_H$ is specified, information from all pages implemented by the ***ProDrive*** will be returned to the initiator in the MODE SENSE data. This page code is only valid in the MODE SENSE command. Specifying page code 04_H in a MODE SELECT command will result in a CHECK CONDITION status with Illegal Request sense key.

NOTE If the allocation length is set to12 bytes or less, the page code field is ignored and illegal page numbers are accepted. If the allocation length is greater than12 bytes, an illegal page code will be rejected. This allows the initiator to receive the 4-byte header and 8-byte block descriptor without receiving specific page information.

ALLOCATION LENGTH (Byte 4) - Specifies the number of bytes the initiator has allocated for returned MODE SENSE data. An allocation length of zero indicates that no MODE SENSE data will be transferred. Any other value indicates the maximum number of bytes that should be transferred. The ***ProDrive*** will terminate the DATA IN phase when allocation length bytes have been transferred or when all available MODE SENSE data have been transferred to the initiator, whichever is less.

MODE SENSE DATA - The MODE SENSE data (Table 5-28) contain a four-byte header, followed by an eight-byte block descriptor, then zero or more "pages". The meanings and organization of these data are the same as for the corresponding MODE SELECT data (Section 5.11.10.2), as modified by the option specified in the page control field of CDB byte 2.

5.11.13.2 MODE SENSE Data

Table 5-28 MODE SENSE Data

Bit / Byte	7	6	5	4	3	2	1	0
0	SENSE DATA LENGTH							
1	MEDIUM TYPE = 0							
2	WP=0	RESERVED = 0						
3	BLOCK DESCRIPTOR LENGTH = 8							

Block Descriptor

0	DENSITY CODE = 00							
1-3	(MSB)	NUMBER OF BLOCKS = 0						(LSB)
4	RESERVED = 0							
5-7	(MSB)	BLOCK LENGTH						(LSB)

Page Descriptors

0	PS	R=0	PAGE CODE					
1	PAGE LENGTH							
2 to n	REFER TO PAGE DEFINITION AND SECTION 5.11.10							

SENSE DATA LENGTH (Byte 0) - Specifies the length in bytes of the following MODE SENSE data that is available to be transferred during the DATA IN phase. The SENSE DATA length does not include itself.

WP - WRITE PROTECTED (Byte 2, Bit 7) - Always set to zero for the ***ProDrive***, indicating that the drive is write enabled.

BLOCK DESCRIPTOR LENGTH (Byte 3) - Specifies the length in bytes of all the block descriptors. It is set to eight for the ***ProDrive***.

BLOCK DESCRIPTORS: The block descriptor specifies the medium characteristics for the drive with a density code, number of blocks, and block length. These characteristics have the same meanings as the corresponding fields in the MODE SELECT parameter list (Section 5.11.10.2).

PAGE DESCRIPTORS:

PS - PARAMETERS SAVEABLE (Byte 0, Bit 7) - Set to zero in each page header indicates that the supported parameters of that page cannot be saved by the ***ProDrive***. A **PS** bit set to one indicates that the supported parameters of the page can be saved by the ***ProDrive***. All pages with parameters that can be changed by the user can be saved on the ***ProDrive***.

5.11.13.4 Rigid Disk Drive Geometry Parameters, Page Code 4_H

Byte \ Bit	7	6	5	4	3	2	1	0
0	RESERVED = 0		PAGE CODE = 4_H					
1	PAGE LENGTH = 12_H							
2	(MSB) NUMBER OF CYLINDERS = 0							
3	NUMBER OF CYLINDERS = 3_H							
4	NUMBER OF CYLINDERS = 42_H							(LSB)
5	NUMBER OF HEADS (3_H or 6_H)							
6-8	(MSB) STARTING CYLINDER - WRITE PRECOMPENSATION = 0							(LSB)
9	(MSB) STARTING CYLINDER - REDUCED WRITE CURRENT = 0							
10	STARTING CYLINDER - REDUCED WRITE CURRENT = 02_H							
11	STARTING CYLINDER - REDUCED WRITE CURRENT = $4E_H$							(LSB)
12-13	(MSB) DRIVE STEP RATE							(LSB)
14-16	(MSB) LANDING ZONE CYLINDER = 0							(LSB)
17-19	RESERVED = 0							

NOTE: The ***ProDrive*** 40S/80S disk drives have 834 cylinders.
The ***ProDrive*** 40S has three heads; the ***ProDrive*** 80S has six heads.

The write precompensation starting cylinders, reduced write current starting cylinders, and drive step rate fields are handled by the embedded SCSI controller on the ***ProDrive***.

LANDING ZONE CYLINDER (Bytes 14-16) - Specifies two's complement location where the target will position the disk heads prior to stopping the spindle with the START/STOP UNIT command. This field is only meaningful with drives which do not automatically seek to the Landing Zone before stopping the spindle. The ***ProDrive*** automatically parks the heads in the Landing Zone, using AIRLOCK, upon disconnection of power.

5.11.14 START/STOP UNIT COMMAND: OPCODE = 1B(hex)

The START/STOP UNIT command (Table 5-29) requests that the logical unit be enabled or disabled for further operations.

TABLE 5-29 START/STOP UNIT Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $1B_H$							
1	LUN = 0			RESERVED = 0				IMMED
2-3	RESERVED = 0							
4	RESERVED = 0							START
5	VU=0		RESERVED = 0				F	L

IMMED - IMMEDIATE (Byte 1, Bit 0) - Set to one indicates that status will be returned as soon as the operation is initiated. An **IMMED** bit set to zero indicates that status will be returned after the operation is completed.

START (Byte 4, Bit 0) - Set to one requests that the drive be started. A **START** bit set to zero requests that the drive be stopped. A request to start or stop the ***ProDrive*** may be repeated without error; there will be no effect on the drive if the requested condition is the same as its current condition.

NOTES. A shorting plug (labeled WS) on the ***ProDrive*** PCB disables/enables the auto-start option. If the shorting plug is not installed, no command is required to start the drive. If the shorting plug is installed, a START/STOP UNIT command is required to enable the drive for operation; this configuration is recommended only for systems requiring power sequencing of devices (usually to limit power supply surge currents).

When the ***ProDrive*** is stopped, due to a START/STOP UNIT command, both the spindle motor and actuator are disabled and do not draw appreciable currents. Starting the drive requires up to 30 seconds before commands requiring disk access can be executed. See TEST UNIT READY, Section 5.11.1, above.

5.11.15 SEND DIAGNOSTIC COMMAND: OPCODE = 1D(hex)

The SEND DIAGNOSTIC command (Table 5-30) requests the drive to perform diagnostic tests on itself. This command is usually followed by a RECEIVE DIAGNOSTIC RESULTS command, except when the SELF TEST (bit 2 of byte 1) is set to one.

5.11.15.1 Command Structure

TABLE 5-30 SEND DIAGNOSTIC Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $1D_H$							
1	LUN= 0			RESERVED = 0		SELF TEST	DEVOFL	UNITOFL
2	RESERVED = 0							
3-4	(MSB)	PARAMETER LIST LENGTH						(LSB)
5	VU=0		RESERVED = 0				F	L

SELF TEST (Byte 1, bit 2) - Set to one directs the ***ProDrive*** to complete its default self test. If the self test is requested, the parameter list length will be set to zero and no data will be transferred. If the self test is successful, the command will be terminated with a GOOD status; otherwise, the command will be terminated with a CHECK CONDITION status with the sense key set to HARDWARE ERROR.

DEVOFL - SCSI DEVICE OFF-LINE (Byte 1, Bit 1) - Not supported. If this bit is set to one on the ***ProDrive***, the command will be terminated with a CHECK CONDITION status; the sense key set will be set to ILLEGAL REQUEST with sense code invalid field.

UNITOFL - LOGICAL UNIT OFF-LINE (Byte 1, Bit 0) - Not supported. If this bit is set to one on the ***ProDrive*** , the command will be terminated with a CHECK CONDITION status; the sense key will be set to ILLEGAL REQUEST with sense code invalid field.

PARAMETER LIST LENGTH (Bytes 3-4) - Specifies the length in bytes of the parameter list that will be transferred during the DATA OUT phase. A parameter list length of zero indicates that no data will be transferred. This condition will not be considered an error.

5.11.15.2 Diagnostic Parameter List

VENDOR UNIQUE (VU) - Vendor Unique, format to be defined.

796

5.11.16 READ CAPACITY COMMAND: OPCODE = 25(hex)

The READ CAPACITY command (Table 5-31) provides a means for the initiator to request information regarding the capacity of the disk drive.

TABLE 5-31 READ CAPACITY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 25_H							
1	LUN=0			RESERVED = 0				RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6-7	RESERVED = 0							
8	VU=0		RESERVED = 0					PMI
9	VU=0		RESERVED = 0				F	L

PMI - PARTIAL MEDIUM INDICATOR (Byte 9, Bit 0) - Set to zero indicates that the information returned in the READ CAPACITY data will be the logical block address and block length (in bytes) of the last logical block of the logical unit. The logical block address in the command descriptor block will be set to zero for this option.

A **PMI** bit set to one indicates that the information returned will be the logical block address and block length (in bytes) of the last logical block address, after which a substantial delay in data transfer will be encountered. This logical block address will be greater than or equal to the logical block address specified in the command descriptor block.

The eight bytes of READ CAPACITY data shown in Table 5-32 will be sent during the DATA IN phase of the command.

TABLE 5-32 READ CAPACITY Data

Byte	DESCRIPTION		
0-3	(MSB)	LOGICAL BLOCK ADDRESS	(LSB)
4-7	(MSB)	BLOCK LENGTH	(LSB)

NOTE: Due to the physical organization of sectors and logical block assignments on the ***ProDrive***, the system designer can predict the initial LBA for all cylinders with a high level of confidence. Formatting assigns consecutive logical block addresses to sectors on a cylinder, with only rare exceptions. The designer can be relatively certain that records stored beginning at a cylinder boundary will occupy contiguous physical sectors (skipping occasional defective sectors according to the defect map) and thus will be optimally accessible. However, exceptions do occur due to grown defects and sector ID errors. Therefore it is recommended that the designer rely on the READ CAPACITY command to check for optimal file assignment.

5.11.17 READ EXTENDED COMMAND: OPCODE = 28(hex)

The READ EXTENDED command (Table 5-33) requests that the target transfer data to the initiator.

TABLE 5-33 READ EXTENDED Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 28_H							
1	LUN = 0			RESERVED = 0				RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6	RESERVED = 0							
7-8	(MSB)	TRANSFER LENGTH						(LSB)
9	VU=0			RESERVED = 0			F	L

LOGICAL BLOCK ADDRESS (Bytes 2-5)- Specifies the logical block at which the read operation is to begin.

TRANSFER LENGTH (Bytes 7-8) - Specifies the number of contiguous logical blocks of data that are to be transferred. A transfer length of zero indicates that no logical blocks are to be transferred. This condition will not be considered an error. Any other value indicates the number of logical blocks that are to be transferred.

5.11.18 WRITE EXTENDED COMMAND: OPCODE = 2A(hex)

The WRITE EXTENDED command (Table 5-34) requests that the target write the data transferred by the initiator to the medium.

TABLE 5-34 WRITE EXTENDED Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $2A_H$							
1	LUN = 0			RESERVED = 0				RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6	RESERVED = 0							
7-8	(MSB)	TRANSFER LENGTH						(LSB)
9	VU=0			RESERVED = 0			F	L

LOGICAL BLOCK ADDRESS (Bytes 2-5) - Specifies the logical block at which the write operation is to begin.

TRANSFER LENGTH (Bytes 7-8) - Specifies the number of contiguous logical blocks of data that will be transferred. A transfer length of zero indicates that no logical blocks will be transferred. This condition will not be considered an error and no data will be written. Any other value indicates the number of logical blocks that will be transferred.

5.11.19 SEEK EXTENDED COMMAND: OPCODE = 2B(hex)

The SEEK EXTENDED command (Table 5-35) requests that the logical unit seek to the specified logical block address.

TABLE 5-35 SEEK EXTENDED Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $2B_H$							
1	LUN = 0			RESERVED = 0				RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6-8	RESERVED = 0							
9	VU=0		RESERVED = 0				F	L

5.11.20 WRITE AND VERIFY COMMAND: OPCODE = 2E(hex)

The WRITE AND VERIFY command (Table 5-36) instructs the ***ProDrive*** to write the data transferred from the initiator to the medium and verify that the data is written correctly.

TABLE 5-36 WRITE AND VERIFY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $2E_H$							
1	LUN = 0			RESERVED = 0			BYTCHK	RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6	RESERVED = 0							
7-8	(MSB)	TRANSFER LENGTH						(LSB)
9	VU=0		RESERVED = 0				F	L

BYTCHK - BYTE CHECK (Byte 1, Bit 1) - Must be set to zero. The ***ProDrive*** only supports medium verification (ECC) (BYTCHK set to zero); it does not support a byte-to-byte comparison of the data on the medium and the data sent from the initiator (BYTCHK set to one). If this bit is set to one, the command will be terminated with a CHECK CONDITION status with ILLEGAL REQUEST sense key.

LOGICAL BLOCK ADDRESS (Bytes 2-5) - Specifies the logical block at which the write operation is to begin.

TRANSFER LENGTH (Bytes 7-8) - Specifies the number of contiguous logical blocks of data that will be transferred. A transfer length of zero indicates that no logical blocks will be transferred. This condition will not be considered an error and no data will be written.

5.11.21 VERIFY COMMAND: OPCODE = 2F(hex)

The VERIFY command (Table 5-37) requests that the target verify the data written on the medium.

TABLE 5-37 VERIFY Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $2F_H$							
1	LUN = 0			RESERVED = 0			BYTCHK	RELADR=0
2-5	(MSB)	LOGICAL BLOCK ADDRESS						(LSB)
6	RESERVED = 0							
7-8	(MSB)	VERIFICATION LENGTH						(LSB)
9	VU=0		RESERVED = 0				F	L

BYTCHK - BYTE CHECK (Byte 1, Bit 1) - Must be set to zero. See the explanation of BYTCHK in the WRITE AND VERIFY command (Section 5.11.20). If this bit is set to one, the command will be terminated with a CHECK CONDITION status with the ILLEGAL REQUEST sense key.

LOGICAL BLOCK ADDRESS (Bytes 2-5) - Specifies the logical block at which the verify operation is to begin.

VERIFICATION LENGTH (Bytes 7-8) - Specifies the number of continuous logical blocks of data that are to be verified. A transfer length of zero indicates that no logical blocks are to be verified. This condition will not be considered an error. Any other value indicates the number of logical blocks to be verified.

5.11.22 READ DEFECT DATA COMMAND: OPCODE = 37(hex)

The READ DEFECT DATA command (Table 5-38) requests that the target transfer the medium defect data to the initiator.

TABLE 5-38 READ DEFECT DATA Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 37_H							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0			P	G	DEFECT LIST FORMAT		
3-6	RESERVED = 0							
7-8	(MSB)	ALLOCATION LENGTH						(LSB)
9	VU = 0		RESERVED = 0				F	L

P - PRIMARY (BYTE 2, BIT 4) - Set to one indicates that the initiator requests the primary (factory) list of defects be returned.

G- GROWN (BYTE 2, BIT 3) - Set to one indicates that the initiator requests the grown list of defects be returned.

NOTE: With bits P and G both set to a value of one, the ***ProDrive*** is requested to return the primary and the grown list of defects. Only the Defect List Header bytes will be returned if both the P and G bits are set to a value of zero.

DEFECT LIST FORMAT (Byte 2, Bits 2-1) - Specifies the preferred format for the defect list to be returned by the ***ProDrive***. If a format not supported by the ***ProDrive*** is requested, the drive will return the defect data in Physical Sector Format. In this case, the ***ProDrive*** will create the CHECK CONDITION status with RECOVERED ERROR sense key after the defect list data list has been transferred. Two defect data formats are supported by the ***ProDrive***:

PHYSICAL SECTOR FROM INDEX FORMAT (101_B) - This format will return the physical cylinder, head and sector location from index of the medium defects.

BYTES OFFSET FROM INDEX (100_B) - This format will return the physical cylinder, head and the bytes offset from index of the defect location. The offset number reported represents the first byte of the defective sector.

ALLOCATION LENGTH (Bytes 7-8)- Specifies the number of bytes the initiator has allocated for returned defect data. An allocation length of zero indicates that no defect data are to be transferred. Any other value indicates the maximum number of bytes to be transferred. The ***ProDrive*** will terminate the DATA IN phase when allocation length bytes have been transferred or when all available defect data have been transferred to the initiator, whichever is less.

The defect data list contains a four byte header (Table 5-39) followed by zero or more defect descriptors.

TABLE 5-39 Defect List Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED = 0							
1	RESERVED = 0			P	G	DEFECT LIST FORMAT		
2-3	(MSB)	DEFECT LIST LENGTH						(LSB)

P AND G (Byte 1, Bits 4 & 3) - Indicate which defect list is actually returned by the ***ProDrive***. The defect list format specifies the actual format of the defect list returned by the ***ProDrive***. The formats of the defect descriptors are shown in Tables 5-40 and 5-41. The defect list length specifies the total length in bytes of the defect descriptors that follow. The defect list length is equal to eight times the number of defect descriptors. If the allocation length of the CDB is too small to transfer all of the defect descriptors, the defect list length will not be adjusted to reflect the truncation.

TABLE 5-40 Physical Sector Format

Byte	Defect Descriptor(s):		
0-2	(MSB)	CYLINDER NUMBER	(LSB)
3	HEAD NUMBER		
4-7	(MSB)	SECTOR NUMBER	(LSB)

TABLE 5-41 Bytes Offset From Index Format

Byte	Defect Descriptor(s):		
0-2	(MSB)	CYLINDER NUMBER	(LSB)
3	HEAD NUMBER		
4-7	(MSB)	BYTES OFFSET	(LSB)

5.11.23 WRITE BUFFER COMMAND: OPCODE = 3B(hex)

The WRITE BUFFER command (Table 5-42) is used in conjunction with the READ BUFFER command as a diagnostic function for testing the target memory and the SCSI bus integrity. This command will not alter the medium.

TABLE 5-42 WRITE BUFFER Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $3B_H$							
1	LOGICAL UNIT NUMBER			RESERVED = 0		MODE		
2	BUFFER ID = 0							
3-5	RESERVED = 0							
6-8	(MSB)	TRANSFER LENGTH						(LSB)
9	CONTROL BYTE							

BUFFER ID (Byte 2) - Must be be set to zero. Any other Buffer ID code will result in a CHECK CONDITION status with a sense key of ILLEGAL REQUEST (05_H).

TRANSFER LENGTH (Bytes 6-8) - Specifies the maximum number of bytes that are to be transferred during the DATA OUT phase.

The function of this command and the meaning of the transfer length field depend on the contents of the mode field. The mode field is defined as follows:

Bit2	Bit1	Bit0	MODE
0	0	0	Write combined header and data
0	0	1	Vendor unique
0	1	0	Write data
0	1	1	Reserved
1	0	0	Not supported
1	0	1	Not supported
1	1	0	Reserved
1	1	1	Reserved

5.11.23.1 COMBINED HEADER AND DATA Mode (000_B)

In this mode, data to be transferred is preceded by a four-byte header which contains all reserved bytes. These four bytes of header must be accounted for in the specified transfer length (bytes 6-8); the amount of data to be stored in the ***ProDrive*** buffer is the transfer length minus four. The initiator should attempt to ensure that the transfer length is not greater than four plus the available length returned in the header of the READ BUFFER command (mode 000_B). If the transfer length exceeds this amount, the ***ProDrive*** will return CHECK CONDITION status with the sense key of ILLEGAL REQUEST (05_H).

5.11.23.2 VENDOR UNIQUE Mode (001B)

Not used by ***ProDrive***.

5.11.23.3 DATA Mode (010B)

In this mode, the DATA OUT phase contains buffer data. The transfer length (bytes 6-8) specifies the maximum number of bytes that will be transferred during the DATA OUT phase and stored in the buffer. The initiator should attempt to ensure that the transfer length does not exceed the capacity of the buffer. (The buffer capacity can be determined by the available length field in the READ BUFFER header.) If the transfer length field specifies a transfer that would exceed the buffer capacity, the ***ProDrive*** will return CHECK CONDITION status with a sense key of ILLEGAL REQUEST (05_H).

5.11.24 READ BUFFER COMMAND: OPCODE = 3C(hex)

The READ BUFFER command (Table 5-43) is used in conjunction with the WRITE BUFFER command as a diagnostic function for testing ***ProDrive*** memory and the SCSI bus integrity. This command does not alter the medium.

TABLE 5-43 READ BUFFER Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $3C_H$							
1	LOGICAL UNIT NUMBER			RESERVED		MODE		
2	BUFFER ID = 0							
3-5	RESERVED = 0							
6-8	(MSB)	ALLOCATION LENGTH						(LSB)
9	CONTROL BYTE							

BUFFER ID (Byte 2) - Must be be set to zero. Any other Buffer ID code will result in a CHECK CONDITION status with a sense key of ILLEGAL REQUEST (05_H)

ALLOCATION LENGTH (Bytes 6-8) - Specifies the maximum number of bytes the initiator has allocated for returned information. An allocation length of zero indicates that no header or data bytes are to be transferred; any other value indicates the maximum number of bytes to be transferred.

The function of this command and the meaning of the allocation length field depend on the contents of the mode field. The mode field is defined as follows:

Bit2	Bit1	Bit0	MODE
0	0	0	Read combined header and data
0	0	1	Vendor unique
0	1	0	Read data
0	1	1	Not supported
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

5.11.24.1 COMBINED HEADER AND DATA Mode (000B)

In this mode, header and data bytes are returned to the initiator during the DATA IN phase. A four-byte READ BUFFER header (Table 5-44) is followed by data bytes from the ***ProDrive*** data buffer. The specified allocation length (bytes 6-8) must account for both header and data bytes. The ***ProDrive*** terminates the DATA IN phase when the allocated number of bytes of header plus data have been transferred or when all available header and data have been transferred to the initiator, whichever occurs first.

TABLE 5-44 READ BUFFER Header

Bit / Byte	7	6	5	4	3	2	1	0
0	RESERVED							
1-3	(MSB)	AVAILABLE LENGTH						(LSB)

AVAILABLE LENGTH (Bytes 1-3) - Specifies the total number of data bytes available in the drive's data buffer. This number is not reduced to reflect the allocation length nor is it reduced to reflect the actual number of bytes written using the WRITE BUFFER command. Following the READ BUFFER header, the ***ProDrive*** will transfer data from its data buffer. The number of data bytes transferred following the READ BUFFER header will be the allocation length minus four or 64K bytes, whichever is less.

5.11.24.2 VENDOR UNIQUE Mode (001B)

Not used by ***ProDrive***.

5.11.24.3 DATA Mode (010B)

In this mode, the DATA IN phase contains buffer data only. The ***ProDrive*** terminates the DATA IN phase when the allocated number of bytes of data have been transferred or when all data have been transferred to the initiator, whichever occurs first.

5.11.25 READ LONG COMMAND: OPCODE = E8(hex)

The READ LONG command (Table 5-45) requests that the ***ProDrive*** transfer data to the initiator. For each sector read, the ***ProDrive*** will transfer 512 data bytes followed by 6 ECC bytes.

TABLE 5-45 READ LONG Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = $E8_H$							
1	LUN = 0			(MSB) LOGICAL BLOCK ADDRESS				
2-3	LOGICAL BLOCK ADDRESS							(LSB)
4	TRANSFER LENGTH							
5	VU = 0		RESERVED = 0				F	L

LOGICAL BLOCK ADDRESS - Specifies the logical block at which the READ LONG operation will begin.

TRANSFER LENGTH - Specifies the number of logical blocks to be transferred. A transfer length of zero indicates that no logical blocks are to be transferred. Acceptable values are 00-FF_H.

5.11.26 WRITE LONG COMMAND: OPCODE = EA(hex)

The WRITE command (Table 5-19) requests that the data transferred to the ***ProDrive*** be written in the area specified by the logical block address. The data passed during the WRITE LONG operation includes 512 data bytes followed by 6 ECC bytes for each sector. The WRITE LONG command is usually preceded by a READ LONG command. The number and order of the bytes in the WRITE LONG command should be the same as in the READ LONG command.

TABLE 5-46 WRITE LONG Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = EA_H							
1	LUN = 0			(MSB) LOGICAL BLOCK ADDRESS				
2-3	LOGICAL BLOCK ADDRESS							(LSB)
4	TRANSFER LENGTH							
5	VU = 0		RESERVED = 0				F	L

LOGICAL BLOCK ADDRESS - Specifies the logical block at which the WRITE LONG operation will begin.

TRANSFER LENGTH - Specifies the number of contiguous logical blocks of data to be transferred. A transfer length of zero indicates that logical blocks will be transferred. Acceptable values are 00-FF_H.

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6.1 GENERAL INFORMATION

The ProDrive features extremely high reliability. This is achieved through the simplicity of the mechanical design and the extensive use of microelectronics. These drives are designed for fast, easy subassembly replacement with no adjustments, greatly reducing the amount of downtime for unscheduled repairs.

6.2 MAINTENANCE PRECAUTIONS

Observing the following precautions during service activity will help avoid damage to the drive and personal injury to the service technician.

a) Do NOT open or remove the metal bubble or its seals.

b) Do not lift the drive by the faceplate or the PCB.

c) Avoid harsh shocks to the drive at any time.

d) Do not move the drive for 20 seconds after DC power is removed; this ensures that the actuator is completely locked.

6.3 PREVENTATIVE MAINTENANCE

No preventative maintenance is required for the ***ProDrive***.

6.4 MAINTENANCE LEVELS, EQUIPMENT AND SPARES

6.4.1 LEVELS OF MAINTENANCE

Corrective maintenance on the drive requires certain minimum levels of technical expertise and facilities. Capabilities in this area will vary greatly from user to user. Maintenance procedures for the ***ProDrive*** are categorized in two levels. The first level involves on-site exchange of subassemblies or the drive itself. The second level involves service center and/or factory repair or refurbishment of assemblies and the printed circuit board.

6.4.1.1 Level 1

Unit replacement, circuit board exchange, external shock mount subassembly replacement.

6.4.1.2 Level 2

Level 1 plus major disassembly and refurbishment of the drive and repair of circuit boards.

NOTE: A user's service activity should be limited to Level 1 procedures during the warranty period. The Quantum warranty is null and void if any Level 2 procedure has been attempted. In addition, no repairs are authorized within the HDA. All time and material required to restore the drive to working order will be billed at prevailing rates.

6.4.2 TOOLS, EQUIPMENT AND SPARES

6.4.2.1 Level 1

The following listed items should be available to personnel providing Level 1 maintenance on the ***ProDrive***:

- One drive control PCBA. Quantum part number 800-00-9304
- One shock mount bracket assembly, Quantum part number 480-00-0054
- A #2 Phillips tip

6.4.2.2 Level 2

If the ability to do Level 2 repairs is required, please contact Quantum for information.

APPENDIX A
DISCACHE®

Quantum's ***ProDrive Series*** Intelligent Disk Drives incorporate ***DisCache***, a 64K-byte look-ahead disk cache, to enhance drive performance. This integrated feature is user-programmable, using the MODE SELECT command, and can significantly improve system throughput. The cache parameters are programmable, so the cache can be configured in real time to best meet overall system requirements.

DISCACHE DESCRIPTION

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to "look-ahead" and automatically store the subsequent data from the disk into high-speed RAM (Random Access Memory). If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, ***DisCache*** can provide substantial time savings during half or more of all disk requests. In these instances, ***DisCache*** may save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K-byte data transfer, these delays comprise 80 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache segment. During write operations, ***DisCache*** employs a write-through design, in which data written to the drive is written immediately to the disk. This design ensures data integrity in case of a power loss.

The cache memory is 64K bytes of a DRAM buffer allocated to hold the data which can be directly accessed by the host via the READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (i.e., a multiple of the 512 byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size. In those cases where the cache memory must be used for scratch memory, as in the case of a FORMAT UNIT command, or where the size of the logical block may change, as in the MODE SELECT command, the cache will be emptied. The commands that will force emptying of the cache are:

FORMAT UNIT	READ DEFECT DATA
INQUIRY	READ LONG
MODE SELECT	REASSIGN BLOCKS
MODE SENSE	VERIFY
READ CAPACITY	WRITE LONG

PERFORMANCE BENEFITS

In a drive without ***DisCache***, during sequential reads, there would be a delay due to rotational latency even if the disk actuator were already positioned at the desired cylinder. ***DisCache*** eliminates this rotational latency time -- 8 milliseconds on average -- when requested data resides in the cache.

Moreover, the disk often must service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process may request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With ***DisCache***, even if another process interrupts, the Quantum drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, ***DisCache*** achieves it most

impressive performance gains, saving both seek and latency time -- 27 milliseconds on average -- when desired data resides in the cache.

MAXIMUM FLEXIBILITY, EASY TO USE

Quantum designed ***DisCache*** to be extremely flexible because cache performance is highly application-dependent. Programmable options enable users to adjust caching parameters to optimize performance. These options can be specified and subsequently modified using the SCSI MODE SELECT command. Table A-1 outlines the programmable parameters; the discussion following the table explains the parameters and how they can be used.

TABLE A-1 DisCache Programmable Parameters

Programmable Parameters	DisCache Function	Input Range	Default Value
Cache enable/disable	Activates cache when set (bit=1)	0,1	1
Number of Cache Segments	Sets number of cache segments to be maintained	1,2,4,8,16	4
Write Indexing Enable/Disable	Allows data from write operation to be overwritten in the cache memory to increase cache utilization when this bit is disabled (=0).	0,1	0
Prefetch Only	Allows only prefetch data to be kept in the cache; data from current read is not saved.	0,1	0
Maximum Prefetch	Sets maximum amount of data to be prefetched	0-128 logical blocks	16
Minimum Prefetch	Sets minimum amount of data to be prefetched	0-128 logical blocks	1
Prefetech Enable	Enables/disables prefetch operation	0,1	1

Through the use of these programmable parameters, the caching feature can be tailored to optimize individual system performance. The programmable parameters shown in Table A-1 can be found on MODE SELECT Page 37H. When the Cache Enable/Disable bit (Byte 2, bit 0), is set to zero, caching is disabled. Disabling the cache allows the entire 64 KB of RAM to be used as a transfer buffer. Applications requiring sustained data transfers may benefit from disabling the cache. When disabling the cache, you essentially disable the prefetching and segment divisions. The default value of this bit is one (Cache enabled).

The cache is divided into equal sized segments. Each segment contains one cache entry. A cache entry consists of the data just written to the disk or the requested READ data plus its corresponding prefetch data.

The number of cache segments (Byte 3) indicates how the cache will be divided and the number of entries in the cache table. Setting the number of cache segments to one creates one large 64 KB segment. This may be advantageous for those systems which transfer large blocks of data; however, since this one segment can only hold one cache entry, the data involved with the next access to the disk will overwrite all that is currently in the cache. Setting the number of cache segments to sixteen creates sixteen segments of 4 KB

each. With this configuration you have many different cache entries; however, your transfer buffer is limited to the cache segment size, which happens to be 4 KB in this case. Also, with a small transfer buffer, you may not be able to store the entire block transferred or, there may not be enough room for the desired amount of prefetch data. The default value is four cache segments of 16 KB each. This value was chosen as a compromise between having a large number of cache entries and having a large transfer buffer.

The ***ProDrive Series*** disk drives use a Least Recently Used segment replacement strategy. Each time there is a cache hit on a segment or when data on a segment is replaced, this segment gets time stamped as the most recently used. On a data transfer operation involving reading from or writing to the disk, this data replaces the data in the least recently used cache segment. With Write Indexing disabled (Byte 2, bit 3 set to zero), the ***ProDrive*** automatically marks the segment storing data from a WRITE as the least recently used. This strategy preserves more data in the cache from READs, increasing the likelihood that requested data lies in the cache. The default setting is zero (Write Indexing disabled).

The Prefetch Only bit determines whether the ***ProDrive*** will retain both prefetch and READ data in the cache or will retain only prefetch data. When this bit (Byte 2, bit 2) is set to one, the ***ProDrive*** will only keep prefetch data within a cache segment; the originally requested READ data will be overwritten with prefetch data. If the system anticipates that the requested READ data will not be re-read in the near future (within a certain number of other requests), there is no need to use cache space to store this READ data. Chances for a cache hit on the next READ request will be better if additional prefetch data were stored in place of the READ data in this situation. The default setting is zero (Prefetch Only off).

The size of the cache segments may affect how much data is prefetched. The requested READ data takes up a certain amount of space in the cache segment so the corresponding prefetch data could essentially occupy the rest of the space within the segment. The other factors determining prefetch size are the maximum and minimum prefetch. Values for the prefetch range from 0 to 128 (512-byte) logical blocks. The minimum prefetch indicates the minimum number of logical blocks that must be prefetched before the next drive command can be executed. The maximum prefetch indicates the maximum number of logical blocks that can be prefetched. If another command is issued to the ProDrive drive while it is prefetching, ***ProDrive*** will abort the prefetch only after it has prefetched the minimum number of logical blocks. The minimum prefetch default value is set to one logical block and the maximum prefetch default value is set to sixteen logical blocks.

The Prefetch Enable/Disable option (Byte 2, bit 1) was used by Quantum engineers when developing ***ProDrive's DisCache***. If you feel your system's performance would be better with the prefetching feature disabled, or you see no need for using look-ahead prefetching in your application, disabling the entire cache may be more beneficial than simply disabling the prefetch. The default setting is one (Prefetch enabled).

DESIGNED FOR HIGH PERFORMANCE

DisCache was designed with high performance in mind by incorporating both programmable options and low overhead. ***DisCache*** is configured by Quantum to guarantee that system disk requests are handled as a first priority and look-ahead caching occurs only during the drive's idle time. Efficient cache management ensures minimum command processing time (a few hundred microseconds) associated with this feature.

Finally, the disk drive is the ideal location for this type of look-ahead cache because here the least amount of system overhead is involved. System-level caches incur the same amount of overhead in reading requested data as in anticipating requests. In either case, the system must access the disk and delay other disk accesses as well as other operations. With ***DisCache***, anticipating requested data occurs during otherwise idle time and does not delay other disk accesses. From the system perspective, the overhead cost is minimal while the benefit may be quite significant.

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INTRODUCTION

The ***ProDrive*** disk drives are shipped from the factory as "hard sectored" drives. That is, all physical sector addresses are written on the disks before the drives are shipped. Sector size and number of sectors per track are, therefore, not user selectable. The SCSI peripheral bus uses "logical blocks" as the means of transferring data to and from the disk drives. This appendix describes the physical format of the ***ProDrive*** as it is defined at the factory prior to shipment.

TRACK FORMAT

The ***ProDrive Series*** drives use information on the disks to define the physical sectors. Each sector is capable of holding 512 bytes of data (plus 6 bytes for ECC). Tracks 0 to 589 contain 35 sectors; tracks 590 to 833 contain 28 sectors. One sector is used as a spare for every 6 tracks for defect management. (See Appendix C.) For the ***ProDrive*** 40S (2 disks, 3 heads), the first 590 cylinders have 105 physical sectors available and the last 243 cylinders have 84 sectors. The ***ProDrive*** 80S (3 disks, 6 heads) has 210 and 168 sectors available. These sectors are sequentially numbered beginning with cylinder 0, head 0 through cylinder 833, head 5 in the case of the ***ProDrive*** 80S; or cylinder 833, head 2 in the case of the ***ProDrive*** 40S. Therefore, the ***ProDrive*** 40S contains 82,029 sequentially-numbered sectors, and the ***ProDrive*** 80S contains 164,058 sequentially-numbered sectors, each capable of storing 512 bytes of data.

TRACK AND CYLINDER SKEWING

Since the ***ProDrive*** 40S/80S drives are storage subsystems with integrated SCSI controllers, the function and design of the controller can be optimized specifically for the drive. One method of optimization employed by Quantum to improve data throughput is skewing sector addresses. The purpose of track and cylinder skewing is to minimize latency time and thus increase data throughput when data is sequentially accessed to or from the disk. The two types of skewing employed, track and cylinder skewing, are described below.

TRACK SKEWING

Track skewing reduces latency time which results when the drive must switch read/write heads to access sequential data. Figure B-1 provides an example of track skewing. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and data is ready to be accessed. Since head switch times are defined on ***ProDrive***, the sector addresses can be optimally positioned across track boundaries to minimize the latency time which results when a head switch has to be performed.

Head 0	0	1	2	3	4	5	6	7	8	9	10	11	12		30	31	32	33	34
Head 1	63	64	65	66	67	68	69	70	71	35	36	37	38		58	59	60	61	62
Head 2	91	92	93	94	95	96		103	104	105	70	71	72	73	74			89	90

FIGURE B-1 Example Of A 7-Sector Track Skew
(Shown On An Outer 35-Sector Track)

CYLINDER SKEWING

Cylinder skewing is also used on ***ProDrive*** to minimize latency time during sequential accessing of data. However, instead of minimizing latency time due to head switching, as with track skewing, cylinder skewing is used to minimize latency time due to a single-cylinder seek. The next logical sector of data which crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head at a cylinder and the first sector of data on the first head at the next cylinder. Figure B-2 provides an example of cylinder skewing. Since single-cylinder seek times are defined on the drive, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time which results when a seek has to be performed.

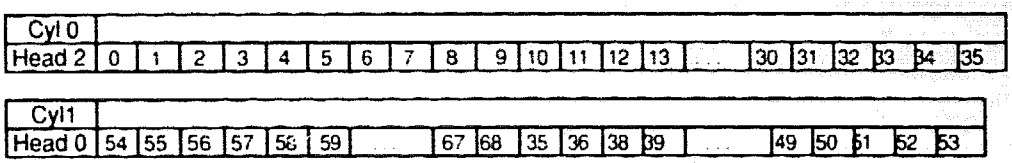


FIGURE B-2 Example Of A 15-Sector Cylinder Skew

APPENDIX C
MEDIA DEFECT HANDLING & ERROR CORRECTING CODE

INTRODUCTION

To ensure long-term data integrity, Quantum's ***ProDrive Series*** intelligent disk drives incorporate media defect handling and error correcting code capabilities. These integrated features eliminate the need for user defect maps, for writing dedicated utility software for defect mapping, and for testing time required during system integration at an OEM site. During system integration and regular use, the drive can continue to scan and compensate for any new defective sectors which may show up later on the disks.

DEFECT DETECTION

Any discrepancy between recorded data and recovered data at the sector level is defined as a data error. In high density digital recording systems, it is necessary to provide an error detection and correction scheme to enhance the operational performance and increase the reliability of the system.

Data errors can be either "soft" (those that are not readily repeatable) or "hard" (those that are repeatable with high probability). Soft errors are generally related to the signal-to-noise ratio of the system. They represent marginal conditions of the media, heads, read/write circuitry, and the controller data synchronizer circuits. Hard errors are most often due to defects, pits, scratches, or thin spots in the media. These defective media areas can be detected and skipped (not used for storage).

DEFECT MANAGEMENT

FACTORY FOUND DEFECTS

ProDrive disk drives are scanned in the factory for defective sectors on the disks. Those defective sectors are deallocated prior to shipment. A factory Defect Map, duplicated on tracks on the drive allocated for this purpose, will contain the locations of all defective sectors found in the drive.

One sector is allocated per defect zone as a replacement sector. Defects found at the factory are skipped using an "In-Line" sparing method, which replaces each sector with the next sector on the track (see Figure C1). In the rare instance where more than one defect is found within the same zone, the additional defects will be mapped into the nearest adjacent zone with a spare sector available. The defect zone size (number of tracks/zone) is a changeable parameter in operating mode page 3 via the MODE SELECT command. The default defect zone size is six tracks per zone in both the ***ProDrive*** 40S and 80S. Changing the zone size will not affect drive operation until after the execution of a FORMAT command.

This approach minimizes media used for replacement and reduces access time to the replacement sector. In addition, cylinder boundaries are well defined, with a simple relationship between each initial sector's physical and logical block addresses, thus providing the host a method to ensure that file records can be stored within cylinder boundaries for optimal accessibility.

ProDrive 40S Head	ProDrive 80S Head								Sectors/ track
CYL 0	CYL 0	x+0	x+1	x+2		25 x+ 32	26 x+ 33	27 x+ 34	28 35
1	1	28 x+ 35	xxxx	29 x+ 36		52 x+ 66	53 x+ 67	54 x+ 68	
2	2								
CYL+1 0	3								
1	4								
2	5	139 x+ 174	140 x+ 175	141 x+ 176		164 x+ 206	165 x+ 207	166 x+ 208	

NOTES
x = logical block address
xxxx = deallocated sector
Zone size is six tracks/zone (default)

FIGURE C-1 Factory Found Defects

FIELD FOUND DEFECTS

ProDrive Series disk drives also contain a Replacement Sector Map in the event additional defects are found during drive usage. Field found, or "grown" defects are also mapped into the one replacement sector located at the end of each zone. However, data from field-found defective sectors are mapped directly into the spare sector location (without shifting subsequent logical blocks, as in the case of the In-Line sparing method); see Figure C2. Similar to the factory sparing method, in the rare instance where there are more than one defect per zone, the additional defects will be mapped into the nearest adjacent zone with a spare sector available. This approach ensures that in most cases a long seek to an alternate cylinder will not be necessary in order to manage additional defects found during drive usage.

ProDrive 40S Head	ProDrive 80S Head								Sectors/ track
CYL 0	CYL 0	x+0	x+1	x+2		25 x+ 32	26 x+ 33	27 x+ 34	28 35
1	1	28 x+ 35	xxxx	30 x+ 37		53 + 67	54 x+ 68	55 x+ 69	
2	2								
CYL+1 0	3								
1	4								
2	5	140 x+ 175	141 x+ 176	142 x+ 177		165 x+ 207	166 x+ 208	29 x+ 36	

NOTES: x = logical block address
xxxx = deallocated sector
Zone size is six tracks/zone (default)

FIGURE C-2 Field Found Defects

Two software configuration "switches" (Post Error and Automatic Reallocation) are available for host control of the field replacement operation. Post Error determines whether or not the ***ProDrive*** will notify the host every time corrected data is passed from the drive. Automatic Reallocation determines whether or not, when corrected data is passed to the host, the drive will automatically add the physical location of that sector onto the Replacement Sector Map, move that sector of data into a replacement sector, then check that the sector was properly duplicated. These two software switches allow the selection of four possible options by the host. The option desired by the host will be specified via the SCSI Mode Select command. (See Section 5.11.10.)

Option 1 (Post Error off, Automatic Reallocation off): This is a "no action" option. That is, the host will not be informed that corrected data is being passed, nor will the ***ProDrive*** take any action to map out the suspect sector.

Option 2 (Post Error off, Automatic Reallocation on): This is a transparent replacement option. When corrected data is passed from the drive, it will not notify the host of the action. However, the drive will automatically add the physical location of the sector containing the corrected data onto the Replacement Sector Map, move that sector of data into a replacement sector, then verify that the move was completed correctly.

Option 3 (Post Error on, Automatic Reallocation off): Every time corrected data is passed to the host, the ***ProDrive*** will notify the host of the recovered error. The drive will not take action to map out the suspect sector.

By logging suspect block addresses passed from the drive, the host can use the SCSI REASSIGN BLOCKS command or the FORMAT UNIT command to manage new defects. The REASSIGN BLOCKS command

can be used to add new defective block locations to the Replacement Sector Map and move the data from those sectors into replacement sectors. Alternately, the drive can be reformatted using the logged suspect block addresses with the FORMAT UNIT command. (See Reformatting.)

Option 4 (Post Error on, Automatic Reallocation on): Every time corrected data is passed to the host, the ***ProDrive*** will notify the host of the recovered error. Also, the drive will automatically add the physical location of that sector onto the Replacement Sector Map, move that sector of data into a replacement sector, and verify that the move was completed correctly.

Reformatting: The SCSI FORMAT UNIT command issued from the host will cause the drive to reorganize data on the disk in a manner identical to the way it was formatted in the factory (i.e., using an In-Line sparing method). In addition to using the original factory In-Line Defect Map and the field Replacement Sector Map, the reformatting operation can also be performed using a host-supplied list of defective logical blocks. If the number of tracks per zone has been altered since the last FORMAT UNIT command, the new zone size will be used in reorganizing the spare sectors.

ERROR CORRECTING CODE

The Quantum ***ProDrive Series*** implementation of error correcting code is a 48-bit computer generated cyclic code, allowing correction of an 11 bit single burst error. In addition, a retry/correction strategy is used to avoid using ECC on soft errors.

OPERATION OF ECC:

If the syndrome is 0 (no errors), data is passed to the SCSI bus.

If the syndrome is not 0 (an error has occurred) and the DISABLE CORRECTION (DCR) bit is set, the ***ProDrive*** performs a retry. If the retry count reaches the limit, the ***ProDrive*** will attempt to use ECC to correct the data. The data will be transferred regardless of whether it is actually possible to correct the data.

If the syndrome is not 0 (an error has occurred), and

- the error is correctable and the ENABLE EARLY CORRECTION (EEC) bit is set, the ***ProDrive*** retries the read and compares the latest syndrome with the previous syndrome and if:

Latest syndrome = 0	The latest data is passed onto the SCSI bus. (Latest try had no errors)
Syndromes are equal	The ***ProDrive*** corrects the data and passes this corrected data onto the SCSI bus. (Defect error)
Syndromes are unequal	The ***ProDrive*** performs a retry. (Soft error) If the retry count has reached the limit, the ***ProDrive*** corrects the data and passes this corrected data to the SCSI bus.

- the error is correctable, and the EEC bit is zero, the ***ProDrive*** performs a retry and rereads the sector. When the EEC bit is set to zero, the ***ProDrive*** will exhaust the retry count before attempting to correct the data.

- the error is not correctable, the ProDrive performs a retry and rereads the sector. If the retry count reaches the limit, the ProDrive reports an uncorrectable data error and no data is passed.

APPENDIX D
GLOSSARY

Actuator	An actuator positions the read/write heads at the desired cylinder. The Quantum actuator consists of a rotary voice coil and the head mounting arms. One end of the head mounting arms attach to the rotor with the read/write heads attached at the opposite end. As current is applied to the rotor, it rotates, positioning the heads over any cylinder on the surface.
Block	The SCSI interface uses logical blocks when transferring data across the bus. A block of data can be set equal to 512, 1024 or 2048 bytes.
Byte	This term indicates an 8-bit unit of information.
Command Descriptor Block (CDB)	The structure used to communicate requests from an initiator to a target.
Connect	The function that occurs when an initiator selects a target to start an operation.
Cylinder	A set of tracks on multiple recording surfaces at any one actuator position or location. The ***ProDrive*** 40S and 80S have 834 data cylinders.
Data Error	Any discrepancy between recorded and recovered data at the sector level. See Appendix C.
Disconnect	The function that occurs when a target releases control of the SCSI bus, allowing it to go to the BUS FREE phase.
Disk/Platter	A very flat circular substrate upon which a magnetic thin film is deposited or coated. Each disk has two surfaces for recording information.
Initiator	An SCSI device (usually a host system) that requests an operation to be performed by another SCSI device.
Latency Time	The period of time in which the read/write heads are waiting for the data to rotate into position such that they can be accessed. Based on the disk rotating speed of 3662 RPM, the maximum latency time is 16.4 milliseconds, and the average latency time is 8.2 milliseconds.
Logical unit	A physical or virtual device addressable through a target.
Logical unit number	An encoded three-bit identifier for the logical unit.
LSB	Least Significant Bit
LUN	Logical Unit Number
ms	Millisecond (10^{-3} seconds)
MSB	Most Significant Bit
Media	The magnetic film that is deposited or coated on an aluminum substrate which is very flat and in the shape of a disk. The media is overcoated to prevent damage to the heads or media during head take off and landing.
µs	Microsecond (10^{-6} seconds)

ns	Nanosecond (10^{-9} seconds)
One	A true signal value
Reconnect	The function that occurs when a target selects an initiator to continue an operation after a disconnect
Reserved	The term used for bits, bytes, fields, and code values that are set aside for future standardization.
SCSI address	The octal representation of the unique address (0-7) assigned to an SCSI device. This address would normally be assigned and set in the SCSI device during system installation.
SCSI ID	The bit-significant representation of the SCSI address referring to one of the signal lines DB(7-0).
SCSI device	A host computer adapter or a peripheral controller or an intelligent peripheral that can be attached to the SCSI bus.
Sector	A physical portion of a track on the disk which is used to store data. The physical sector size is set at 512 bytes on the ***ProDrive***, plus 6 bytes for ECC. Each sector is preceded by ID data, which cannot be overwritten.
Shipping/ Landing Zone	A circular area inside of track 833. The heads are pulled over this area whenever DC power is removed or the disks slow below 3423 RPM for more than 2 sec. This area is used to prevent the heads from touching the surface in data areas, adding to the data integrity and reliability of Quantum drives.
Signal assertion	The act of driving a signal to the true state.
Signal negation	The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).
Signal release	The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).
Status	One byte of information sent from a target to an initiator upon completion of each command.
Surface	One side of a disk in the drive. Surface 0 is the area of the bottom disk where read/write head 0 writes and reads data.
Target	An SCSI device that performs an operation requested by an initiator.
Track	A ring of constant radius on the surface of a disk where data are recorded.
Vendor unique	Indicates bits, fields, or code values that are vendor specific.
Winchester Technology	When used in reference to a disk drive, means that the drive uses continuously loaded, low mass, high compliance head assemblies. Both the head assemblies and the disks operate in a sealed, contamination free environment to allow flying heights of 11 microinches or less. As the heads are continuously loaded, they will contact the media surface when the disk is not spinning. To prevent damaging the media or heads, overcoated media is used.

xx$_H$	Numbers followed by a capital H subscript or denoted (hex) are hexadecimal values. All other numbers are decimal values.
Zero	A false signal value.

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APPENDIX E
QUANTUM REPAIR PROCEDURE

Quantum has two service centers as shown on page iv of this manual. ***ProDrive*** disk drives may be sent to either of these service centers for repair. The following paragraphs describe the procedure for returning drives to one of Quantum's service centers.

RETURN MATERIAL AUTHORIZATION (RMA OR RA)

A) Quantum requires the following from the customer:

1) Model number.
2) Quantum's serial number.
3) Reason for return.
4) Customer's purchase order number.

B) In return, the customer will receive the following information from the Quantum Service Representative:

1) A Return Material Authorization Number (RMA or RA Number).
2) Information regarding applicable charges.
3) The address to return the drive.

REPAIR CHARGES

Flat rate charges apply for all out-of-warranty products returned to Quantum for repair. There is one flat rate charge for all repairs requiring work outside the cover, and a different flat rate for repairs requiring work inside the cover.

Repair of units shipped directly to a Quantum Repair Facility in the United States from International locations will be subject to a surcharge of seventy dollars ($70. U.S.) per shipment to cover the cost of freight forwarding and special handling.

For repair and surcharges in Europe, contact the appropriate repair facility.

PRODRIVE SERIES DRIVE REVISION IDENTIFICATION

Quantum uses a series code identification to indicate revision level of the ***ProDrive Series*** drives as they are manufactured. A series code label is attached to the drive base casting. Whenever a significant change is made to the drive, a new series code will be used to distinguish the drives with the latest change from drives which were manufactured prior to the change.


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DECstation 320 BIOS Services

Device I/O Services

The BIOS (Basic Input/Output System) is the lowest-level interface between other software (application programs and the operating system itself) and the hardware.The BIOS routines provide various device input/output services, as well as bootstrap, and print screen, and other services. Some of the services that BIOS provides, such as the graphics routines, are not available through the operating system.

All calls to the BIOS are made through software interrupts (that is, by means of assembly-language "INT x" instructions). Each I/O device is provided with a software interrupt, that transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Similarly, exit parameters are generally returned from these routines to the caller in CPU registers. To ensure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS routine. To execute a BIOS call, load the registers as indicated under the ".EN" (entry condition). (Register AH contains the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. For example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16H
```

Upon return, AL contains the ASCII character and AH contains the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Following is a quick reference list of software interrupts for all device I/O and system status services.

Service	**Software Interrupts**
Video Display	10 hex (16 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)
Floppy Disk	13 hex (19 dec)
Hard Disk	13 hex (19 dec)
Serial Communications	14 hex (20 dec)
Multi-Tasking Support	15 hex (21 dec)
Joystick	15 hex (21 dec)
Microsecond Delay	15 hex (21 dec)
Extended Memory	15 hex (21 dec)
Virtual Mode	15 hex (21 dec)
Keyboard	16 hex (22 dec)
Line Printer	17 hex (23 dec)
System Clock	1A hex (26 dec)

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Video Display

These routines provide an interface to the video display, which is the half of the console (CON) device that is for output. MS-DOS considers the video display to be the default standard output (STDOUT) device.

Software Interrupt: 10 hex (16 dec)

Function Summary:

Control Routines:

AH	=	00H	Set CRT mode
AH	=	01H	Set cursor type
AH	=	02H	Hard Disk Parameter Pointer
AH	=	03H	Get cursor position
AH	=	04H	Read light pen position
AH	=	05H	Select active page
AH	=	06H	Scroll active page up
AH	=	07H	Scroll active page down

Text Routines:

AH	=	08H	Read attribute/character
AH	=	09H	Write attribute/character
AH	=	0AH	Write character only

Graphics Routines:

AH	=	0BH	Set color palette
AH	=	0CH	Write dot
AH	=	0DH	Read Dot

Other Routines:

AH	=	0EH	Write TTY* to active page
AH	=	0FH	Get CRT mode
AH	=	13H	Write string

*Screen width is determined by the mode previously set. Some control characters (ASCII 00H-1FH) perform the usual special terminal function. These include (but are not limited to) BEL (07H), BS (08H), LF (0AH), and CR (0DH).

Note that AX is modified on all video calls.

Function Descriptions:

Set CRT Mode

Set CRT mode.

Entry Conditions:

AH = 00H
AL = mode value, as follows:

Alpha Modes

AL	=	0	40 x 25 monochrome
AL	=	1	40 x 25 color
AL	=	2	80 x 25 monochrome
AL	=	3	80 x 25 color

Graphics Modes

AL	=	4	320 x 200 color graphics
AL	=	5	320 x 200 monochrome graphics
AL	=	6	640 x 200 monochrome graphics
AL	=	7	80 x 25 monochrome with mono text adapter

Set Cursor Type

Set the cursor type and attribute.

Entry Conditions:

AH = 01H
CH = bit values:
Bits 5-6 cause an invisible or erratically blinking cursor
Bits 4-0 point to the start line for cursor within character cell
CL = bit values:
Bits 4-0 point to the end line for cursor within character cell

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Set Cursor Position

Write (set) cursor position.

Entry Conditions:

AH	=	02H
BH	=	page number (must be 0 for graphics modes or when used with mono text adapter)
DH	=	row (0 = top row)
DL	=	column (0 = leftmost position)

Get Cursor Position

Read (get) cursor position.

Entry Conditions:

AH	=	03H
BH	=	page number (must be 0 for graphics modes or when used with mono text adapter)

Exit Conditions:

DH	=	row of current cursor position (0 represents top row)
DL	=	column of current cursor position (0 represents left most column)
CH	=	cursor type currently set Bits 4-0 point to the start line for cursor within character cell
CL	=	bit values: Bits 4-0 point to the end line for cursor within character cell

Read Light Pen Position

Reads light pen position.

Entry Conditions:

AH	=	04H

Exit Conditions:

AH	0	=	light pen switch not activated
	1	=	light pen values in registers
DH	=	row of current light pen position	
DH	=	column of current light pen position	
CH	=	raster line (0-199)	
BX	=	pixel column (0-319 or 0-639)	

Select Active Page

Select active display page (valid with color graphics adapter in alpha mode).

Entry Conditions:

AH	=	05H	
AL	=	0	through 7 new page value for modes 0, 1
AL	=	0	through 3 new page value for modes 2, 3

Exit Conditions:

BH	=	contents of CRT page register
BL	=	contents of CPU page register

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Scroll Up

Scroll active page up

Entry Conditions:

AH	=	06H
AL	=	number of lines to scroll; this number of lines will be blank at the bottom of the window. (0 means blank entire window)
CH	=	row of upper left corner of scroll window
CL	=	column of upper left corner of scroll window
DH	=	row of lower right corner of scroll window
DL	=	column of lower right corner of scroll window
BH	=	attribute (alpha modes) or color (graphics modes) to be used on blank line.

Attributes:

Alpha modes (0, 1, 2, 3) and monochrome mode (7):

Bits 2, 1, 0	=	foreground color (alpha) In mono, 0 = black, 1 = underline, 7 = white. Bit 3 = foreground intensity
Bits 6, 5, 4	=	background color In mono, 7 = white, other values = black.
Bit 7	=	blink

Select foreground color 0 - 15 and background color 0 - 7 from background color list of Set Color Palette (AH = OBH).

Sample Attributes

Attribute	Alpha Modes	Mono Mode
07H	White on Black	Normal Test
0FH	Bright White on Black	High Intensity Text
87H	Blinking White on Black	Blinking Text
8FH	Blinking Bright White on Black	High Intensity Blinking Text
70H	Black on White	Reverse Video
F0H	Black on Blinking White	Blinking Reverse Video
01H	Blue on Black	Underline Text
09H	Bright Blue on Black	High Intensity Underline Text
00H	Black on Black	Invisible

Color (Graphics Mode)

BH = color palette index

The color is selected from the current palette based on the color palette index. In Modes 4 and 5, BH can be 0-3. In Mode 6, BH can be 0 or 1. All unused bits are zero. See default palettes of Set Color Palette (AH = 11).

Scroll Down

Scroll active page down.

Entry Conditions:

AH	=	07H
AL	=	number of lines to scroll (0 means blank entire window)
CH	=	row of upper left corner of scroll window
CL	=	column of upper left corner of scroll window
DH	=	row of lower right corner of scroll window
DL	=	column of lower right corner of scroll window
BH	=	attribute (alpha modes) or color (graphics modes) to be used on a blank line.

See Scroll Up (AH = 06H) for attribute values and Set Color Palette (AH = 0BH) for color values.

Read Attribute or Color/Character

Read a character and its attribute or color at the current cursor position.

Entry Conditions:

AH	=	08H
BH	=	display page number (not used in graphics modes or with mono text adapter)

Exit Conditions:

AL	=	character read
AH	=	attribute of character (alpha modes only)

Write Attribute Or Color/Character

Write a character and its attribute or color at the current cursor position.

Entry Conditions:

AH	=	09H
BH	=	display page number (not used in graphics modes)
CX	=	number of characters to write
AL	=	character to write
BL	=	attribute of character (for alpha modes) or color of character (for graphics modes). If Bit 7 of BL is set, the color of the character is XOR'ed with the currently displayed color value for the character. See Scroll Up (AH = 06H) for attribute values and Set Color Palette (AH = 0BH) for color values.

Write Character Only

Write character only at current cursor position.

Entry Conditions:

AH	=	0AH
BH	=	display page number (valid for alpha modes only)
CX	=	number of characters to write
AL	=	character to write
BL	=	color of character (graphics modes only)

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Set Color Palette

Select the color palette.

Entry Conditions:

AH = 0BH
BH = Set background color to color value in BL.
Color values are:

0 = black	8 = dark gray
1 = blue	9 = light blue
2 = green	10 = light green
3 = cyan	11 = light cyan
4 = red	12 = light red
5 = magenta	13 = light magenta
6 = yellow	14 = yellow
7 = gray	15 = white

BH = 1 Set default palette to the number (0 or 1) in BL.

In black and white modes:

BL = 0: 1 for white
BL = 1: 1 for black

In 4 color graphics modes:

BL = 0 (1=green/2=red/3=yellow)
BL = 1 (1=cyan/2=magenta/3=white)

In 16 color graphics modes:

(1=blue/2=green/3=cyan/4=red/ 5=magenta/ 6=yellow/ 7=light gray/ 8=dark gray/ 9=light blue/ 10=light green/ 11=light cyan/ 12=light red/ 13=light magenta/ 14=yellow/ 15=white)

Note: For alpha modes, Palette Entry 0 indicates the border color. For graphics mode Palette Entry 0 indicates the border and the background colors.

Note: Some colors may not appear the same on all monitors (e.g., yellow can appear brown).

Write Dot

Write a pixel (dot).

Entry Conditions:

AH	=	0CH
DX	=	row number
CX	=	column number
AL	=	color value (When Bit 7 of AL is set, the resultant color value of the dot is the exclusive OR of the current dot color value and the value in AL.)

Read Dot

Read a pixel (dot).

Entry Conditions:

AH	=	0DH
DX	=	row number
CX	=	column number

Exit Conditions:

AL	=	color value of dot read

Write TTY

Write a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions:

AH	=	0EH
AL	=	character to write
BL	=	foreground color (graphics mode)

Get CRT Mode

Get the current video mode.

Entry Conditions:

AH	=	0FH

Exit Conditions:

AL	=	current video mode. See Set CRT Mode (AH = 00H) for values AH = number of columns on screen
BH	=	current active display page

Write String

Write a string of characters.

Entry Conditions:

AH		=	13H
ES:BP		=	pointer to the string of characters to be written
CX		=	number of characters in the string to display
DX		=	starting cursor position (DH = row, DL = column)
BH		=	page number (for alpha modes)
BL		=	attribute for characters (If attributes are not in the string, see below.)
AL	0	=	Cursor is not moved, string is characters only, attribute is in BL.
	1	=	Cursor is moved to the next character position after the last character written, string is characters only, attribute is in BL.
	2	=	Cursor is not moved, string has alternating characters and attributes.
	3	=	Cursor is moved to the next character position after the last character written, string has alternating characters and attributes.

Equipment

This service returns the equipment flag (hardware configuration of the computer system) in the AX register.

Software Interrupt: 11 hex (17 dec)

The equipment flag returned in the AX register has the following meanings for each bit:

Reset	=	the indicated equipment is not in the system
Set	=	the indicated equipment is in the system
Bit 0		diskette installed
Bit 1		math coprocessor
Bits 3,2		not used
Bits 5,4		initial video mode
	01 =	40 x 25 BW on color graphics adapter
	10 =	80 x 25 BW on color graphics adapter
	11 =	80 x 25 BW on monochrome text adapter
Bits 7,6		number of diskette drives (only if Bit 0 = 1)
	00 =	1
	01 =	2
Bit 8		not used
Bits 11,10,9		number of RS232 cards
Bit 12		not used
Bit 13		not used
Bits 15,14		number of printers

Memory Size

This service returns the total number of kilobytes of RAM in the computer system (contiguous starting from address 0) in the AX register. The maximum value returned is 640 (280 hex).

Software Interrupt: 12 hex (18 dec)

Floppy Diskette Drive I/O Support

These routines provide a means to control diskette drive operation.

Software Interrupt: 13 hex (19 dec)

Function Summary:

AH	=	00H Reset all disks
AH	=	01H Return status of last disk operation
AH	=	02H Read sectors from disk
AH	=	03H Write sectors to disk
AH	=	04H Verify sectors on disk
AH	=	05H Format track on disk
AH	=	15H Read disk type
AH	=	16H Get diskette change line status
AH	=	17H Set diskette type for format

Function Descriptions:

Reset All Disks

Resets the floppy diskette system, reset associated hardware, and recalibrate all drives.

Entry Conditions:

AH = 00H

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

Return Status of Last Diskette Operation

Return the status of the last diskette operation in AH.

Entry Conditions:

AH = 01H
DL = 80H

Exit Conditions:

AH = status of the last operation.

See the following section, "Exits From All Floppy Disk Calls," for values.

Read Sectors From Disk

Read the specified sectors from disk into RAM.

Entry Conditions:

AH	=	02H
DL	=	drive number (0-1)
DH	=	head number (0-1)
CH	=	track number (0-79)
CL	=	sector number (1-15)
AL	=	number of sectors to read (1-18)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:

AH	=	03H
DL	=	drive number (0-1)
DH	=	head number (0-1)
CH	=	track number (0-79)
CL	=	sector number (1-15)
AL	=	number of sectors to write (1-18)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

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Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:

AH	=	04H
DL	=	drive number (0-1)
DH	=	head number (0-1)
CH	=	track number (0-79)
CL	=	sector number (1-18)
AL	=	number of sectors to verify (1-18)

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

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Format Track On Disk

Format the specified track.

> **Note:** Function Call 23 must be performed before using this routine.

To format 360K diskettes, the gap length for format and end of track parameters of the disk parameter table (INT 1EH) must be changed. These parameters should be restored when formatting is complete.

Entry Conditions:

AH	=	05H
DL	=	drive number (0-1)
DH	=	head number (0-1)
CH	=	track number (0-79)
AL	=	number of sectors per track (used only for DMA bound check)
ES:BX	=	pointer to sector format table consisting of four bytes per sector. The first byte is the track number. The second byte is the head number. The third byte is the sector number. The fourth byte is the sector size code:

00	=	128 bytes/sector
01	=	256 bytes/sector
02	=	512 bytes/sector
03	=	1024 bytes/sector

For Track 0, Head 1, on a nine-sector/track diskette formatted with an interleave of 1 (256 bytes/sector) the table would be:

```
00H,01H,01H,02H, 00H,01H,02H,02H, 00H,01H,03H,02H
00H,01H,04H,02H, 00H,01H,05H,02H, 00H,01H,06H,02H
00H,01H,07H,02H, 00H,01H,08H,02H, 00H,01H,09H,02H
```

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

Read Disk Type

Return the disk type.

Entry Conditions:

AH	=	15H
DL	=	drive number (0-1)

Exit Conditions:

AH	0	=	not present
	1	=	diskette with no change line.
	2	=	diskette with change line
	3	=	hard disk Get Disk Change Line Status Test to see if diskette has changed.

Get Disk Change Line Status

Test to see if diskette has changed.

Entry Conditions:

AH	=	16H
DL	=	drive number (0-1)

Exit Conditions:

AH	00	=	[NC] diskette has not changed
	06	=	[C] diskette has changed

Also see the following section called "Exits From All Floppy Disk Calls."

Set Disk Type For Format

Set the diskette type for the next FORMAT command.

Entry Conditions:

AH		=	23H
AL	00	=	not used
	01	=	360K media in a 360K drive
	02	=	360K media in a 1.2M drive
	03	=	1.2M media in a 1.2M drive 1.44M media in a 1.44M drive
	04	=	720K disk in 720K drive
DL		=	drive number (0-1)

Exit Conditions:

See the following section, "Exits From All Floppy Disk Calls."

Exits From All Floppy Disk Calls

[NC]	=	operation was successful (AH = 00H)	
[C]	=	operation failed	
AH		01H =	Bad command or parameter
		02H =	Address mark not found
		03H =	Write protected
		04H =	Sector not found
		06H =	Diskette has changed
		08H =	DMA overrun error
		09H =	DMA boundary error
		10H =	Bad CRC on disk read
		20H =	Controller failed
		40H =	Seek failed
		80H =	Device timeout

Hard Disk Support

The following routines provide access to Hard Disk operations.

Software Interrupt: 1E hex (19 dec)

Function Summary:

AH	=	00H Reset all disks
AH	=	01H Return status of last disk operation
AH	=	02H Read sectors from disk
AH	=	03H Write sectors to disk
AH	=	04H Verify sectors on disk
AH	=	05H Format track on disk
AH	=	06H Unused
AH	=	07H Unused
AH	=	08H Return current hard disk parameters
AH	=	09H Initialize hard disk parameters
AH	=	0AH Read long
AH	=	0BH Write long
AH	=	0CH Perform seek on hard disk
AH	=	0DH Reset hard disk
AH	=	0EH Unused
AH	=	0FH Unused
AH	=	10H Test for hard disk ready
AH	=	11H Recalibrate hard disk
AH	=	12H Unused
AH	=	13H Unused
AH	=	14H Controller internal diagnostic
AH	=	15H Read disk type

Reset Hard Disks

Reset the hard disk system. Reset associated hardware, and recalibrate all drives.

Entry Conditions:

AH	=	00H
DL	=	drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Return Status of Last Hard Disk Operation

Return the status of the last hard disk operation in AL.

Entry Conditions:

AH	=	01H
DL	=	80H

Exit Conditions:

AL	=	status of the last operation.

See the following section, "Exits From All Hard Disk Calls," for values.

Read Sectors From Disk

Read the specified sectors from disk into RAM.

Entry Conditions:

AH	=	02H
DL	=	drive number (80H-81)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023) (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
CL Bits 5-0	=	sector number (1-17)
AL	=	number of sectors to read (1-80)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section named "Exits From All Hard Disk Calls."

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Write Sectors To Disk

Write the specified sectors from RAM to disk.

Entry Conditions:

AH	=	03H
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023) (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
CL Bits 5-0	=	sector number (1-17)
AL	=	number of sectors to write (1-80 hex)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Verify Sectors On Disk

Verify the specified sectors.

Entry Conditions:

AH	=	04H
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023) (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
CL Bits 5-0	=	sector number (1-17)
AL	=	number of sectors verify (1-80 hex)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Format Track On Disk

Format the specified track

Entry Conditions:

AH	=	05H
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (01023) (See CL Bits 7, 6)
CL Bits 7,6	=	most significant part of cylinder number
ES:BX	=	pointer to sector format table consisting of two bytes for each sector. The first byte is 00 for a good sector, and 80H for a bad sector. The second byte is the sector number. For a 17-sector track with an interleave of 2, the table is:

00H,01H, 00H,0AH, 00H,02H, 00H,0BH, 00H,03H, 00H,0CH, 00H,04H, 00H,0DH, 00H,05H, 00H,0EH, 00H,06H, 00H,0FH, 00H,07H, 00H,10H, 00H,08H, 00H,11H, 00H,09H

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Return Current Hard Disk Parameters

Return the current parameter values for the specified hard disk.

Entry Conditions:

AH	=	08H
DL	=	drive number (80H-81H)

Exit Conditions:

DL	=	number of hard disk drives attached
DH	=	maximum usable value for head number
CH	=	least significant part of maximum usable value for cylinder number
CL Bits 7,6	=	most significant part of maximum usable value for cylinder number
CL Bits 5-0	=	maximum usable value for sector number

See also the following section, "Exits From All Hard Disk Calls."

Initialize Hard Disk Parameters

Initialize the hard disk parameters for the specified hard disk.The values are taken from the current drive parameter table pointed to by INT 41H for Drive 80H, and INT 46H for Drive 81H.

Entry Conditions:

AH	=	09H
DL	=	drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Read Long

Read specified sectors and four ECC bytes per sector from disk to RAM.

Entry Conditions:

AH	=	0AH
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023). (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
CL Bits 5-0	=	sector number (1 -17)
AL	=	number of sectors to read (1-79 hex)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Write Long

Write specified sectors plus four ECC bytes per sector from RAM to disk.

Entry Conditions:

AH	=	0BH
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023). (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
CL Bits 5-0	=	sector number (1 -17)
AL	=	number of sectors to write (1-79 hex)
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Perform Seek On Hard Disk

Seek to the specified hard disk track.

Entry Conditions

AH	=	0CH
DL	=	drive number (80H-81H)
DH	=	head number (0-15)
CH	=	least significant part of cylinder number (0-1023). (See CL Bits 7, 6)
CL Bits 7, 6	=	most significant part of cylinder number
ES:BX	=	pointer to disk buffer

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Reset Hard Disk

Reset the hard disk system. Reset associated hardware, and recalibrate all hard disk drives.

Entry Conditions:

AH = 0DH
DL = drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Test For Hard Disk Ready

Check to see if the specified hard disk drive is ready.

Entry Conditions:

AH = 10H
DL = drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Recalibrate Hard Disk

Recalibrate the specified hard disk drive.

Entry Conditions:

AH = 11H
DL = drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Controller Internal Diagnostic

Perform internal diagnostic on the hard disk controller.

Entry Conditions:

AH = 14H
DL = drive number (80H-81H)

Exit Conditions:

See the following section, "Exits From All Hard Disk Calls."

Read Disk Type

Return the disk type and the number of sectors available on the hard disk.

Entry Conditions:

AH	=	15H
DL	=	drive number (80H-81H)

Exit Conditions:

AH 0	=	Not present
3	=	Hard disk drive
CX:DX	=	Number of sectors available on the hard disk. (Assumes 512 byte sectors.)

Exits From All Hard Disk Calls

[NC]	=	operation was successful (AH = 00H)
[C]	=	operation failed
AH		
01H	=	Bad command or parameter
02H	=	Address mark not found
04H	=	Sector not found
05H	=	Reset failed
07H	=	Drive parameter command failed
09H	=	DMA boundary error
0AH	=	Bad sector flag detected
10H	=	Bad ECC on disk read
11H	=	Data corrected during read
20H	=	Controller failed
40H	=	Seek failed
80H	=	Device timeout
AAH	=	Drive not ready
BBH	=	Undefined error occurred
CCH	=	Write error

Serial Communications

These routines provide asynchronous byte stream I/O to and from the RS-232C serial communications port.

Software Interrupt: 14 hex (20 dec)

Function Summary:

AH	=	00H Initialize comm port
AH	=	01H Transmit character
AH	=	02H Receive character
AH	=	03H Get current comm status
DX	=	communication port number (0 or 1)

Function Descriptions:

Initialize Comm Port

Initialize the communication port according to the parameters in AL and DX.

Entry Conditions:

AH	=	00H
AL	=	RS-232C parameters, as follows:
DX	=	Communications port number (0 or 1)

7 6 5	4 3	2	1 0
Baud Rate	Parity	Stop Bits	Word Length

000 = 110 baud	x0 = none	0 = 1 bit	10 = 7 bits
001 = 150 baud	01 = odd	1 = 2 bits	11 = 8 bits
010 = 300 baud	11 = even		
011 = 600 baud			
100 = 1200 baud			
101 = 2400 baud			
110 = 4800 baud			
111 = 9600 baud			

Exit Conditions:

AX = RS-232 status; see "Get Current Comm Status" (AH =03H)

Transmit Character

Transmit (output) the character in AL

Entry Conditions:

AH	=	01H
AL	=	character to transmit
DX	=	port number (0 or 1)

Exit Conditions:

AH	=	RS-232 status; see "Get Current Comm Status (AH =03H) If Bit 7 is set, the routine is unable to transmit the character because of a timeout error.

AL is preserved.

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH contains the RS-232 status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout Bit (7), if set, indicates that data set ready was not received. Thus, AH is non- zero only when an error occurs. If Bit 7 is set, the other bit values are not meaningful.

Entry Conditions:

AH	=	02H
DX	=	port number (0 or 1)

Exit Conditions:

AL	=	character received
AH	=	RS-232 status; see "Get Current Comm Status" (AH =03H)

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Get Current Comm Status

Read the communication status in AX.

Entry Conditions:

AH	=	03H
DX	=	port number (0 or 1)

Exit Conditions:

AH = RS-232 status, as follows (set = true):

- Bit 0 = data ready
- Bit 1 = overrun error
- Bit 2 = parity error
- Bit 3 = framing error
- Bit 4 = break detect
- Bit 5 = transmitter holding register empty
- Bit 6 = transmitter shift register empty
- Bit 7 = timecut occurred

AL = modem status, as follows (set = true):

- Bit 0 = delta clear to send
- Bit 1 = delta data set ready
- Bit 2 = trailing edge ring detector
- Bit 3 = delta receive line signal detect
- Bit 4 = clear to send
- Bit 5 = data set ready
- Bit 6 = ring indicator
- Bit 7 = receive line signal detect

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Multi-Tasking Support

Hooks, Joystick Support, Microsecond Delay, 80286 Virtual Mode Support, Extended Memory Support.

Software Interrupt: 15 hex (21 dec)

Function Summary:

Device Open

Entry Conditions:

AH	=	80H
BX	=	Device ID
CX	=	Process ID

Device Close

Exit Conditions: None

Entry Conditions:

AH	=	81H
BX	=	Device ID
CX	=	Process ID

Exit Conditions: None

Program Terminate

Entry Conditions:

AH	=	82H
BX	=	Device ID

Exit Conditions: None

Event Wait

Entry Conditions:

AH	=	83H	
AL	=	0	Set interval
ES:BX	=		Pointer to a byte in caller's memory that has the sign bit set after the time interval expires.
CX,DX	=		The number of microseconds to elapse before pointed the high order byte in the caller's memory to by ES:BX is set.
AL	=	1	Cancel event wait

Exit Conditions: None

Joystick Support

Entry Conditions:

AH	=	84H	
DX	=	0	Read the current joystick switch setting. On return, AL contains the switch settings in Bits 4-7.
DX	=	1	Read the resistive inputs of the game adapter. The following values are returned:
			AX = Joystick A x value
			BX = Joystick A y value
			CX = Joystick B x value
			DX = Joystick B y value

Entry Conditions:

AH	=	85H	
AL	=	0	Sys Req key pressed
DX	=	1	Sys Req key released

Exit Conditions: None

Wait

Wait indicated number of microseconds.

Entry Conditions:

AH	=	86H Wait indicated number of microseconds
CX,DX	=	Number of microseconds to wait before returning.

Exit Conditions: None

Move Block of Memory

Transfers the contents of a block of memory from memory addressed above 1024K to memory addressed below 1024K. This uses the 80286 processor "protected" mode.

Entry Conditions:

AH	=	87H
ES:SI	=	A pointer to a Global Descriptor Table (GDT) as defined in the following table. The calling program must have previously set up this table.
CX	=	Number of 16-bit words to be transferred. The source and destination global descriptors must contain a length field of at least (2 * CX - 1)

GDT: Descriptor Usage (each entry is 8 bytes)

0	Dummy
1	Segment address of this GDT
2	Pointer to area from which to move data
3	Pointer to area to receive the data
4	BIOS code segment descriptor
5	BIOS stack segment descriptor

Exit Conditions:

AH	=	00H Operation successful
AH	=	01H RAM parity error
AH	=	02H Exception interrupt occurred
AH	=	03H Gating of address line 20 failed

Carry flag set if error
Zero flag set if successful

Extended Memory Size

Returns the amount of extended memory starting at address 1024K.

Entry Conditions:

AH = 88H

Exit Conditions:

AX = Amount of contiguous available memory in kilobytes starting at address 1024K.

Processor to Virtual Mode

Set the 80286 processor into protected virtual memory mode.

Entry Conditions:

AH	=	89H
ES:SI	=	Pointer to a Global Descriptor Table (GDT) set up by the calling program as defined in the following table.
BH	=	Offset within the Interrupt Descriptor Table (IDT) that contains the first eight interrupts
BL	=	Offset within the Interrupt Descriptor Table that contains the second eight hardware interrupts.

GDT:DescriptorUsage (each entry is 8 bytes)

0	Dummy
1	Segment address of this GDT
2	Pointer to the IDT
3	Pointer to user's data segment
4	Pointer to user's extra segment
5	Pointer to user's stack segment
6	Pointer to user's code segment
7	Pointer to BIOS code segment

Exit Conditions:

AH	=	00H Operation successful

Device Busy Wait Loop

Entry Conditions:

AH	=	90H		
AL	=	Type code		
		00H - 7FH	=	Non re-entrant devices
		80H - BFH	=	Re-entrant devices. ES:BX points to data block
		C0H - FFH	=	Wait only

Exit Conditions: None

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Interrupt Complete

Entry Conditions:

AH = 91H
AL = Type code (See function AH = 90H)

Exit Conditions: None

Keyboard

The following routines provide access to keyboard functions.

Software Interrupt: 16 hex (22 dec)

Function Summary:

AH = 00H Read Keyboard Input
AH = 01H Read Keyboard Status
AH = 02H Read Shift Status
AH = 03H Set Typematic Rate
AH = 05H Stuff Keyboard Buffer
AH = 10H Read Extended Keyboard Input
AH = 11H Read Extended Keyboard Status
AH = 12H Read Extended Shift Status

Function Descriptions:

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read).

Entry Conditions:

AH = 00H

Exit Conditions:

AL = ASCII value of character
AH = keyboard scan code

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Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to be read from the keyboard or not. If a character is available, return the ASCII value of the character and the key board scan code. The entry remains in the keyboard buffer (non- destructive read).

Entry Conditions:

AH = 01H

Exit Conditions:

Z = 1 no character is available
Z = 0 a character is available, in which case:
AL = ASCII value of character
AH = keyboard scan code

Get Shift Status

Return the current shift status.

Entry Conditions:

AH = 02H

Exit Conditions:

AL = current shift status (bit settings: set = true, reset = false)

Bit	0	=	RIGHT SHIFT key pressed
Bit	1	=	LEFT SHIFT key pressed
Bit	2	=	CTRL (control) key pressed
Bit	3	=	ALT (alternate mode) key
Bit	3	=	pressed
Bit	4	=	SCROLL state active
Bit	5	=	NUMBER lock engaged
Bit	6	=	CAPS lock engaged
Bit	7	=	INSERT state active

Set Typematic Rate

Entry Conditions:

AH = 03H
AL = 5
BL = Typematic rate (00 - 1F hex)
BH = Typematic delay (00 - 3 hex)

Exit Conditions: None

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Stuff Keyboard Buffer

Entry Conditions:

AH	=	05H
CH	=	Scan Code to Place in Keyboard Buffer
CL	=	ASCII Character to Place in Keyboard Buffer

Exit Conditions:

AL	=	0	Store is Successful
AL	=	1	Store is Unsuccessful
CY	=	1	Error

Read Extended Keyboard Input

Entry Conditions:

AH	=	10H

Exit Conditions:

AL	=	ASCII Character
AH	=	Scan Code

Read Extended Keyboard Status

Includes extended read interface for extended keyboard.

Entry Conditions:

AH	=	11H

Exit Conditions:

Z	=	1	No Character Available
Z	=	0	Character Available, in which case
AL	=	ASCII Character	
AH	=	Scan Code	

Read Extended Shift Status

Entry Conditions:

AH = 12H

Exit Conditions:

AL = Shift Status Byte — Bit = true, (on or depressed)
Shift Status Byte — Bit = false (or off)

Bit	0	=	Right Shift key
Bit	1	=	Left Shift key
Bit	2	=	Ctrl (control) key
Bit	3	=	Alt (alternate mode) key
Bit	4	=	Scroll Lock
Bit	5	=	Num Lock
Bit	6	=	Caps Lock
Bit	7	=	Ins(ert)

AH = Extended Shift Status —

Bit	=	1	currently depressed
Bit	=	0	not currently depressed
Bit	0	=	Left Ctrl key
Bit	1	=	Left Alt key
Bit	2	=	Right Ctrl key
Bit	3	=	Right Alt key
Bit	4	=	Scroll Lock key
Bit	5	=	Num Lock key
Bit	6	=	Caps Lock key
Bit	7	=	SysRq key

Line Printer

These routines provide an interface to the parallel line printer.

Software Interrupt: 17 hex (23 dec)

Function Summary:

AH	=	00H Print character
AH	=	01H Initialize printer port
AH	=	02H Get current printer status

Function Descriptions:

Print Character

Print a character.

Entry Conditions:

AH	=	00H
AL	=	character to be printed
DX	=	printer to be used (0-2)

Exit Conditions:

AH	=	printer status; see the following section "Get Current Printer Status (AH = 02H). If Bit 0 is set, the character could not be printed because of a timeout error.

Initialize Printer Port

Initialize the printer port.

Entry Conditions:

AH	=	01H
DX	=	printer to be used (0-2)

Exit Conditions:

AH	=	printer status; (See the following section "Get Current Printer Status" (AH = 02H)

Get Current Printer Status

Read the printer status in AH.

Entry Conditions:

AH = 02H

Exit Conditions:

AH = printer status, as follows (set = true):

Bit	0	=	timeout occurred
Bit	1	=	[unused]
Bit	2	=	[unused]
Bit	3	=	I/O error
Bit	4	=	selected
Bit	5	=	out of paper
Bit	6	=	acknowledge
Bit	7	=	not busy

(**Note:** If printer port specified by DX does not exist, the status value is not meaningful.)

System Clock

These routines provide the means of reading and setting the system clock tick counter, the CMOS read time clock, and the system alarm function.

Software Interrupt: 1A hex (26 dec)

Function Summary:

AH	=	00H Read system clock
AH	=	01H Set system clock
AH	=	02H Read CMOS time of day
AH	=	03H Set CMOS time of day
AH	=	04H Read CMOS date
AH	=	05H Set CMOS date
AH	=	06H Set the alarm
AH	=	07H Reset the alarm
AL	=	80H Set up sound multiplexer

Function Descriptions:

Read System Clock

Read the system clock value kept in RAM.

Note: The clock runs at a rate of 1,193,180/65,536 per second. (About 18.2 ticks per second.) 24 hours equals 1800B0h ticks.

Entry Conditions:

AH	=	00H

Exit Conditions:

AL	=	If the timer has not exceeded 24 hours since the last time this function was called, AL contains 0, otherwise it contains 1.
CX	=	high (most significant) portion of clock count.
DX	=	low (least significant) portion of clock count.

Set System Clock

Set the system clock value kept in RAM.

Entry Conditions:

AH	=	01H
CX	=	high (most significant) portion of clock count
DX	=	low (least significant) portion of clock count

Read CMOS Time Of Day

Read the time of day kept in CMOS.

Entry Conditions:

AH	=	02H

Exit Conditions:

CH	=	hours in BCD
CL	=	minutes in BCD
DH	=	seconds in BCD
DL	=	daylight savings time (1=yes, 0=no)

Set CMOS Time Of Day

Set the time of day kept in CMOS.

Entry Conditions:

AH	=	03H
CH	=	hours in BCD
CL	=	minutes in BCD
DH	=	seconds in BCD
DL	=	If daylight savings time, 1. Otherwise 0

Read CMOS Date

Read the date kept in CMOS

Entry Conditions:

AH	=	04H

Exit Conditions:

CH	=	century in BCD
CL	=	year in BCD
DH	=	month in BCD
DL	=	day in BCD

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Set CMOS Date

Set the date kept in CMOS

Entry Conditions:

AH	=	05H
CH	=	century in BCD
CL	=	year in BCD
DH	=	month in BCD
DL	=	day in BCD

Set The Alarm

Set the alarm function to generate an INT 4AH at the specified time. The user must provide an alarm routine and initialize the vector for interrupt 4AH to point to this routine.

Entry Conditions:

AH	=	06H
CH	=	hours in BCD
CL	=	minutes in BCD
DH	=	seconds in BCD

Exit Conditions:

[NC]	=	CMOS clock operating correctly, and no other alarm is currently in process.
[C]	=	An alarm is currently in progress, or the CMOS clock is not operating correctly.

Reset The Alarm

Reset the alarm function set by Function 6.

Entry Conditions:

AH = 07H

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MS-DOS Memory Map

High-Level Memory Map

Hex Address 0-16 Meg	Description
000000	Interrupt Vector Table (INTs 00h - FFh)
000400	ROM BIOS Data Area
000500	MS-DOS & BASIC Data Area
000600	RESERVED
000700	MS-DOS interface drivers to ROM BIOS I/O routines (IBMBIO.COM)
Note 1	MS-DOS interrupt handler service routines (INT 21h functions)
Note 1	MS-DOS structures, buffers, stack space and installable device drivers
Note 1	Resident portion of command interpreter (COMMAND.COM), Interrupt handlers for INT 22h (terminate), INT 23h (Control-Break), INT 24h (Critical Error) and code to reload the transient portion of COMMAND.COM.
Note 1	Transient Program Area. Used by external commands and utilities.
Note 1	Transient portion of COMMAND.COM Command interpreter, internal commands, batch processor, external command loader.
Note 2	End of conventional RAM
0A0000	RESERVED for EGA type display buffer
0B0000	REFERVED for MDPA type display buffer
0B8000	RESERVED for CGA type display buffer
0C0000	RESERVED for ROM BIOS extensions on I/O adapters
0F8000	ROM BIOS Initialization Diagnostic Routines
100000	Extended (upper Meg) RAM
FF8000	Duplicated code assignment of addresses 0F8000-0FFFFF

Notes:

1 These addresses are not absolute as they depend on the hardware installed and/or the software driver configuration. But the relative order of these items is preserved.

2 The Transient Program Area extends to all of the conventional RAM installed. Maximum of 640K.

Interrupt Vector Table

Hex Address Seq. Offset	Interrupt Number	Description
0:0	00	Divide by zero (CPU generated)
0:4	01	Single Step (CPU generated)
0:8	02	Non-Maskable Interrupt (H/W generated)
0:C	03	Software Break Point Interrupt
0:10	04	Arithmetic Overflow (CPU generated)
0:14	05	Print Screen
0:18	06	Invalid Op-code Exception (CPU generated)
0:1C	07	Processor Extension not available Exception (CPU generated)
0:20	08	Timer Clock Tick (H/W generated IRQ0)
0:24	09	Keyboard (H/W generated IRQ1)
0:28	0A	I/O Channel available (H/W generated IRQ9) re-directed from Slave Interrupt Controller
0:30	0B	I/O Channel available, usually secondary serial communications (H/W generated IRQ3)
0:34	0C	I/O Channel available, usually primary serial communications (H/W generated IRQ4)
0:2C	0D	I/O Channel available (H/W generated IRQ5) hard disk
0:38	0E	Floppy Disk (H/W generated IRQ6)
0:3C	0F	Printer (H/W generated IRQ7)
0:40	10	Video BIOS I/O Call
0:44	11	BIOS Equipment Check I/O Call
0:48	12	BIOS Memory Size I/O Call
0:4C	13	Diskette and Hard Disk BIOS I/O Call
0:50	14	RS-232 Communications BIOS I/O Call
0:54	15	I/O Systems BIOS Extension Call
0:58	16	Keyboard BIOS I/O Call

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Hex Address Seq. Offset	Interrupt Number	Description
0:5C	17	Printer BIOS I/O Call Interrupt Vector Table
0:60	18	Boot Strap Loader Failure Hook
0:64	19	Boot Strap Loader
0:68	1A	Time Date BIOS I/O Call
06C	1B	Keyboard Control-Break Hook
0:70	1C	Timer Clock Tick Hook
0:74	1D	Video Display Parameters Pointer
0:78	1E	Floppy Diskette Parameters Pointer
0:7C	1F	Video Graphics Characters Pointer (Characters 128-255 only)
0:80	20	MS-DOS Program Terminate
0:84	21	MS-DOS Functions I/O Call
0:88	22	MS-DOS Programs' Terminate Routine
0:8C	23	MS-DOS Programs' Control-Break Exit Routine
0:90	24	MS-DOS Programs' Critical Error Routine
0:94	25	MS-DOS Absolute Disk Read Call
0:98	26	MS-DOS Absolute Disk Write Call
0:9C	27	MS-DOS Terminate and Stay Resident Call
0:A0	28-3F	RESERVED for MS-DOS
0:CC	33	RESERVED for Mouse Driver
0:100	40	Re-vectored Diskette BIOS INT 13h I/O Call when Fixed Disk is Present
0:104	41	Fixed Disk Drive #1 parameters pointer
0:108	42	Re-vectored Video BIOS INT 10h I/O Call when optional video ROM is present.
0:10C	43 E	EGA Video Display parameters
0:110	44-45	RESERVED for BIOS
0:118	46	Fixed Disk Drive #2 parameters pointer
0:11C	47-5F	RESERVED
0:180	60-66	RESERVED

Hex Address Seq. Offset	Interrupt Number	Description
0:19C	67	RESERVED for Lotus/Intel/ Microsoft Expanded Memory Manager Support
0:1A0	68-6F	Not Used
0:1C0	70	Real-time Clock (H/W generated IRQ8)
0:1C4	71	Re-direction of old PC style INT 0Ah (IRQ2)
0:1C8	72	I/O Channel Available (H/W generated IRQ10)
0:1CC	73	I/O Channel Available (H/W generated IRQ11)
0:1D0	74	I/O Channel Available (H/W generated IRQ12)
0:1D4	75	Numeric Coprocessor (H/W generated IRQ13)
0:1D8	76	Fixed Disk (H/W generated IRQ14)
0:1DC	77	I/O Channel Available (H/W generated IRQ15)
0:1E0	78-7F	Not Used
0:200	80-85	RESERVED by BASIC
0:218	86-F0	Used by BASIC
0:3C4	F1-FF	Not Used

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ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:0	8	RS-232 Communications Adapter Installed Base Address Table (max. of 4 entries)
40:8	8	Parallel Printer Adapter Installed Base Address Table (max. of 4 entries)
40:10	2	Installed Equipment Flag (same as INT 11h return word)
40:12	1	Initialization/Diagnostic scratch byte
40:13	2	System Memory Size in kilobytes (640K max.)
40:15	2	Initialization/Diagnostic scratch word
40:17	1	Primary Keyboard Shift Status
		Bit — Description 1 — 1=Insert state is on 6 — 1=Caps Lock state is on 5 — 1=Num Lock state is on 4 — 1=Scroll Lock state is on 3 — 1=Alt key is depressed 2 — 1=Ctrl key is depressed 1 — 1=Left Shift key is depressed 0 — 1=Right Shift key is depressed
40:18	1	Secondary Keyboard Shift Status
		Bit — Description 7 — 1=Insert key is depressed 6 — 1=Caps Lock key is depressed 5 — 1=Num Lock key is depressed 4 — 1=Scroll Lock key is depressed 3 — 1=Suspend Mode is active 2 — 1=Sys Req key is depressed 1 — 1=Left Alt key is depressed 0 — 1=Left Ctrl key is depressed
40:19	1	Alt-numpad accumulator
40:1A	2	Keyboard Buffer Head pointer

ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:1C	2	Keyboard Buffer Tail pointer
40:1E	20h	16 entry Keyboard Buffer
40:3E	1	Floppy Disk Recalibration Status
		Bit **Description** 7 1=Floppy disk operation completed 6-2 Not Used 1 0=Floppy Drive 1 needs re-calibration 0 0=Floppy Drive 0 needs re-calibration
40:3F	1	Floppy Disk Motor On Status
		Bit **Description** 7 Write/Read Operation 6 Not Used 5,4 00=Drive 0 selected 0 1=Drive 1 selected 3,2 Not Used 1 1=Drive 1 motor on 0 0=Drive 0 motor on
40:40	1	Floppy disk motor on Time-out Value-Timer Clock ticks left until diskette motors are turned off
40:41	7	Floppy Disk S/W Status of last floppy disk INT 13h I/O operation
40:42	7	Floppy Disk Controller Status Byte Area
40:49	1	Current BIOS video mode
40:4A	2	Current BIOS video screen column width
40:4C	2	Current BIOS video screen buffer length in bytes
40:4E	2	Current BIOS video display page starting offset address
40:50	10h	Row/Column cursor coordinates for each of up to 8 display pages
40:60	2	Current BIOS video cursor type
40:62	1	Current BIOS video display page

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ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:63	2	Base I/O port address of the active display care
40:65	1	Copy of value written to Mode Selected Register
40:66	1	Copy of value written to Color Palette Register
40:67	4	ROM initialization code optional ROM offset/segment address storage
40:6B	1	Last unexpected hardware interrupt that occurred or FFh if it was an unexpected software interrupt
40:6C	2	Least significant word of Timer Clock Tick count
40:6F	2	Most significant word of Timer Clock Tick count
40:70	1	24-hour Timer Clock Tick rollover counter.
40:71	1	Keyboard Control-Break flag **Bit Description** 7 1-Keyboard Break 6-0 Not Used
40:72	2	Warm Restart flag = 1234h, if it's a warm start= anything else if it's a cold boot
40:74	1	Hard Disk S/W status of last INT 13h I/O operation
40:75	1	# of Hard Disk attached to system
40:76	1	Copy of Hard Disk control byte
40:77	1	Hard Disk port offset
40:78	4	Parallel Printer time-out table (max. of 4 entries)
40:7C	4	RS-232 Communications time-out table (max. of 4 entries)
40:80	2	Keyboard buffer start offset location pointer (offset from 40:0)
40:82	2	Keyboard buffer end offset location pointer (offset from 40:0)
40:84	1	EGA # of CRT Rows - 1


SOFTWARE
(CONT'D)

ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:85	2	EGA # of bytes/character in EGA Font Table
40:87	1	EGA Miscellaneous Information Byte 1

Bit	Description
7	High bit of video mode, 1 = don't clear buffer display
6,5	EGA memory size in 64K chunks 00=64K, 01=128K, 10=192K, 11=256K
4	RESERVED
3	0=EGA active, 1=not active
2	0=Write to CRT anytime 1=Wait for display enable
1	0=Color monitor attached to EGA card 1=Monochrome monitor attached to EGA card
0	0=Emulate cursor type

40:88	1	EGA Miscellaneous Information Byte 2

Bit	Description
7-4	EGA Feature Bits
30	EGA DIP switches

40:89	1	RESERVED
40:8B	1	Last floppy disk rate selected
40:8C	1	Hard disk status register copy
40:8D	1	Hard disk error register copy
40:8E	1	Hard disk interrupt flag
40:8F	1	Multi-rate floppy disk controller flag

Bit	Description
7-1	RESERVED
0	Always=1

40:90	2	Floppy drive 0/1 Media State Table
40:92	2	Floppy drive 0/1 Operation State Table
40:94	2	Floppy drive 0/1 Current Track Table

ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:96	1	Enhanced Keyboard Flags **Bit — Description** 7 — 1=Read ID bytes command in progress 6 — 1=First of ID bytes was last 5 — 1=Force Num Lock if 101-keyboard 4 — 1=101-key keyboard is attached 3 — 1=Right ALT key is depressed 2 — 1=Right Ctrl key is depressed 1 — 1=Keyboard controller E0 command was last 0 — 1=Keyboard controller E1command was last
40:97	1	Keyboard LED and Flags data area **Bit — Description** 7 — 1=Indicates 3 failures of sending data to keyboard 6 — 1=LED Update in progress 5 — 1=Re-send received from keyboard 4 — 1=Acknowledge received from keyboard 3 — 1=Not Used (Must be 0) 2 — 1=Caps Lock LED is on 1 — 1=Num Lock LED is on 0 — 1=Scroll Lock LED is on
40:98	2	Real-time Clock user wait flag offset address
40:9A	2	Real-time Clock user wait flag segment address
40:9C	2	Real-time Clock wait count low word
40:9E	2	Real-time Clock wait count high word
40:A0	1	Real-time Clock wait active flag
40:A1	7	RESERVED
40:A8	4	EGA-pointer to table of EGA pointers
40:AC	9	RESERVED

ROM BIOS Data Area

Starting Address	Length In Bytes	Description
40:B5	1	Proprietary Information Flag **Bit** **Description** 7-1 RESERVED 0 Floppy Swap DriveFlag =1, swap drives =0, don't swap drives **Note:** Valid for 2 floppy drive systems only
40:B6	4Ah	RESERVED

MS-DOS & BASIC Data Area

Starting Address	Length In Bytes	Description
50:0	1	Print Screen Status Flag =0, Print Screen not active or successful =1, Print Screen in progress =FFh, Print Screen encountered error
50:1	3	RESERVED
50:4	1	MS-DOS Single Floppy Drive Mode Status Byte =0, Logical drive A: last accessed =1, Logical drive B: last accessed
50:5	FBh	RESERVED

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Keyboard ASCII and Scan Codes

Keyboard ASCII and Scan Codes

The table in this appendix lists the keys on the DECstation 320 keyboard in the key number order, along with the hardware scan codes and ASCII code they generate. For each key, the following entries are given:

Scan Code — A value which uniquely identifies the physical key on the keyboard that is pressed.

Keyboard Legend — The physical marking(s) on the key. If there is more than one marking, the upper one is listed first.

ASCII Code — The ASCII codes associaed with the key. The four modes are:

> Normal — The normal ASCII value (returned when only the indicated key is depressed).
>
> SHIFT — The shifted ASCII value (returned when SHIFT is also depressed).
>
> CTRL — The control ASCII value (returned when CTRL is also depressed).
>
> ALT — The alternate ASCII value (returned when ALT is also depressed).

Remarks — Any remarks or special functions.

The following special symbols appear in the table:

x Values preceded by "x" are extended ASCII codes (codes preceded by an ASCII NUL, 00).

— No ASCII code is generated but the special function described in the Remarks column is performed. If no comment is included, the key does not generate a code and no function is performed.

Note: All numeric values in the table are expressed in hexadecimal.

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Keyboard Scan Codes

AT Mode KB Scan Make Code	AT Mode KB Scan Break Code	AT Mode System Scan Code and XT Mode KB Scan Make Code	AT Mode System Scan Code and XT Mode KB Scan Break Code	ASCII NORM	ASCII SFT	ASCII CTL	ASCII ALT	KEY #	Description
76	F076	01	81	1B	1B	1B	—	1	Esc
05	F005	3B	BB	3B	54	5E	x068	2	F1
06	F006	3C	BC	3C	55	5F	X069	3	F2
04	F004	3D	BD	3D	56	60	X06A	4	F3
0C	F00C	3E	BE	3E	57	61	X06B	5	F4
03	F003	3F	BF	3F	58	62	X06C	6	F5
0B	F00B	40	C0	40	59	63	X06D	7	F6
83	F083	41	C1	41	5A	64	X06E	8	F7
0A	F00A	42	C2	42	5B	65	X06F	9	F8
01	F001	43	C3	43	5C	66	X070	10	F9
09	F009	44	C4	44	5D	67	X071	11	F10
78	F078	57	D7	57	76	7F	X08A	12	F11
07	F007	58	D8	58	77	80	X08B	13	F12
E0,12	E0,F0,14								
E0,76	F0,77,7737		B7	2A	—	72	—	14	Print Scan
7E	F07E	46	C6	—	—	—	—	15	Scroll Lock
E1,14,77									
E1,F0,		E1,	E1						
14,40,		10,	9D						
77,77,		45	C5	—	—	—	—	16	Pause Break
0E	F00E	29	A9	60	7E	—	—	17	- or /
16	F016	02	82	31	21	—	X078	18	! or 1
1E	F01E	03	83	32	40	—	X079	19	@ or 2
26	F026	04	84	33	23	—	X07A	20	# or 3
25	F025	05	85	34	24	—	X07A	21	$ or 4
2E	F02E	06	86	35	25	—	X07C	22	% or 5
36	F036	07	87	36	5E	—	X07D	23	^ or 6
3D	F03D	08	88	37	26	—	X07E	24	& or 7
3E	F03E	09	89	38	2A	—	X07F	25	* or 8
46	F046	0A	8A	39	28	—	X080	26	(or 9
45	F045	0B	8B	40	29	—	X081	27	) or 0
4E	F04E	0C	8C	2D	5F	1F	X082	28	_or -
55	F055	0D	8D	3D	2B	—	X083	29	+ or =
66	F066	0E	8E	08	08	7F	—	30	Backspace
70	F070	52	D2	52	—	—	—	31	Insert

AT Mode KB Scan Make Code	AT Mode KB Scan Break Code	AT Mode System Scan Code and XT Mode KB Scan Make Code	AT Mode System Scan Code and XT Mode KB Scan Break Code	ASCII NORM	ASCII SFT	ASCII CTL	ASCII ALT	KEY #	Description
6C	F06C	47	C7	47	—	X077	—	32	Home/Clr Scn
7D	F07D	49	C9	X049	—	X084	—	33	Pg Up/Top of Text
77	F077	45	C5	—	—	—	—	34	Num lock
4A	F04A	35	B5	2F	—	—	—	35	/
7C	F07C	37	B7	2A	—	72	—	36	*/Prt Scrn/ CPSCRN
7B	F07B	4A	CA	2D	—	—	—	37	—
0D	F00D	0F	8F	09	00F	—	—	38	Tab
15	F015	10	90	71	51	11	X010	39	Q or q
1D	F01D	11	91	77	57	17	X011	40	W or w
24	F024	12	92	65	45	05	X012	41	E or e
2D	F02D	13	93	72	52	12	X013	42	R or r
2C	F02C	14	94	74	54	14	X014	43	T or t
35	F035	15	95	79	59	19	X015	44	Y or y
3C	F03C	16	96	75	55	15	X016	45	U or u
43	F043	17	97	69	49	09	X017	46	I or i
44	F044	18	98	6F	4F	0F	X018	47	O or o
4D	F04D	19	99	70	50	10	X019	48	P or p
54	F054	1A	9A	5B	7B	1B	—	49	{ or [
5B	F05B	1B	9B	5D	7D	1D	—	50	} or]
5D	F05D	2B	AB	5C	7C	1C	—	51	| or \
71	F071	53	D3	X053	—	—	—	52	Delete
69	F069	4F	CF	X04F	—	X075	—	53	End
7A	F07A	51	D1	X051	—	X076	—	54	Pg Dn
6C	F06C	47	C7	X047	37	X077	—	55	7, Home
75	F075	48	C8	X048	38	—	—	56	8 or ▲
7D	F07D	49	C9	X049	39	X084	—	57	9 or PgUp
79	F079	4E	CE	2B	—	—	—	58	+
58	F058	3A	BA	—	—	—	—	59	Caps Lock
1C	F01C	1E	9E	61	41	01	X01E	60	A or a
1B	F01B	1F	9F	73	53	13	X01F	61	S or s
23	F023	20	A0	64	44	04	X020	62	D or d
2B	F02B	21	A1	66	46	06	X021	63	F or f
34	F034	22	A2	67	47	07	X022	64	G or g
33	F033	23	A3	68	48	08	X023	65	H or h
3B	F03B	24	A4	6A	4A	0A	X024	66	J or j
42	F042	25	A5	6B	4B	0B	X025	67	K or k
4B	F04B	26	A6	6C	4C	0C	X026	68	L or l
4C	F04C	27	A7	3B	3A	—	—	69	: or ;

AT Mode KB Scan Make Code	AT Mode KB Scan Break Code	AT Mode System Scan Code and XT Mode KB Scan Make Code	AT Mode System Scan Code and XT Mode KB Scan Break Code	ASCII NORM	ASCII SFT	ASCII CTL	ASCII ALT	KEY #	Description
52	F052	28	A8	27	22	—	—	70	" or '
5A	F05A	1C	9C	0D	0D	0A	—	71	Enter
6B	F06B	4B	CB	X04B	34	X073	—	72	4 or ◀
73	F073	4C	CC	—	35	—	—	73	5
74	F074	4D	CD	X04D	36	X074	—	74	6 or ▶
12	F012	3A	AA	—	—	—	—	76	Shift
1A	F01A	2C	AC	7A	5A	1A	X02C	77	Z or z
22	F022	2D	AD	78	58	18	X020	78	X or x
21	F021	2E	AE	63	43	03	X02E	79	C or c
2A	F02A	2F	AF	76	56	16	X02F	80	V or v
32	F032	30	B0	62	42	02	X030	81	B or b
31	F031	31	B1	6E	4E	0E	X031	82	N or n
3A	F03A	32	B2	6D	4D	0D	X032	83	M or m
41	F041	33	B3	2C	3C	—	—	84	< or ,
49	F049	34	B4	2E	3E	—	—	85	> or .
4A	F04A	35	B5	2F	3F	—	—	86	? or /
59	F059	36	B6	—	—	—	—	87	Shift
75	F075	48	C8	X048	—	—	—	88	▲
69	F069	4F	CF	X04F	31	X075	—	89	1 or End
72		50						98	2 or ▼
7A	F07A	51	D1	X051	33	X076	—	91	3 or Pg Dn
14	F014	1D	9D	—	—	—	—	92	Ctrl
11	F011	38	B8	—	—	—	—	93	Alt
29	F029	39	B9	20	20	20	X020	94	Space
11	F011	E0,	E0,						
38			B8	—	—	—	—	95	Alt
14	F014	1D	9D	—	—	—	—	96	Ctrl
6B	F06B	4B	CB	X04B	—	X073	—	97	◀
72	F072	50	D0	X050	—	X075	—	98	▼
74	F074	E0,	E0,						
		4D	CD	X04D	—	X074	—	99	▶
70	F070	52	D2	X052	30	—	—	100	0 or Ins
71	F071	53	D3	X053	2E	—	—	101	. or Del
5A	F05A	1C	9C	0D	0D	0A	—	102	Enter

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