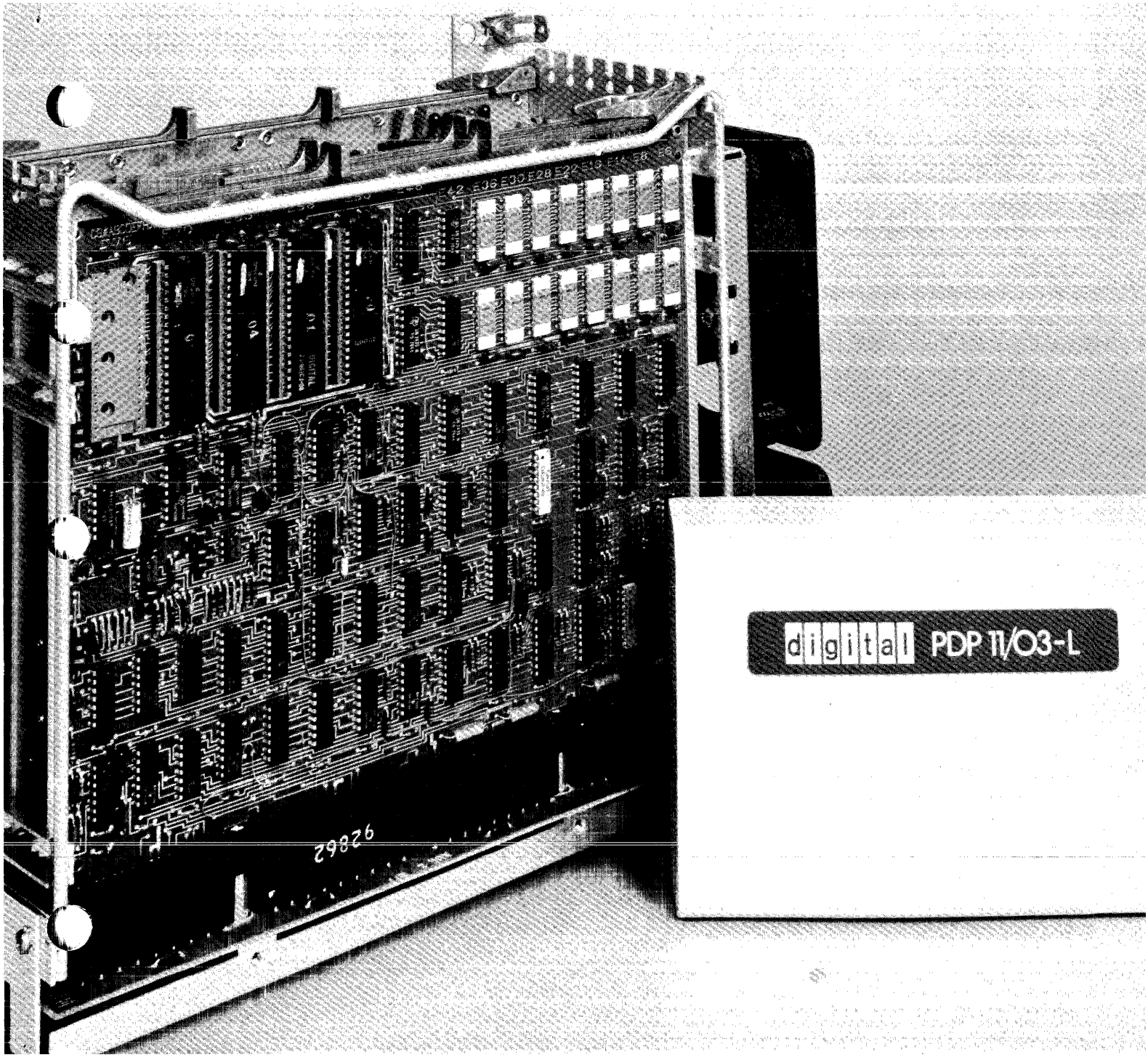
BDV11 bus terminator, bootstrap, and diagnostic ROM technical manual



BDV11 bus terminator, bootstrap, and diagnostic ROM technical manual

EK-BDV11-TM-001

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CHAPTER 1
INTRODUCTION

1.1 MANUAL SCOPE

The BDV11 is an LSI-11 bus option that provides both 120-ohm terminations for LSI-11 bus signal lines and diagnostic aids that help a user to determine the operating condition of his system. The BDV11 module can be equipped with a variety of read-only memories (ROMs) to provide the user with bootstrap and additional diagnostic capabilities; in such a case, a new option designation is assigned, e.g., BDV11-AA.

This manual gives a technical description of only the BDV11 module. Each variation of the BDV11 is described in a user manual that pertains only to that variation. The reader should be familiar with the LSI-11 microcomputer and its peripheral equipment. The necessary information can be obtained from the *1977–1978 Microcomputer Handbook** published by DIGITAL.

1.2 GENERAL DESCRIPTION

The BDV11 logic components are mounted on a 26.7 × 21.6 cm (10.5 × 8.5 in) quad-height printed circuit board (Figure 1-1) that can be inserted in any LSI-11 bus quad backplane. Physical space on the module is reserved by DIGITAL for 4K words of ROM; this ROM space contains diagnostic and bootstrap programs for a number of system components. Furthermore, user-available space is furnished on the module for 2K words of eraseable, programmable ROM (EPROM) and 16K words of ROM or EPROM. This 18K of user ROM can be executed directly or loaded into ROM for later execution; all ROM is mapped into only 256 words of LSI-11 I/O address space.

The BDV11 contains switches that permit the user to choose diagnostic and bootstrap programs for execution and a diagnostic light display that indicates failures in these programs. In addition, the BDV11 module is equipped with a green LED that monitors dc power, two test points for the dc power, a HALT/ENABLE switch that allows the user to force the CPU into the halt mode, and a RESTART switch that enables the user to re-boot the system. All of these controls are edge-mounted. A switch mounted in the interior of the module permits control of the LSI-11 line-time clock (LTC) function.

*See Paragraph 1.4 for ordering information.

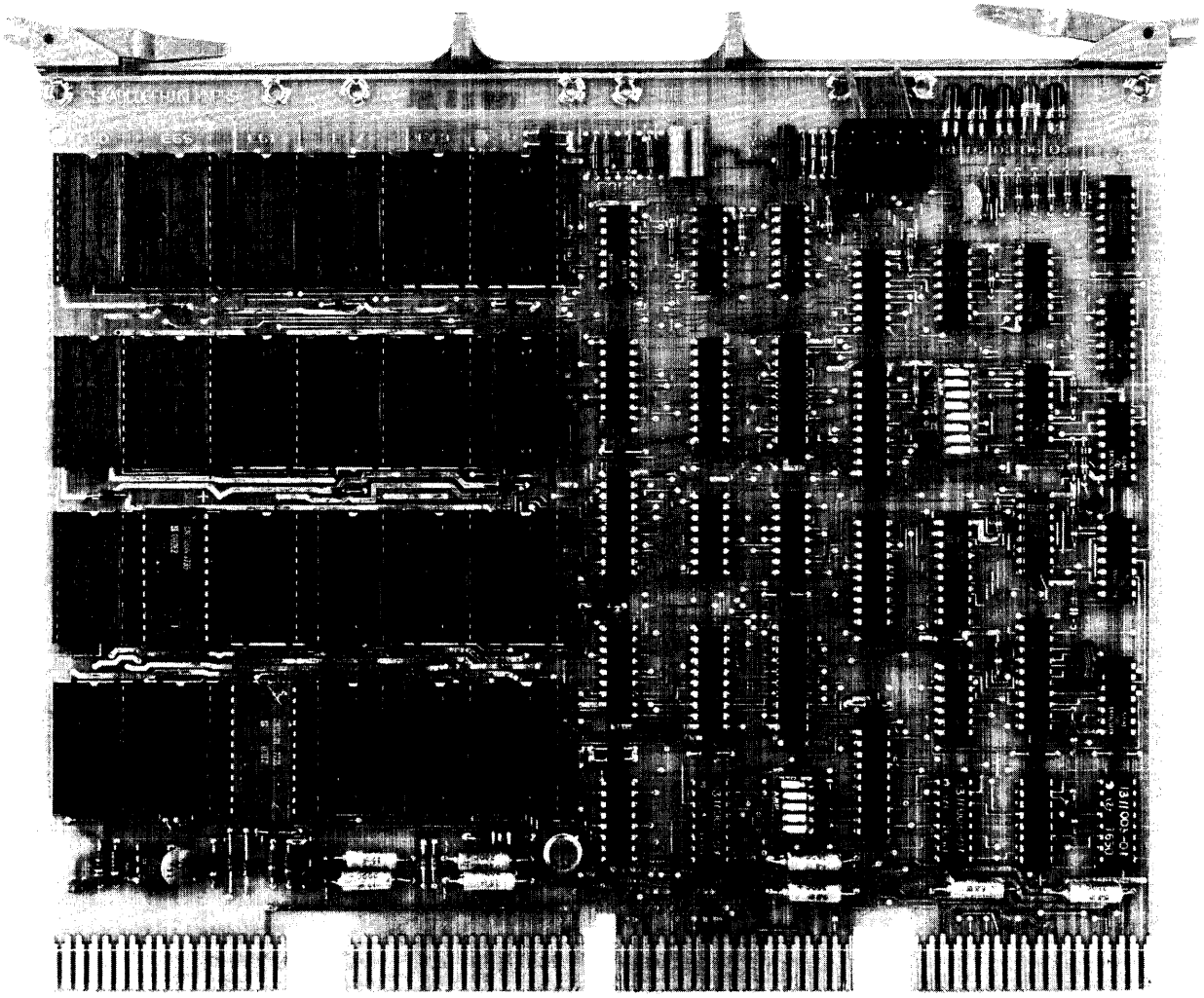


Figure 1-1 BDV11 Module

1.3 BDV11 SPECIFICATIONS

The specifications listed in Table 1-1 are for informational purposes only and are subject to change without notice.

Table 1-1 BDV11 Specifications

Item	Specification
Physical Characteristics	
Length (without handles)	26.7 cm (10.5 in)
Height (without handles)	21.6 cm (8.5 in)
Depth	1.27 cm (0.5 in)
Electrical Characteristics	
BDV11 Module Type	M8012
Power Requirements	+5 Vdc @ 1.6 A (max) +12 Vdc @ 0.07 A (max)
LSI-11 Bus Loading	2 ac unit loads
Environmental Requirements	
Operating Temperature*	5°–50° C (41°–122° F)
Operating Humidity	10–95%, with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)

* The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mm Hg (29.92 in Hg); maximum allowable operating temperature must be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitudes.

1.4 RELATED PUBLICATIONS

Information that is useful to the BDV11 user can be found in the following DIGITAL publications.

Publication	Document Number	Remarks
BA11-N Mounting Box Technical Manual	EK-BA11N-TM-001	In microfiche library; also available in hard copy
BA11-N Mounting Box User's Guide	EK-BA11N-UG-001	Available in hard copy
Microcomputer Handbook, 1977–1978 (2nd Edition)	EB-07948-53/77	Available in hard copy
PDP-11 Software Handbook	EB-08127-20/70	Available in hard copy

For information concerning microfiche libraries, contact:

Digital Equipment Corporation
132 Parker St.
Maynard, MA 01754

Attn: Micropublishing Group
(PK3-2/T12)

Hard copy documents can be ordered from:

Digital Equipment Corporation
444 Whitney St.
Northboro, MA 01531

Attn: Communications Services (NR2/M15)
Customer Services Section

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter describes the steps to take before installing the BDV11 in a backplane and tells how and where to install the module. Detailed information concerning the installation of LSI-11 system components can be found in the reference publications listed in Paragraph 1.4. Refer to the specific BDV11-variation user manual for procedures that check for correct system operation after the installation.

2.2 PRELIMINARY STEP

A number of switches on the module must be set before the module is inserted in the backplane. The diagnostic/bootstrap switches are used for maintenance and system configuration; the BEVNT switch is used to select the mode of control of the LSI-11 bus BEVNT signal. The location of these switches is shown in Figure 3-1; their operation is described in Paragraphs 3.1.1 and 3.1.2. Ensure that the switches are in the desired positions before installing the module.

2.3 INSTALLING THE MODULE IN A BACKPLANE

The BDV11 can be inserted in any LSI-11 quad backplane. In multiple-backplane systems the module must be inserted in the last backplane of the system. When inserting the module, make sure the power is turned off. Connector A of the module is inserted in connector A of the backplane (connector A on the module is the right-most connector when viewing the component side of the module with the connector fingers pointing down; connector A on the backplane is on the left side when viewing the slot side of the backplane). The LSI-11 bus signals will appear on module connectors A and B.

The BDV11 is equipped with metal extractor-type handles that facilitate module insertion and removal. When inserting such a module into the backplane, begin by sliding the module, component side up, into the card guides. Slide the module all the way in and just start the module connector fingers into the backplane connectors. Fit the prongs of the handles into the holes in the card frame (Figure 2-1). Press in on both handles simultaneously to fully insert the fingers in the backplane connector.

To remove the module, pull both handles out simultaneously until the prongs of the handle are clear of the holes in the card frame. The module fingers will now be nearly free of the backplane connector and the module can be removed easily.

CAUTION

The module and/or the backplane assembly might be damaged if the module is inserted or removed with the power on or if the module is inserted upside down.

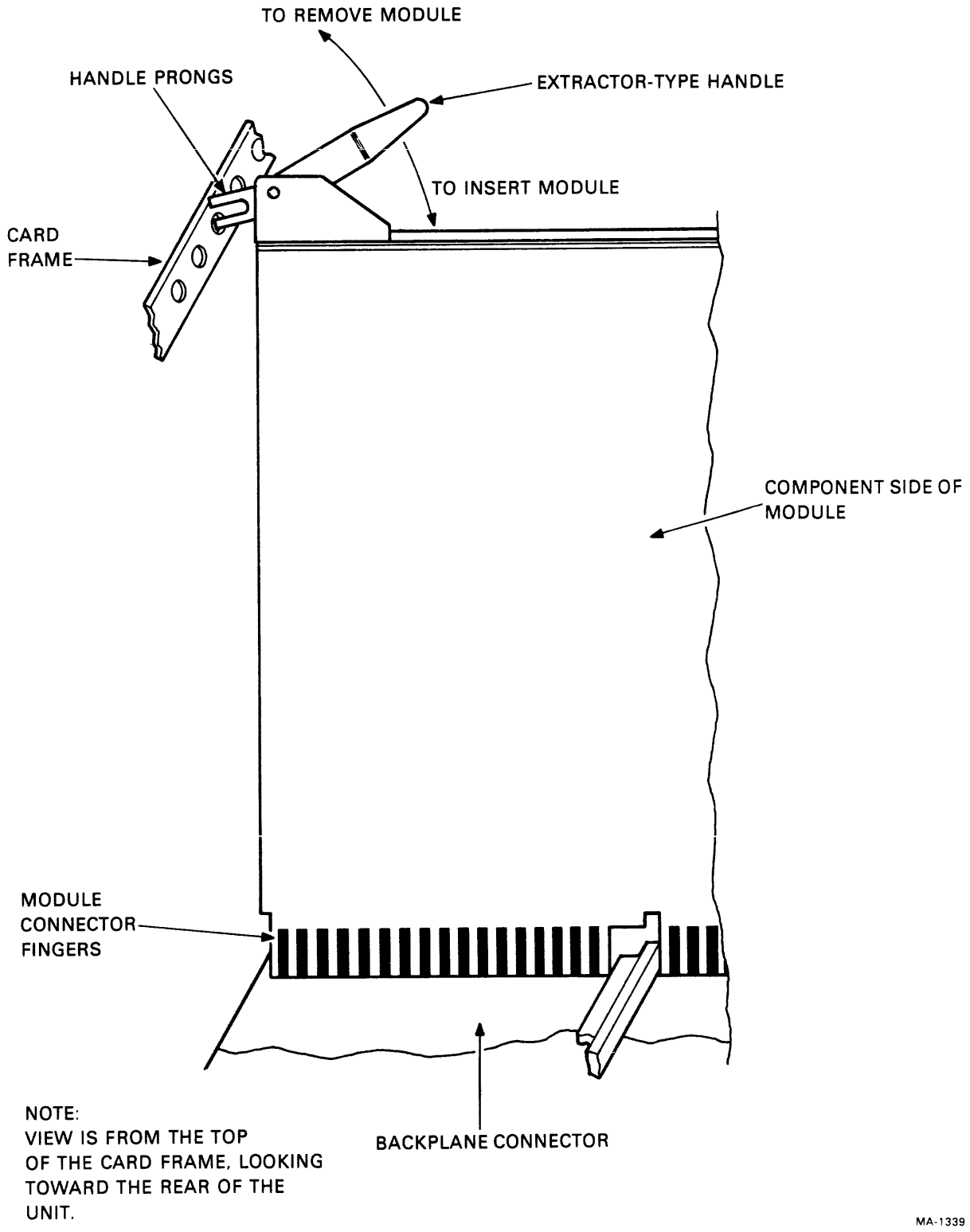


Figure 2-1 Insertion and Removal of Modules Having Extractor-Type Handles

2.4 MODULE PIN-OUTS AND LOGIC DRAWINGS

The M8012 print set includes logic drawings. Signal names in the logic drawings have the following form.

SOURCE SIGNAL POLARITY

SOURCE indicates the particular sheet of the drawings where the signal originates. SIGNAL NAME is the proper name of the signal; the names used in the drawings are also used in this manual. POLARITY is either H or L to indicate the voltage level of the signal when asserted: H ≈ +3 V; L ≈ Ground.

As an example, the signal SH2 REG L originates on sheet 2 of the drawings and means when REG is true, this signal is at approximately ground level.

LSI-11 bus signal lines do not carry a SOURCE indicator. These names represent a bidirectional wire-ORed bus. As a result, multiple sources for a particular bus signal exist. The LSI-11 bus signal names begin with a "B" for "bussed." The bus pin-outs for the BDV11 are listed in Table 2-1.

Table 2-1 BDV11 Bus Pin-Outs

Mnemonic	Pin	Mnemonic	Pin
+5	AA2	BIAKI L*	AM2
+5	BA2	BIAK 0 L	AN2
+12	AD2	BINIT L	AT2
BBS7 L	AP2	BDMGI L*	AR2
BDAL 0 L	AU2	BDMGO L*	AS2
BDAL 1 L	AV2	BIRQ L	AL2
BDAL 2 L	BE2	BRPLY L	AF2
BDAL 3 L	BF2	BSYNC L	AJ2
BDAL 4 L	BH2	BDC OK H	BA1
BDAL 5 L	BJ2	GND	AC2
BDAL 6 L	BK2	GND	AT1
BDAL 7 L	BL2	GND	BC2
BDAL 8 L	BM2	GND	BT1
BDAL 9 L	BN2	MSPARE A (-12 V)	AK1†
BDAL 10 L	BP2		AL1
BDAL 11 L	BR2	MSPARE B(EXT R CLK)	BK1†
BDAL 12 L	BS2		BL1
BDAL 13 L	BT2	SSPARE 4	BC1
BDAL 14 L	BU2	SSPARE 5	BD1
BDAL 15 L	BV2	SSPARE 6	BE1
BDIN L	AH2	SSPARE 7	BF1
BDOUT L	AE2	SSPARE 8 (EXT T CLK)	BH1
BHALT L	AP1		

* These signals are not bussed; they are daisy-chained.

† This jumper is wired on the backplane.

CHAPTER 3
OPERATION

3.1 SWITCHES AND INDICATORS

There are two lever switches (S1 and S2) and five LEDs (D1–D4 and D6) mounted on the front edge of the BDV11 module, and two dip-socket switch units (E15 and E21) mounted on the interior of the module. These components are identified in Figure 3-1 and described in the following paragraphs.

3.1.1 POWER OK LED (D6), HALT/ENABLE Switch (S1), RESTART Switch (S2), and BEVNT L Switch (Section 5 of E21)

These components are maintenance aids. Table 3-1 describes the function of each component.

3.1.2 Diagnostic/Bootstrap Switches

The dip-socket switch units, E15 and E21, are used with BDV11 variations. The switches, except switch 5 of E21, allow the user to select diagnostic programs and/or a bootstrap program that run automatically when power is turned on or when the system is re-booted. (Refer to the appropriate user manual for details.) The 12 individual switches comprise the switch register, which can be read at bus address 177524. (Table 3-2 includes a description of this register and its function in the BDV11.)

3.1.3 Diagnostic Light Display

The diagnostic light display is used primarily with BDV11 variations. In these applications, the display indicates the area of failure of a diagnostic or bootstrap. Figure 3-2 illustrates the left front edge of the module (as viewed from the rear of the mounting box), showing the five LEDs that comprise the display. D6 is the POWER OK LED, which is lighted when the +12 Vdc and +5 Vdc supplies are operating correctly and which indicates the octal point for the display value. Refer to the appropriate user manual for information.

3.2 HARDWARE REGISTERS

The BDV11 contains six hardware registers. These are listed in Table 3-2, together with a functional description of each.

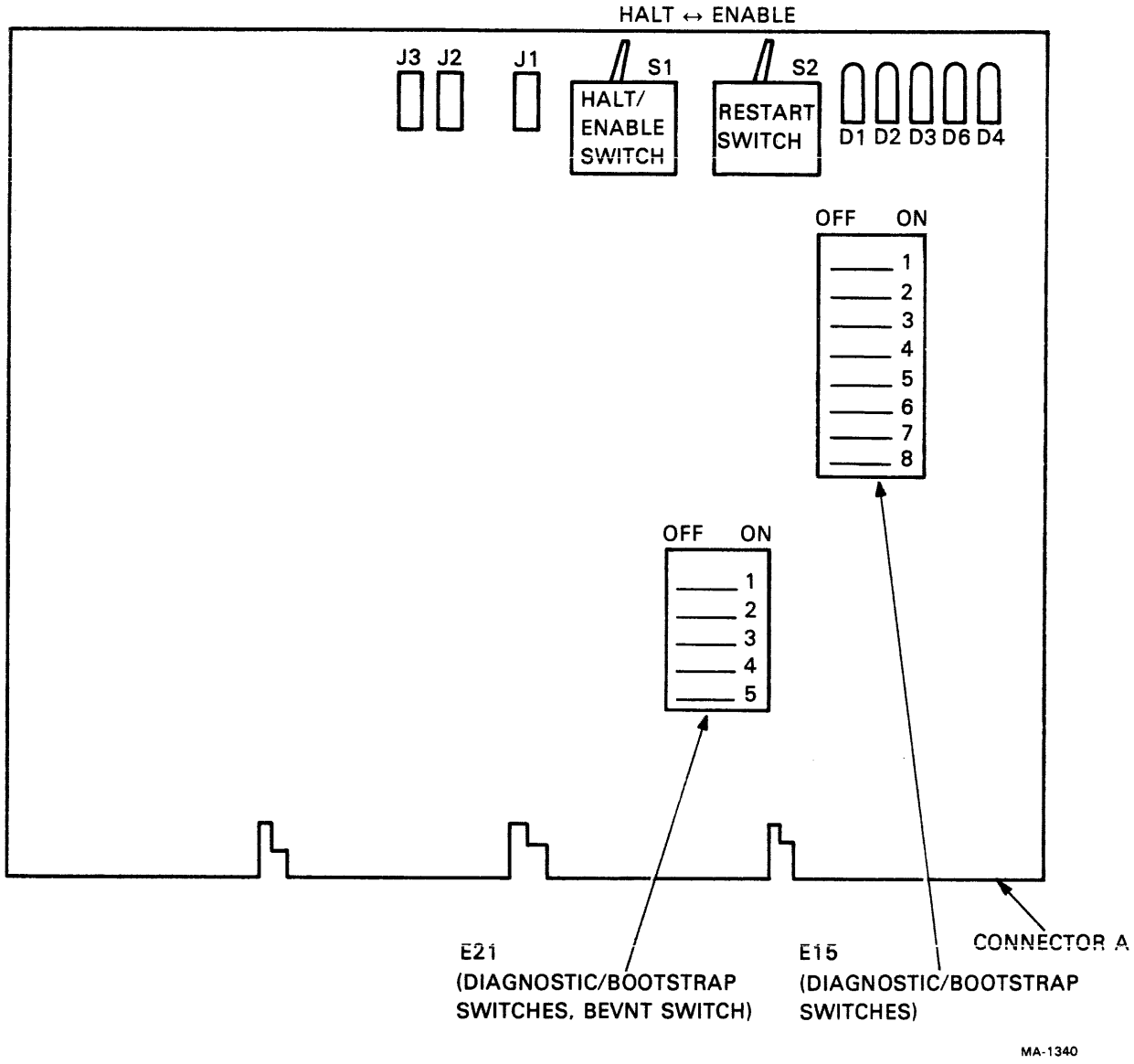


Figure 3-1 BDV11 Switches and Indicators

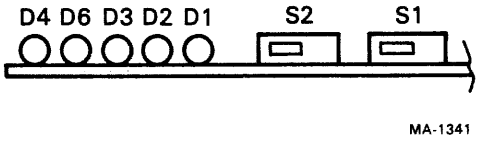


Figure 3-2 Diagnostic Light Display

Table 3-1 Functions of the Maintenance Aids

Component	Function
POWER OK LED	This green LED is lighted when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560-ohm resistor in series to prevent damage from a short circuit; use at least a 20,000-ohm/V meter to measure the voltage.) **Jack Color Voltage** J1 Black Ground J2 Red +5 Vdc J3 Purple +12 Vdc Secondarily, the LED indicates the octal point for the diagnostic light display (Paragraph 3.1.3).
HALT/ENABLE Switch	When this switch is in the ENABLE position, the LSI-11 CPU can operate under program control. If the switch is placed in the HALT position, the CPU enters the halt mode and responds to console ODT commands. While in the halt mode, the CPU can execute single instructions, facilitating maintenance of the system. Program control is re-established by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to Chapter 2 of the *1977–1978 Microcomputer Handbook* for a description of console ODT command usage.
RESTART Switch	When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, the system can be re-booted at any time for maintenance purposes.
BEVNT L Switch	Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open) the LSI-11 bus BEVNT L signal can be controlled by the power supply-generated LTC signal. When the switch is on (closed), the LTC function is program-controlled; i.e., a single-bit, write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.) The KW11-L line-time clock option also uses bit 6 as the enable bit.

Table 3-2 BDV11 Hardware Registers

Register	Size	Function	Bus Address
Page Control Register (PCR)	16 bits	Controls mapping of ROM pages into physical ROM addresses. Cleared when power is turned on or when RESTART switch is activated.	177520 (word or byte addressable; can be read or written)
Read/Write Register	16 bits	Maintenance register used for diagnostics. Cleared when power is turned on or when RESTART switch is activated.	177522 (word or byte addressable; can be read or written)
Switch Register	12 bits	Used for maintenance and system configuration (selects diagnostic and/or bootstrap programs for execution). Bits 0–11 of the register (corresponding to E15-1 through E15-8 and E21-1 through E21-4, respectively) are associated with BDAL <0:11> L, respectively; when an individual switch of the register is closed (on), the corresponding BDAL signal is low (1).	177524 (read-only register)
Display Register	4 bits	Controls the diagnostic light display. Bits 0–3 of the register control LEDs D1–D4, respectively; when a bit is set, the corresponding LED is off. Cleared (all lights on) when power is turned on or when RESTART switch is activated.	177524 (word or byte addressable; write-only register)
BEVNT Register	1 bit	When cleared, this register clamps the BEVNT signal low (if the BEVNT switch is closed). This action permits program control of the LSI-11 line-time clock (LTC) function. Register cleared when power is turned on or when RESTART switch is activated.	177546 (word or byte addressable; write-only register)

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 ADDRESSING ROM ON THE BDV11 MODULE

A block of 256 LSI-11 bus addresses is reserved for use in addressing ROM locations on the BDV11 module. This block resides in the upper 4K address bank (28K–32K), which is normally used for peripheral-device addressing, and consists of byte addresses 173000–173776 (512 byte addresses correspond to 256 word addresses in the LSI-11 addressing scheme).

The BDV11 logic enables all 2048 locations in a selected 2K ROM (or 1024 locations in a 1K ROM) to be addressed by just these 256 bus addresses. The logic includes a page control register (PCR) at bus address 177520; the contents of this read/write register determine the specific ROM location that is accessed when one of the 256 bus addresses is placed on the BDAL lines. The PCR is loaded with "page" information, i.e., the PCR contents point to one of 16 (or one of 8) 128-word pages in the selected ROM (16 pages × 128 words = 2048 words). To illustrate, if the PCR contents represent pages 0 and 1, bus addresses 173000–173776 access ROM locations 0000–0377; if the PCR contents represent pages 10 and 11, bus addresses 173000–173776 access ROM locations 2000–2377. Table 4-1 relates bus addresses, PCR pages, and ROM locations.

At the top of each column of PCR pages in Table 4-1 appear two circuit component designations; column 1, for example, is headed by E53/E48. These designations represent the ROMs and EPROMs that one might find on a BDV11 module. For instance, the BDV11-AA is supplied with 2K words of diagnostic ROM. The ROM inserted in socket XE53 supplies the high byte (bits 8–15) of these 2K words, while the ROM inserted in socket XE48 supplies the low byte (bits 0–7). To access the BDV11 diagnostic ROM locations, the user must load the PCR with the pages in column 1; thus, when 12 and 13, for example, are loaded in the PCR, diagnostic ROM locations 2400–2777 can be addressed by the LSI-11 BDAL signals. Another variation of the BDV11 could have 1K-word EPROMs inserted in sockets XE57/XE40 (E57 supplies the high byte, while E40 supplies the low byte). To access these EPROM locations, the user would load the PCR with pages in column 3; thus, with 44 and 45 in the PCR, EPROM locations 1000–1377 are accessible.

As Table 4-1 implies, the PCR pages are assigned to specific module ROM sockets. Furthermore, the sockets are assigned specific kinds of ROMs, as indicated in Table 4-2; e.g., the diagnostic/bootstrap ROM can occupy only sockets XE53 and XE48. Thus, a specific ROM can be addressed only when the PCR contains the page or pages assigned to the socket that the ROM occupies. To illustrate, if 2K ROMs are inserted in sockets E39 and E50, they can be addressed only when the PCR contains pages 360–377. The page/socket assignments indicated in Table 4-1 apply to the BDV11 module shipped by DIGITAL. There are eight locations on the BDV11 printed circuit board in which jumpers are inserted selectively to achieve these assignments. It is possible to change the factory arrangement of these jumpers; by doing so, the user can cause the CPU to execute instructions directly from a ROM or EPROM of the user's choice when power is turned on, rather than from the diagnostic ROMs. Paragraph 4.7 describes the jumpers in detail and shows how they can be rearranged.

Table 4-1 BDV11 Bus Addresses/PCR Pages

Bus Address	PCR Pages												ROM Location Accessed
	E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50	
173000–173376	0	20	40	50	200	220	240	260	300	320	340	360	0000–0177
173400–173777	1	21	41	51	201	221	241	261	301	321	341	361	0200–0377
173000–173376	2	22	42	52	202	222	242	262	302	322	342	362	0400–0577
173400–173777	3	23	43	53	203	223	243	263	303	323	343	363	0600–0777
173000–173376	4	24	44	54	204	224	244	264	304	324	344	364	1000–1177
173400–173777	5	25	45	55	205	225	245	265	305	325	345	365	1200–1377
173000–173376	6	26	46	56	206	226	246	266	306	326	346	366	1400–1577
173400–173777	7	27	47	57	207	227	247	267	307	327	347	367	1600–1777
173000–173376	10	30			210	230	250	270	310	330	350	370	2000–2177
173400–173777	11	31			211	231	251	271	311	331	351	371	2200–2377
173000–173376	12	32			212	232	252	272	312	332	352	372	2400–2577
173400–173777	13	33			213	233	253	273	313	333	353	373	2600–2777
173000–173376	14	34			214	234	254	274	314	334	354	374	3000–3177
173400–173777	15	35			215	235	255	275	315	335	355	375	3200–3377
173000–173376	16	36			216	236	256	276	316	336	356	376	3400–3577
173400–173777	17	37			217	237	257	277	317	337	357	377	3600–3777

Table 4-2 Functions of ROM Sockets

Sockets	ROM Function	Sockets	ROM Function
XE53/XE48	2K Diagnostic/Bootstrap	XE47/XE42	2K System ROM
XE58/XE44	2K Diagnostic/Bootstrap (reserved for DIGITAL)	XE51/XE38	2K System ROM
		XE55/XE37	2K System ROM
XE57/XE40	1K EPROM	XE60/XE41	2K System ROM
XE52/XE36	1K EPROM	XE59/XE45	2K System ROM
XE39/XE50	2K System ROM	XE54/XE49	2K System ROM
XE43/XE46	2K System ROM		

The PCR is a 16-bit register comprising two 8-bit bytes. The low byte consists of bits 0–7, while the high byte consists of bits 8–15. When page 6, for instance, is loaded into the low byte of the PCR, bus addresses 173000–173376 access the 128 ROM locations in the block 1400–1577. When a bus address falls in this range, the logic considers only the low byte of the PCR. On the other hand, if a bus address is in the range 173400–173777, only the high byte of the PCR is used to select the ROM location.

Table 4-3 relates the PCR contents to the PCR page for pages 0–17. As an example, if the PCR is loaded with data 000400, the PCR low byte contains data 000, while the high byte contains data 001. The PCR bytes can be loaded separately. To select ROM locations 1600–1777, for instance, one only needs to load the PCR high byte with page 7; thus, the high byte contains 007, while the low byte can contain anything. Table 4-4 lists the PCR contents for the remaining PCR pages.

Table 4-3 PCR Contents/Page Relationship, Pages 0–17

PCR Contents	PCR Page	PCR High Byte (Bits 15–8)	PCR Low Byte (Bits 7–0)
000400	0		000
	1	001	
001402	2		002
	3	003	
002404	4		004
	5	005	
003406	6		006
	7	007	
004410	10		010
	11	011	
005412	12		012
	13	013	
006414	14		014
	15	015	
007416	16		016
	17	017	

Table 4-4 PCR Contents, Pages 20–57, 200–377

Page	Contents	Page	Contents	Page	Contents
20, 21	010420	240, 241	120640	340, 341	160740
22, 23	011422	242, 243	121642	342, 343	161742
24, 25	012424	244, 245	122644	344, 345	162744
26, 27	013426	246, 247	123646	346, 347	163746
30, 31	014430	250, 251	124650	350, 351	164750
32, 33	015432	252, 253	125652	352, 353	165752
34, 35	016434	254, 255	126654	354, 355	166754
36, 37	017436	256, 257	127656	356, 357	167756
40, 41	020440	260, 261	130660	360, 361	170760
42, 43	021442	262, 263	131662	362, 363	171762
44, 45	022444	264, 265	132664	364, 365	172764
46, 47	023446	266, 267	133666	366, 367	173766
		270, 271	134670	370, 371	174770
50, 51	024450	272, 273	135672	372, 373	175772
52, 53	025452	274, 275	136674	374, 375	176774
54, 55	026454	276, 277	137676	376, 377	177776
56, 57	027456				
		300, 301	140700		
200, 201	100600	302, 303	141702		
202, 203	101602	304, 305	142704		
204, 205	102604	306, 307	143706		
206, 207	103606	310, 311	144710		
210, 211	104610	312, 313	145712		
212, 213	105612	314, 315	146714		
214, 215	106614	316, 317	147716		
216, 217	107616				
		320, 321	150720		
220, 221	110620	322, 323	151722		
222, 223	111622	324, 325	152724		
224, 225	112624	326, 327	153726		
226, 227	113626	330, 331	154730		
230, 231	114630	332, 333	155732		
232, 233	115632	334, 335	156734		
234, 235	116634	336, 337	157736		
236, 237	117636				

4.2 BDV11 BLOCK DIAGRAM

Figure 4-1 shows a block diagram of the BDV11 logic. The DC005 transceivers monitor the LSI-11 bus BDAL lines. When an address in the upper 4K bank of bus addresses is placed on the BDAL lines, the transceivers gate the address information onto the BDV11 DAL lines. If the address is one of those assigned to the BDV11 (173000–173777, 177520, 177522, 177524, 177546), the transceivers generate ADDRESS MATCH signals. These signals cause the control logic to decode the bus address and to respond to the protocol signals that effect bus data transfers.

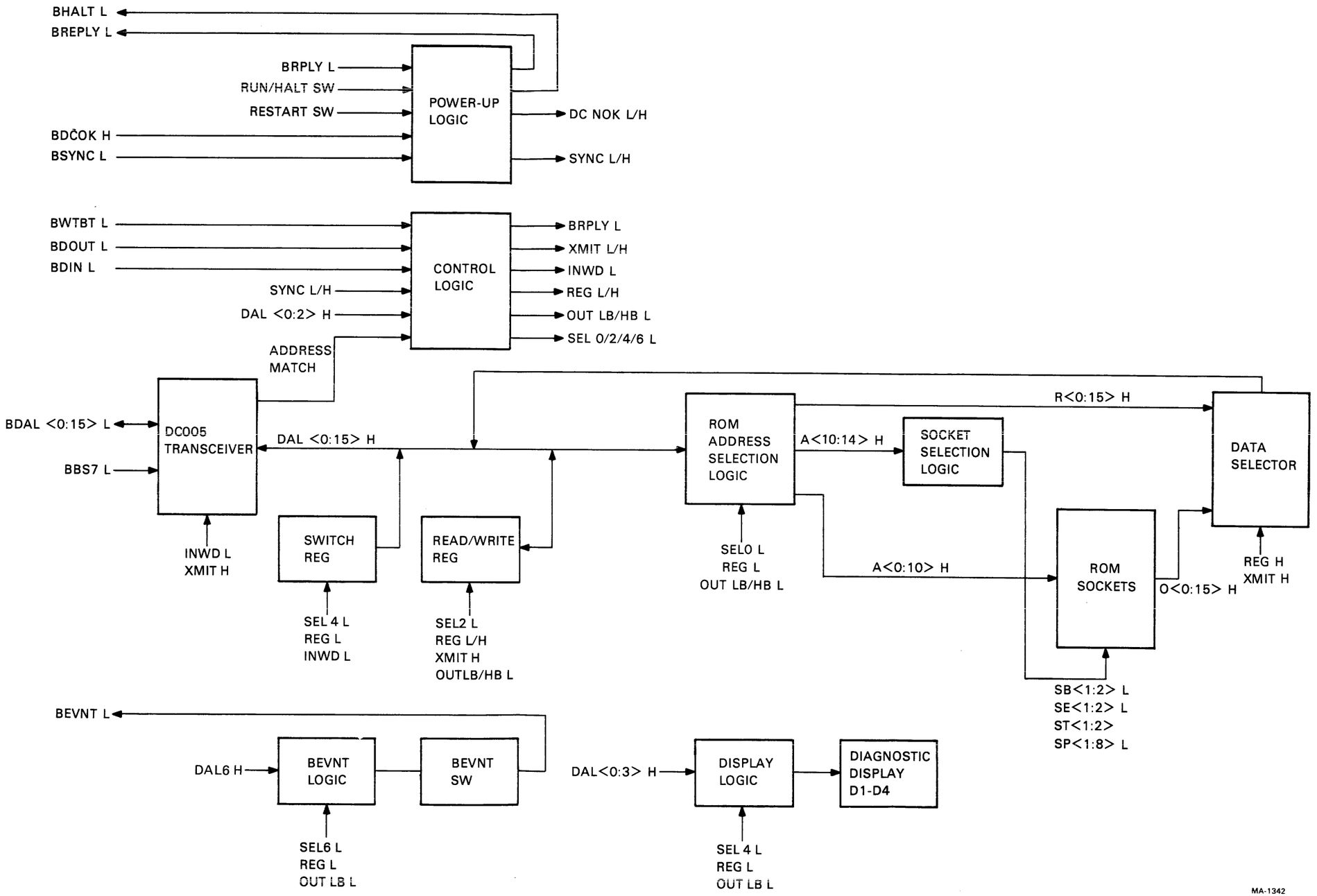


Figure 4-1 BDV11 Block Diagram

The bus address placed on the BDAL lines can be the address of one of the BDV11 registers, or the address of a ROM location. If one of the registers has been addressed, the control logic asserts those signals that are necessary to carry out the operation directed by the protocol signals that follow. For example, if the 16-bit read/write register is addressed, the control logic asserts the signals that permit the register to be either read or written. When the actual transfer of data takes place, the information is gated to or from the register on the DAL lines in response to the protocol signals.

If the bus address is that of a ROM location, the address is loaded into the ROM address selection logic. This logic includes the PCR, which contains page information previously loaded by a writing operation into the PCR. The address selection logic decodes the address and asserts relative address signals (A0 H - A10 H) that are applied to all the ROM sockets. Other address signals (A10 H - A14 H) are applied to the socket selection logic; this logic generates signals that select the particular ROM identified by the PCR page information. This ROM responds to the relative address signals and places the data in the addressed location on the O<0:15> H lines. The data is then gated onto the DAL lines by the data selector and placed on the BDAL lines in response to the protocol signals.

The data selector is also used when the PCR is read. When this operation is executed, the PCR page information carried on the R<0:15> L lines is gated onto the DAL lines and from those lines to the bus.

All the foregoing logic blocks are described in detail in the following paragraphs. The power-up logic, the BEVNT logic, and the display logic (all of which are self-descriptive, functionally) are also discussed. For detailed information concerning bus transfer operations, refer to the *1977–1978 Microcomputer Handbook.*

4.3 TRANSCEIVER/SWITCH REGISTER LOGIC

Figure 4-2 shows the transceiver/switch register logic for bits 0–3. The DC005 transceiver is a bidirectional buffer between the LSI-11 data/address lines, BDAL <0:15> L, and the BDV11 data/address lines, DAL <0:15> H. The transceiver also provides a constant generator (which is used for selecting BDV11 diagnostic and bootstrap addresses) and comparison circuits for address selection.

The transfer of information between the BDAL lines and the DAL lines is controlled by signals XMIT H and INWD L, which are generated in the control logic in response to the LSI-11 bus protocol signals. XMIT H and INWD L are related to bus transfer cycles as follows.

INWD L	XMIT H	Bus Transfer Cycle
LO	LO	No transfer (DAL and BDAL lines open)
LO	HI	DATI (DAL→BDAL)
HI	LO	DATO/DATOB (BDAL→DAL)
HI	HI	DATO/DATOB (BDAL→DAL)

Information can also be put on the BDAL lines by the transceiver JAV inputs. These three inputs drive three bus lines directly, overriding the XMIT H and INWD L control signals (JAV3, JAV2, and JAV1 are paired with BUS3, BUS2, and BUS1, respectively, in each DC005). A high input causes a low to be transmitted on the corresponding bus line, while a low or open input causes an open condition to occur on the bus line. The JAV inputs allow the user to read the contents of the switch register and are related to the BDAL<0:2> L signals as follows.

	BDAL0 L	BDAL1 L	BDAL2 L
JAV3 (HI/LO-OR-OPEN)	(LO/OPEN)*	–	–
JAV2 (HI/LO-OR-OPEN)	–	(LO/OPEN)	–
JAV1 (HI/LO-OR-OPEN)	–	–	(LO/OPEN)

* When JAV3, for example, is high, BDAL0 L is low; when JAV3 is low or open, BDAL0 L is open.

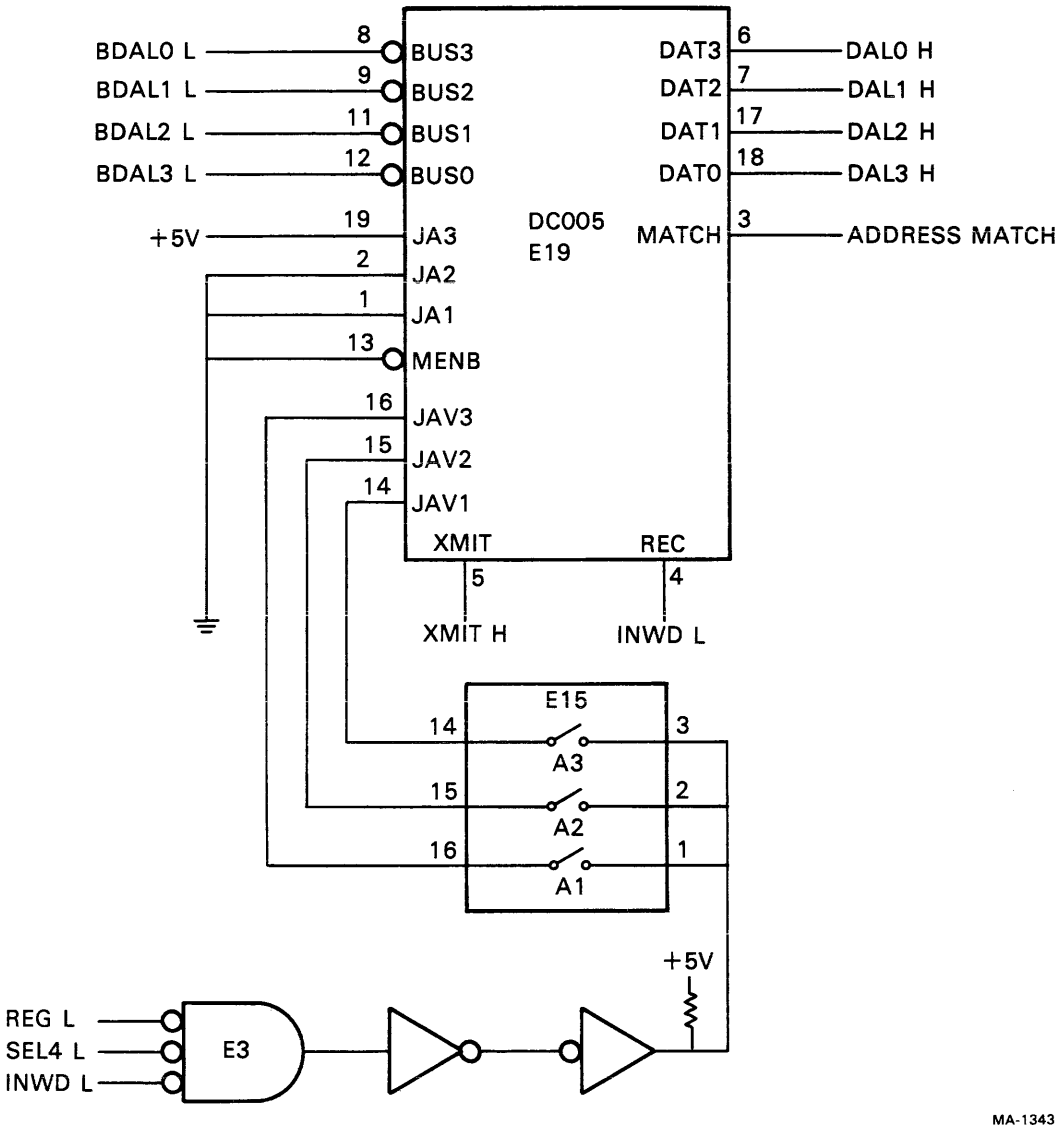


Figure 4-2 Transceiver and Switch Register Logic, Bits 0–3

The JA inputs of the transceiver are part of the comparison circuits. When the signal state at a JA input is the same as that at the corresponding bus line, a match exists. If three matches exist, and if the MENB L signal is low, the MATCH output of the DC005 is open-circuited. This open-collector output permits more than one transceiver output to be wire-ANDed, thereby forming a composite address match signal. The relation between the JA signals and the BDAL signals, and between MENB L and MATCH H is shown below.

	BDAL0 L	**BDAL1 L**	**BDAL2 L**
JA3 (GROUND/OPEN)	LO/HI	-	-
JA2 (GROUND/OPEN)	-	LO/HI	-
JA1 (GROUND/OPEN)	-	-	LO/HI

MENB L	**JA-BDAL Match**	**MATCH H**
HI	All 3 match	LO
LO	All 3 match	OPEN
LO	One mismatch	LO

4.4 CONTROL LOGIC

The control logic (Figure 4-3) includes a DC004 protocol chip (E8) and an 82S23 PROM (E9). The PROM monitors LSI-11 bus addresses via the DC005 transceivers and generates two important signals. One of these, at output D0(1) is asserted (high) when the address of any of the BDV11 registers is placed on the bus. The other, at output D1(1), is also asserted when a register is addressed; furthermore, this output is wire-ANDed (at A) with two signals from transceiver E17 (MATCH and DAL12 H) to produce an enabling signal when any one of the assigned bus addresses (173000–173777) is placed on the BDAL lines.

This enabling signal is applied to the DC004 ENB input, allowing this chip to generate signals that select the BDV11 registers for data transfers (SEL0 L, SEL2 L, SEL4 L, and SEL6 L). The DC004 also generates the protocol signals that permit data transfers to take place. Tables 4-5, 4-6, and 4-7 relate the inputs and outputs of the DC004.

As an example of the control logic operation, consider the following description. Figure 4-4 represents the sequence of operations in a DATO bus cycle. Let us assume that we are going to place page information in the BDV11 PCR, address 177520. When this address is put on the BDAL lines, PROM E9 asserts outputs D0 and D1, and wire-AND gate A causes the DC004 ENB input to go high (because BSYNC L is high, INWD L is high and the bus address causes the DC005 transceivers to assert MATCH and DAL signals; refer to Table 4-6). When the processor asserts BSYNC L, flip-flop E10 is set, generating the REG H and REG L signals; in addition, the DC004 generates SEL0 L (Table 4-5), thereby completing the "device-selected" operation in the BDV11 (SEL0 L remains low until BSYNC L is negated). Now the CPU places the PCR page information on the BDAL lines and asserts BDOUT L. As Table 4-7 shows, both the OUTHB L and OUTLB L signals, as well as the BRPLY L, signal, are asserted. (Even though ENB might have gone low when the page information was placed on the BDAL lines, this input was high when BSYNC L was asserted.)

The OUTHB L and OUTLB L signals clock the PCR, loading it with the page information on the DAL lines. After the CPU negates the BDOUT L signal, the BDV11 negates BREPLY L and the CPU terminates the operation by negating BSYNC L.

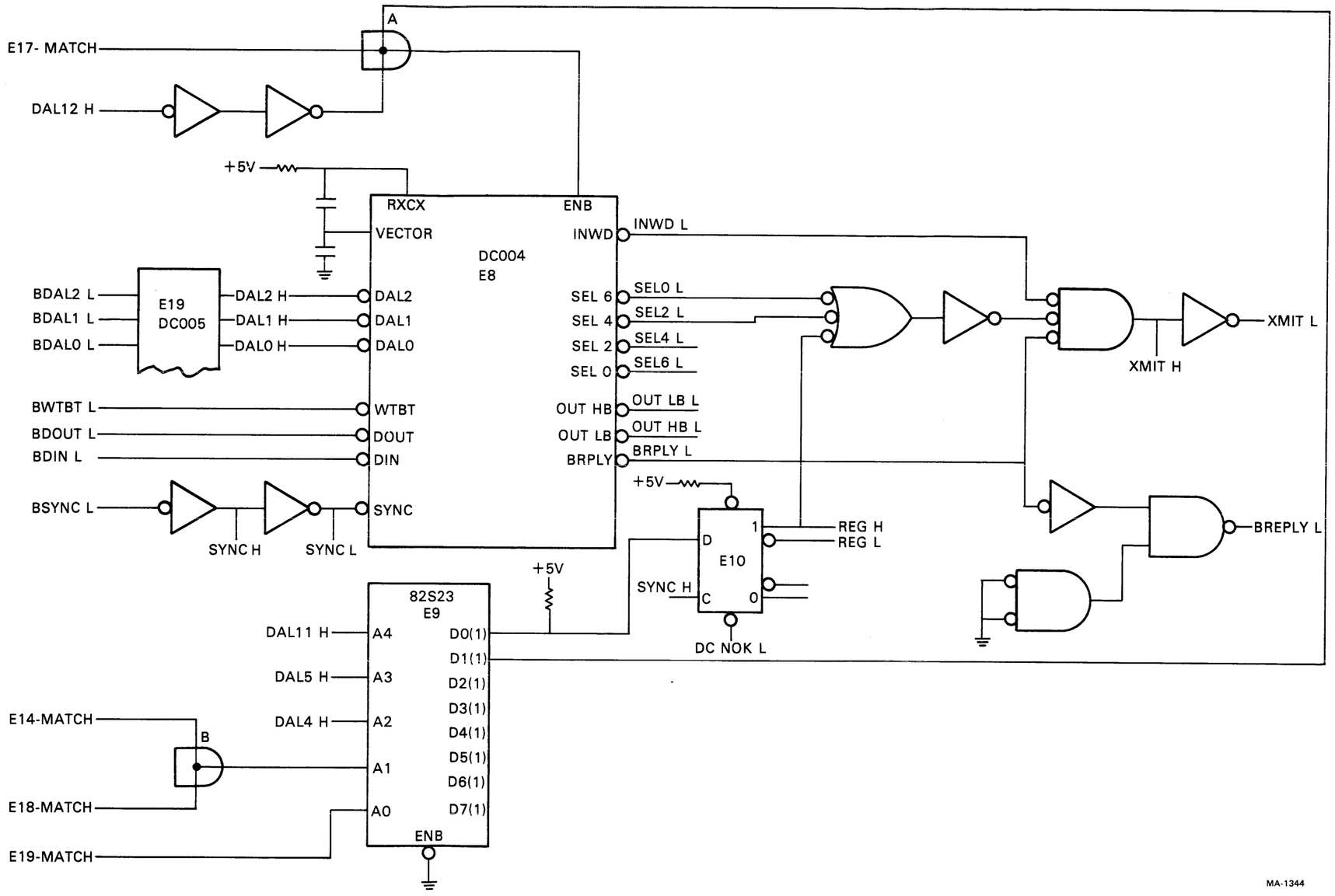


Figure 4-3 Control Logic

Table 4-5 DC004 Select Outputs

Inputs				Outputs			
BSYNC L	ENB*	BDAL2 L*	BDAL1 L*	SEL0 L	SEL2 L	SEL4 L	SEL6 L
L	H	H	H	L	H	H	H
L	H	H	L	H	L	H	H
L	H	L	H	H	H	L	H
L	H	L	L	H	H	H	L

*H and L for these signals indicate the state of the input line at the falling edge of BSYNC.

Table 4-6 DC004 Protocol Signals

Inputs			Outputs	
BSYNC L	BDIN L	ENB*	INWD L	BREPLY L
H	X	X	H	H
L	X	H	H	H
L	L	L	L	H
L	H	L	L	L

*H and L for these signals indicate the state of the input line at the falling edge of BSYNC.

Table 4-7 DC004 Byte Signals

Inputs					Outputs		
BSYNC L	BDOUT L	ENB*	BWTBT L	BDAL0 L*	OUTHB L	OUTLB L	BREPLY L
L	L	L	H	X	L	L	H
			L	L	L	H	H
			L	H	H	L	H
		H	L	X	L	L	L
			L	L	L	H	L
			L	H	H	L	L

*H and L for these signals indicate the state of the input line at the falling edge of BSYNC.

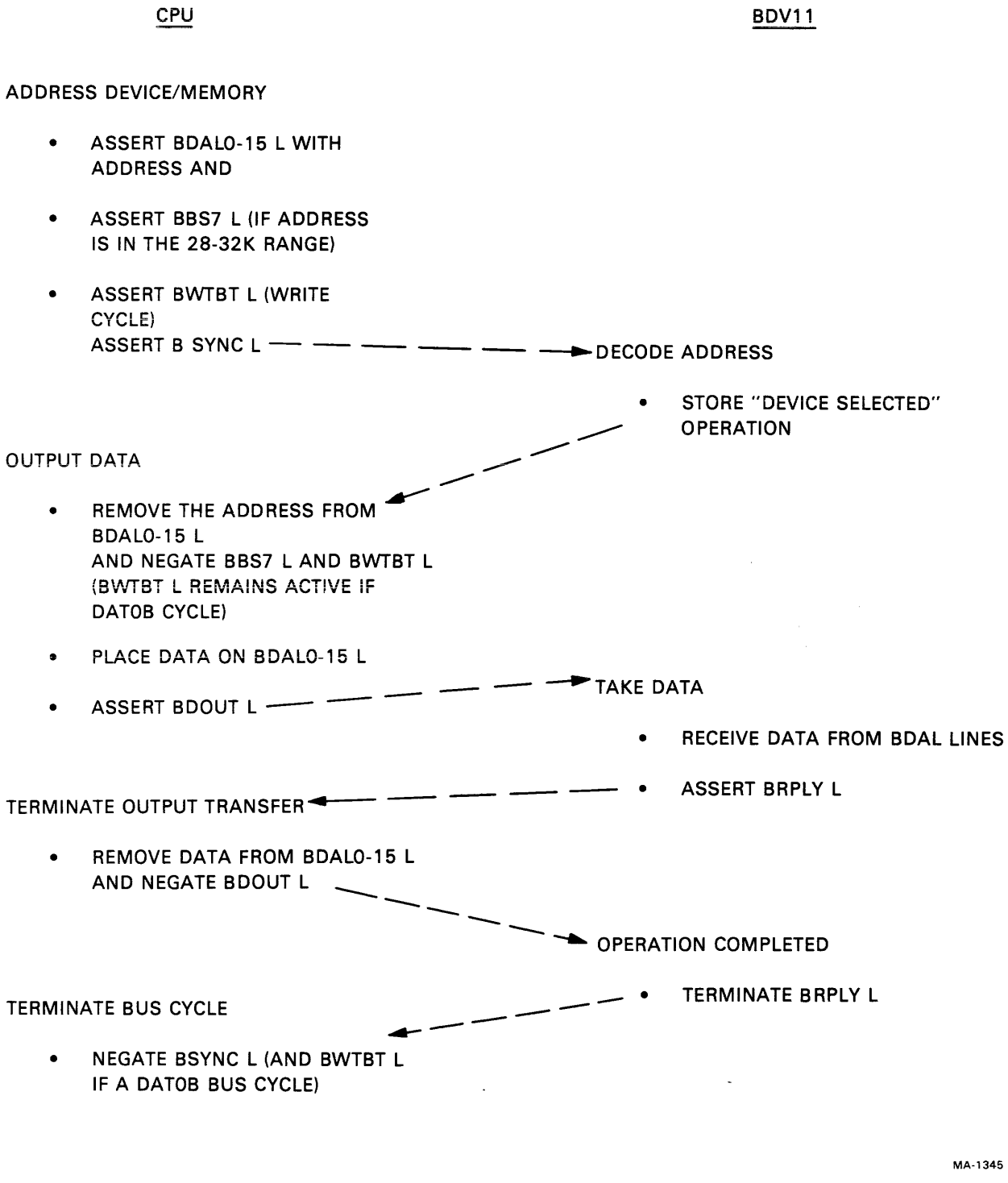


Figure 4-4 Operation Sequence, DATO Cycle

4.5 POWER-UP LOGIC

The power-up logic (Figure 4-5) includes the ENABLE/HALT switch and the RESTART switch. In normal operation, the ENABLE/HALT switch is in the ENABLE position. When the switch is placed in the HALT position, inverter E16 causes NAND gate E7A to assert the BHALT L signal. The CPU enters the halt mode and responds to console ODT commands. To resume operation, the user must return the switch to the ENABLE position and enter a "P" command at the console terminal.

The RESTART switch must be cycled to re-boot the system. If the switch is in the position shown in Figure 4-5, cycling the switch lever generates a pulse that is differentiated by capacitor C13. The leading edge of the negative spike is inverted by E13 and causes E7B to negate the BDCOK H signal; thus, DC NOK L is asserted, initializing the BDV11 registers. When the negative spike decays, NAND gate E7B is disabled; the reasserted BDCOK H signal causes the CPU to carry out a power-up sequence and normal operation is resumed. BDCOK H can also be negated by the LSI-11 power supply, which negates the BDCOK H signal if the dc voltages fall below specified levels.

The bus BREPLY L signal is asserted during the protocol routine when E8 asserts BRPLY. Contrarily, the bus BSYNC L signal causes SYNC H and SYNC L to be asserted, also during the protocol routine.

4.6 ROM ADDRESS SELECTION LOGIC

The logic shown in Figure 4-6 decodes the 256_{10} LSI-11 bus addresses and produces the 2048_{10} addresses needed to access ROM locations. Several examples are given here to illustrate how the logic works.

In the first example, assume that we want to address location 0400 in the diagnostic/bootstrap ROMS, which occupy sockets XE53 and XE48. Table 4-1 shows that to address this location we must have page 2 in the PCR; then, bus address 173000 will access location 0400. It is usual (but not necessary) to load the PCR with a pair of pages. Therefore, we will put pages 2 and 3 in the PCR by addressing the PCR at address 177520 and loading it with data 001402; i.e., the PCR low byte contains 002 and the high byte contains 003 (Figure 4-7).

Now, address 173000 is placed on the LSI-11 BDAL lines. Bits 1–8 of the address are loaded into the flip-flops, E33 (because the bus addresses differ only in the first 9 bits, BDAL<9:15> L need not be considered). ROM address bits A0–A6 assume the logic state of DAL bits 1–7, respectively. The logic looks at DAL8 H to determine which of the PCR bytes will form ROM address bits A7–A14. Since DAL8 H is low, the low byte is selected; i.e., E32 gates R<0:3> H to A<7:10> H and E34 gates R<4:7> H to A<11:14> H. Bits A0–A10 are used to select the ROM location 0400; bits A11–A14 are used to select the correct ROM, i.e., the ROMs in sockets XE53 and XE48. (This procedure is explained in the next section.)

Now that the PCR contains pages 2 and 3, any ROM location from 0400 to 0777 can be addressed. Consider location 0600, for example, which is addressed by bus address 173400. Example 2 in Figure 4-7 illustrates the bit selection. Because DAL8 H is high, the high byte of the PCR is selected to form ROM address bits A7–A14. Bits A0–A10 select ROM location 0600, while bits A11–A14 again select sockets XE53/XE48.

The same bus address, 173400, can address seven other ROM locations, providing the PCR page number is changed. For example, let us address ROM location 3200. To do this, we must change the PCR high byte from page 3 to page 15. We can do this either by loading 006414 (pages 14 and 15) into the PCR or by loading only the high byte with 015. (This can be done by keeping the LSI-11 bus BWTBT L signal asserted throughout the data transfer cycle; thus, only OUT HB L is asserted and only the PCR high byte is loaded.) Let us load only the high byte, as illustrated in Example 3, Figure 4-7. The high byte again forms bits A7–A14 of the ROM address, and we have location 3200 being addressed.

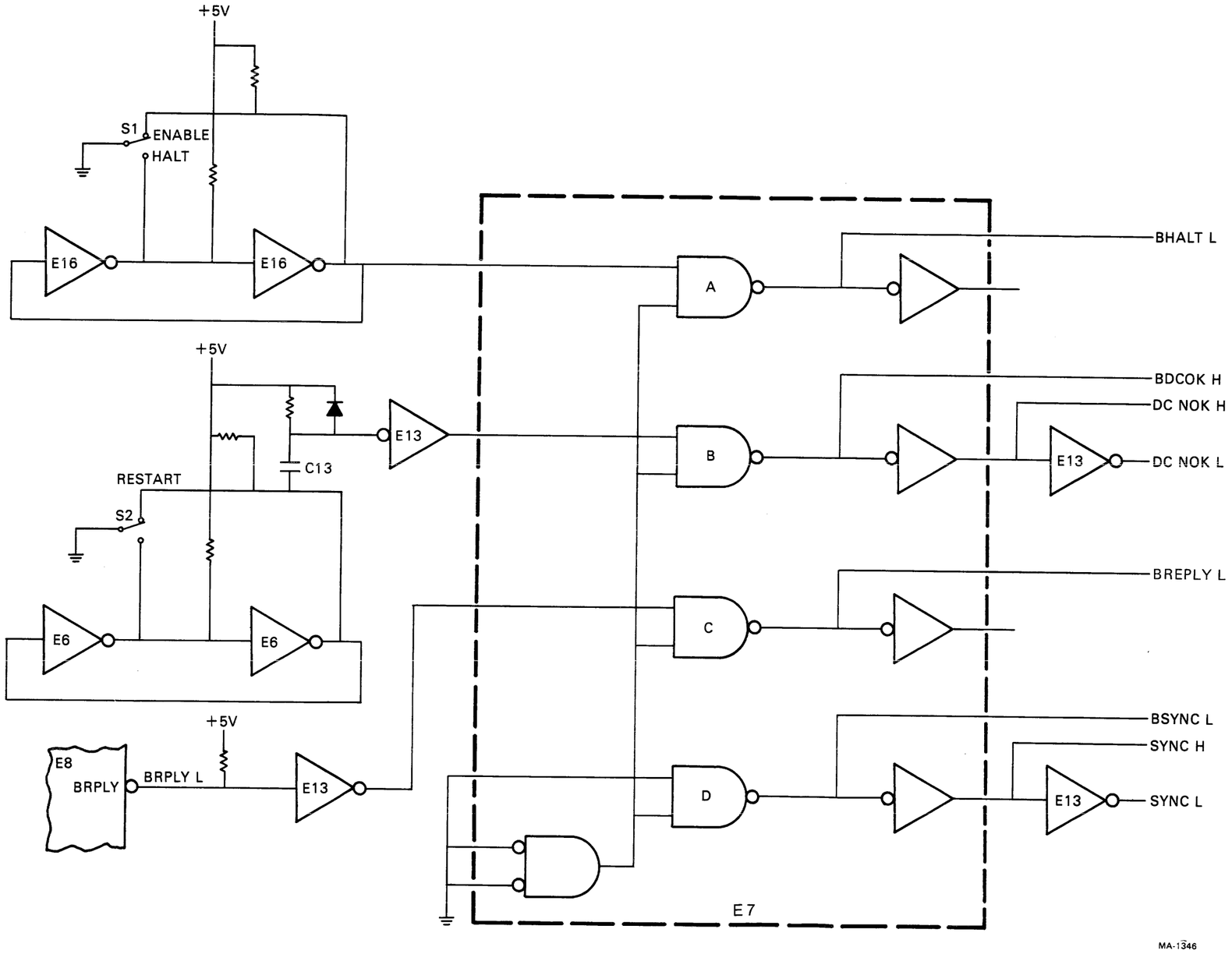
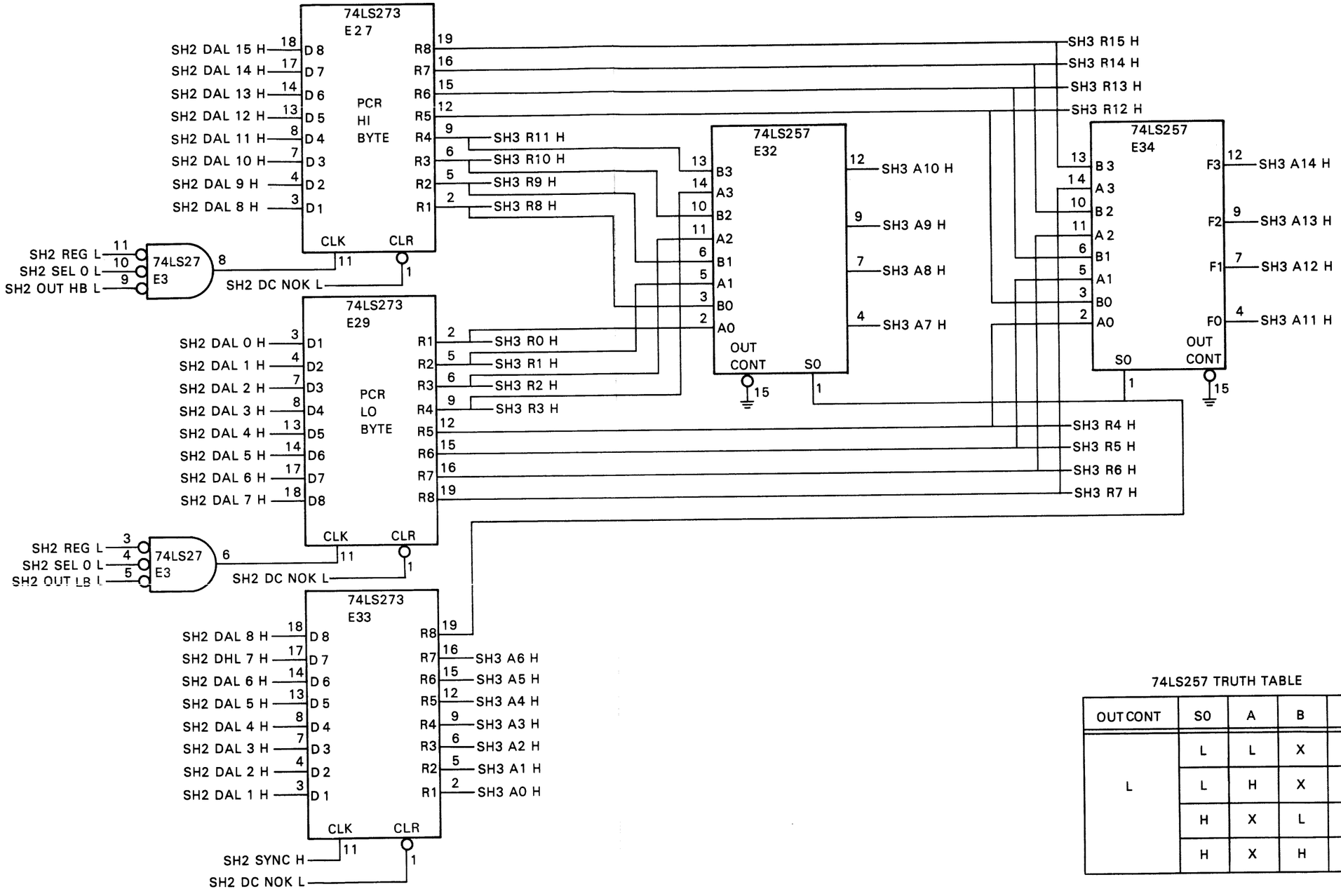


Figure 4-5 Power-Up Logic



74LS257 TRUTH TABLE

OUT CONT	S0	A	B	F
L	L	L	X	L
	L	H	X	H
	H	X	L	L
	H	X	H	H

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Figure 4-6 ROM Address Selection Logic

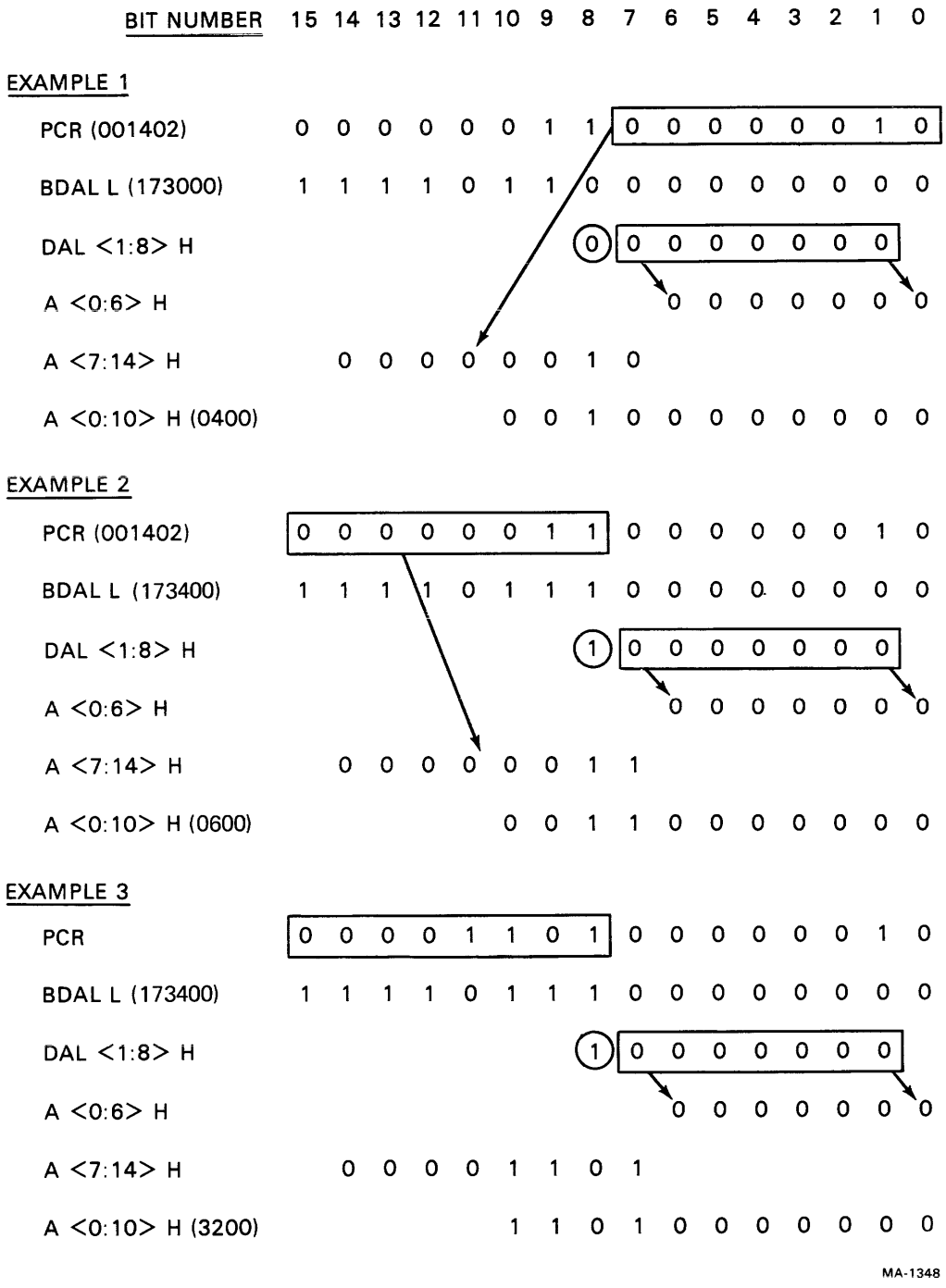


Figure 4-7 Address Bit Selection

Note that the PCR and the flip-flops are cleared whenever DC NOK L is asserted; this happens when the RESTART switch is activated or when the dc voltages drop below reliable operating levels. Also, since the R<0:15> H signals can be gated onto the DAL<0:15> H lines, the PCR can be read as well as written.

4.7 SOCKET SELECTION LOGIC

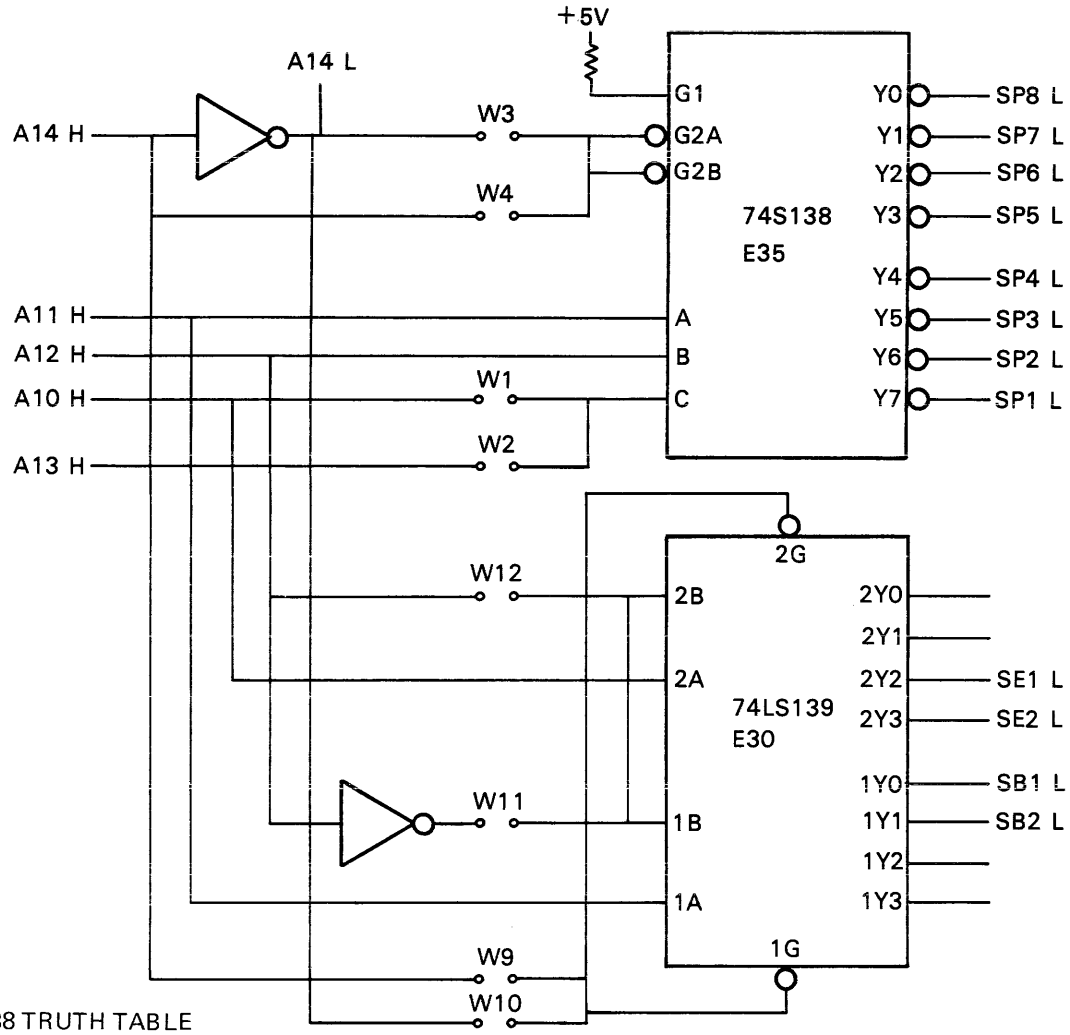
The socket selection logic determines which pair of sockets responds to the ROM address signals (although the ROMs in the sockets actually respond, we will state, for ease of explanation, that the sockets respond). The selection signals SB1 L, SB2 L, SE1 L, SE2 L, and SP1 L through SP8 L are generated by two decoders, E30 and E35 (Figure 4-8). Each selection signal causes two sockets to respond to the address signals; one socket contains the high-byte ROM, the other contains the low-byte ROM. Table 4-8 includes the relationship between the selection signals and the selected sockets.

Jumpers are inserted selectively in positions W1–W4 and W9–W12. These jumpers cause the PCR page numbers and the selection signals (and, therefore, the sockets) to be related in definite ways. Earlier, Table 4-1 indicated that PCR pages are assigned to specific ROM sockets. This is true within the confines stated for Table 4-1; i.e., the table applies only to the BDV11 module shipped by DIGITAL. On such a module, jumpers W1–W4 and W9–W12 are arranged as indicated under Group A in Table 4-8. Thus, PCR pages 0–17, for example, cause selection signal SB1 L to be asserted, and SB1 L causes sockets XE53 and XE48 to respond to address signals A<0:10> H. Other combinations of jumpers are possible, as indicated by Groups B through G in Table 4-8. Note that each selection signal always selects the same pair of sockets; however, the relation of PCR pages to selected sockets varies with jumper configuration.

Now, in Example 1 in the preceding section, the PCR was loaded with pages 2 and 3 so that bus address 173000 could address location 0400. This location was specified by 11 ROM address bits, A0 H – A10 H. The remaining four ROM address bits, A11 H – A14 H, are applied to the socket selection logic; here, they determine the ROMs in which location 0400 is addressed. If we assumme that we have a BDV11-AA, which has the Group A jumper arrangement, sockets XE53 and XE48 should be selected; i.e., SB1 L should be asserted by decoder E30 (Figure 4-8). With a jumper in both W9 and W12, SB1 L is asserted when A14 H is low, A12 H is low, and A11 H is low (A10 H and A13 H are irrelevant). Figure 4-7, Example 1, shows that the three signals are low, as they are for all pages in the 0–17 range. That these signals are low for pages 0–17 is indicated by the entry in the primary address column of Table 4-8; i.e., for addresses in the 0–2K range, address bits A11 H – A14 H are low. Note that there is correlation between PCR pages and primary addresses throughout Table 4-8.

The jumper configurations in Groups B–G allow a choice of where program execution begins. That is, the user can cause the CPU to execute instructions directly from a system ROM or an EPROM when power is turned on, rather than from the diagnostic/bootstrap ROM. To illustrate, in the preceding example the PCR contained pages 2 and 3; hence, bus address 173000 addressed location 0400 in ROMs E53 and E48. However, if jumpers W1–W4 are arranged as shown in Group F, the same PCR pages, 2 and 3, will cause bus adress 173000 to address location 0400 in ROMs E54 and E49; or, if jumpers W9–W12 are arranged as in Group B, 173000 will address 0400 in E57 and E40.

Note that in both of these examples, one group of four jumpers is not specified; i.e., W9–W12 are not specified in Group F and W1–W4 are not specified in Group B. These unspecified jumpers can have any arrangement as long as there is no conflict in chip selection. To illustrate: If we have the Group F configuration, we want PCR page 0 to cause 173000 to addresss 0000 in XE54/XE49; but, if jumpers W9–W12 are arranged as in Group A or B, PCR page 0 causes two other sockets to respond to the same address. Therefore, either there can be *no* chips in these other sockets, or the arrangement of W9–W12 must be changed; for instance, there would be no conflict at all if W9–W12 were arranged as in Group C.



74S138 TRUTH TABLE

G1	G2	C	B	A	OUT LOW
H	L	L	L	L	Y0 (SP8 L)
		L	L	H	Y1 (SP7 L)
		L	H	L	Y2 (SP6 L)
		L	H	H	Y3 (SP5 L)
		H	L	L	Y4 (SP4 L)
		H	L	H	Y5 (SP3 L)
		H	H	L	Y6 (SP2 L)
		H	H	H	Y7 (SP1 L)

74LS139 TRUTH TABLE (EACH HALF)

G	B	A	OUT LOW
L	L	L	YO(SB1 L)
	L	H	Y1 (SB2 L)
	H	L	Y2 (SE1 L)
	H	H	Y3 (SE2 L)

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Figure 4-8 Socket Selection Logic

Table 4-8 BDV11 Selection Signals/Sockets

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Selection Signal	Primary Addresses (A<0:14>H)	Sockets Selected
A	R	I	I	R	I	R	R	I	0–17	SB1 L	0K–2K	XE53/XE48
									20–37	SB2 L	2K–4K	XE58/XE44
									40–47	SE1 L	4K–5K	XE57/XE40
									50–57	SE2 L	5K–6K	XE52/XE36
									360–377	SP1 L	30K–32K	XE39/XE50
									340–357	SP2 L	28K–30K	XE43/XE46
									320–337	SP3 L	26K–28K	XE47/XE42
									300–317	SP4 L	24K–26K	XE51/XE38
									260–277	SP5 L	22K–24K	XE55/XE37
									240–257	SP6 L	20K–22K	XE60/XE41
									220–237	SP7 L	18K–20K	XE59/XE45
									200–217	SP8 L	16K–18K	XE54/XE49
B	*	*	*	*	I	R	I	R	40–57	SB1 L	4K–6K	XE53/XE48
									60–77	SB2 L	6K–8K	XE58/XE44
									0–7	SE1 L	0K–1K	XE57/XE40
									10–17	SE2 L	1K–2K	XE52/XE36
C	*	*	*	*	R	I	R	I	200–217	SB1 L	16K–18K	Ibid
									220–237	SB2 L	18K–20K	
									240–247	SE1 L	20K–21K	
									250–257	SE2 L	21K–22K	
D	*	*	*	*	R	I	I	R	240–257	SB1 L	20K–22K	Ibid
									260–277	SB2 L	22K–24K	
									200–207	SE1 L	16K–17K	
									210–217	SE2 L	17K–18K	
E	I	R	I	R	*	*	*	*	270–277	SP1 L	23K–24K	XE39/XE50
									250–257	SP2 L	21K–22K	XE43/XE46
									230–237	SP3 L	19K–20K	XE47/XE42
									210–217	SP4 L	17K–18K	XE51/XE48
									260–267	SP5 L	22K–23K	XE55/XE37
									240–247	SP6 L	20K–21K	XE60/XE41
									220–227	SP7 L	18K–19K	XE59/XE45
									200–207	SP8 L	16K–17K	XE54/XE49
F	R	I	R	I	*	*	*	*	160–177	SP1 L	14K–16K	Ibid
									140–157	SP2 L	12K–14K	
									120–137	SP3 L	10K–12K	
									100–117	SP4 L	8K–10K	
									60–77	SP5 L	6K–8K	
									40–57	SP6 L	4K–6K	
									20–37	SP7 L	2K–4K	
									0–17	SP8 L	0K–2K	

*See text describing these configurations.

Table 4-8 BDV11 Selection Signals/Sockets (Cont)

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Selection Signal	Primary Addresses (A<0:14>H)	Sockets Selected
G	I	R	R	I	*	*	*	*	70–77	SP1 L	7K–8K	Ibid
									50–57	SP2 L	5K–6K	
									30–37	SP3 L	3K–4K	
									10–17	SP4 L	1K–2K	
									60–67	SP5 L	6K–7K	
									40–47	SP6 L	4K–5K	
									20–27	SP7 L	2K–3K	
									0–7	SP8 L	0K–1K	

NOTE
R = Removed; I = Inserted

*See text describing these configurations.

4.8 ROM SOCKETS LOGIC

Figure 4-9 represents the ROM sockets and shows the address signals and enabling signals for each functional group of sockets. The diagnostic/bootstrap ROM sockets (which are selected by signals SB1 L and SB2 L) are supplied with 11 address bits, since these sockets are reserved for 2K-word ROMs. The EPROM sockets (selected by signals SE1 L and SE2 L) are reserved for 1K ROMs; therefore, these sockets are supplied with 10 address bits. The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs; five jumpers on the BDV11 module permit ROMs of either size to be used. Figure 4-10 shows how these five jumpers control the selection signals for the system ROM sockets, and relates the jumpers to the types of ROM that can be used in the BDV11. (If ROMs other than 8316E, 2716, and 2708 are used, they must meet the specifications given in Appendix A.)

The output data from the selected memory is applied to data selectors that gate the data onto the DAL <0:15> H lines. These selectors also allow the user to read the contents of the PCR.

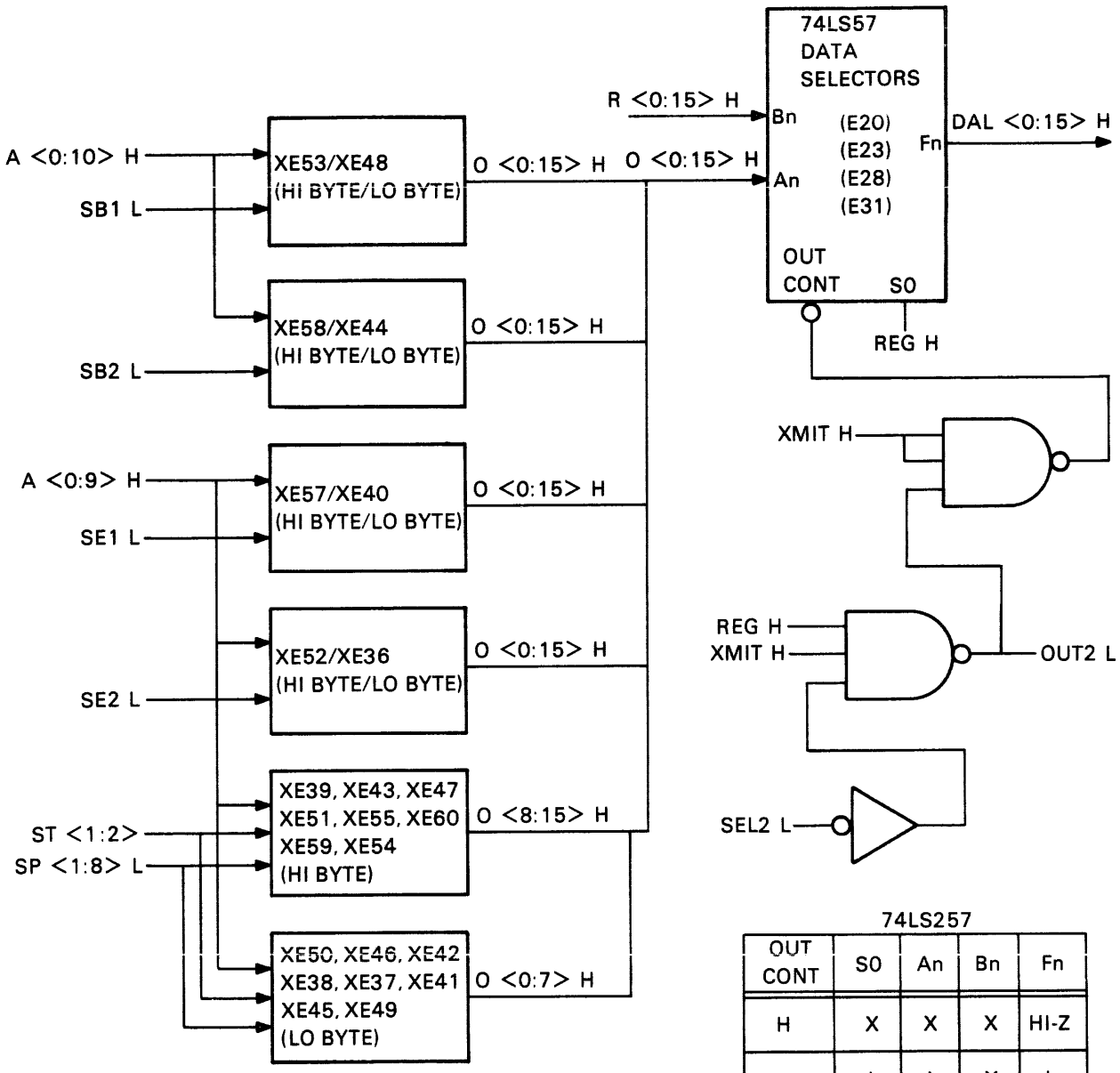
4.9 BEVNT LOGIC

The logic shown in Figure 4-11 permits the user to choose how to control the LTC function. When the BEVNT switch, E21, is open, the bus BEVNT L signal can be controlled by the LTC signal generated in the LSI-11 power supply. If the switch is closed, the BEVNT L signal can be program controlled.

Program control is effected by the 1-bit register, E10. Address 177546 is placed on the BDAL lines, causing signals SEL6 L and REG L to be asserted by the control logic. When data bit 6 is issued, the OUT LB L signal causes E2 to clock the flip-flop, loading it with the state of DAL6 H. If DAL6 H is high, the flip-flop output turns Q4 off, permitting the LTC signal to assert BEVNT L; but, if DAL6 H is low, Q4 is switched on and clamps BEVNT L low. Note that the register is cleared when the power is turned on or when the system is re-booted.

4.10 DISPLAY LOGIC

The display logic and the diagnostic LEDs, D1–D4, are illustrated in Figure 4-12. Address 177524 results in E25 being clocked when data bits 0–3 are issued; the flip-flop outputs cause the respective LEDs to glow, indicating the source of the program error. All the flip-flops are cleared when power is turned on or when the system is re-booted; hence, display value 17_8 is indicated; i.e., all the LEDs (including the green POWER OK indicator) are lighted. If the LEDs indicate 17_8 and the PC = 173000, the ENABLE/HALT switch might be in the HALT position, or a bus error might have occurred.



74LS257

OUT CONT	SO	An	Bn	Fn
H	X	X	X	HI-Z
L	L	L	X	L
	L	H	X	H
	H	X	L	L
	H	X	H	H

NOTE:
XE53/X48, XE58/XE44 ARE DIAGNOSTIC ROM SOCKETS (XE58/XE44 RESERVED FOR DIGITAL);
XE57/XE40, XE52/XE36 ARE EPROM SOCKETS; REMAINING SOCKETS ARE 16K SYSTEM ROM SOCKETS.

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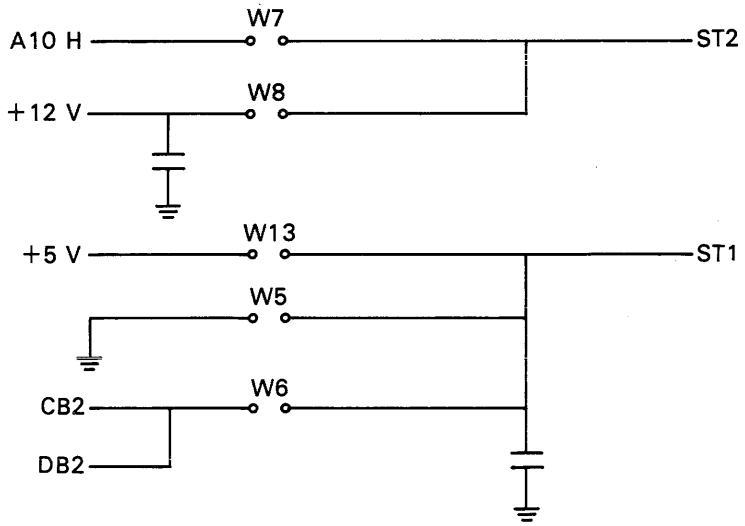
Figure 4-9 Logic Block Diagram, ROM Sockets



ROM TYPE	JUMPERS INSERTED[1]				
	W5	W6	W7	W8	W13
2708[2]	R	I	R	I	R
2716	R	R	I	R	I
8316E[3]	I	R	I	R	R
8316E[4]	R	R	I	R	I

1. I=INSERTED; R=REMOVED
2. CB2 AND DB2 MUST BE SUPPLIED WITH EXTERNAL -5V POWER.
3. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	LOW

4. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	HIGH

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Figure 4-10 System ROM Jumpers

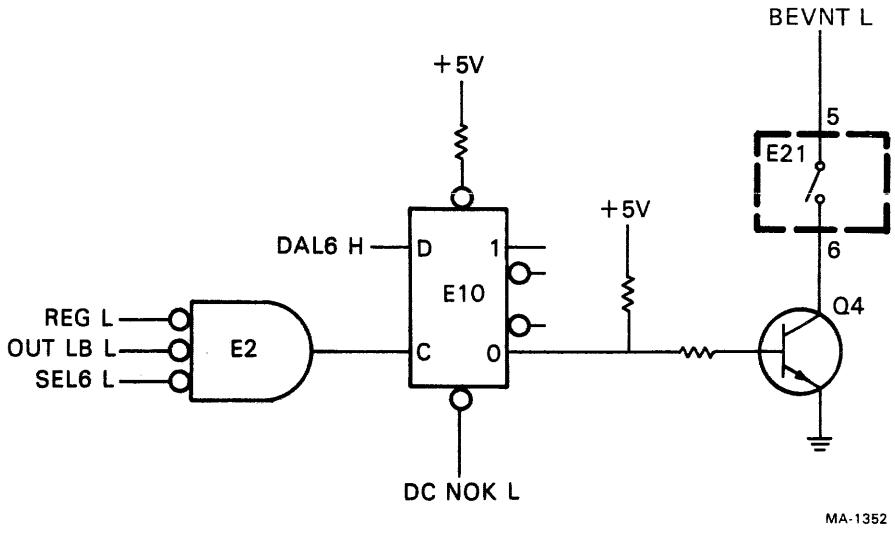


Figure 4-11 BEVNT Logic

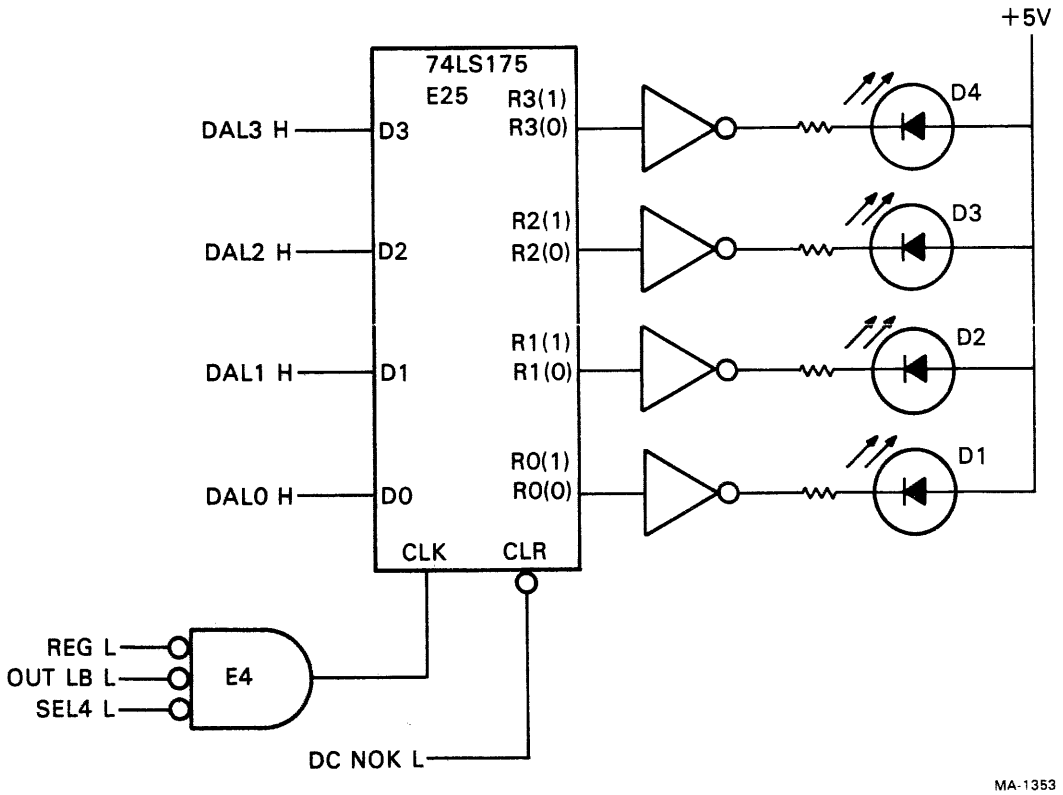
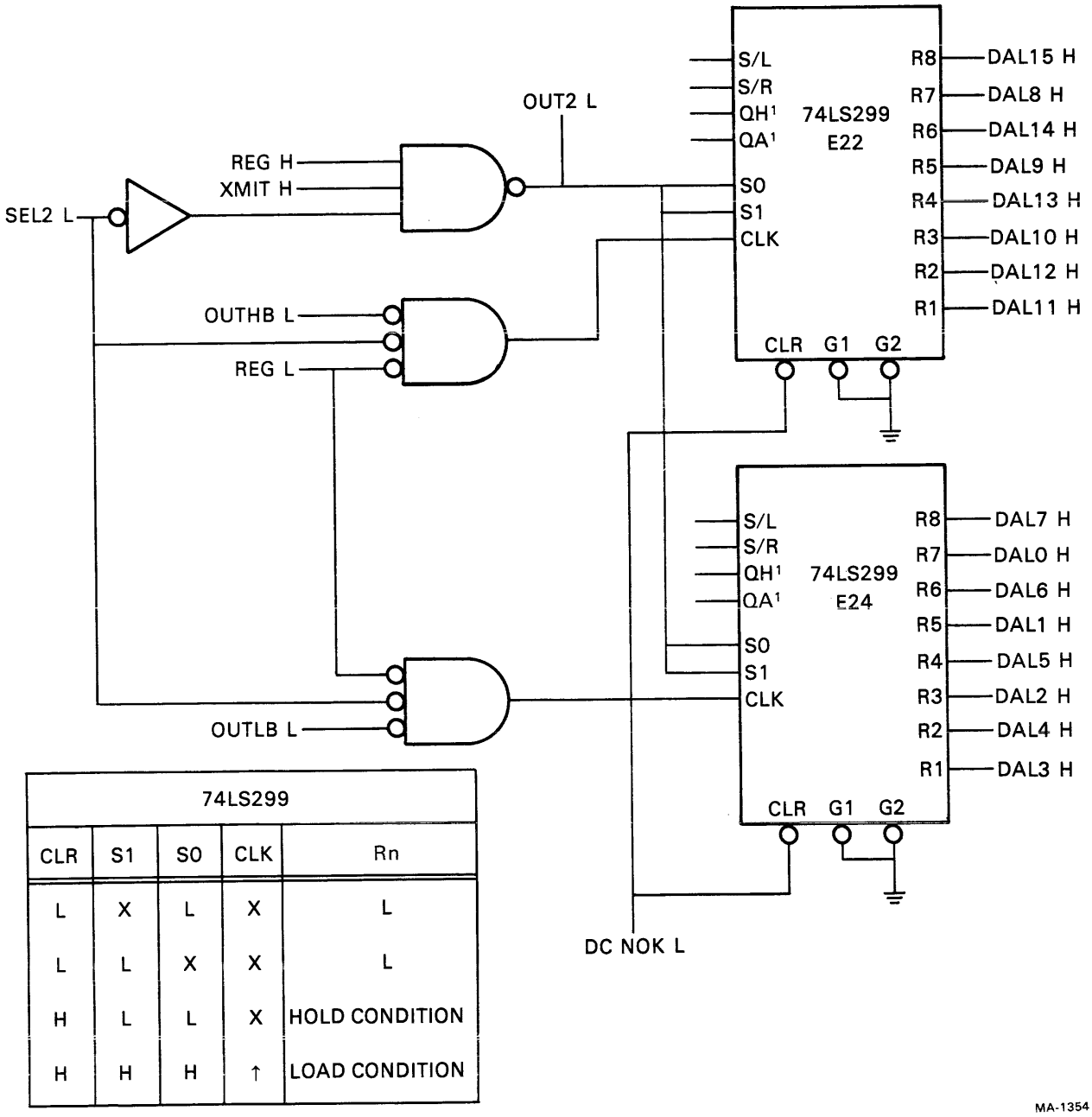


Figure 4-12 Display Logic/LEDs D1–D4

4.11 READ/WRITE REGISTER LOGIC

The read/write register logic is shown in Figure 4-13. The logic includes two 8-bit universal shift registers, 74LS299 integrated circuits, which are used only in the "hold" and "load" modes.

When the register is addressed, the SEL2 L, REG H, and REG L signals are asserted by the control logic. If the register is being read, the control logic also asserts the XMIT H signal. The asserted OUT2 L signal puts the register into the hold condition; thus, the information on the DAL lines is that held in the register output stages. On the other hand, when the register is to be written, the XMIT H signal is negated and the register is placed in the load condition. Either or both bytes of the register are clocked and the data on the DAL lines is loaded into the output stages of the register. The entire register is cleared when power is turned on or when the system is re-booted.



74LS299				
CLR	S1	S0	CLK	Rn
L	X	L	X	L
L	L	X	X	L
H	L	L	X	HOLD CONDITION
H	H	H	↑	LOAD CONDITION

Figure 4-13 Read/Write Register Logic

APPENDIX A
ROM SPECIFICATIONS

This appendix gives specifications of the ROMs recommended for use in BDV11 variations. If ROMs other than those listed are used, they must meet the specifications listed here.

2708-TYPE EPROM (1K × 8 ORGANIZATION)

READ OPERATION
DC AND OPERATING CHARACTERISTICS

T_A = 0° C TO 70° C, V_{CC} = +5 V ±5%, V_{DD} = +12 V ±5%, V_{BB}[1] = −5 V ±5%, V_{SS} = 0 V, UNLESS OTHERWISE NOTED.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
I_{LI}	ADDRESS AND CHIP SELECT INPUT SINK CURRENT		10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	μA	V_{OUT} = 5.5 V, $\overline{CS}$/WE = 5 V
I_{DD}[3]	V_{DD} SUPPLY CURRENT		65	mA	WORST CASE SUPPLY CURRENTS:
I_{CC}[3]	V_{CC} SUPPLY CURRENT		10	mA	ALL INPUTS HIGH
I_{BB}[3]	V_{BB} SUPPLY CURRENT		45	mA	$\overline{CS}$/WE = 5V; T_A = 0° C
V_{IL}	INPUT LOW VOLTAGE	V_{SS}	0.65	V	
V_{IH}	INPUT HIGH VOLTAGE	3.0	V_{CC}+1	V	
V_{OL}	OUTPUT LOW VOLTAGE		0.45	V	I_{OL} = 1.6 mA
V_{OH1}	OUTPUT HIGH VOLTAGE	3.7		V	I_{OH} = −100 μA
V_{OH2}	OUTPUT HIGH VOLTAGE	2.4		V	I_{OH} = −1 mA
P_D	POWER DISSIPATION		800	mW	T_A = 70° C

NOTES:
1. V_{BB} MUST BE APPLIED PRIOR TO V_{CC} AND V_{DD}. V_{BB} MUST ALSO BE THE LAST POWER SUPPLY SWITCHED OFF.
2. TYPICAL VALUES ARE FOR T_A = 25° C AND NOMINAL SUPPLY VOLTAGES.
3. THE TOTAL POWER DISSIPATION OF THE 2704/2708 IS SPECIFIED AT 800 mW. IT IS NOT CALCULATED BY SUMMING THE VARIOUS CURRENTS (I_{DD}, I_{CC}, and I_{BB}) MULTIPLIED BY THEIR RESPECTIVE VOLTAGES SINCE CURRENT PATHS EXIST BETWEEN THE VARIOUS POWER SUPPLIES AND V_{SS}. THE I_{DD}, I_{CC}, AND I_{BB} CURRENTS SHOULD BE USED TO DETERMINE POWER SUPPLY CAPACITY ONLY.

AC CHARACTERISTICS

T_A = 0° C TO 70° C, V_{CC} = +5 V ±5%, V_{DD} = +12 V ±5%, V_{BB} = −5 V ±5% V_{SS} = 0 V, UNLESS OTHERWISE NOTED.

		2708-1 LIMITS		2708 LIMITS		
SYMBOL	PARAMETER	MIN.	MAX.	MIN	MAX.	UNITS
t_{ACC}	ADDRESS TO OUTPUT DELAY		350		450	ns
t_{CO}	CHIP SELECT TO OUTPUT DELAY		120		120	ns
t_{DF}	CHIP DESELECT TO OUTPUT FLOAT	0	120	0	120	ns
t_{OH}	ADDRESS TO OUTPUT HOLD	0		0		ns

CAPACITANCE[1]

T_A = 25° C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
C_{IN}	INPUT CAPACITANCE	4	6	pF	V_{IN} = 0 V
C_{OUT}	OUTPUT CAPACITANCE	8	12	pF	V_{OUT} = 0 V

NOTE
1. THIS PARAMETER IS PERIODICALLY SAMPLED AND IS NOT 100% TESTED.

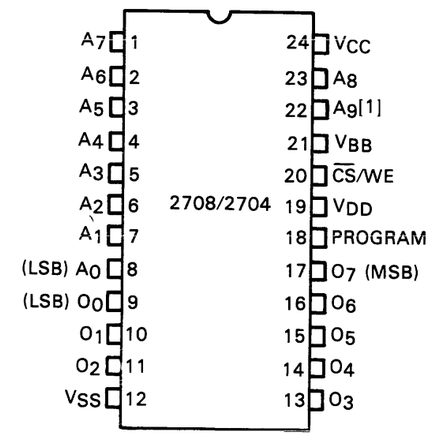
AC TEST CONDITIONS:

OUTPUT LOAD: 1 TTL GATE AND C_L = 100 pF
INPUT RISE AND FALL TIMES: ≤20 ns
TIMING MEASUREMENT REFERENCE LEVELS: 0.8 V AND 2.8 V FOR INPUTS; 0.8 V and 2.4 V FOR OUTPUTS.
INPUT PULSE LEVELS: 0.65 V TO 3.0 V

PIN NAMES

A_0–A_9	ADDRESS INPUTS
O_1–O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONFIGURATION



NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

MA-1381

8316E-TYPE ROM (2K × 8 ORGANIZATION)

DC AND OPERATING CHARACTERISTICS

T_A = 0° C TO +70° C, V_{CC} = 5 V ±10% UNLESS OTHERWISE SPECIFIED.

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)		10	μA	V_{IN} = 0 to 5.25 V
I_{LOH}	OUTPUT LEAKAGE CURRENT		10	μA	CHIP DESELECTED, V_{OUT} = 4.0 V
I_{LOL}	OUTPUT LEAKAGE CURRENT		-20	μA	CHIP DESELECTED, V_{OUT} = 0.4 V
I_{CC}	POWER SUPPLY CURRENT		120	mA	ALL INPUTS 5.25 V DATA OUT OPEN
V_{IL}	INPUT "LOW" VOLTAGE	-0.5	0.8	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.4	V_{CC} +1.0 V	V	
V_{OL}	OUTPUT "LOW" VOLTAGE		0.4	V	I_{OL} = 2.1 mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4		V	I_{OH} = -400 μA

NOTE

1. TYPICAL VALUES FOR T_A = 25° C AND NOMINAL SUPPLY VOLTAGE.

AC CHARACTERISTICS

T_A = 0° C TO +70° C, V_{CC} = +5 V ±10%, UNLESS OTHERWISE SPECIFIED.

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNIT
t_A	ADDRESS TO OUTPUT DELAY TIME		450	ns
t_{CO}	CHIP SELECT TO OUTPUT ENABLE DELAY TIME		120	ns
t_{DF}	CHIP DESELECT TO OUTPUT DATA FLOAT DELAY TIME	10	100	ns

CONDITIONS OF TEST FOR AC CHARACTERISTICS

OUTPUT LOAD ..... 1 TTL GATE AND C_L = 100 pF
INPUT PULSE LEVELS ..... 0.8 TO 2.4 V
INPUT PULSE RISE AND FALL TIMES (10% TO 90%) ..... 20 ns
TIMING MEASUREMENT REFERENCE LEVEL
INPUT ..... 1 V AND 2.2 V
OUTPUT ..... 0.8 V AND 2.0 V

CAPACITANCE[2]

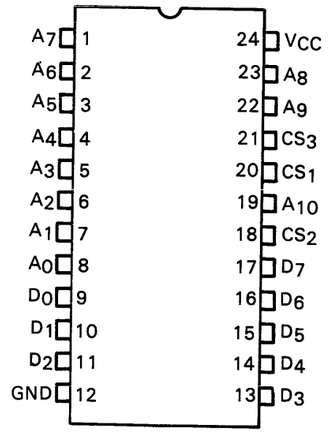
T_A = 25° C, f = 1 MHz

SYMBOL	TEST	LIMITS TYP.	LIMITS MAX.
C_{IN}	ALL PINS EXCEPT PIN UNDER TEST TIED TO AC GROUND	5 pF	10 pF
C_{OUT}	ALL PINS EXCEPT PIN UNDER TEST TIED TO AC GROUND	10 pF	15 pF

NOTE

2. THIS PARAMETER IS PERIODICALLY SAMPLED AND IS NOT 100% TESTED.

PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
D_7–D_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

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READ OPERATION
DC AND OPERATING CHARACTERISTICS

T_A = 0° C To 70° C, V_{CC}[1,2] = +5 V ±5%, V_{PP} [2] = V_{CC} ±0.6 V[3]

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	μA	V_{IN} = 5.25 V
I_{LO}	OUTPUT LEAKAGE CURRENT		10	μA	V_{OUT} = 5.25 V
I_{PP1}[2]	V_{PP} CURRENT		5	mA	V_{PP} = 5.85 V
I_{CC1}[2]	V_{CC} CURRENT (STANDBY)		25	mA	PD/PGM = V_{IH}, $\overline{CS}$ = V_{IL}
I_{CC2}[2]	V_{CC} CURRENT (ACTIVE)		100	mA	$\overline{CS}$ = PD/PGM = V_{IL}
V_{IL}	INPUT LOW VOLTAGE	-0.1	0.8	V	
V_{IH}	INPUT HIGH VOLTAGE	2.2	V_{CC}+1	V	
V_{OL}	OUTPUT LOW VOLTAGE		0.45	V	I_{OL} = 2.1 mA
V_{OH}	OUTPUT HIGH VOLTAGE.	2.4		V	I_{OH} = -400 μA

NOTES

1. V_{CC} MUST BE APPLIED SIMULTANEOUSLY OR BEFORE V_{PP} AND REMOVED SIMULTANEOUSLY OR AFTER V_{PP}.
2. V_{PP} MAY BE CONNECTED DIRECTLY TO V_{CC} EXCEPT DURING PROGRAMMING. THE SUPPLY CURRENT WOULD THEN BE THE SUM OF I_{CC} AND I_{PP1}.
3. THE TOLERANCE OF 0.6 V ALLOWS THE USE OF A DRIVER CIRCUIT FOR SWITCHING THE V_{PP} SUPPLY PIN FROM V_{CC} IN READ TO 25 V FOR PROGRAMMING.
4. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
5. t_{ACC2} IS REFERENCED TO PD/PGM OR THE ADDRESSES, WHICHEVER OCCURS LAST.

AC CHARACTERISTICS

T_A = 0° C TO 70° C, V_{CC}[1] = +5 V ±5%, V_{PP}[2] = V_{CC} ±0.6 V [3]

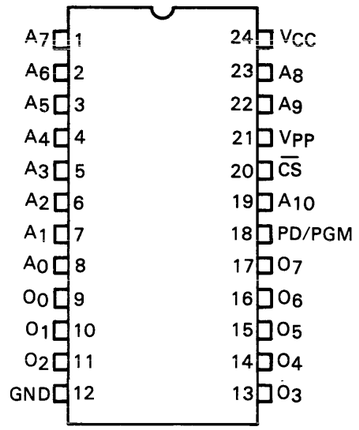
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{ACC1}	ADDRESS TO OUTPUT DELAY		450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM TO OUTPUT DELAY		450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	CHIP SELECT TO OUTPUT DELAY		120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM TO OUTPUT FLOAT	0	100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	CHIP DESELECT TO OUTPUT FLOAT	0	100	ns	PD/PGM = V_{IL}
t_{OH}	ADDRESS TO OUTPUT HOLD	0		ns	PD/PGM = $\overline{CS}$ = V_{IL}

CAPACITANCE[4]

T_A = 25° C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
C_{IN}	INPUT CAPACITANCE	4	6	pF	V_{IN} = 0 V
C_{OUT}	OUTPUT CAPACITANCE	8	12	pF	V_{OUT} = 0 V

PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

AC TEST CONDITIONS

OUTPUT LOAD:1 TTL GATE AND C_L = 100 pF
INPUT RISE AND FALL TIMES: ≤20 ns
INPUT PULSE LEVELS: 0.8 V TO 2.2 V
TIMING MEASUREMENT REFERENCE LEVEL:
INPUTS 1 V AND 2 V
OUTPUTS 0.8 V AND 2 V.

MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUT (9–11, 13–17)
READ	V_{IL}	V_{IL}	+5	+5	D_{OUT}
DESELECT	DON'T CARE	V_{IH}	+5	+5	HIGH Z
POWER DOWN	V_{IH}	DON'T CARE	+5	+5	HIGH Z
PROGRAM	PULSED V_{IL} TO V_{IH}	V_{IH}	+25	+5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	+5	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	+5	HIGH Z

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